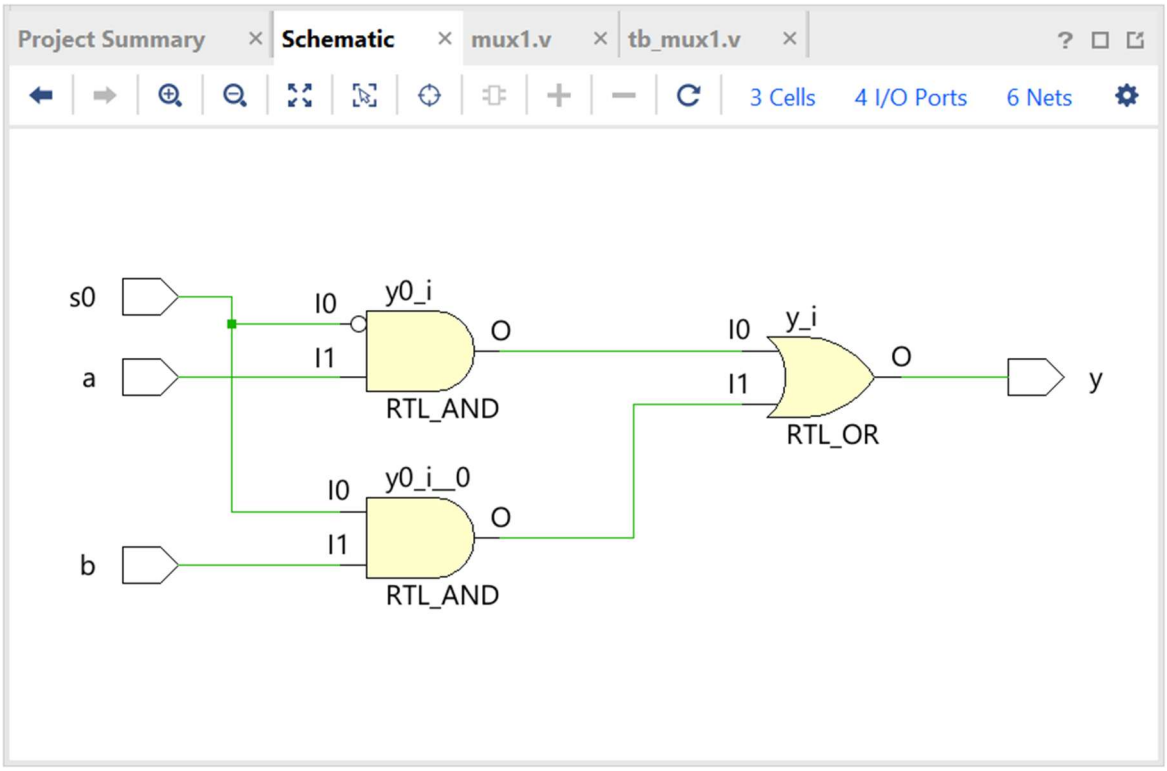
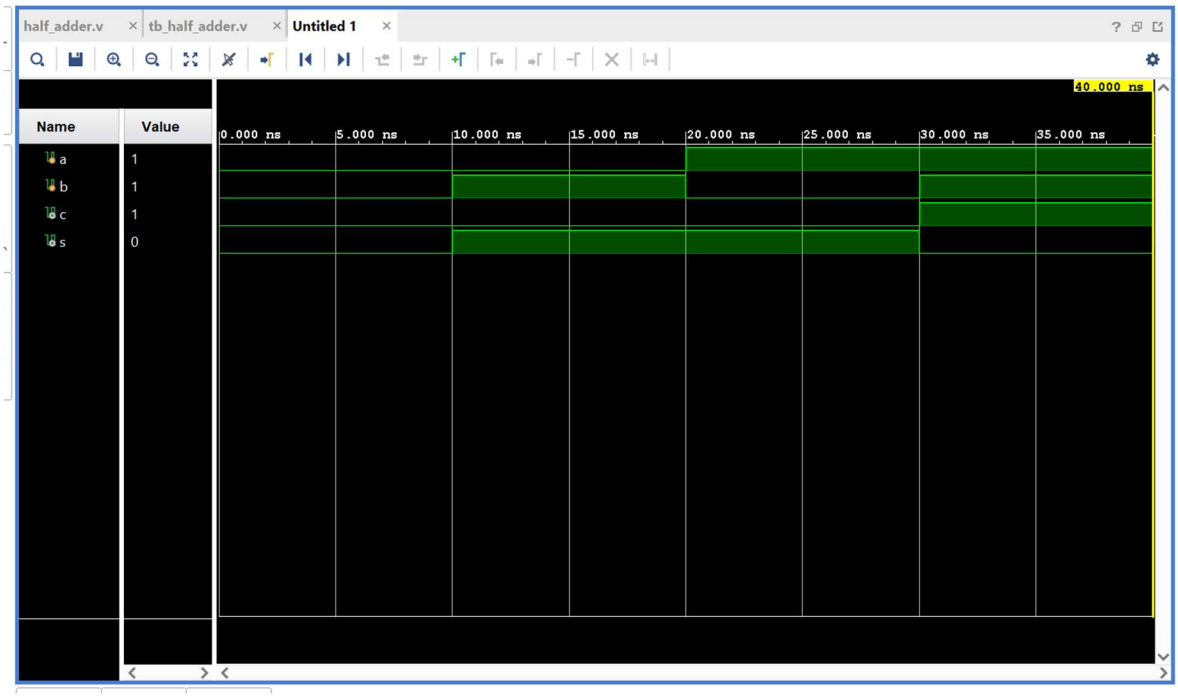
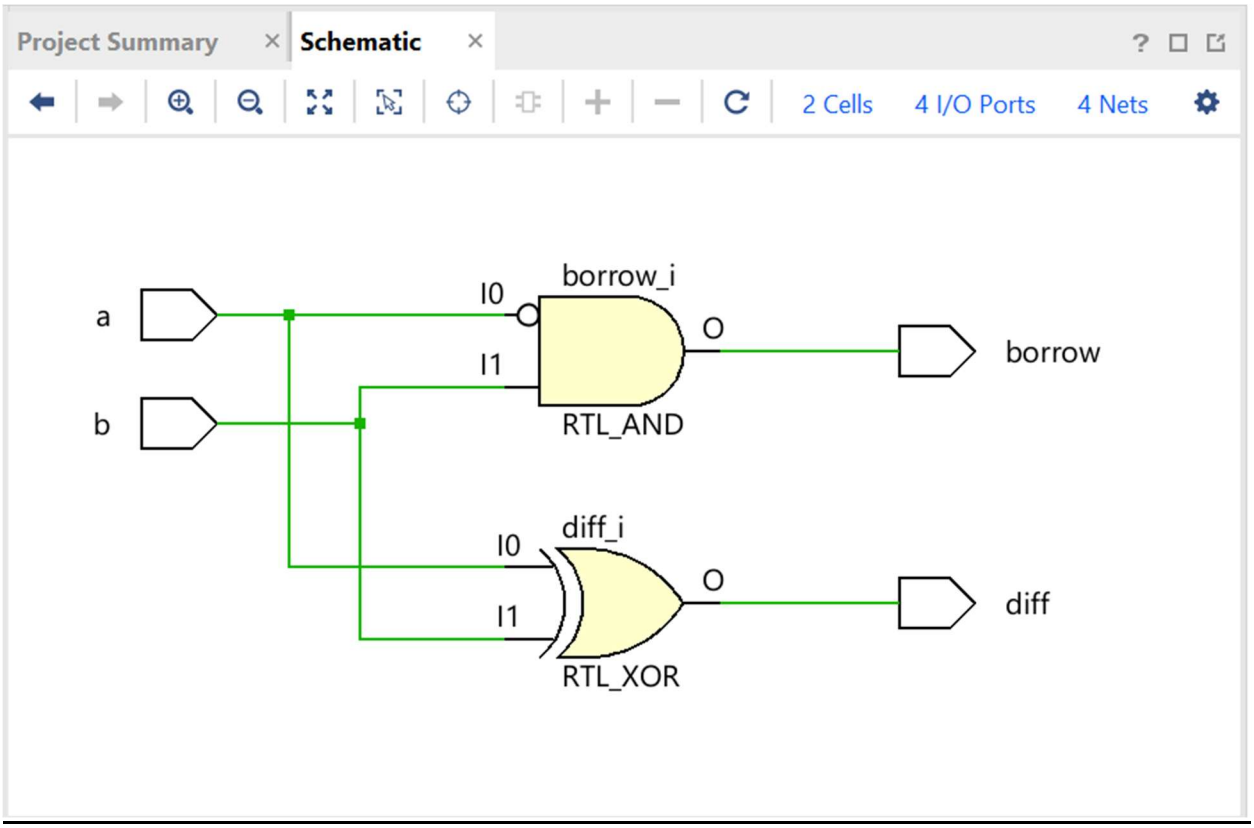
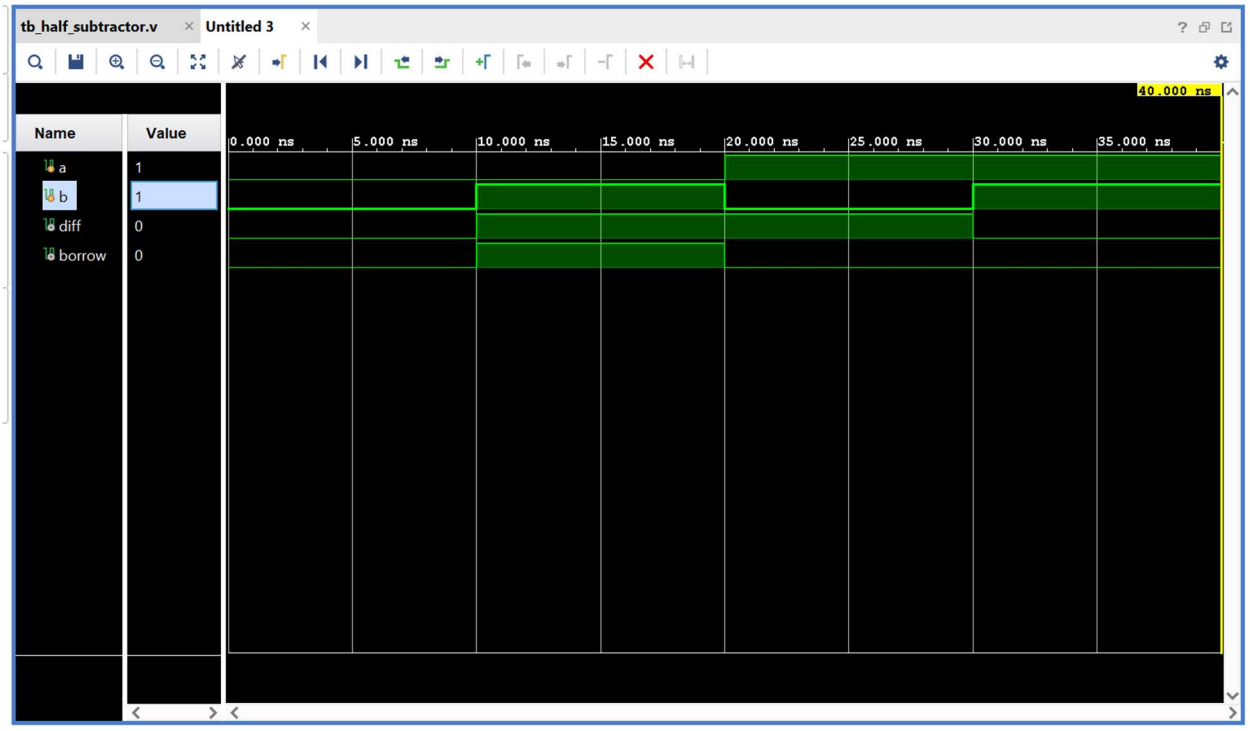
HALF ADDER:


Project Summary
Schematic
mux1.v
tb_mux1.v
3 Cells
4 I/O Ports
6 Nets
s0
a
b
I0
I1
y0_i
O
RTL_AND
y0_i__0
I0
I1
O
RTL_AND
I0
I1
y_i
O
RTL_OR
y

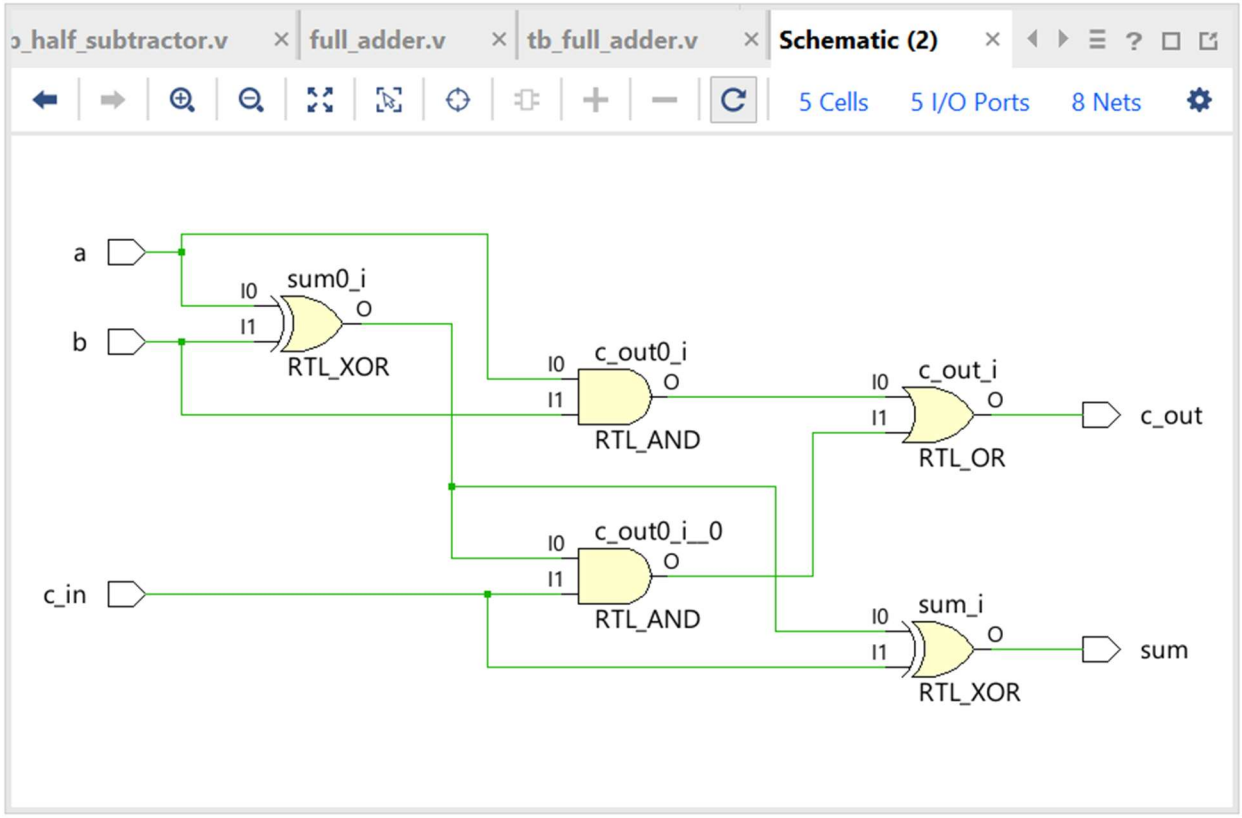

half_adder.v
tb_half_adder.v
Untitled 1
Name
Value
a
b
c
s
1
1
1
0
0.000 ns
5.000 ns
10.000 ns
15.000 ns
20.000 ns
25.000 ns
30.000 ns
35.000 ns
40.000 ns

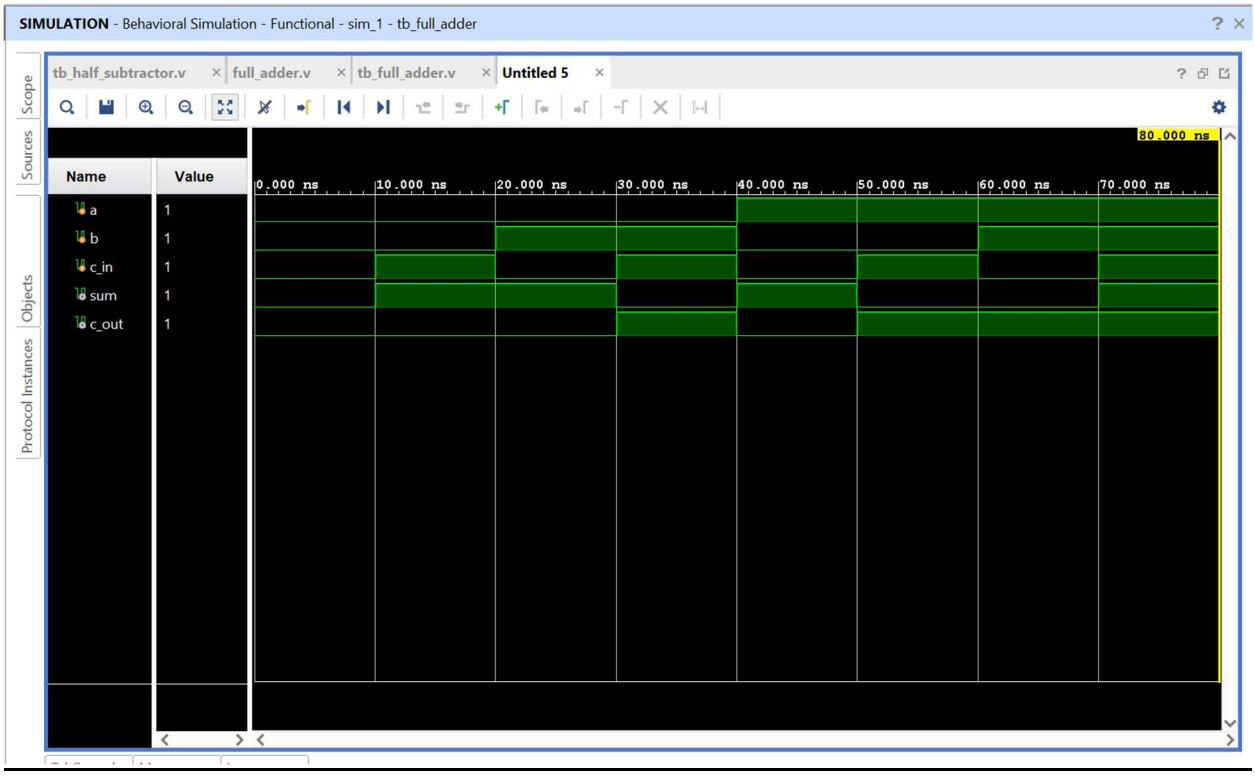
HALF SUBTRACTOR:



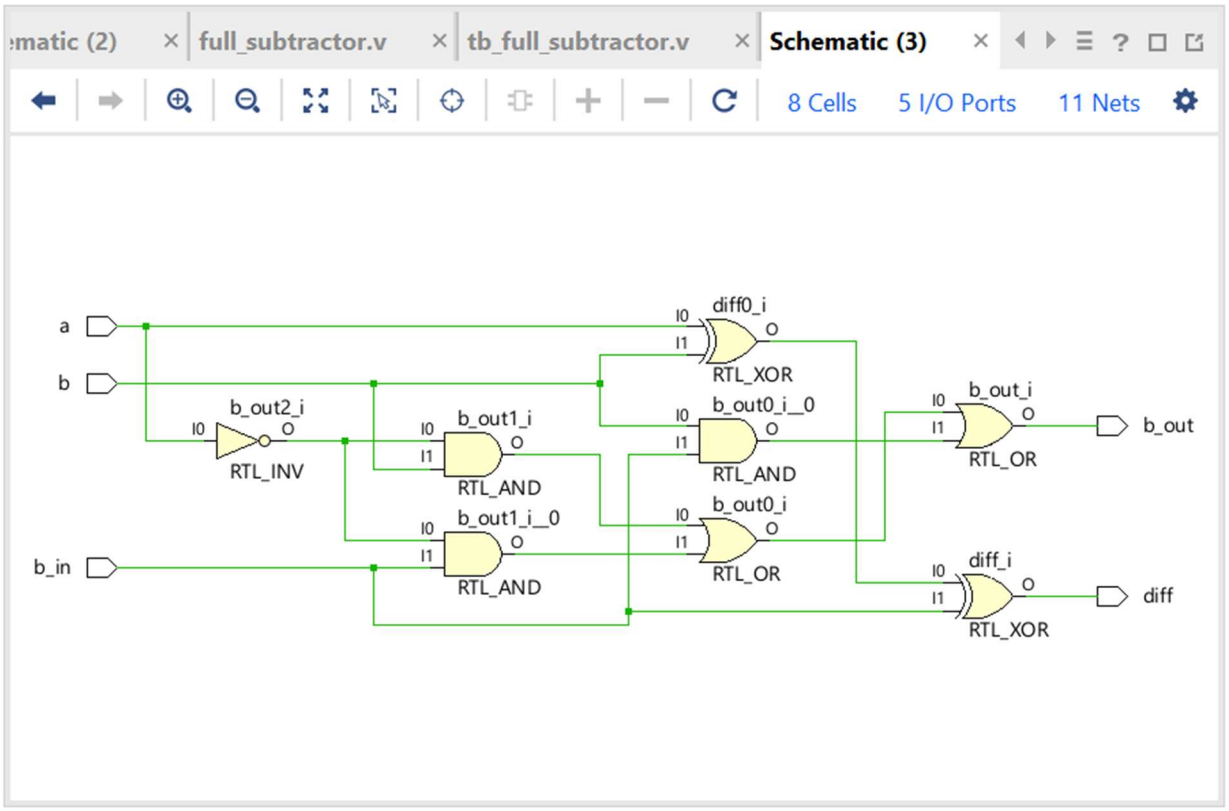


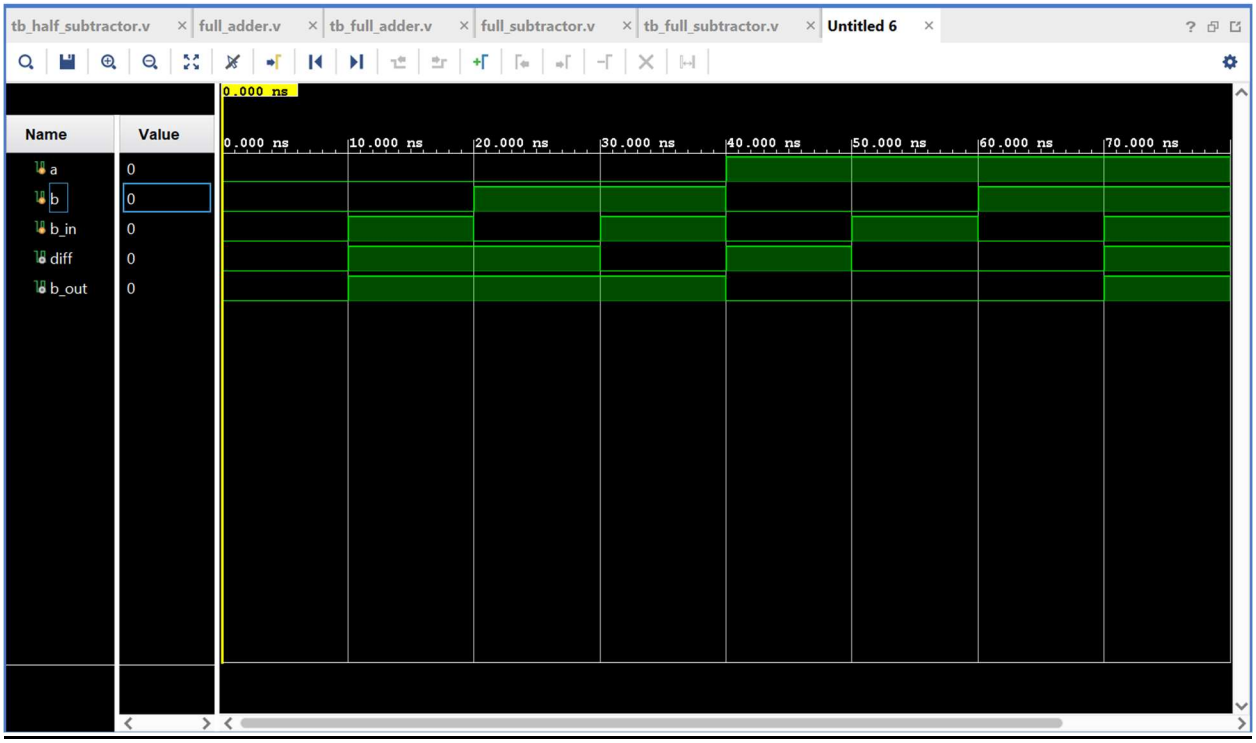
FULL ADDER:


half_subtractor.v
full_adder.v
tb_full_adder.v
Schematic (2)
5 Cells
5 I/O Ports
8 Nets
a
b
c_in
sum0_i
RTL_XOR
c_out0_i
RTL_AND
c_out_i
RTL_OR
c_out
c_out0_i__0
RTL_AND
sum_i
RTL_XOR
sum
I0
I1
O


SIMULATION - Behavioral Simulation - Functional - sim_1 - tb_full_adder
tb_half_subtractor.v
full_adder.v
tb_full_adder.v
Untitled 5
Scope
Sources
Objects
Protocol Instances
Name
Value
a
b
c_in
sum
c_out
1
80.000 ns
0.000 ns
10.000 ns
20.000 ns
30.000 ns
40.000 ns
50.000 ns
60.000 ns
70.000 ns

FULL SUBTRACTOR:





UNIVERAL: