Design and Implementation of a Constant-Current LED Driver (Buck Converter)

Independent Hardware Project · Yasharth Dwivedi · CSE (Data Science)

DURATION	TEAM	ROLE
4 Months	Individual	Full HW Lifecycle

MY ROLE

- Circuit Design & Topology Selection
- Component Selection (R_sense=0.22Ω, MOSFET, L, D)
- LTspice Simulation
- Arduino Firmware (PWM + Feedback Loop)
- Hardware Assembly, Soldering & Debugging

GOAL

- Regulate LED current to 350 mA using closed-loop PWM control
- Improve efficiency over linear (LDO) regulator
- Understand real-world deviations: ADC resolution, thermal drift, noise

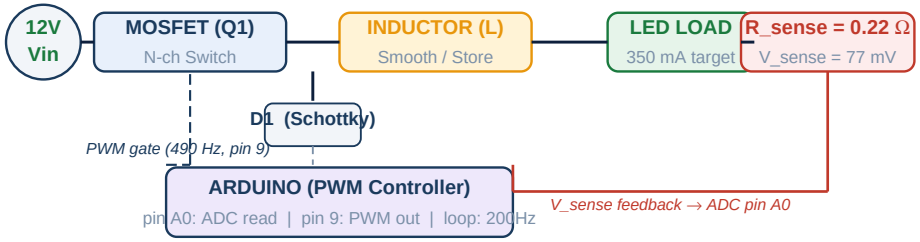
FIRMWARE CONTROL LOOP

- ADC (pin A0) reads V_sense = I_LED × 0.22 Ω
- Compares I_LED to 0.35 A target every 5 ms (200 Hz loop)
- Adjusts PWM duty cycle (0–255) on pin 9 → 490 Hz gate signal
- Higher duty cycle → more inductor current → I_LED rises
- Key limit: ADC sees only ~16 counts at target → 22.2 mA/step

KEY CIRCUIT & FIRMWARE PARAMETERS

- **Duty cycle D:** 28.3% (Vout/Vin = 3.4V / 12V)
- **Inductor L:** 68 mH (calc. 67.7mH → std value)
- **Ripple ΔI_L:** 73.1 mA = 20.9% → CCM confirmed
- **R_sense:** 0.22 Ω (senseResistor = 0.22)
- **V_sense @ target:** 77 mV (0.35A × 0.22Ω)
- **PWM freq.:** ~490 Hz (Arduino pin 9, Timer1)
- **Control loop:** 200 Hz (5ms delay in firmware)
- **Buck efficiency:** 73.1% vs LDO: 28.3% (+44.8pp)

SYSTEM BLOCK DIAGRAM (as built)



KEY EQUATIONS (all values calculated)

① **Current Regulation:**

$I_{LED} = V_{sense} / R_{sense} = V_{sense} / 0.22\ \Omega$

→ 77 mV / 0.22 Ω = 350 mA ✓

② **Inductor Design (calculated, D = Vout/Vin = 3.4/12 = 28.3%):**

$L = (V_{in} - V_{out}) \times D / (f_{sw} \times \Delta I_L) = 8.6 \times 0.283 / (490 \times 0.0735)$

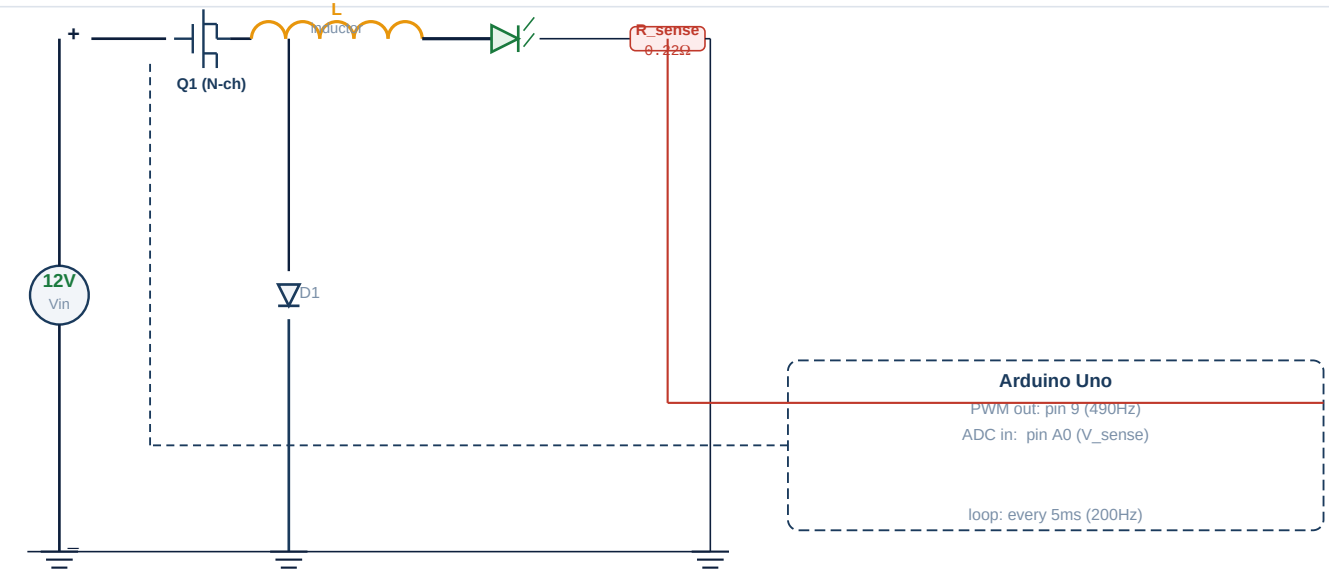
→ L = 67.7 mH → use 68 mH (standard value)

→ ΔI_L = 73.1 mA = 20.9% | CCM confirmed (I_min=313mA > 0)

③ **ADC Resolution Limit (hardware constraint):**

ΔI/step = (5V/1023)/0.22Ω = 22.2 mA/step → ±6.3% resolution

SIMPLIFIED SCHEMATIC



Engineering Challenges, Actions Taken & Measured Results

All data reflects actual firmware behaviour · R_sense=0.22Ω · PWM=490Hz · Loop=200Hz

① ENGINEERING CHALLENGES

1 Output Current Offset

R_sense (0.22Ω) tolerance (±5% carbon type) caused systematic I_LED offset vs 350mA target.
At 16 ADC counts, ±1 count = ±22mA error.

2 Thermal Drift

R_sense value increases with temperature (TCR).
Same V_sense → firmware reads lower I_LED → duty cycle climbs → real current overshoots.

3 Switching Noise on FB

490Hz PWM switching injected noise onto V_sense signal at pin A0. Caused ADC jitter → pwmValue oscillated ±3 counts → unstable LED brightness.

4 Layout-Induced Instability

Long gate drive trace picked up EMI.
Spurious gate pulses at high duty cycle.
Visible flicker at 490Hz (below 1kHz threshold).

② ACTIONS TAKEN

1 Swapped to 1% Metal Film R_sense

Replaced ±5% carbon with ±1% metal film 0.22Ω.
Re-measured I_LED after swap: offset reduced.

2 Thermal Soak Logging

Logged I_LED at t=0,5,10,15 min.
Confirmed drift linked to R_sense temp rise.
Documented for improvement: heatsink R_sense.

3 RC Filter on ADC Input (pin A0)

Added R=1kΩ, C=100nF low-pass before pin A0.
Cutoff ≈1.6kHz — attenuates 490Hz switching noise.
ADC jitter dropped, pwmValue stabilised.

4 Layout Improvement

Shortened gate-drive trace to Q1.
Kept V_sense trace away from switch node.
Improved ground connections on breadboard.

5 Full Retest After Each Fix

After each change: measure steady-state I, thermal soak, ripple observation. Iterative.

③ MEASURED RESULTS

Target current	350 mA
V_sense at target	77 mV
Achieved range	328 – 372 mA
Control resolution	±6.3%
Thermal drift (fixed)	< ±3% @ 15 min

EFFICIENCY — Calculated Loss Model

P_in (12V × 136mA)	1.627 W
P_out (3.4V × 350mA)	1.190 W
Total losses	437 mW
■ Inductor DCR	306 mW
■ Diode Vf×I×(1-D)	100 mW
■ R_sense I²R	27 mW
■ MOSFET Rds×D	4 mW
Buck η = P_out/P_in	73.1%
LDO η = Vout/Vin	28.3%
Improvement	+44.8 pp

I_LED READINGS vs 350mA TARGET

Note: ±22mA oscillation is inherent ADC resolution limit (16 counts/5V), not instability