Analysis and Design of Current Starved Ring VCO

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Abstract—**This paper focuses on and analysis and design of current starved voltage controlled ring oscillator. The analysis includes effect of delay time, phase noise, layout area, technology etc. on the frequency of oscillation at various power supplies and control voltages. The simulation results shows that the circuit has higher tuning range and low power consumption suitable for various application domains. Added benefit of this VCO is to maintain a constant amplitude level and oscillation. It is also proved here that the frequency of oscillation is inverse of the supply voltage and therefore consuming less power.**

Keywords—VCO, Inverter, Ring VCO, Delay cell, Current starved ring VCO, Delay, Phase noise.

I. INTRODUCTION

The voltage controlled oscillator (VCO) plays a very important role in communication systems due to low power consumption, wide frequency range of operation and its high integration capability [1]. It is an electronic device that uses amplification, feedback, and a resonant circuit to generate a repeating voltage waveform at a particular frequency. The frequency, or rate of repetition per unit time, is variable with an applied voltage. VCOs are important integral part of phase-locked loops, clock recovery circuits, frequency synthesizers and in almost all digital and analog systems.

The application requirements of VCO include high frequency, low power consumption, phase stability, large electrical tuning range, linearity of frequency on the control voltage, less area, low cost and large gain factor. The design of ring VCO involves tradeoffs in terms of area, speed, power, frequency and different application domain [2].

The objective of this paper is to analyze and design current starved ring VCO. The analysis includes delay, phase noise layout are and effect of technology on it.
The rest of the paper includes introduction of the CMOS based ring oscillator in section II followed by current starved ring VCO in section III. The analysis of delay and phase noise is provided in section IV and V respectively. Simulation results of three stage current starved ring VCO at different technologies along with the layout design are portrayed in section VI. Finally conclusions are drawn in section VII.

II. CMOS RING OSCILLATOR

An oscillator is an amplifier that provides its own input signal. The primary purpose of an oscillator is to generate a given waveform at a constant peak amplitude and specific frequency and to maintain this waveform within certain limits of frequency and amplitude. The most basic CMOS ring oscillators employs odd number of single ended inverters connected in a chain. The output of N^{th} stage is fed back to the input of first stage. There are no stable operation point exits because of odd number of inversions in ring oscillator. To sustain oscillation, Barkhausen criteria must be satisfied also every stage should add 180°/N phase and The block diagram of N- stage (N = odd, >1) ring VCO is shown in Fig. 1.

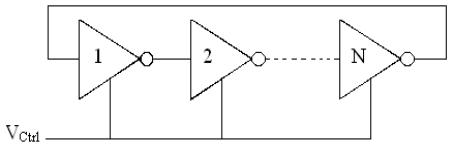

Fig. 1. *Single ended N-stage ring VCO*

The propagation time (t_d) of transition of signal through the complete chain determines the period of ring oscillator and is given by the equation (1) as

$$T = 2 \times N \times t_d \tag{1}$$

Here N is the number of inverters (delay stages) in a chain. The factor 2 results due to the fact that a complete cycle requires a low to high and high to low transitions. The equation (1) is valid only for $2Nt_d >> t_f + t_r$ (t_r and t_f are the rise and fall time periods, respectively). Thus the oscillation frequency can be expressed as

$$f_0 = \frac{1}{T} = \frac{1}{2Nt_d} \tag{2}$$

Hence the oscillation frequency of an N-stage ring oscillator can be tuned by varying the time delay of each stage [3,4].

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Also the oscillation frequency is inversely related to and depends only on the delay time (t_d) and the number N of delay stages. Also for the given interval of time, the signal passes through each stage is twice.

III. Current Starved Ring VCO

Ring oscillators can be realized by a number of ways. As frequency of oscillations depends on delay introduced by each inverter stage so delay should be voltage controlled. One way to control the dealy is to control the amount of current available to charge or discharge the capacitive load of each stage. This type of circuit is called a current starved ring VCO. In this VCO basically the control voltage (V_{ctrl}) modulates the turn-on resistances of the pull-down transistor and pull-up transistors through a current mirror. These variable resistances control the current available to charge or discharge the load capacitances. Large value of V_{ctrl} allows a large current to flow, producing a small resistance resulting into small delay. Current starved ring VCO uses variable bias currents to control its oscillation frequency as illustrated in Fig. 2 [5].

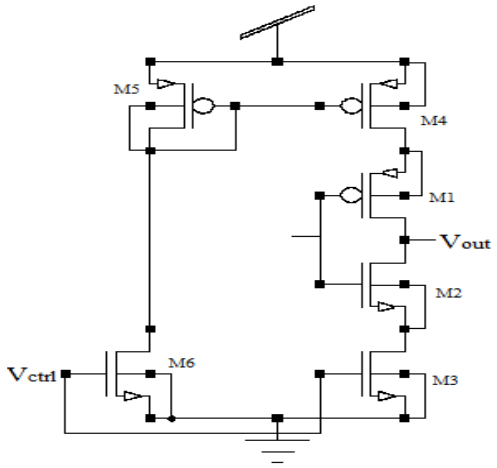

Fig. 2. *Delay stage for current starved ring VCO*

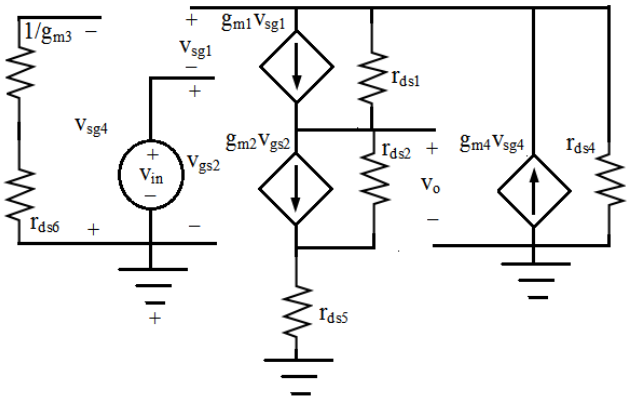

Fig. 3. *Small signal equivalent model of delay cell of current starved ring VCO*

The transistors $M1$ and $M2$ operate as inverters while $M3$ and $M4$ operate as current sink and current source respectively. The current sources limit the current available to inverters. The drain currents of transistors $M5$ and $M6$ are same and set by the input control voltage (V_{ctrl}). The current in transistors $M4$ and $M5$ are mirrored from bias stage to each inverting stage. The bias circuit is used to provide correct polarization for transistor $M3$ and $M4$ [6]. The benefit of this configuration is that the oscillation frequency can be tuned for a wide range by changing the value of control voltage. Fig. 3 shows the small signal equivalent model of a delay cell of starved ring VCO.

From the small signal equivalent model the incremental gain of current starved ring VCO can be given as

$$\frac{\Delta V_{Out}}{\Delta V_{In}} = 2 \tag{3}$$

Thus from equation (3), is the necessary gain condition of single delay cell.

The variation of control voltage (V_{ctrl}) determines the frequency range and linearity of VCO. The major drawback of this stage is longer rise/fall time when bias current is quite small because the voltage swing of the VCO becomes slower. In addition to this, if bias current is increased then the voltage headroom of the current source MOS transistors becomes narrow. The oscillation frequency (f_{osc}) is derived as follows. The total capacitance on the drains of $M3$ and $M4$ is given as.

(4)

$$C_{total} = C_{out} + C_{in}$$
$$= C_{ox}(W_p L_p + W_n L_n) + 3/2 C_{ox}(W_p L_p + W_n L_n)$$

where C_{in}, C_{out}, C_{ox} and C_{total} are the input capacitance, output capacitance, oxide related capacitance and total capacitance, respectively. The total capacitance is sum of the output and input capacitances of the inverter, and is given by

$$C_{total} = \frac{5}{2} C_{ox}(W_p L_p + W_n L_n) \tag{5}$$

The oscillation frequency is determined by the bias current (I_d), number of stages (N), total capacitance (C_{total}) and control voltage (V_{ctrl}) as

$$f_{osc} = \frac{I_d}{2NC_{total}V_{ctrl}} \tag{6}$$

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The relation between the control voltage V_{ctrl} and supply current (I_c) is given [7] as

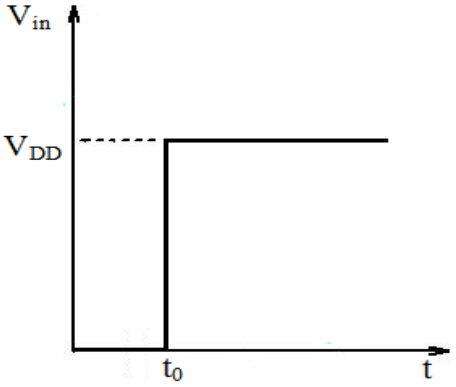
$$V_c - V_{th} = I_c R + \sqrt{\frac{2I_c}{k_n\left(W/L\right)}} \tag{7}$$

here k_n is the transconductance and V_{th} is the threshold voltage of transistor.

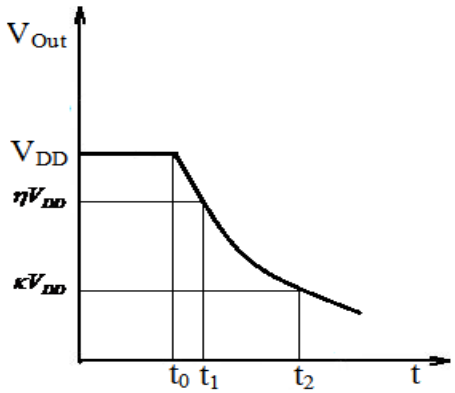
IV. Delay Analysis

As the frequency of oscillation of ring oscillator is determined by delay time of inverter stage, so calculation of delay time in terms of model parameters is necessary. By applying an ideal pulse to current starved inverter as shown in Fig. 4(a) the output is obtained which is given in Fig. 4(b). If delay time is proportional to $t_2 - t_0$, than it is needed to calculate value of $t_2 - t_0$. In this delay stage, gate voltage of transistor $M4$ is supplied through bias circuit which is determined by current of transistor $M5$. Current of transistor $M5$ is controlled by V_{ctrl}, which is applied at the gate of transistors $M6$ and $M3$.

Thus for $t_0 < t < t_1$, $V_{in} = V_{DD}$ and $V_{Out} = [V_{DD}, V_{DD} - V_t]$, transistor $M2 \rightarrow$ saturation, transistor $M3 \rightarrow$ saturation and transistor $M1 \rightarrow$ cut off.



(a)



(b)

Fig. 4. *(a) Input pulse and (b) Output of delay cell of current starved ring VCO*

Here current is determined by transistor $M3$, because current flowing through $M3$ is same as current of transistor $M6$ which is controlled by current mirror formed by transistors $M5$ and $M4$ respectively.

For, $V_{DD} - V_{th} < V_{out} < V_{DD}$ and $V_{DD} - V_{th} = \eta V_{DD}$ then $0 < \eta < 1$. Thus current (I_D) of transistor $M3$ is given by

$$I_{DS3} = \frac{1}{2} u_n C_{OX} \frac{W}{L}\left(V_{gs3} - V_{th}\right)^2 \tag{8}$$

$$dt = -\frac{C_L}{(1/2)u_n C_{OX}(W/L)\left(V_{gs3} - V_{th}\right)^2} dV_{out} \tag{9}$$

$$\int_{t_0}^{t_1} dt = -C_L \int_{V_{DD}}^{\eta V_{DD}} \frac{1}{I_{Dn}} dV_{out} \tag{10}$$

As $\left(V_{gs3} - V_{th}\right)$ is a constant value, hence we can write

$$\int_{t_0}^{t_1} dt = \frac{-2C_L}{u_n C_{OX}(W/L)\left(V_{gs3} - V_{th}\right)^2} \int_{V_{DD}}^{\eta V_{DD}} dV_{out} \tag{11}$$

also

$$t_1 - t_0 = \frac{-2C_L(1-\eta)V_{DD}}{u_n C_{OX}(W/L)\left(V_{gs3} - V_{th}\right)^2} \tag{12}$$

Thus for, $t_1 < t < t_2$, $\left(V_{gs3} - V_{th}\right)$ for Transistor $M2 \rightarrow$ Linear, and Transistor $M3 \rightarrow$ Saturation.

$$I_{C_L} \cong -I_{D2} = C_L \frac{dV_{out}}{dt} \tag{13}$$

For, $V_{out} < V_{DD} - V_{th}$

$$\int_{t_1}^{t_2} dt = -C_L \int_{\eta V_{DD}}^{\kappa V_{DD}} \frac{1}{I_{D2}} dV_{out} \tag{14}$$

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$$\int_{t_1}^{t_2} dt = -\frac{C_L}{u_n C_{OX}(W/L)} \int_{\eta V_{DD}}^{\kappa V_{DD}} \frac{1}{(V_{gs2}-V_{th})V_{ds2} - (1/2)V_{ds2}^2} dV_{out} \quad (15)$$

$$V_{ds2} = V_{out} - V_{ds3} \cong V_{out} \quad (16)$$

$$V_{gs2} \cong V_{in} = V_{DD} \quad (17)$$

$$t_2 - t_1 = \frac{C_L}{u_n C_{OX}(W/L)(V_{DD}-V_{th})} \ln\left(\frac{\eta-\kappa}{\kappa}\right) \quad (18)$$

After adding equation (12) and equation (18) we get $t_{delay} = t_2 - t_0$.

$$t_{delay} = \frac{2C_L(1-\eta)V_{DD}}{u_n C_{OX}(W/L)(V_{gs3}-V_{th})^2} + \frac{C_L}{u_n C_{OX}(W/L)(V_{DD}-V_{th})} \ln\left(\frac{\eta-\kappa}{\kappa}\right) \quad (19)$$

With the assumption of noisy supply voltage can be wriiten at for current starved inverter.

$$\Delta t \cong A \times \Delta V_{DD} + \frac{B}{\Delta V_{DD}} \quad (20)$$

$$A \cong \frac{2C_L(1-\eta)}{\mu_n C_{ox}(W/L)(V_{gs3}-V_{th})^2} \quad (21)$$

$$B \cong \frac{C_L}{\mu_n C_{ox}(W/L)} \ln\left(\frac{\eta-\kappa}{\kappa}\right) \quad (22)$$

$$0 < (V_{gs3}-V_{th}) < 1 \rightarrow (V_{gs3}-V_{th})^2 << 1$$

$$\frac{2C_L(1-\eta)}{\mu_n C_{ox}(W/L)(V_{gs3}-V_{th})^2} > \frac{C_L}{\mu_n C_{ox}(W/L)} \ln\left(\frac{\eta-\kappa}{\kappa}\right) \quad (23)$$

If $\ln\left(\frac{\eta-\kappa}{\kappa}\right) < 1$, $A > B$

So, Δt of current starved inverter is proportional to ΔV_{DD}.

V. Phase Noise Analysis

An electrical oscillator has three different noise regions with the noise power shaped ~1/Δf³, ~1/Δf and a constant noise floor, respectively. CMOS ring oscillators have a wide 1/Δf³-region because of the large 1/f-noise of short channel MOSFETs and the lack of passive resonant elements. Phase noise is result of low frequency fluctuations of the CMOS inverter propagation delays. The delay fluctuations are caused by the MOSFET drain currents that charge and discharge the node capacitances.

The rise and fall times of CMOS inverter can be expressed as.

$$t_{HL} = \frac{C_{node} V_{DD}}{\hat{I}_{DN}} \quad (24)$$

$$t_{LH} = \frac{C_{node} V_{DD}}{\hat{I}_{DP}} \quad (25)$$

Where $\hat{I}_{DN}$ and $\hat{I}_{DP}$ are the average peaks of the NMOS and PMOS drain currents I_{DN} and I_{DP} that charge and discharge the node capacitance C_{node}, respectively. The propagation delay for rising and falling edges is

$$t_{PHL} = \tfrac{1}{2} t_{HL},\ t_{PLH} = \tfrac{1}{2} t_{LH} \quad (26)$$

The cycle time T of a CMOS inverter ring oscillator with N-stages is.

$$T = \sum_{j=1}^{n} \left(t_{pHLj} + t_{pLHj}\right) \quad (27)$$

Low frequency MOSFET drain current noise appears as low frequency modulation of the average peak drain currents

$$\hat{I}_{DN,Pj}(t) = \hat{I}_{DN,P}\left(1 + n_{IN,Pj}(t)\right) \quad (28)$$

The current $\hat{I}_{DN,P}$ represents the nominal average peak current of the NMOS or PMOS and $n_{IN,Pj}$ represents the normalized, time-dependent deviation from the nominal value in stage j due to low-frequency drain current noise. Time dependent cycle time is

$$T(t) = \sum_{j=1}^{n} \left(t_{pHL}\left(1 - n_{INj}(t)\right) + t_{pLH}\left(1 - n_{IPj}(t)\right)\right) \quad (29)$$

$$T_0 = \sum_{j=1}^{n} \left(t_{pHL} + t_{pLH}\right) = n\left(t_{pHL} + t_{pLH}\right) = 2n\bar{t}_p \quad (30)$$

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where T_0 is nominal cycle time value. If power density spectrum of the normalized low - frequency drain current has discrete lines at $\pm f_m$ than the corresponding phase deviation is

$$\phi(t) = -\frac{4\pi t_{pHL} n_{IN}}{T_0^2 \omega_m} \sin(\omega_m t) = \phi_P \sin(\omega_m t) \tag{31}$$

Hence single-sideband phase noise is given by

$$\varsigma(\Delta f) = \frac{f_0^2}{\Delta f^2} \frac{1}{n} \left(\frac{t_{pHL}^2}{\bar{t}_p^{\,2}} n_{IN}^2(\Delta f) + \frac{t_{pLH}^2}{\bar{t}_p^{\,2}} n_{IP}^2(\Delta f) \right) \tag{32}$$

Figure of merit $\varsigma_{norm}(\Delta f)$ also called as normalized phase noise value is given as

$$\varsigma_{norm}(\Delta f) = \frac{1}{\Delta f} \frac{V_{DD}}{C_{OX} lm W n L_{eff}^2} \left[\left(\frac{I_{DC}}{\hat{I}_{DN}} \right)^3 KF_N + \left(\frac{I_{DC}}{\hat{I}_{DP}} \right)^3 KF_P \right] \tag{33}$$

where KF_N and KF_P are flicker noise coefficients and technology dependent parameters.

VI. Simulation Results

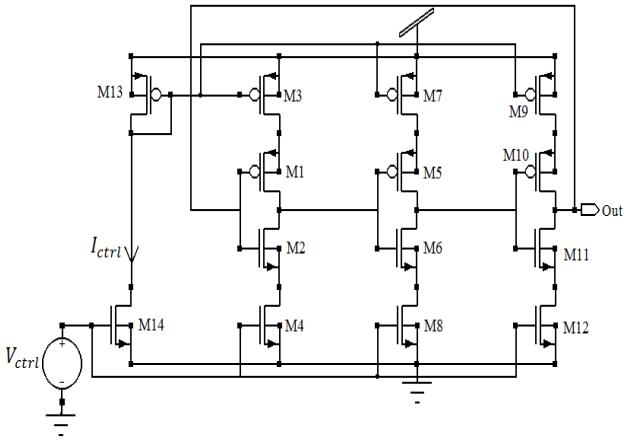

Fig. 5. *Schematic diagram of three stage current starved ring VCO*

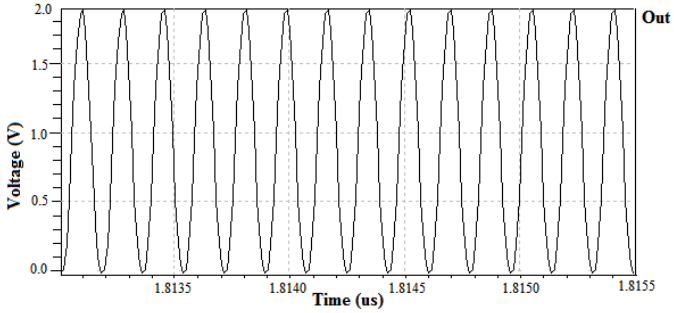

Fig. 6. *Output waveform of of three stage current starved ring VCO*

Fig. 5 shows the schematic diagram of basic three stage current starved ring VCO and Fig. 6 is the corresponding output waveform. Fig. 7 depicts the layout diagram of three stage current starved ring VCO which occupies area of $284\ \mu m^2$.

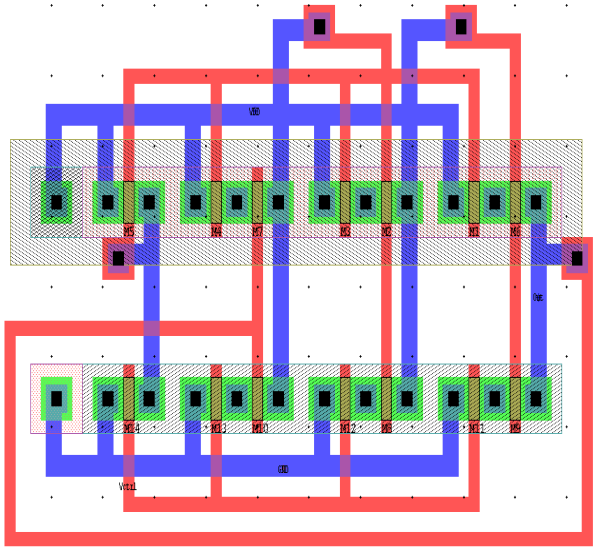

Fig. 7. *Layout diagram of three stage current starved ring VCO*

TABLE I. Simulation Results of Three Stage Current Starved Ring VCO using 180 nm CMOS Technology at Different Supply Voltages

Control Voltage (V)	Frequency (GHz) at 180 nm CMOS Technology		
	Supply Voltage 1V	*Supply Voltage 2V*	*Supply Voltage 3V*
0.4	0.1703	0.3831	0.6289
0.6	0.8474	1.2520	1.6066
0.8	1.1549	2.1985	2.0516
1.0	1.2267	2.7355	2.8716

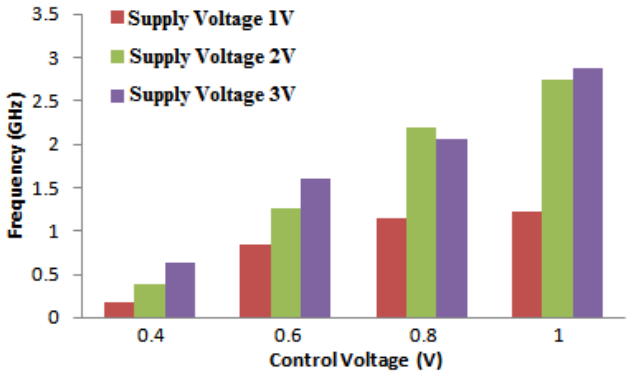

Fig. 8. *Comparative analysis of frequency at different supply voltages*

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The further analysis includes the effect of technology and supply voltages. Table I summarizes the variation of oscillation frequency for supply voltages at 180 nm CMOS technology with variation of control voltages and it is graphically shown in Fig. 8. Table II and Table III illustrate the effect of CMOS technologies on frequency of oscillation and power consumption and their respective plots are shown in Fig. 9 and Fig. 10.

TABLE II. SIMULATION RESULTS OF THREE STAGE CURRENT STARVED RING VCO AT DIFFERENT TECHNOLOGY

Control Voltage (V)	Frequency (GHz) at Supply Voltage 3V		
	Technology 90 (nm)	*Technology 130 (nm)*	*Technology 180 (nm)*
0.4	1.373	0.938	0.6289
0.5	1.818	1.356	0.8385
0.6	2.799	2.206	1.6066
0.7	3.104	2.801	1.8265
0.8	3.285	3.150	2.0516
0.9	3.405	3.317	2.6278
1.0	3.513	3.392	2.8716

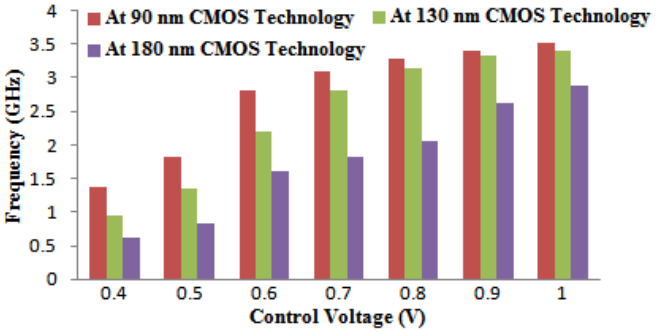

Fig. 9. *Comparative analysis of frequency at different CMOS technologies*

TABLE III. POWER CONSUMPTION OF THREE STAGE CURRENT STRARVED RING VCO AT DIFFERENT TECHNOLOGY

Control Voltage (V)	Power Consumption (mW) at Supply Voltage 3V		
	Technology 90 (nm)	*Technology 130 (nm)*	*Technology 180 (nm)*
0.4	0.9562	0.7900	0.5494
0.5	2.4532	1.8000	1.6239
0.6	3.6710	3.0698	2.1568
0.7	4.9001	4.5067	3.2578
0.8	6.9008	5.7316	4.0300
0.9	7.1567	6.7380	4.8321
1.0	8.9865	7.5984	5.5641

It can be said that with advancement in technology frequency achieved up to $3.5\,GHz$ at 90 nm technologies with trade off of power consumption.

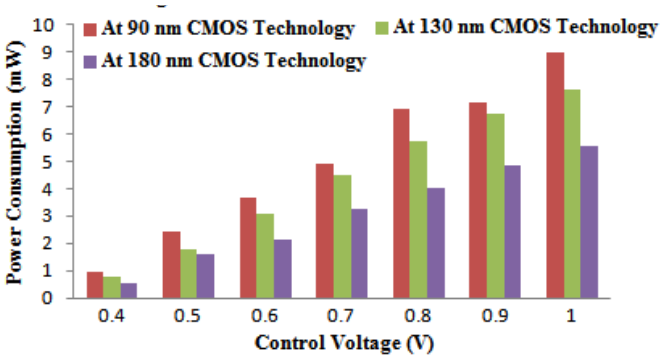

Fig. 10. *Comparative analysis of power consumption at different CMOS technologies*

VII. CONCLUSION

In this paper the design, analysis, modeling and implementation of current starved ring VCO is done. The major aspect of analysis was phase noise, delay and layout area. From the simulation results given in different tables it can be said that higher oscillation frequency can be achieve by increasing control voltage and at high technology. The frequency of $3.5\,GHz$ is achieved at 90 nm CMOS technology. Oscillation frequency can also be changed by variation in supply voltages.

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