

# A Highly Linear OTA-Less 1-1 MASH VCO-Based $\Delta\Sigma$ ADC With an Efficient Phase Quantization Noise Extraction Technique

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**Abstract**—In this article, an efficient technique is introduced to extract the quantization noise of a multi-phase voltage-controlled oscillator (VCO)-based quantizer (VCOQ) in the time domain as a pulsedwidth modulated (PWM) signal. Using this technique, a new highly linear VCO-based 1-1 multi-stage noise shaping (MASH) delta-sigma analog-to-digital converter (ADC) structure is presented. This architecture does not require any operational transconductance amplifier (OTA)-based analog integrators or power-hungry linearization methods. The first stage is a closed-loop multi-phase VCO-based voltage-to-phase (V-to-P) converter, and the second stage is an open-loop multi-phase VCO-based voltage-to-frequency (V-to-F) converter. Using the proposed technique, the phase quantization error of the first stage is extracted as a pulse signal and then fed to the second stage. The input of the first VCO is a very small amplitude signal, and the input of the second VCO is a two-level PWM signal. Therefore, the VCO non-linearity does not limit the overall ADC performance, mitigating the need for power-hungry linearization methods. The prototype achieves second-order noise shaping with a DR/SFDR/SNR/SNDR of 82.7/88.7/80.3/79.7 dB for an input signal BW of 2 MHz. The fabricated design consumes 1.248 mW from a 0.9-V supply.

**Index Terms**—Analog-to-digital converter (ADC), delta-sigma modulator, multi-stage noise shaping (MASH), nonlinearity, pulsedwidth modulated (PWM) generator, voltage-controlled oscillator (VCO)-based quantizer (VCOQ).

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## I. INTRODUCTION

CONVENTIONAL  $\Delta\Sigma$  analog-to-digital converters (ADCs) utilize operational transconductance amplifiers (OTAs) in their loop filter implementation followed by multi-bit voltage-domain quantizers. With process scaling, the intrinsic gain of the transistors as well as the voltage headroom decreases. This makes OTA design increasingly more difficult in advanced CMOS processes. Also, since the voltage headroom reduces, the multi-bit voltage domain quantizers become more difficult to design due to their noise and offset requirements.

Recently, there has been a lot of research focus on finding alternative digital solutions to replace traditional analog blocks. Time-domain quantization methods, such as using voltage-controlled oscillator (VCO)-based quantizers (VCOQs), are an attractive alternative. VCOs are implemented using simple inverters. Due to their highly digital nature, they benefit from technology scaling. As the transistor dimension reduces, the inverter delay decreases, which results in a higher timing resolution of the VCO-based ADCs. Moreover, VCO-based ADCs feature inherent quantization noise shaping and guaranteed monotonicity. Despite these advantages, the VCO nonlinearity often limits the performance of these ADCs. Several techniques have been introduced to increase the order of noise shaping and mitigate the VCO nonlinearity.

In [1], a VCOQ is placed in a closed loop and is used as a voltage-to-frequency (V-to-F) converter. The high in-band gain of the filter preceding the VCOQ reduces the VCO nonlinearity. However, to provide more than first-order noise shaping, this architecture requires OTAs. In [2], a residue cancellation architecture is used to reduce the VCO nonlinearity effect. A coarse flash ADC is used before the VCO to reduce the voltage swing at the input of the VCO. Since the input voltage swing of the VCO is small, this method suppresses the VCO nonlinearity. To achieve more than first-order noise shaping, this architecture also requires OTAs. To cancel VCO nonlinearity, two-stage architectures were used in [3]–[5]. In [3], each stage is an open-loop VCOQ. Even though no OTAs were used, the order of noise shaping is limited to one. To increase the noise-shaping order, [4] and [5] employ OTAs in their loop filters. In [6] and [7], the input of the VCOs is

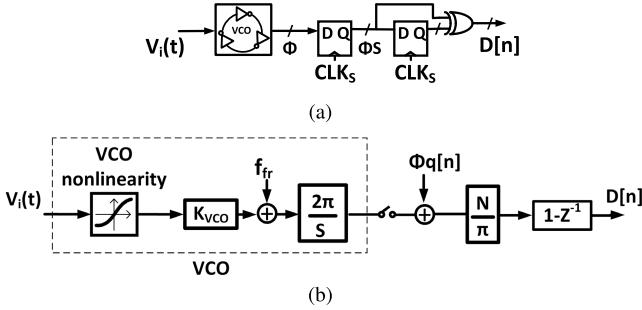


Fig. 1. Open-loop first-order VCO-based V-to-F converter. (a) Conceptual realization. (b) Block diagram.

a pulsewidth modulated (PWM) signal. Since the VCOs are forced to work at only two frequencies, they are inherently linear. However, power-hungry PWM generators are needed at the input to avoid performance degradation. In [8]–[11], the VCO-based ADC is used as a voltage-to-phase (V-to-P) converter. Since the VCO acts as an integrator followed by a quantizer, its input signal swing reduces, and therefore, the VCO nonlinearity is mitigated. This architecture also uses OTAs to implement higher order noise shaping. Second-order OTA-less  $\Delta\Sigma$  ADCs were implemented in [12] and [13]. Reference [12] features a passive integrator to increase the order of noise shaping of a V-to-P converter, and [13] uses two VCOs as integrators to form a single loop delta-sigma ADC. While no OTA is used in these architectures, their performance is limited to around 11 bits. Also, a third-order OTA-less modulator is introduced in [14]. Although linearity-enhanced VCOs are used, the linearity of the modulator is still limited to 10.5 bits.

In this article and [15], a novel highly linear OTA-less 1-1 multi-stage noise shaping (MASH) VCO-based ADC is proposed. The first stage is a closed-loop VCO-based ADC, where a multi-phase VCOQ is used as a V-to-P converter. An efficient technique is introduced to extract the quantization noise of a multi-phase VCOQ in the time domain as a PWM signal. The PWM signal is then applied to the second stage, which is an open-loop multi-phase VCOQ used as a V-to-F converter. Since the first stage is a closed-loop V-to-P converter and the input of the second stage is a PWM signal, the VCO nonlinearity is mitigated in this architecture. The prototype achieves second-order noise shaping with high linearity without using OTAs.

The rest of this article is organized as follows. The architectural level of the 1-1 MASH VCO-based ADC is presented in Section II. In Section III, the efficient quantization noise extraction of a multi-bit VCOQ is elaborated. The implementation details are discussed in Section IV. In Section V, the effect of non-idealities are explained. Section VI provides the measurement results, and finally, Section VII concludes this article.

## II. ARCHITECTURAL-LEVEL ANALYSIS OF OTA-LESS 1-1 MASH VCO-BASED ADC

In this section, first, the basic concept of first-order V-to-F and V-to-P conversion is described. Then, the system-level

concept of the proposed architecture is provided. This architecture achieves second-order noise shaping and mitigates the VCO nonlinearity without using OTAs or power-hungry linearization methods.

### A. Open-Loop First-Order VCO-Based V-to-F Converter

A conceptual realization of an open-loop first-order VCO-based V-to-F converter is shown in Fig. 1(a). The VCO consists of back-to-back connected delay cells. Compared to single-phase VCOQs that only use the information of one VCO output tap, multi-phase VCOQs use multiple VCO output taps. In Fig. 1, the frequency of the VCO is controlled by  $V_i(t)$ , and the VCO output phase is defined as

$$\phi(t) = \int_{-\infty}^t (2\pi K_{VCO} V_i(t) + 2\pi f_{fr}) dt \quad (1)$$

where  $K_{VCO}$  and  $f_{fr}$  are the V-to-F gain and the free-running frequency of the VCO, respectively. Assuming  $N$  delay cells are used for the VCO implementation, each  $\pi/N$  phase change of the VCO translates to one delay element output change. As can be seen in Fig. 1(a), a set of registers is used to sample the VCO output phase taps. The current sampled values are then differentiated with the previous sampled values using a set of XOR gates to generate the output. The output represents the VCO output phase change between the two sampling instances. It is proportional to the frequency of the VCO as well as the input signal. Fig. 1(b) shows the block diagram of the first-order V-to-F converter. Since the phase digitization occurs at the sampling of the VCO output taps, the quantization error ( $\phi_q$ ) that is in the phase domain is added after the VCO and before the differentiator ( $1 - z^{-1}$ ). The output of the VCOQ is

$$D[n] = \int_{(n-1)T_S}^{nT_S} 2N(K_{VCO} V_i(t) + f_{fr}) dt + \frac{N}{\pi} [\phi_q(nT_S) - \phi_q((n-1)T_S)]. \quad (2)$$

Approximating the continuous time integration as a discrete-time integration and using  $z$ -transforms, the output is

$$D(z) = (2NK_{VCO} T_S z^{-1}) V_i(z) + 2N f_{fr} T_S + \left(\frac{N}{\pi}\right) (1 - z^{-1}) \phi_q(z) \quad (3)$$

where  $\phi_q$  is the phase quantization noise and has a value between  $[0-(\pi/N)]$ . This architecture provides first-order noise shaping and has a very digital friendly implementation. Notice that since the input signal is directly connected to the input of the VCO, a large-signal swing can produce high-amplitude harmonics and degrade the performance significantly.

### B. Closed-Loop First-Order VCO-Based V-to-P Converter

In conventional implementations of V-to-P converters [8], [9], the intrinsic dynamic element matching (DEM) capability of a VCOQ is lost. Therefore, an additional DEM block is required to address the DAC mismatch issue. In [10], a novel implementation of a closed-loop  $\Delta\Sigma$  ADC using a VCO-based integrator is introduced, which provides an intrinsic DEM

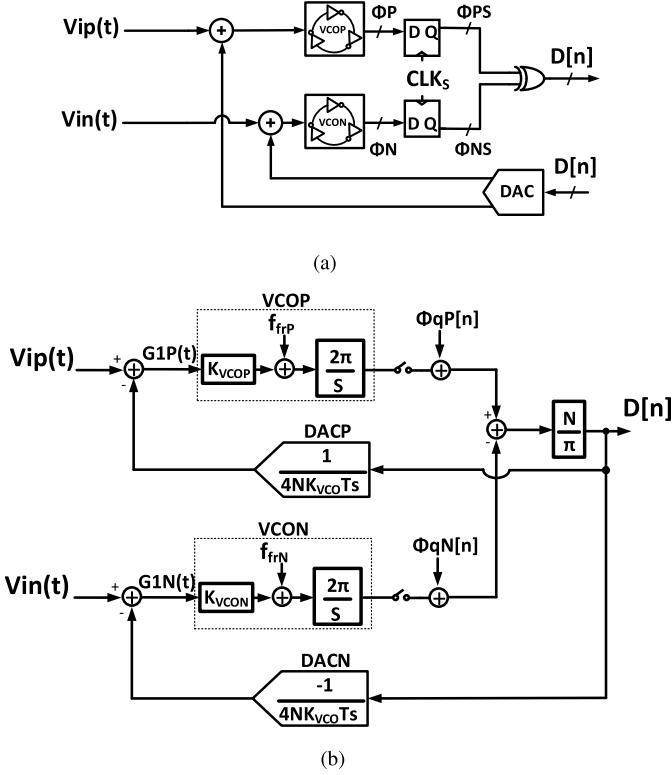


Fig. 2. Closed-loop first-order VCO-based V-to-P converter. (a) Conceptual realization. (b) Block diagram.

scheme of clocked averaging (CLA). This architecture is shown in Fig. 2(a). In this architecture, two VCOs are used in a pseudo-differential manner. The output phase is measured by comparing the output phase of the two VCOs to each other and then fed back to the input using a thermometer DAC. As shown in [10], in this architecture, the free-running frequency of the VCOs can be chosen freely, and also, this architecture does not need an explicit DEM block. Fig. 2(b) shows the block diagram of the closed-loop first-order V-to-P converter. Since the phase of each VCO is sampled before being compared using the XOR gates, two independent noise sources,  $\phi_{qP,N}$ , exist in the system. Fig. 2(b) shows a first-order CT  $\Delta\Sigma$  assuming the feedback gain is the inverse of the integration gain. Therefore, considering the two VCOs are identical ( $K_{VCOP,N} = K_{VCO}$  and  $f_{frP,N} = f_{fr}$ ), the output is

$$D(z) = (2NK_{VCO}T_S z^{-1}) V_{id}(z) + \left(\frac{N}{\pi}\right) (1 - z^{-1}) (\phi_{qP}(z) - \phi_{qN}(z)) \quad (4)$$

where  $V_{id}$  is the differential input signal. In (4), the continuous time integration is approximated as a discrete-time integration.

### C. Proposed Multi-Phase VCO-Based 1-1 MASH ADC

Fig. 3 shows the conceptual block diagram of the proposed multi-phase VCO-based 1-1 MASH ADC. For the sake of simplicity, a single-ended architecture is shown in this block diagram, while the real implementation is pseudo-differential. In this architecture, the first stage is a closed-loop first-order V-to-P converter, and the second stage is an open-loop V-to-F converter. The quantization noise of the first stage that is in the phase domain is extracted in the time domain as

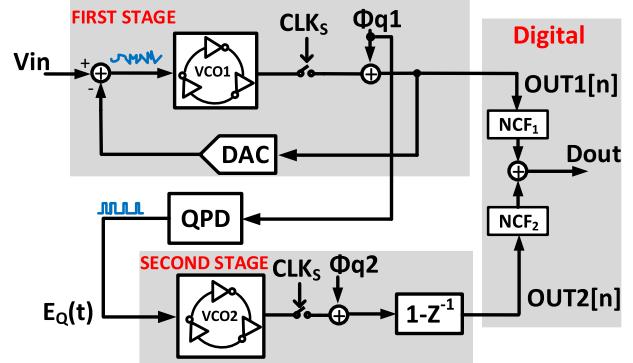


Fig. 3. Block diagram of the proposed 1-1 MASH ADC.

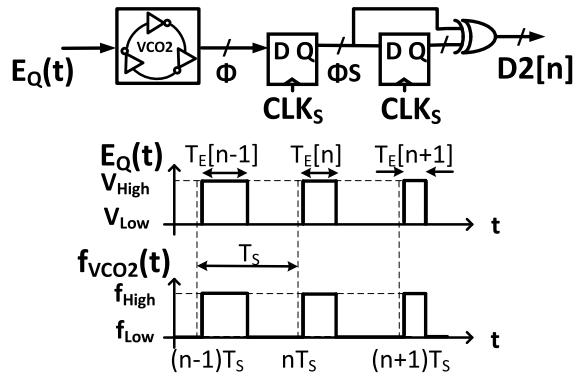


Fig. 4.  $f_{VCO2}(t)$  behavior when a PWM signal is applied to its input.

a PWM signal [ $E_Q(t)$ ] and fed to the second stage. The quantization noise extraction is done using a quantization phase detector (QPD) block. The detailed implementation of the QPD block is explained in Section III. Since  $VCO_1$  is used as an integrator, its input voltage variation is small; therefore,  $VCO_1$  nonlinearity is suppressed. Also, since the input signal of  $VCO_2$  is a two-level PWM signal,  $VCO_2$  operates at only two frequencies, which makes the second-stage VCO inherently linear.

Fig. 4 shows the  $VCO_2$  frequency [ $f_{VCO2}(t)$ ] change when the PWM signal of  $E_Q(t)$  is applied to its input.  $f_{VCO2}(t)$  switches between  $f_{Low}$  and  $f_{High}$  when  $E_Q(t)$  changes from  $V_{Low}$  to  $V_{High}$ .

Assuming  $E_Q(t)$  is always equal to  $V_{Low}$  at the sampling instances and its pulsewidth is a sampled signal, as shown in [16], and using  $z$ -transforms, the output is

$$D_2(z) = 2N(f_{High} - f_{Low})z^{-1}T_E(z) + 2NT_S f_{Low} + \left(\frac{N}{\pi}\right)(1 - z^{-1})\phi_{q2}(z) \quad (5)$$

where  $T_E$  is the pulsewidth of  $E_Q(t)$ .

As can be seen, the time-domain information ( $T_E$ ) goes to the output with a linear gain of  $2N(f_{High} - f_{Low})$ , and the quantization noise is first-order shaped. In (5),  $2NT_S f_{Low}$  is a constant value and can be removed in a pseudo-differential architecture.

Fig. 5 shows the linear model block diagram of the 1-1 MASH ADC. As shown in Section III, the QPD block converts the quantization error from the phase domain to the

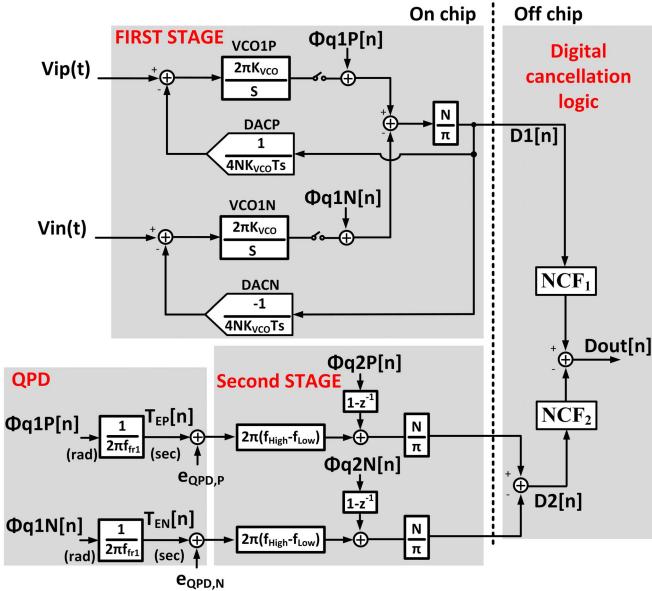


Fig. 5. Linear model of the proposed 1-1 MASH ADC.

time domain with a gain of  $1/(2\pi f_{\text{fr}1})$ . In Fig. 5,  $e_{\text{QPD},P,N}$  are the QPD error added due to the mismatch in QPD. The effect of mismatch in QPD is explained in Section V-C1. Based on the linear model shown in Fig. 5 and considering  $e_{\text{QPD},P,N} = 0$ , first-stage output ( $D_1[n]$ ) and the second-stage output ( $D_2[n]$ ) are

$$\left\{ \begin{array}{l} D_1(z) = (2NK_{\text{VCO}1}T_S z^{-1})V_{id}(z) \\ \quad + \left(\frac{N}{\pi}\right)(1-z^{-1})(\phi_{q1P}(z) - \phi_{q1N}(z)) \\ D_2(z) = \left(\frac{N}{\pi}\right)\frac{(f_{\text{High}} - f_{\text{Low}})}{f_{\text{fr}1}}z^{-1}(\phi_{q1P}(z) - \phi_{q1N}(z)) \\ \quad + \left(\frac{N}{\pi}\right)(1-z^{-1})(\phi_{q2P}(z) - \phi_{q2N}(z)). \end{array} \right. \quad (6)$$

In order to cancel  $\phi_{q1}$  and second-order shape  $\phi_{q2}$ , the following noise cancellation filters (NCFs) are required:

$$\begin{aligned} \text{NCF}_1(z) &= z^{-1} \\ \text{NCF}_2(z) &= \frac{f_{\text{fr}1}}{(f_{\text{High}} - f_{\text{Low}})}(1-z^{-1}) = \frac{(1-z^{-1})}{G}. \end{aligned} \quad (7)$$

Therefore, the final output can be derived as

$$\begin{aligned} D_{\text{OUT}}(z) &= (2NK_{\text{VCO}1}T_S z^{-2})V_{id}(z) \\ &\quad + \left(\frac{N}{\pi}\right)\left(\frac{f_{\text{fr}1}}{f_{\text{High}} - f_{\text{Low}}}\right)(1-z^{-1})^2 \\ &\quad \times (\phi_{q2P}(z) - \phi_{q2N}(z)). \end{aligned} \quad (8)$$

As seen in (8), the second-stage quantization noise is second-order shaped.

### III. PROPOSED QUATIZATION NOISE EXTRACTION TECHNIQUE

When VCOQ is operating as a V-to-P converter, the quantization noise, which is in the phase domain ( $\phi_q$ ), is not explicitly available. In this section, an efficient method to extract  $\phi_q$  in the time domain is presented.

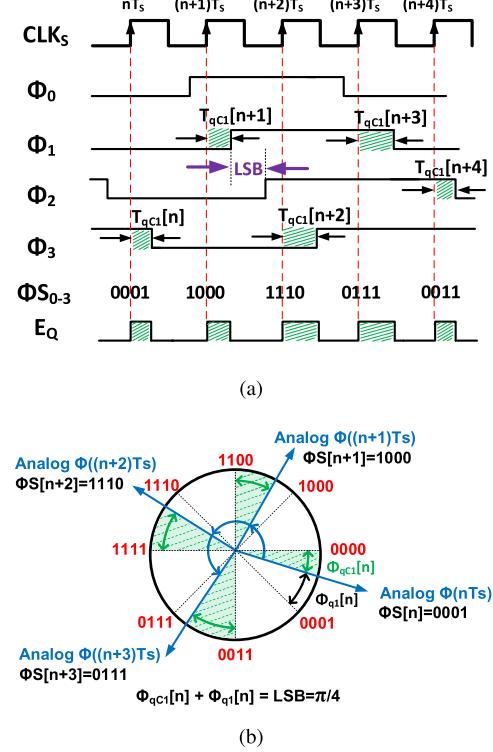


Fig. 6. VCO1 output and phase quantization noise. (a) Timing diagram. (b) Phase diagram. [17].

Fig. 6(a) and (b) shows the timing and phase diagrams of one of the multi-phase VCOQs used in the first stage, respectively. For the sake of simplicity, a 2-bit VCOQ is illustrated, while the actual implementation utilizes 5-bits.  $\phi_i$ s are the output phase taps of the VCO, and  $\phi_{S,i}$  is the sampled VCO output code. As shown in Fig. 6(a), the information propagates from  $\phi_0$  to  $\phi_3$ . Thus, when  $\phi_0$  goes from low to high,  $\phi_1$  does the same thing after some delay. Therefore, looking at the  $\phi_S$  code, there is always either all zeros on the left and ones on the right, or vice versa. This characteristic is used later on to extract the quantization noise.

$\phi_q$  is the quantization noise, and it is in the phase domain.  $\phi_{qC1}$  is defined as  $LSB - \phi_{q1}$ , which is easier to extract in the time domain compared to  $\phi_{q1}$ .  $\phi_{qC1}$  is the amount of VCO phase change from the rising edge of  $CLK_S$  to the transition edge of one of the VCO output phase taps, which toggles first after the rising edge of  $CLK_S$  in each sampling period. This time period is shown as  $T_{qC1}$  in Fig 6(a).  $\phi_{qC1}$  (the shifted version of  $\phi_{q1}$ ) can be extracted in the time domain, as described in the following.

$\phi_{qC1}$  is defined as

$$\phi_{qC1}[n] = \int_{T_{qC1}[n]} 2\pi f_{\text{VCO}1} dt. \quad (9)$$

As (9) shows,  $\phi_{qC1}[n]$  is the integration of the VCO frequency over the time period of  $T_{qC1}[n]$ . Since VCO<sub>1</sub> is in a closed loop, the input signal variation of VCO<sub>1</sub> is small. Therefore, the VCO<sub>1</sub> frequency variation is also small, resulting in a linear relationship between  $\phi_{qC1}[n]$  and  $T_{qC1}[n]$ , as shown in the following equation:

$$\phi_{qC1}[n] \approx 2\pi f_{\text{fr}1} T_{qC1}[n]. \quad (10)$$

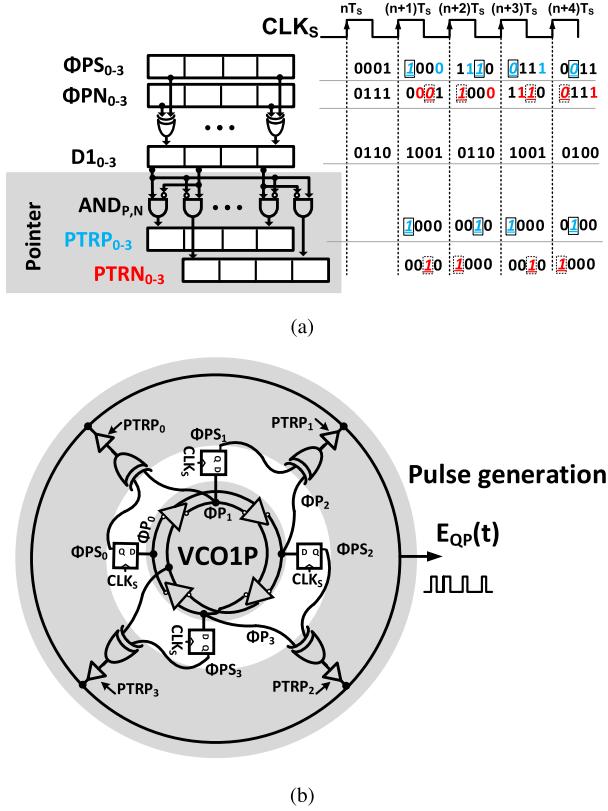


Fig. 7. Phase quantization noise extraction in the time domain as a PWM signal. (a) Detecting the proper output phase tap carrying  $\phi_{QC1}$ . (b) PWM pulse generation corresponding to  $\phi_{QC1}$ .

Since there is a linear relationship between  $\phi_{QC1}$  and  $T_{qC1}$ , the quantization noise can be represented in the time domain. The accuracy of (10) depends on the  $f_{VCO1}$  variation. The shaded areas in Fig. 6(a) show the representation of  $\phi_{QC1}$  in the time domain ( $T_{qC1}$ ). The LSB difference between  $\phi_q1$  and  $\phi_{QC1}$  does not affect the performance of the ADC since it is canceled in the digital filter NCF<sub>2</sub>.

As shown in Fig. 6(a), only one of the VCO output taps carries a valid  $\phi_{QC1}$  signal during each sampling period. Therefore, extracting  $\phi_{QC1}$  in the time domain requires first detecting the proper output phase tap carrying  $\phi_{QC1}$ . Next, the PWM pulse corresponding to  $\phi_{QC1}$  has to be generated. The desired extracted pulse is shown as  $E_Q(t)$  in Fig. 6(a).

To select the proper output phase tap of  $VCO_{1P,N}$  at each sampling instance, the VCO phase information in the last sampling period can be used. By knowing which of the VCO phase taps had the last transition in the previous sampling period, the next phase tap is the one carrying the quantization noise. As an example, looking at the  $(n+2)T_s$  sampling instance of Fig. 6(a),  $\phi_2$  had the last transition, and therefore,  $\phi_3$  is carrying  $\phi_{QC1}$ . To detect the last transition, the  $\phi_S$  code can be used. As mentioned earlier, the zeros or ones are propagating from left to right in the  $\phi_S$  code. Therefore, the transition from zero to one or one to zero in the  $\phi_S$  code represents the phase tap that had the last transition. This is derived from the circuit shown in Fig. 7(a). The operation of this circuit is also shown in the same picture. The first-stage

output (D1) is applied to two sets of AND gates ( $AND_{P,0-3}$ ) to generate two-pointer ( $PTR_{P,N}$ ) signals. During each sampling period, the output of a single AND gate in each set toggles high (indicating the phase tap that has the last transition in the previous sampling period).

After detecting the phase tap that has the last transition in the previous sampling period, the PWM pulse that represents  $\phi_{QC1}$  in the time domain can be simply generated by using two sets of XOR gates followed by tri-state buffers. Fig. 7(b) shows the PWM generation for  $VCO_{1P}$ . As shown in Fig. 7(b), each sampled VCO phase tap is XORed with the next phase tap. These XOR gates generate different pulses at the output. Next, the pointer signal (PTR) selects the one that carries  $\phi_{QC1}$  through a tri-state buffer. In this way, the desired PWM pulse is generated. Both the pointers and the PWM generator blocks have been implemented using simple combinational logic with a similar design implemented for  $VCO_{1N}$ .

Similar phase quantization noise extraction technique can be used in the other ADC architectures, such as 0-1-1 MASH ADC [18] or 0-2 MASH ADC [19], with SAR ADC used in the first stage, both providing only simulation results.

#### IV. CIRCUIT DETAILS

The simplified schematic of the proposed 1-1 MASH  $\Delta\Sigma$  modulator and its timing is shown in Fig. 8. The first stage is a first-order CT  $\Delta\Sigma$  modulator. The input signal is connected to a pair of 2.5-k $\Omega$  resistors. The output of the first stage is subtracted from the input signal through a pair of 32-element resistive DACs. Each DAC element is an 80-k $\Omega$  resistor. Then, the difference between the input and the output of the first stage is applied to a pair of VCOs. The outputs of VCO<sub>1</sub>s are sampled and then compared together, using XOR gates to generate the first-stage output. Since there are two VCOs in the first stage and their outputs are being sampled before being compared together, two separate quantization noise sources exist in the first stage. To extract the first-stage quantization noise, the QPD block is used. The implementation of the QPD block is also pseudo-differential. As shown in Fig. 8, most of the QPD blocks are implemented by combinational logic. The extracted pulses are then applied to the second stage. The second stage consists of two open-loop VCOs followed by frequency encoders. To complete the MASH structure, NCF<sub>1</sub> and NCF<sub>2</sub> are used at the output of the first and second stages, respectively. Next, the key building blocks of the modulator are described.

##### A. VCOs

The 32-stage (5-bit) VCOs have been used in both stages. Fig. 9 shows the delay cells used in the first-stage VCOs. Each delay cell consists of four cross-coupled inverter pairs. The width of the outer pair is designed to be four times more than the inner pair. The frequency of  $VCO_{1P,N}$  is adjusted by controlling the tail current. Since VCO<sub>1</sub> thermal noise is directly added at the input, large-size delay cells have been used to lower the VCO<sub>1</sub> phase noise.

In this design, the VCO<sub>2</sub> delay cells have been implemented by two cross-coupled inverter pairs. Here, also the width of

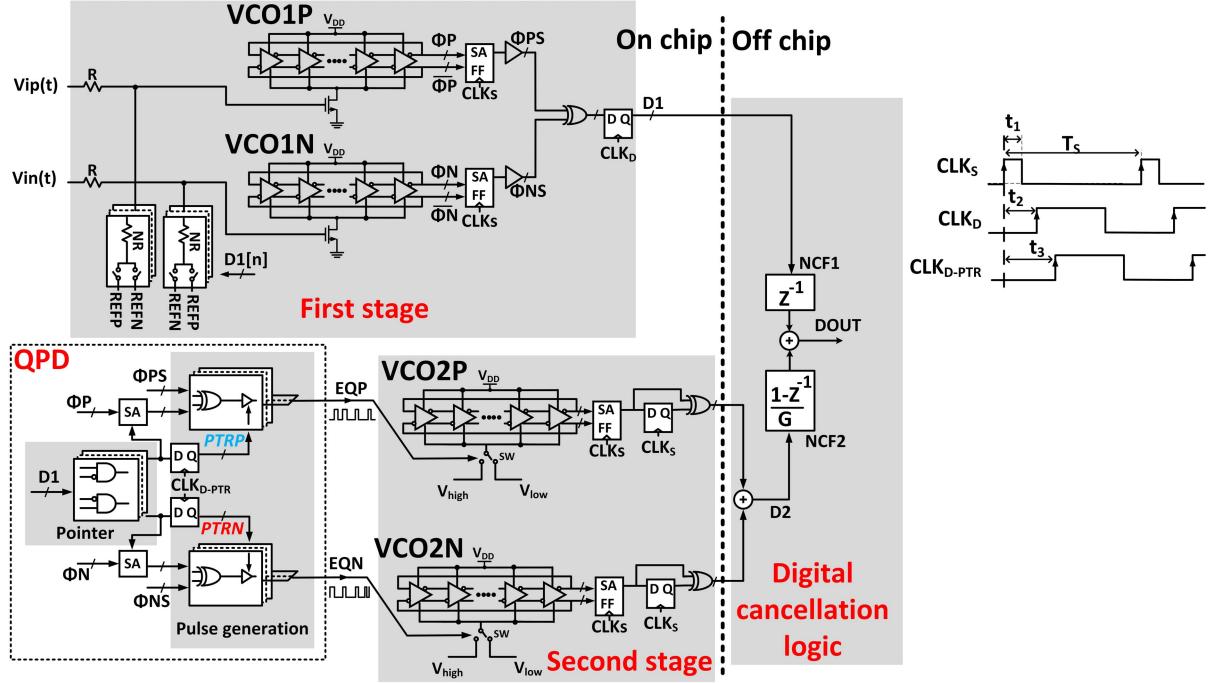


Fig. 8. Simplified schematic of the proposed 1-1 MASH ADC.

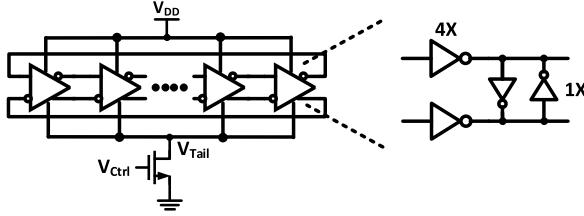


Fig. 9. Delay cell used in the first-stage VCO.

the inner pair is one-fourth of the outer pair. Unlike the first-stage VCOs, no tail current is used in the second-stage VCOs, and the frequency of the VCOs is controlled by changing their ground voltage. Since the input-referred thermal noise of the second stage is shaped by the first order, standard cell inverter gates with the minimum length are used to simplify the design and the layout. The frequency of the second-stage VCO is changed by switching the ground voltage of  $VCO_{2P,N}$  between  $V_{High}$  and  $V_{Low}$  through a pair of T-gate switches.

Based on (8), a higher value of  $G$  [ $(f_{High} - f_{Low})/f_{fr1}$ ] is desired to reduce the effect of the second-stage quantization noise at the output. Lower values of  $f_{fr1}$  help with increasing  $G$  as well as relaxing the phase noise of VCO<sub>1</sub>s. Note that lowering  $f_{fr1}$  will make the linear approximation of the phase to time-domain quantization noise [shown in (10)] less accurate, which results in more  $\phi_{q1}$  leakage to the output and hence a performance degradation. Also, to increase  $G$ , a higher value of  $(f_{High} - f_{Low})$  is desired. It is important to make sure that  $(f_{High} - f_{Low})$  is not too high such that it saturates the second-stage output. In order to avoid second-stage saturation, the phase change between two samples of the VCO<sub>2</sub> output

phase must be less than  $\pi$  radians. Also, since the dominant source of noise at the output is the thermal noise (as shown in Section V-D), increasing  $(f_{High} - f_{Low})$  after some point would not affect the SNDR and only increases the second-stage power consumption.

### B. Sense Amplifiers

The VCOs output signals are not rail-to-rail. Therefore, sense amplifier (SA) blocks are needed to convert these signals to rail-to-rail and feed them to the following digital circuitry.

As can be seen in Fig. 8, SA flip-flops (SA-FFs) are used in the first and second stages. SA-FFs only operate on the rising edge of the  $CLK_S$ , and they keep their output values on the rest of the time. This way, they consume a small amount of power. On the other hand, the SAs used in the QPD block are required to operate continuously, and therefore, their power consumption can be high. Fig. 10 shows the schematic of the implemented SA. To avoid the high power consumption of the SAs used in the QPD block, only one SA is ON during each sampling period, and the rest of the 31 SAs are kept OFF. The proper SA is selected using the PTR signal. This way, the corresponding VCO output tap is amplified rail-to-rail and sent to the pulse extraction circuit.

### C. Pulse Extension

As can be seen in (10), the pulselength has a linear relationship with  $\phi_{q1}$ . Therefore, this pulselength can be very narrow. If it is too small, the pulse cannot be completely generated due to the non-zero rise/falls time of the QPD block. In addition, in practice, if the pulselength is too small, the second-stage VCO frequency cannot reach its expected high frequency

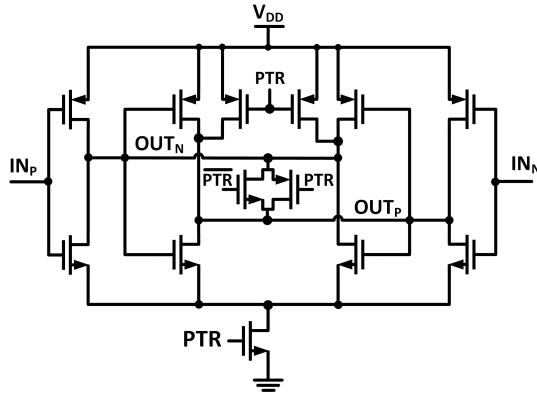


Fig. 10. Schematic of the SA.

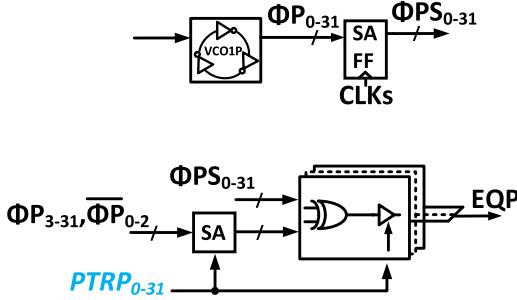


Fig. 11. Pulse extension.

before the pulse goes down again. In this case, some of  $\phi_{qC1}$  will be lost, which will result in performance degradation. To avoid this issue, a method similar to dead-zone elimination in PLLs is used. In the applied pulse extension technique, an offset is added to all the pulses [6]. This ensures that the frequency of second-stage VCO is able to switch completely between  $f_{\text{High}}$  and  $f_{\text{Low}}$  for any  $\phi_{qC1}$  value.

In this design, an offset value of two LSBs is added to all the samples. Fig. 11 shows the modified pulse generation circuit, where the pulse extension technique is incorporated. By XORing each sampled VCO phase tap ( $\phi_{PS,i}$ ) with the third next phase tap ( $\phi_{P,i+3}$ ), two LSBs are added to all the samples. Note that due to the usage of the pulse extension technique, the limited rise/fall times would not affect  $\phi_{qC1}$  extraction if the added time offset size is designed to be larger than the rise time to let  $E_{Q1}(t)$  settle to the high value before it has to go to the low value again [20].

Since the offset value of two LSBs is added to all the pulses, the maximum  $E_{Q1}(t)$  pulselength could be approximately  $3 \times$  LSB. In order to avoid loss of information,  $E_{Q1}(t)$  needs to be at its low value at the sampling instances; otherwise, the pulse will interfere with the next sample in the pulse generation. Therefore, the maximum  $E_{Q1}(t)$  pulselength ( $3 \times$  LSB) needs to be smaller than  $T_S$ . Each LSB size in the time domain is  $1/(2 \times N \times f_{\text{fr1}})$ . Since  $N=32$  and  $T_S = 8$  ns in this prototype,  $f_{\text{fr1}}$  must be higher than 6 MHz.

## V. EFFECT OF NON-IDEALITIES

In this section, the effect of some of the non-ideality factors on the performance of the prototype is explained.

TABLE I  
EFFECT OF TEMPERATURE CHANGE ON THE PERFORMANCE OF THE PROPOSED ADC

Corner	$G$	Uncal. SQNR (dB)	Cal. SQNR (dB)
TT 27°C	9.9	86.6	86.6
TT 120°C	11	83.92	86.8
TT 0°C	10.16	85.53	85.9

### A. Analog-Digital Filtering Mismatch

MASH architectures, in general, are sensitive to analog-digital filtering mismatch.  $G$  [shown in (7)] is the gain that  $\phi_{q1P,N}$  sees in its path through the QPD and second stage to the second-stage output. As shown in (7), the gain of  $\text{NCF}_2$  is a function of  $f_{\text{fr1}}$ ,  $f_{\text{High}}$ , and  $f_{\text{Low}}$ . Any mismatch between the estimated digital value of the gain and the real analog value would result in first-stage quantization noise leakage and performance degradation. To obtain a good estimate of the gain, a foreground calibration is used. The proposed calibration method is shown in Fig. 12. To calculate  $G$ , three parameters  $f_{\text{fr1}}$ ,  $f_{\text{High}}$ , and  $f_{\text{Low}}$  are required to be extracted in the calibration mode. To calculate  $f_{\text{fr1}}$ , the output sampled phase of the first-stage VCO is digitally differentiated, and multiple samples are averaged. Then, in order to find  $f_{\text{High}}$  and  $f_{\text{Low}}$ , VCO<sub>2</sub> ground is connected to  $V_{\text{Low}}$ , and the frequency of VCO<sub>2</sub> is calculated by averaging multiple samples of the second-stage output. This way  $f_{\text{High}}$  can be extracted. Next, VCO<sub>2</sub> ground is connected to  $V_{\text{High}}$ , and  $f_{\text{Low}}$  is extracted in a similar way. By knowing  $f_{\text{fr1}}$ ,  $f_{\text{High}}$ , and  $f_{\text{Low}}$ ,  $\text{NCF}_2$  can be accurately calibrated.

As shown in (7),  $G$  is a function of the VCOs frequencies and, thus, PVT dependent. The foreground calibration takes care of changes in frequency due to process variations. To show the effect of temperature on the performance, the postlayout extracted of the proposed ADC is simulated for three different corners of TT 0 °C, TT 27 °C, and TT 120 °C. Table I shows the value of  $G$ , uncalibrated SQNR, and calibrated SQNR. Note that in these simulations, the thermal noise is not included. Uncalibrated SQNR is the ADC's SQNR where the value of  $G$  is assumed to be 9.9 ( $G$  in TT 27 °C corner).

As can be seen in (7),  $G$  is the ratio of the first- and second-stage frequencies. Therefore, when the temperature was changed to 0 °C and 120 °C,  $G$  only changed by approximately 11%. Also, as can be seen in Table I, the uncalibrated SQNR drops by around 2.5 dB.

It is also important to note that as the input common-mode voltage changes,  $f_{\text{fr1}}$  changes as well. This will change the required  $G$  value. In Section VI, the effect of common-mode voltage variation is investigated further.

### B. VCO Mismatch

Fig. 2(b) shows the block diagram of the first stage. As can be seen in Fig. 2(b), when there is no mismatch between VCO<sub>1</sub>s, the free-running frequencies of positive and negative paths cancel out each other. In practice, there is a mismatch between  $f_{\text{fr1}P}$  and  $f_{\text{fr1}N}$ . As shown in Fig. 2(b), since

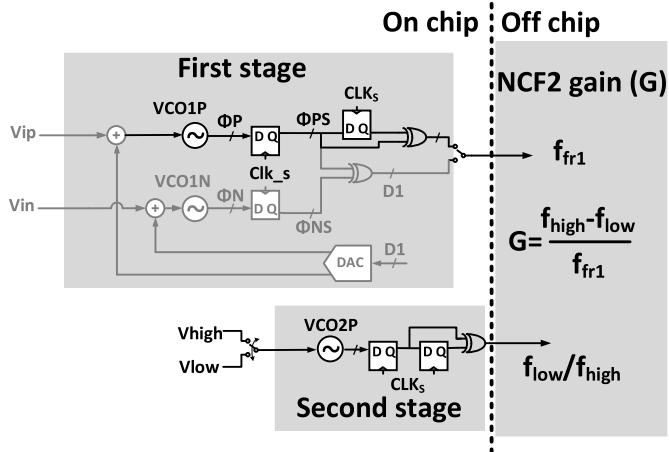


Fig. 12. Calibration mode to find NCF<sub>2</sub> gain ( $G$ ).

the VCO<sub>1</sub>s' free-running frequencies are added before the integration, the mismatch between them can be seen as an added offset, which results in a dynamic range (DR) reduction. This is similar to an input offset of the integrators in a first-order conventional OTA-based delta-sigma modulator. Moreover, as shown in Fig. 5, the quantization in the phase domain ( $\phi_{q1P,N}$ ) gets mapped to the time domain with a gain of  $1/(2\pi f_{fr1P,N})$ . In the presence of a mismatch between  $f_{fr1P}$  and  $f_{fr1N}$ , the two paths see different gains. This results in first-stage quantization noise leakage at the output.

To see the effect of  $K_{VCO1}$  mismatch, the first-stage VCOs gains,  $K_{VCO1P}$  and  $K_{VCO1N}$ , in the presence of mismatch can be defined as

$$\begin{aligned} K_{VCO1P} &= K'_{VCO1} + \Delta \\ K_{VCO1N} &= K'_{VCO1} - \Delta \end{aligned} \quad (11)$$

where  $K'_{VCO1}$  is the average value of the two  $K_{VCO1}$ s and  $2\Delta$  is the difference between  $K_{VCO1P}$  and  $K_{VCO1N}$ . First assume  $K'_{VCO1}$  is equal to  $K_{VCO1}$  [shown in the feedback DAC of Fig. 2(b)]. In this case, the positive path integration gain is increased by  $\Delta$ , and the negative path gain is decreased by  $\Delta$ . Since the first-stage input and the DAC output are differential signals, the input signal of the integrators has equal magnitude but opposite sign. Therefore, by increasing the integration gain of the positive path and decreasing the integration gain of the negative path by the same value, the difference between the output of the integrators remains the same as before. Notice that since the gains of the positive and negative paths are different, the even harmonic cancellations of VCO nonlinearity is not perfect. Fortunately, since the VCO<sub>1</sub>s input signal swing is small, the even harmonics leakage will be negligible and would not affect the performance.

In case  $K'_{VCO1}$  is different from  $K_{VCO1}$ , the integration gain and the feedback gain of the first stage will not be the inverse of each other, and therefore, an extra high-frequency pole will show up in the NTF. This is similar to the gain difference of the integration and feedback of a first-order conventional OTA-based delta-sigma modulator. The new NTF is approximately

equal to

$$NTF(z) = \frac{(1 - z^{-1})}{1 - \left(1 - \frac{K'_{VCO1}}{K_{VCO1}}\right)z^{-1}}. \quad (12)$$

The second stage is a pair of open-loop VCO quantizers operating in the frequency domain. As it is shown in Fig. 5, the two quantization noise sources of  $\phi_{q1P}$  and  $\phi_{q1N}$  go to the second-stage output with the gain of  $(N/\pi)(f_{High} - f_{Low})/f_{fr1}$ . In the presence of the mismatch between the second-stage VCOs, each of  $\phi_{q1P}$  and  $\phi_{q1N}$  sees a different gain in its path through the second stage to the output.  $f_{HighP,N}$  and  $f_{LowP,N}$  can be measured in the calibration phase, and therefore, their mismatch can be compensated through digital filters. Notice that to reduce VCOs mismatch effect, a careful layout is executed.

### C. QPD Non-Idealities

*1) Effect of Mismatch in QPD:* Different paths in QPD can have a slightly different delay due to the routing and transistor mismatch. Even though the rising edge of the  $E_Q(t)$  will be always fixed due to the re-timing of the PTR signal, the falling edge may get affected by the delay mismatch on each path in QPD. This delay mismatch can be modeled as an error source at the input of positive and negative paths of the second stage (as shown in Fig. 5). This error then gets first order shaped due to NCF<sub>2</sub>. The shaped error then is added to other noise sources and can degrade the performance. As an example, considering OSR is 30 and the desired accuracy just due to this noise source at the output being better than 86 dB, the sigma of the mismatch must be better than 30 ps. This mismatch requirement is met by a careful layout.

*2) Effect of Non-Zero Setup/Hold Time of the Quantizer:* As shown in Fig. 8, the output phases of the first-stage VCOs are sampled by SA-FFs. Then, the sampled phases are compared together using a set of XOR gates. After that, a set of re-timing FFs generates the first-stage output code. If the toggling edge of VCO<sub>1</sub> output happens right before the rising edge of  $CLK_S$ , the SA-FF might not detect the change and the sampled output may be an incorrect value by one unit (LSB). Fig. 13 shows the timing diagram of one of the first-stage VCOs. In Fig. 13, a 3-bit (8-taps) VCO is shown for simplicity, while the real implementation is 5-bit (32-level). As shown in Fig. 13,  $\phi_1$  changes right before the sampling instance of  $nT_S$ . In Fig. 13, two cases are shown. The first case is when the quantizer works properly and samples  $\phi_1$  as one. The second case is when the quantizer fails to detect this change and samples  $\phi_1$  as zero. In the second case, the quantized value is incorrect by one LSB. In other words, the quantizer adds an error of one LSB in the second case compared to the first case. This extra LSB that is added to some of the codes is an extra error and needs to be extracted as well. The added error plus the ideal quantization noise is the new quantization noise of the first stage. In the first case, the PTR signal shows that  $\phi_1$  had the last transition in the previous sampling period, and in the second case,  $\phi_0$  is detected by the PTR signal as the last transition. Therefore, as shown in Fig. 13, the generated pulse [ $E_Q(t)$ ] for the two cases has one LSB difference. In the

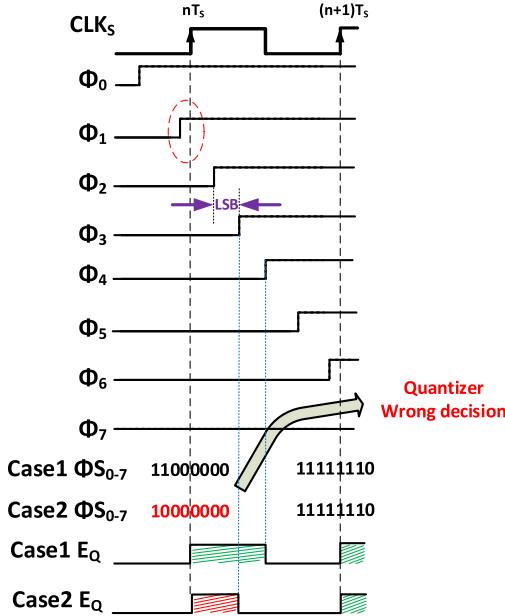


Fig. 13. Effect of wrong decision of the quantizer.

other words, since in this design, the PTR signal generation is performed using the first-stage output code, any wrong decision of the first-stage quantizer is a part of the first-stage quantization noise and captured and extracted in the QPD block. This quantization noise (the added error and the ideal quantization noise) is then canceled at the final output. Therefore, the wrong decision of the first-stage quantizer has no effect on the performance of this architecture.

3) *Effect of Slow Rise/Fall Time of QPD*: As discussed in [21], this effect can be modeled as a low-pass filter in the Q-extraction path. Fig 14 shows the effect of non-zero rise-fall time of the Q-extraction path. In Fig 14, two VCO phase signals are considered in which one of them is  $t_0$  time delayed compared with the other one. Also, the frequency of the VCO is assumed to be fixed due to the first-stage feedback. As can be seen, even though there is a slow rise/fall time in  $E_Q(t)$  signal, the difference between the width of the two pulses is still  $t_0$ .

Note that due to the use of the pulse extension technique, the limited rise/fall times do not affect the Q-extraction if the two LSBs are designed to be larger than the rise time. Using the pulse extension technique, all the samples experience the same added error due to the slow rise time. Also, since all the samples use the same circuit in the Q-extraction path (considering no mismatch between different routes), the same error is added to all the extracted pulses due to the slow fall time. Since these errors are the same for all the samples, they act as an offset, and therefore, they will be removed at the output of NCF<sub>2</sub> due to the derivative function.

#### D. Thermal and Flicker Noise Effect

In this design, the output SNDR is limited by thermal and flicker noise of the front-end blocks. These blocks are the input resistors, DAC and VCO<sub>1</sub>s. Thermal and flicker noise due to the second stage will be shaped by one order and, therefore,

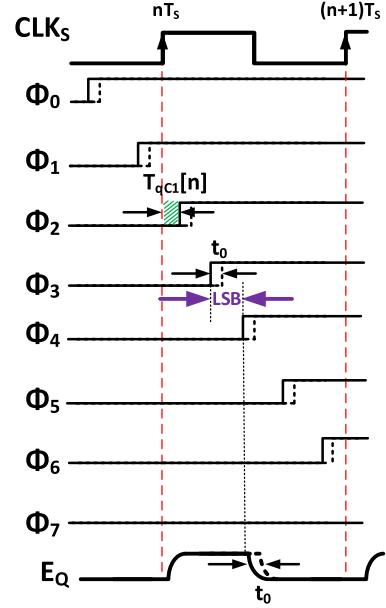
Fig. 14. Slow rise/fall time effect on the  $E_Q(t)$  signal.

TABLE II  
EFFECT OF NOISE ON THE PERFORMANCE

Simulation condition	SNDR (dB)
Without thermal and flicker noise	86.6
Only with $R_{in}$ and DAC thermal noise	84.12
Only with VCO <sub>1</sub> s noise	82
All noise	81

has a minor effect on the overall SNR. Table II shows the different scenarios of postlayout simulation.

## VI. MEASUREMENT RESULTS

The prototype ADC was fabricated in a 65-nm CMOS process with an active area of  $0.26 \text{ mm}^2$ . The chip is assembled in a 48-pin QFN package. Fig. 15 shows the test board, package, and the die micrograph. The digital outputs of both stages go through thermometer to binary converters inside the chip. Also, single-ended outputs for digital bits are used.

In this design, to ease the layout, the first stage and the QPD block are partitioned to 32 equivalent sub-blocks. Each sub-block contains one element of the required pseudo-differential circuitry, including the VCO<sub>1</sub> delay cell, DAC elements, SA, SA-FF, and the required  $\phi_{qC1}$  extraction circuitry of each VCO<sub>1</sub> phase tap. Therefore, by having the layout of one sub-block drawn, the entire first-stage and QPD that contain 32 of these sub-blocks can be easily laid out. While creating the layout in this way is easier, it is not an optimum method to minimize the layout size.

The performance of the ADC is summarized in Table III and compared with the state-of-the-art CT  $\Delta\Sigma$  modulators with similar specifications. The ADC consumes 1.248 mW at a sampling frequency of 125 MHz from a 0.9-V supply. Fig. 16 shows the power breakdown of the ADC. The analog blocks (VCOs and DAC) consume 279  $\mu\text{W}$ , and

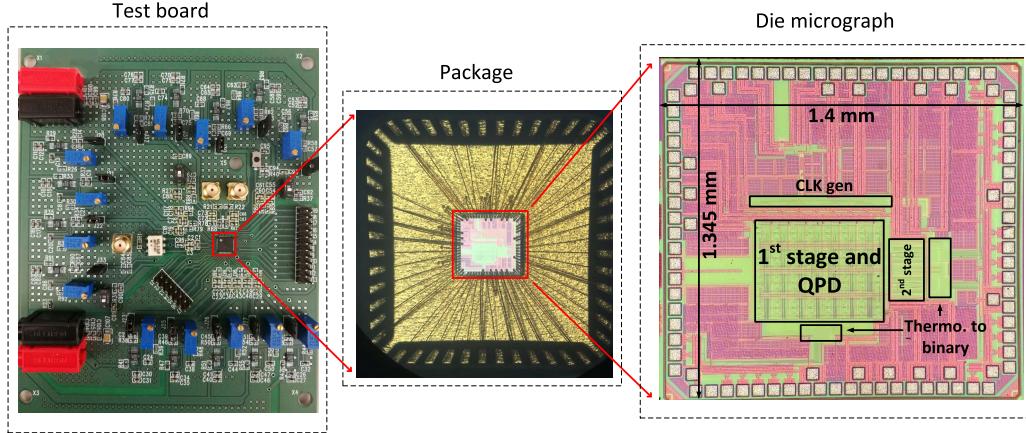


Fig. 15. Test board, the package, and the die micrograph.

TABLE III  
PERFORMANCE SUMMARY AND COMPARISON TO PRIOR ART

Architecture Reference	VCO-based CTDSM						Conventional CTDSM				
	This work	[12]	[2]	[14]	[11]	[13]	[3]	[22]	[23]	[24]	[25]
NTF order	2 <sup>nd</sup>	2 <sup>nd</sup>	2 <sup>nd</sup>	3 <sup>rd</sup>	1 <sup>st</sup>	2 <sup>nd</sup>	1 <sup>st</sup>	3 <sup>rd</sup>	4 <sup>th</sup>	4 <sup>th</sup>	3 <sup>rd</sup>
Need OTA	No	No	Yes	No	No	No	No	Yes	Yes	Yes	Yes
Process(nm)	<b>65</b>	40	90	65	130	65	40	65	55	130	65
Fs(MHz)	<b>125</b>	330	600	1600	250	205	1600	1000	140	256	320
BW(MHz)	<b>2</b>	6	10	10	0.4	2	2.5	40	10	2.2	2
SNDR(dB)	<b>79.7</b>	68.6	78	65.7	82.9	74.7	64.2	59.5	72.2	90.4	74.4
SNR(dB)	<b>80.3</b>	—	79.1	66.2	—	—	—	76	—	80.5	—
DR(dB)	<b>82.7</b>	70.8	—	71	88.5	77.6	—	—	77	92	82
Power(mW)	<b>1.248</b>	0.524	16	3.7	1.05	1	2.57	1.57	4.5	5	0.256
Area(mm <sup>2</sup> )	<b>0.26</b>	0.028	0.36	0.01	0.13	0.06	0.017	0.027	0.09	0.33	0.013
FOM <sub>W</sub> (fJ/step)	<b>39.6</b>	19.9	123.2	119.3	118	59	150.9	42	23.6	37.8	291.4
FOM <sub>S</sub> (dB)	<b>171.7</b>	169.2	166	160	168.7	167.5	158.2	161.4	170.2	177.3	160.4

$$FOM_W = \text{Power}/(2 \times \text{BW})/2^{ENOB}$$

$$FOM_S = SNDR + 10 \times \log_{10}(\text{BW}/\text{Power})$$

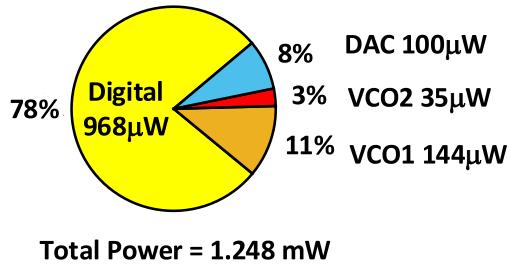


Fig. 16. Power breakdown.

the digital blocks consume 968  $\mu$ W. The ADC achieves peak DR/SFDR/SNR/SNDR of 82.7/88.7/80.3/79.7 dB in a 2-MHz signal BW resulting in an ENOB of 12.95 and FoMs of 171.7 dB. The output power spectral density (PSD) of the first stage along with the final output is shown in Fig. 17(a) with a 500-kHz, -1-dBFS (1.25 V<sub>pp</sub>) differential input signal. The input common-mode voltage ( $V_{CM}$ ) is set to 0.43 V in this measurement, and  $f_{fr1}$  is around 10.5 MHz. Also, in this measurement,  $V_{High}$  and  $V_{Low}$  are 0.68 and 0.4 V, respectively, and VCO<sub>2</sub> frequency switches between around 7 and 78 MHz. The first stage shows first-order noise shaping, while the final output shows second-order noise shaping. The authors believe

that the small in-band harmonics are the result of input voltage leakage to the input of VCO<sub>1</sub>s. Also, the spurs around  $f_{fr1}$  are believed to be from the first-stage VCOs [21]. The measured SNR and SNDR plotted as functions of the input amplitude are shown in Fig. 17(b); the modulator achieves a DR of 82.7 dB. NCF<sub>2</sub> gain,  $G$  (shown in Fig. 8), has a value of 6.6. Notice that this value is smaller than the value used in the simulations (shown in Table I). As seen in Fig. 17(a), the performance is limited by the thermal noise. Therefore, increasing the value of  $G$  only results in an increase in the second-stage power without an improvement in performance. The measurements have been done for 65 536 sampled points with 32 times averaging of the PSD.

As  $V_{CM}$  changes,  $f_{fr1}$  changes, and as a result,  $G$  changes. To show this effect,  $V_{CM}$  has been changed, and the overall SNDR is measured. Fig. 18 shows  $f_{fr1}$  and SNDR variation with respect to  $V_{CM}$ . In Fig. 18, SNDR before and after the calibration is shown. To compensate for the performance degradation due to the  $f_{fr1}$  variation, the calibration is applied to optimize the value of  $G$ .

To show the effect of analog-digital filtering mismatch, the NCF<sub>2</sub> gain ( $G$ ) was changed manually in the digital domain, while the ADC test setup was kept at its maximum performance. As shown in Fig. 19, there is less than a 1-dB

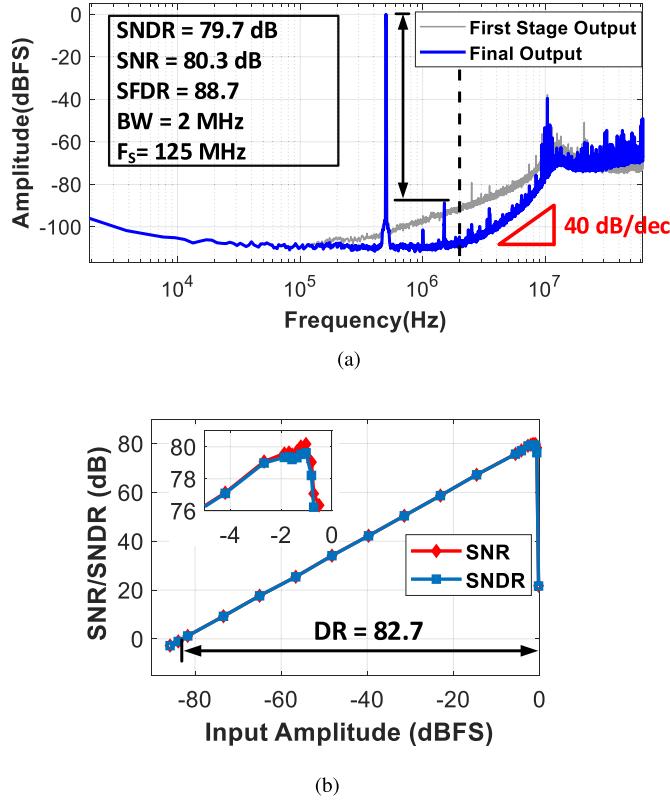


Fig. 17. (a) Measured output PSD. (b) Measured SNR/SNDR versus input amplitude. The measurements have been performed for 65 536 sampled points.

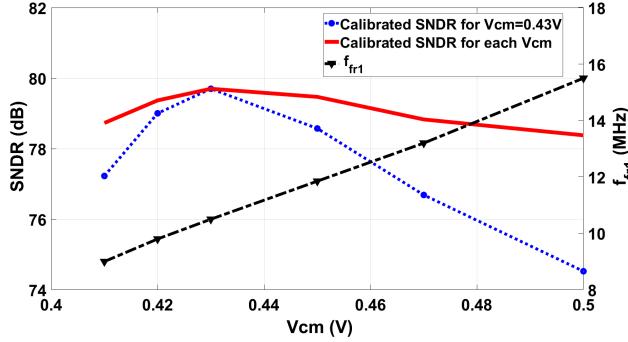


Fig. 18. Measured  $f_{fr1}$  and SNDR variation with respect to  $V_{CM}$  variation.

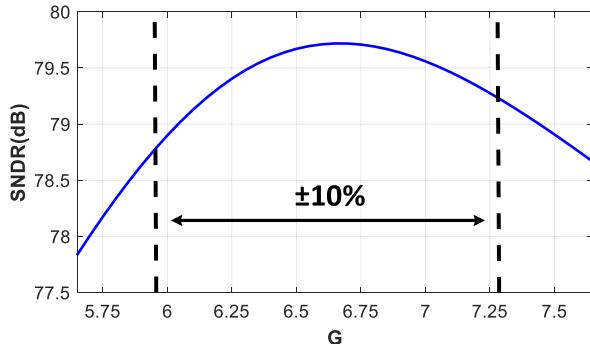


Fig. 19. Effect of NCF<sub>2</sub> gain ( $G$ ) variation from its nominal value.

drop in SNDR for  $G$  varying by ±10%. The reason for the small performance degradation is that SNDR is limited to the thermal noise, and also, the first-stage quantizer is 5-bit and its

quantization noise is first-order shaped. Notice that the price for this low sensitivity to  $G$  variation is a high number of quantizer levels, which results in more power consumption in the digital part of the first stage as well as the QPD block.

A highly linear second-order OTA-less VCO-based ADC is realized by using low power and scaling friendly circuits. The performance of the ADC compares favorably with state-of-the-art CT  $\Delta \Sigma$  modulators. Since the proposed ADC is implemented using digital scaling friendly blocks, this architecture will provide additional benefits in advanced technology nodes.

## VII. CONCLUSION

A highly linear 1-1 MASH VCO-based ADC is implemented without the use of OTAs or power-hungry linearization methods. The measured prototype ADC has a 79.7-dB SNDR with an  $FoM_S$  of 171.7 dB. This is the best  $FoM_S$  reported for VCO-based ADCs to date. This performance is achieved by utilizing an efficient circuit to extract the quantization error of a multi-phase VCO-based phase quantizer in the time domain as a PWM signal.

## APPENDIX

### ESTIMATION OF PHASE DOMAIN QUANTIZATION NOISE OF THE FIRST STAGE IN TIME DOMAIN

As (9) shows,  $\phi_{qC1}$  is the integration of the VCO frequency over the time period of  $T_{qC1}[n]$ . When  $f_{VCO1}$  has a small variation, the phase domain quantization noise can be approximately mapped to the time domain linearly, as shown in (10). Making this approximation more accurate results in better cancellation of the first-stage quantization noise at the output. To make this approximation more accurate, VCO<sub>1</sub> frequency variation with respect to  $f_{fr1}$  has to be reduced. Here, the effect of different parameters on the  $f_{VCO1}$  variation is discussed.

Fig. 2(b) shows the linear model of the first stage. The output of the first stage is shown in (4), where the continuous integration is approximated as a discrete-time integration. Replacing  $V_{id}$  with  $2V_{ip}$  in (4), VCO<sub>1P</sub> input signal [ $G_{1P}(t)$ ] is

$$\begin{aligned} G_{1P}(t) &= V_{ip}(t) - V_{ip}(t - T_S) + \left( \frac{1}{4\pi K_{VCO} T_S} \right) \\ &\times ((\Phi_{qP}(nT_S) - \Phi_{qN}(nT_S)) \\ &- (\Phi_{qP}((n-1)T_S) - \Phi_{qN}((n-1)T_S))). \end{aligned} \quad (13)$$

Therefore, the frequency of the VCO is

$$\begin{aligned} f_{VCO1P}(t) &= K_{VCO}(V_{ip}(t) - V_{ip}(t - T_S)) + \left( \frac{1}{4\pi T_S} \right) \\ &\times ((\Phi_{qP}(nT_S) - \Phi_{qN}(nT_S)) \\ &- (\Phi_{qP}((n-1)T_S) - \Phi_{qN}((n-1)T_S))) + f_{fr1}. \end{aligned} \quad (14)$$

Equation (14) shows that  $f_{VCO1P}$  is a function of the input voltage change between two consecutive samples as well as the shaped quantization noise. Maximum  $f_{VCO1P}$  variation happens when the first two terms of  $f_{VCO1P}$  have their maximum

variation. The maximum amplitude of the first-stage output ( $D[n]$ ) is  $N/2$ . Therefore, based on the transfer function of (4), the maximum value of  $K_{VCO1}V_{ip}(t)$  is approximately  $f_S/8$ . The first term of  $f_{VCO1P}$  is a difference of two consecutive samples of the input signal multiplied by  $K_{VCO1}$ . Therefore, the maximum variation of the first term of  $f_{VCO1P}$  is

$$\begin{aligned}\Delta_{\max}(K_{VCO}(V_{ip}(t) - V_{ip}(t - T_S))) \\ = \text{Max}(K_{VCO}(V_{ip}(t) - V_{ip}(t - T_S))) \\ - \text{Min}(K_{VCO}(V_{ip}(t) - V_{ip}(t - T_S))) \\ = \left| \left(1 - e^{-\frac{j\pi}{OSR}}\right) \right| \frac{f_S}{4}. \quad (15)\end{aligned}$$

$\Phi_{qP,N}$  has a value between 0 and  $\pi/N$ . As a result, the maximum difference of two consecutive samples of  $\Phi_{qP} - \Phi_{qN}$  is  $2\pi/N$ . Thus, the maximum variation of the second term of  $f_{VCO1P}$  is

$$\begin{aligned}\Delta_{\max}\left(\frac{1}{4\pi T_S}\right)((\Phi_{qP}(nT_S) - \Phi_{qN}(nT_S)) \\ - (\Phi_{qP}((n-1)T_S) - \Phi_{qN}((n-1)T_S))) = \frac{f_S}{2N}. \quad (16)\end{aligned}$$

Based on these two equations, the maximum  $f_{VCO1P}$  variation normalized to  $f_{fr1}$  is

$$\frac{\Delta_{\max}(f_{VCO1})}{f_{fr1}} = \left( \left| \left(1 - e^{-\frac{j\pi}{OSR}}\right) \right| + \frac{2}{N} \right) \frac{f_S}{4f_{fr1}}. \quad (17)$$

As it can be seen, the relative variation of the VCO frequency compared with the  $f_{fr1}$  is function of OSR,  $N$ ,  $f_S$ , and  $f_{fr1}$ . As the quantizer levels ( $N$ ) increases, the quantization noise variation at the input of the VCO decreases. Also, as OSR increases, the signal variation from one sample to the next one decreases, which results in less input signal leakage to the input of the VCO and less VCO frequency variation. Increasing  $f_{fr1}$  results in less frequency variation relative to the free-running frequency and, therefore, better accuracy in extracting the quantization noise in the time domain. The drawback of increasing  $f_{fr1}$  is higher power consumption for the same phase noise. Also, as  $f_S$  increases, assuming OSR remains the same, more frequency variation relative to  $f_{fr1}$  is observed. This will result in less accuracy of mapping quantization noise from the phase domain to the time domain and, therefore, less  $\phi_{q1}$  cancellation at the final output and, hence, a performance (SNDR) degradation. To avoid this,  $f_{fr1}$  also needs to be scaled at the same rate to achieve the same accuracy of estimation of the quantization noise in the time domain as the lower sampling frequency.

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