Computer Organization 2021

HOMEWORK 3

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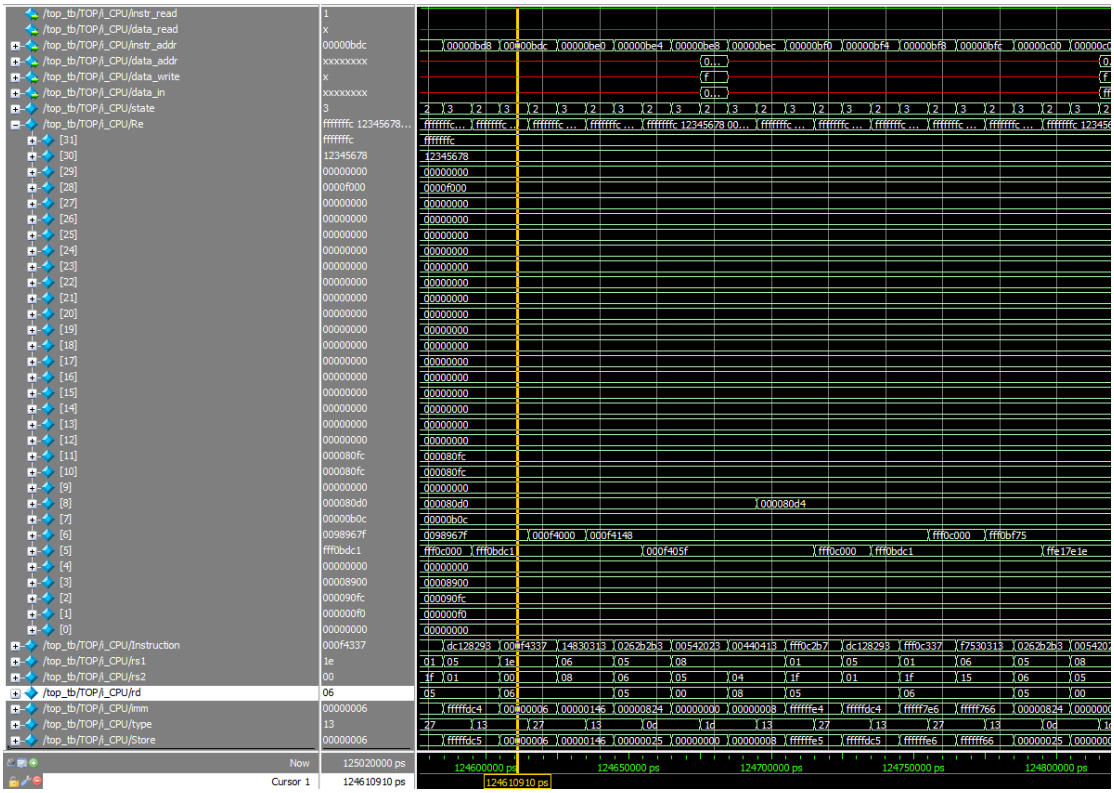
實驗結果圖:

(波形圖及模擬完成截圖) 節錄：total cycle = 13505

```
# DM[  12] = ffffcccc, pass
# DM[  13] = 000000cc, pass
# DM[  14] = 0000cccc, pass
# DM[  15] = 00000d9d, pass
# DM[  16] = 00000004, pass
# DM[  17] = 00000003, pass
# DM[  18] = 00001a6, pass
# DM[  19] = 00000ec6, pass
# DM[  20] = 2468b7a8, pass
# DM[  21] = 5dbf9f00, pass
# DM[  22] = 00012b38, pass
# DM[  23] = fa2817b7, pass
# DM[  24] = ff000000, pass
# DM[  25] = 12345678, pass
# DM[  26] = 0000f000, pass
# DM[  27] = 00000f00, pass
# DM[  28] = 000000f0, pass
# DM[  29] = 0000000f, pass
# DM[  30] = 56780000, pass
# DM[  31] = 78000000, pass
# DM[  32] = 00005678, pass
# DM[  33] = 00000078, pass
# DM[  34] = 12345678, pass
# DM[  35] = ce780000, pass
# DM[  36] = fffff000, pass
# DM[  37] = fffff000, pass
# DM[  38] = fffff000, pass
# DM[  39] = fffff000, pass
# DM[  40] = fffff000, pass
# DM[  41] = fffff000, pass
# DM[  42] = 1357a064, pass
# DM[  43] = 13578000, pass
# DM[  44] = fffff004, pass
# DM[  45] = 000174a8, pass
# DM[  46] = fffffb37, pass
# DM[  47] = 00007740, pass
# DM[  48] = 00005af3, pass
# DM[  49] = ffffff17, pass
# DM[  50] = 000000e8, pass
# DM[  51] = 00005af3, pass
# DM[  52] = 000f405f, pass
# DM[  53] = ffe17ele, pass
#
#
#
#
#         ****************************
#         **                        **       |\__||
#         **  Congratulations !!    **      / O.O  |
#         **                        **    /_____   |
#         **  Simulation PASS!!     **   /^ ^ ^ \  |
#         **                        **  |^ ^ ^ ^ |w|
#         ****************************   \m___m__|_|
#
#
# total cycle:     12501
# ** Note: $finish    : D:/User/CPU/top_tb.v(67)
#    Time: 125020 ns  Iteration: 1  Instance: /top_tb
# 1
# Break in Module top_tb at D:/User/CPU/top_tb.v line 67
```



程式運作流程:

基本上就是：我以有限狀態機的方式去實作
分成兩到三個 cycle(branch, load 會有 3 個 cycle)
第一個 cycle 讀 instr_out 到 instruction，順便紀錄 rs1, rs2, rd。
第二個 cycle 開始實做指令，便依照判斷回去第一個 cycle 或是第三個 cycle
若到第三個 cycle 就讀 data_in 到 register 中回去第一個 cycle

心得

(請寫下完成本次作業的心得、學到哪些東西、困難點的部分。)

困難點在於，要將每個指令完成，另外，也要考慮 address 可能不是 4 的倍數 sb 13($t0)這種東西，因此搞了非常久的時間，也學會了 verilog 的特殊用法，$signed(), $unsigned()，這兩個用法就可以將每個指令分別完成，因為也要考慮到從 memory 輸入和 cpu 的輸出有極大的關係，因此我們必須多跑一個 cycle，以達到我們的目標。