ME581 Lab 4 Report

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Abstract

The objective of this study was to develop and simulate a PID control system for a fifth-order analog plant, with the aim of attaining comparable performance and stability goals. This laboratory experiment builds upon the fourth lab by introducing an additional roll-off filter to the hardware-in-the-loop (HIL) setup. Initially, we design the notch filter and controller using Python simulation. Subsequently, the control system design is validated through hardware implementation, employing a microcontroller along with resistors and capacitors. The experimental results, unfortunately, could not be successfully obtained due to both technical challenges and inherent impracticality.

1 Discussion

Figure 1 illustrates the HIL setup with the incorporation of additional components. These new components include a roll-off filter and input summers. The roll-off filter comprises a $5k\Omega$ resistor and a $10\mu F$ capacitor, resulting in a break frequency of approximately 20.232 rad/sec for the roll-off filter. This additional components filter the input signal to decrease the excitation of the high frequency vibration mode. The reason why we implement a hardware filter instead of a digital rolloff filter is because the digital one only filters out the frequencies that are lower than it own. By incorporating these components along with the existing components, a fifth-order analog plant for the updated HIL setup is completed.

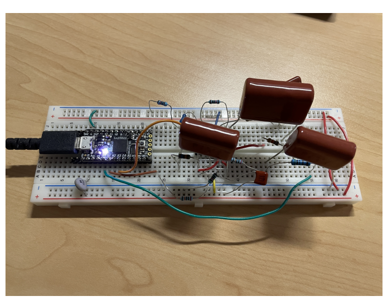

Figure 1: Breadboard setup

I initially designed a notch filter with loopshaping method by looking at the bode plot. Figure 3 clearly illustrates the undesirable excitement present in the plant without the notch filter, particularly between 1 and 10 Hz. The notch filter, represented by equation (1), is depicted in Figure 2 as a bode plot. And as you can see in Figure 3, once the notch filter was implemented, this excitement was cancelled out.

$$N(z) = \frac{0.7759z^2 - 1.512z + 0.7545}{z^2 - 1.512z + 0.5304} \tag{1}$$

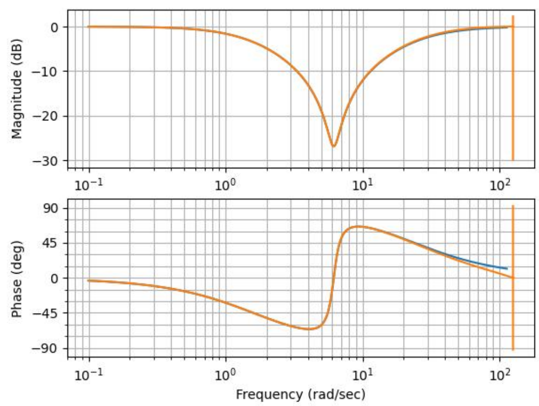

Figure 2: Bode plot of the designed notch filter

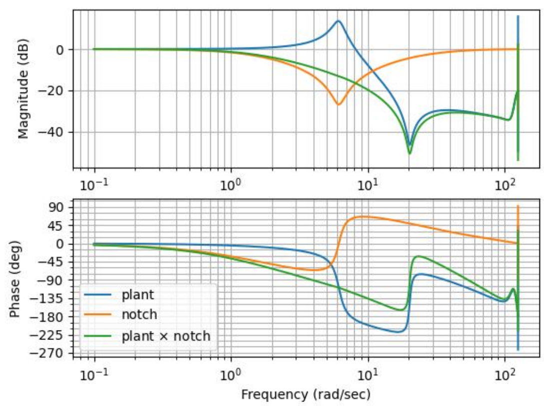

Figure 3: Frequency responses of plant, notch filter, and integration of both

Moving forward, I proceeded to design a controller using the loopshaping method. In line with the objectives of the lab, I selected $\omega_p = 0$ to get the desired settling time. Through multiple simulations and tests, I determined that $\omega_z = 0.16$ offered the best performance for disturbance step response. The controller is introduced in (2) with the bode plot shown in Figure. With this designed controller, the system demonstrated stability and theoretically fulfilled all the specified objectives for this lab. By providing a clear explanation of the design process and referring to the corresponding figure, your description effectively conveys the steps you took to address the low frequency excitement and design an appropriate controller for your system.

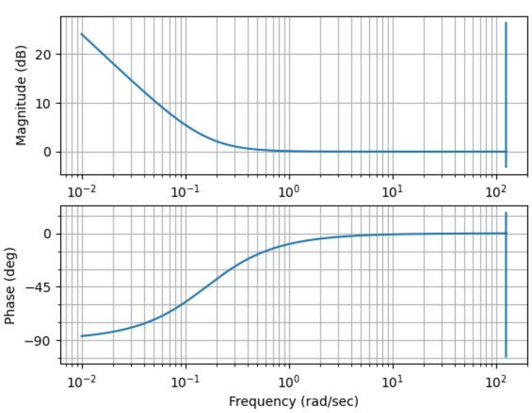

Figure 4: Bode plot of the designed controller

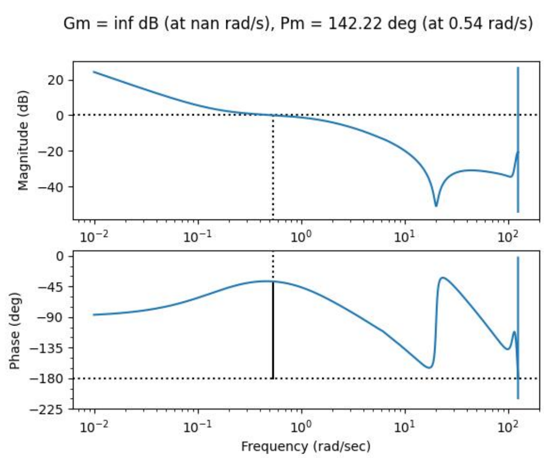

Figure 5: Frequency responses of the integration of both

The simulation of the entire closed loop system is shown as Figure 6 7.

$$C(z) = \frac{1.002z - 0.998}{z - 1} \tag{2}$$

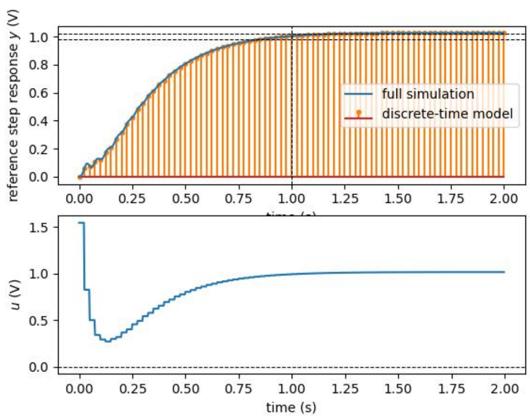

Figure 6: Simulation of reference step response y

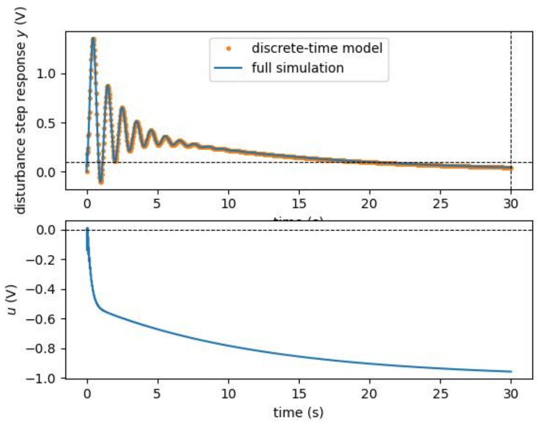

Figure 7: Simulation of disturbance step response y

Moving forward to the preparation for HIL test. First, I checked out the constants and equations that have to be determined and implemented. One of them was the feedforward gain k_{ff} which was the inverse of the DC gain of the designed analog plant. Based on the simulation, the DC gain is 1.01. Next, implemented the notch filter and controller that were designed during the simulation process. The snippet codes for both $N(z)$ and $C(z)$ and their corresponding difference equations are provided below:

```
Nz_num = [1, -1.512, 0.7545]        # Numerator for the Notch Filter
Nz_den = [1, -1.512, 0.5304]        # Denominator for the Notch Filter
Cz_num = [1, 0.16]                  # Numerator for the Controller
Cz_den = [1, 0.]                    # Denominator for the Controller

# Difference equation for Notch Filter
new = (Nz_num[0]*uf[0] + Nz_num[1]*uf[1] + Nz_num[2]*uf[2]
        - Nz_den[1]*uk[0] - Nz_den[2]*uk[1])/Nz_den[0]

# Difference equation for Controller
new = (e[0] + Cz_num[1]*e[1] - Cz_den[1]*uc[0])/Cz_den[0]
```

Unfortunately, the HIL implementation was unsuccessful due to issues with the components. Despite attempting various value modifications, the responses remained the same. As a result, the experimental results of this lab report will rely solely on the simulation.

- As shown in Figure 6, the peak overshoot of the response is less than 2%.
- The response settles within 2% of its steady-state value within 1 sec as Figure 6 shown.

- As shown in Figure 6, the peak value of input is less than $2V$.
- As shown in Figure 7, the response to a unit step disturbance input goes down to less than $0.1V$ within 30 seconds.
- As shown in Figure 7, the peak of the input is less than $2V$.
- As shown in Figure 5, the positive gain margin is greater than $20dB$.
- As shown in Figure 5, the negative gain margin is extended to $-\infty$.
- As shown in Figure 5, the phase margin is $142.22degrees$ which is $\geq 90degrees$.

2 Summary

In summary, this lab report presents the design process of the notch filter and controller. While the simulation results demonstrate successful performance, it is important to note that practical implementation may not yield the desired outcome.