

# ME581 Lab 3 Report

Yenpang Huang

May 2023

## Abstract

The purpose of this study was to design and simulate a PID control system for a fourth-order analog plant, aiming to achieve comparable performance and stability objectives. Following a methodology similar to Lab 2, we employed a Python script to determine an optimal combination of control gains, including feedforward, proportional, integral, and derivative components. The designed control system was then validated through hardware implementation, utilizing a microcontroller along with resistors and capacitors. To gain insights into the system's behavior, we conducted a stability analysis by examining its pole-zero map. This analysis provided valuable information about the system's stability characteristics. Furthermore, we extended our investigation by simulating the system at a double sampling rate to assess its performance compared to the normal sampling rate. The obtained results from both the simulation and hardware implementation demonstrated the successful achievement of all specified objectives.

## 1 Discussion

In order to enhance the realism of the plant simulation, this laboratory experiment involves constructing a fourth-order plant by combining two second-order plants, as illustrated in Figure 1. The obtained hardware results, depicted in Figure 2, illustrate the output when using only a feedforward gain of  $k_{ff} = 1$ .

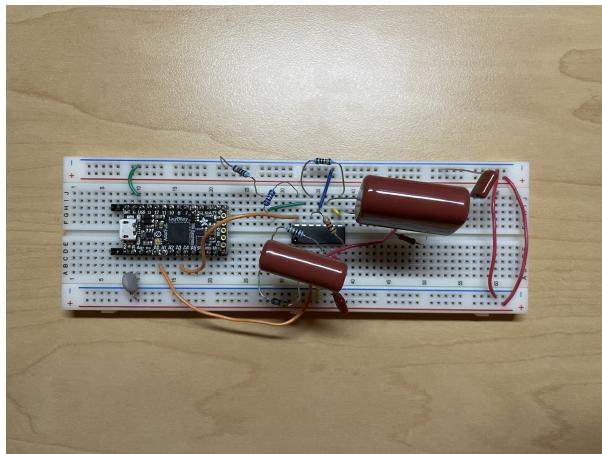


Figure 1: Breadboard setup

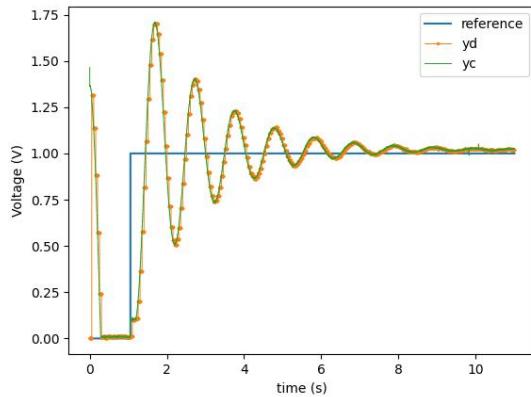


Figure 2: Output signal without controller

Initially, the derivative control was determined using the root locus plot in the SISO tool, as depicted in Figure 3. A gain value of  $k_d = 0.25$  was chosen to effectively dampen the overshoot response. Next, the integral gain was tuned to enhance the system's ability to settle down in the presence of disturbance step input. By setting  $k_i = 0.2$ , the system achieved a settling time of less than 0.1 volt within 30 seconds, as demonstrated in Figure 4. Finally, a slight increase in the proportional gain to  $k_p = 0.2$  was implemented to improve the transient response speed. The behavior of the system with the PID controller is illustrated in Figure 5.

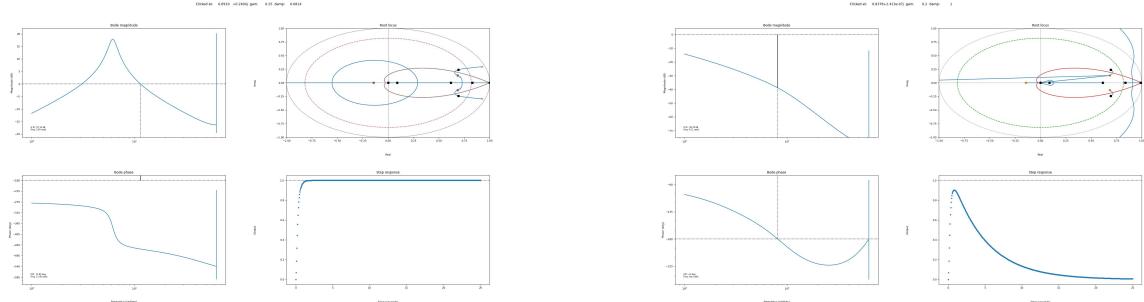


Figure 3: SISO tool for derivative gain and r step input

Figure 4: SISO tool for integral gain and d step input

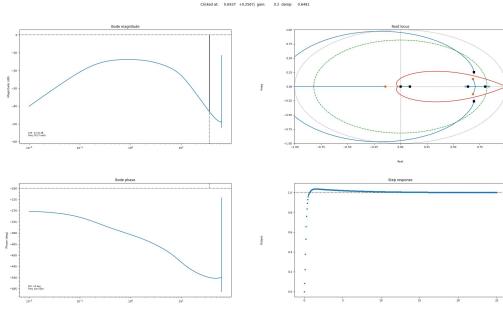


Figure 5: SISO tool for proportional gain and r step input

Subsequent to determining the PID control gains, a hardware test was conducted to validate their performance. Surprisingly, the response exhibited an overshoot, contrary to what was observed during the simulation, as depicted in Figure 6. To address this issue, the DC gain problem was identified and attributed to the feedforward gain, which is the inverse of the DC gain. Consequently, the feedforward gain was adjusted by reducing it from 1 to 0.92. The resulting response is shown in Figure 7. Consequently, the optimal combination of control gains was determined to be  $k_p = 0.2$ ,  $k_i = 0.2$ ,  $k_d = 0.25$ , and  $k_{ff} = 0.92$ . However, it is important to note that modifying the feedforward gain also impacts the system's rising time, leading to slight differences between the hardware and simulation results.

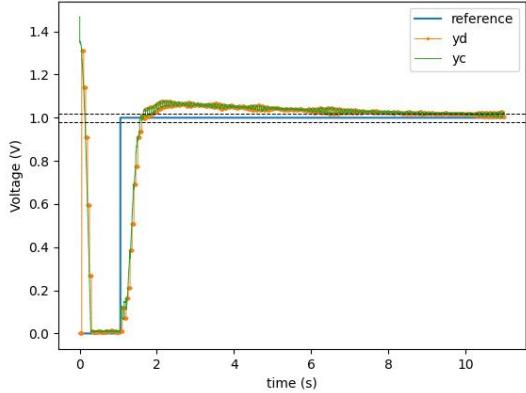


Figure 6: Response with  $k_{ff} = 1$  to a unit step  $r$  input

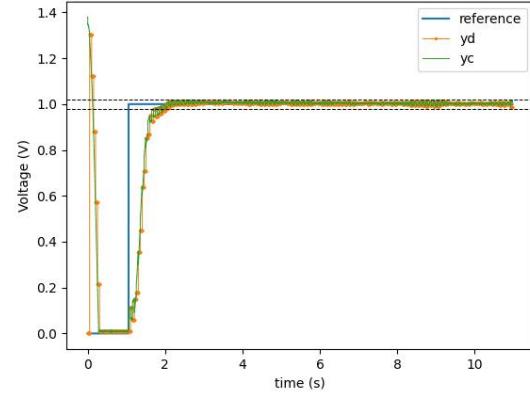


Figure 7: Response with  $k_{ff} = 0.92$  to a unit step  $r$  input

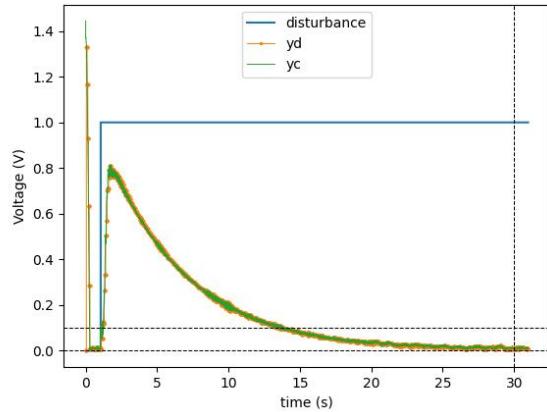


Figure 8: Output response to a unit step  $d$  input

- As shown in Figure 7, the peak overshoot of the  $y$  response is lower than the upper dotted line which indicates it is  $\leq 2\%$
- The response settles within 2% of its steady-state value within 1 sec as Figure 7 shown.
- As shown in Figure 8, the response to a unit step disturbance input goes down to less than  $0.1V$  within 30 seconds.
- As shown in Figure 7, the steady-state tracking error in response to  $r$  input is zero.
- As shown in Figure 8, the steady-state tracking error in response to  $d$  input is zero.

Based on the pole-zero map depicted in Figure 10, it is evident that the dominant poles of the system are located inside the unit circle, indicating system stability. However, the presence of poles close to the origin and on the imaginary axis suggests a relatively slow response and the possibility of oscillations. Overall, the pole-zero map provides valuable information about the system's behavior and serves as a useful tool for tuning the system to achieve specific objectives, as demonstrated in the SISO tool section. In addition to the pole-zero map analysis, the concept of discrete controller's timing is crucial in evaluating the system's precision and consistency. During the hardware test, it was observed that the actual sampling intervals deviated from the expected value of 0.005 (default sampling intervals), with measurements averaging around 0.004. These deviations can be attributed to inherent delays in the hardware components.

- As shown in Figure 9, the positive gain margin is roughly  $20dB$  which is  $\geq 10dB$ .
- As shown in Figure 9, the negative gain margin is extended to  $-\infty$ .
- As shown in Figure 9, the phase margin is  $68.56 degrees$  which is  $\geq 50 degrees$ .

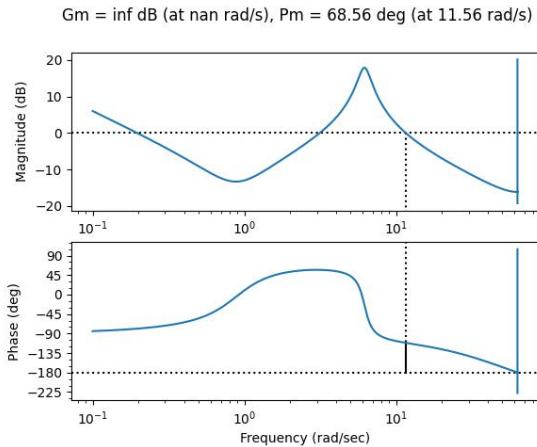


Figure 9: Bode plot

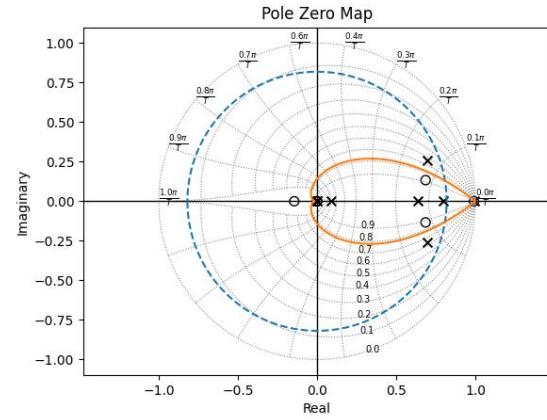


Figure 10: Pole-Zero map

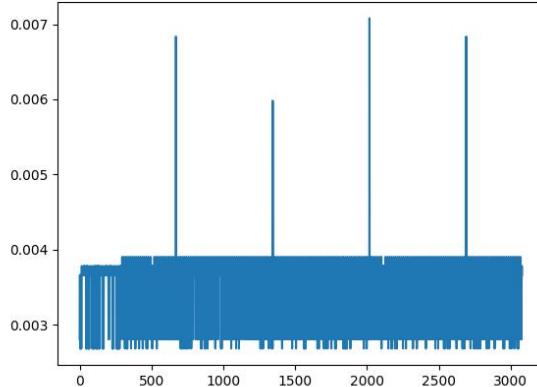


Figure 11: Sampling intervals during a test

To explore the impact of discrete controller's timing on system behavior, the sampling rate was doubled, and the results were compared to those obtained at the default sampling rate. As illustrated in Figure 12, doubling the sampling rate led to improved performance, which was expected due to the halving of the sampling interval ( $dt$ ), resulting in finer resolution. However, this improvement did not hold true for the system with PID controller. Figure 13 reveals that the new system with PID actually became unstable at the doubled sampling rate, performing worse than the default sampling rate system. This instability is also evident in the pole-zero map shown in Figure 14, where a pole is clearly located outside the unit circle, indicating instability. The instability observed in the system with PID controller at the doubled sampling rate can be attributed to the interaction with high-frequency components, resulting in aliasing effects. The Nyquist frequency in this case also doubled, but simply doubling the sampling rate does not resolve the aliasing caused by the original high-frequency components. The instability is eliminated when the derivative control is removed, as demonstrated in Figure 15. This behavior highlights the importance of considering aliasing effects and the need for careful analysis when implementing derivative control. It is worth noting that the system with derivative control experienced instability even in the simulation stage.

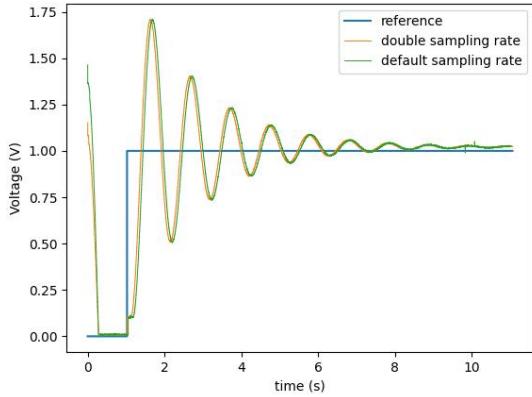


Figure 12: Response without tuned gains in two sampling rate

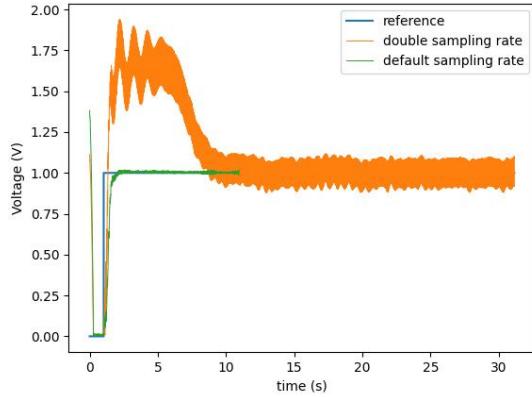


Figure 13: Response without tuned gains in two sampling rate

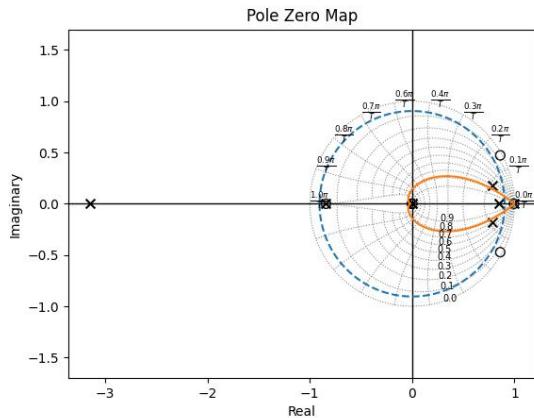


Figure 14: Pole-zero map of the new system

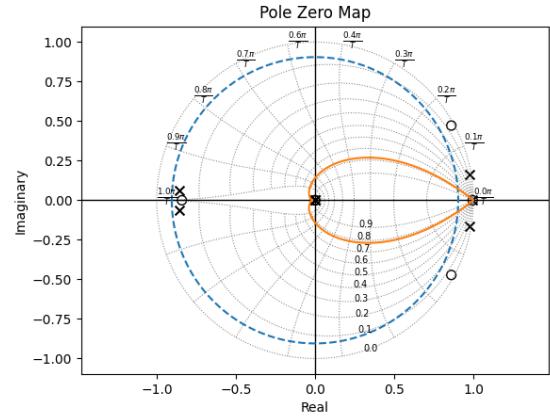


Figure 15: Pole-zero map of the new system without  $k_d$

## 2 Summary

In conclusion, this report highlights the successful tuning of control gains that have met the desired performance and stability margin objectives. The effectiveness of the tuned gains has been validated through hardware testing.

Furthermore, the experiments conducted by doubling the sampling rate have provided valuable insights. It is important to note that a higher sampling rate does not necessarily result in improved system performance. The results indicate that doubling the sampling rate did not consistently benefit the system. This finding emphasizes the importance of carefully considering the impact of sampling rate on system accuracy and performance when designing control strategies.