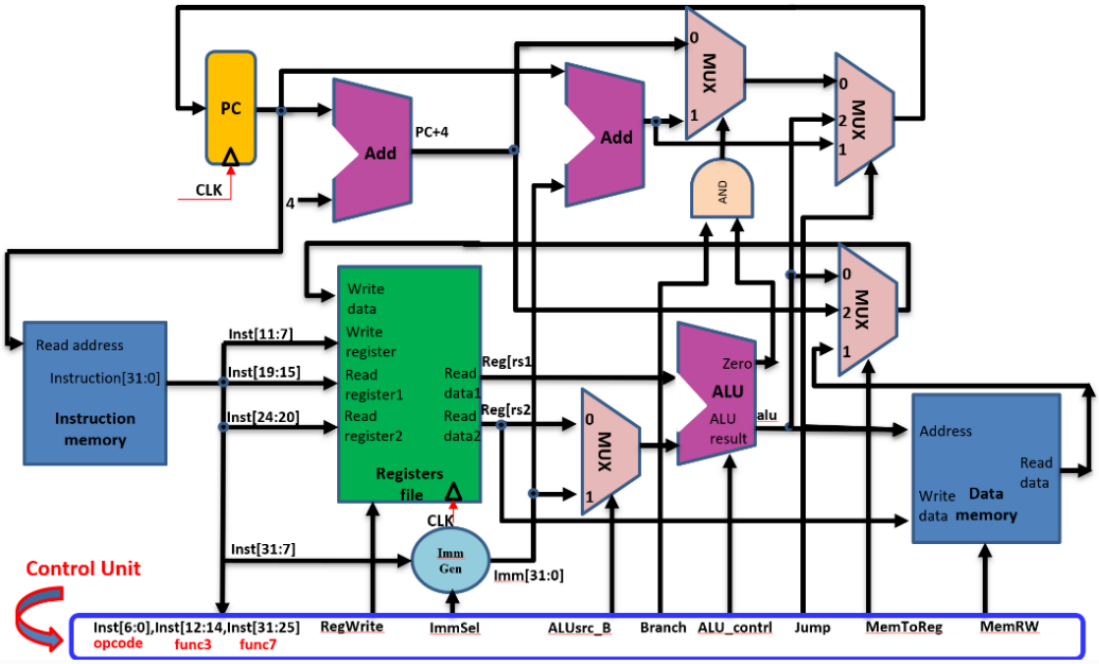
单周期CPU 例题

数据通路

1. Assume that the logic blocks used to implement a processor's datapath have the following latencies:

Clk-to-Q	RegFile Read	Register Setup	MUX	Adder	ALU	ImmGen	I/D-Mem Read	D-Mem Setup	Single Gate
5ns	35ns	20ns	15ns	20ns	90ns	40ns	300ns	200ns	5ns

- "Clk-to-Q" is the time needed after the rising clock edge for the new register value to appear on the output. This value applies to the PC only.
- "Register setup" is the amount of time a register's data input must be stable before the rising edge of the clock. This value applies to both the PC and Register File.
- "D-Mem Setup" is the amount of time a D-Mem's data input must be stable before the rising edge of the clock. This value applies to the D-Mem.
- Ignore the delay of the control signal.
- 我们约定使用下图的数据通路 **请注意，考试的时候尤其是选择器未必使用这种通路**



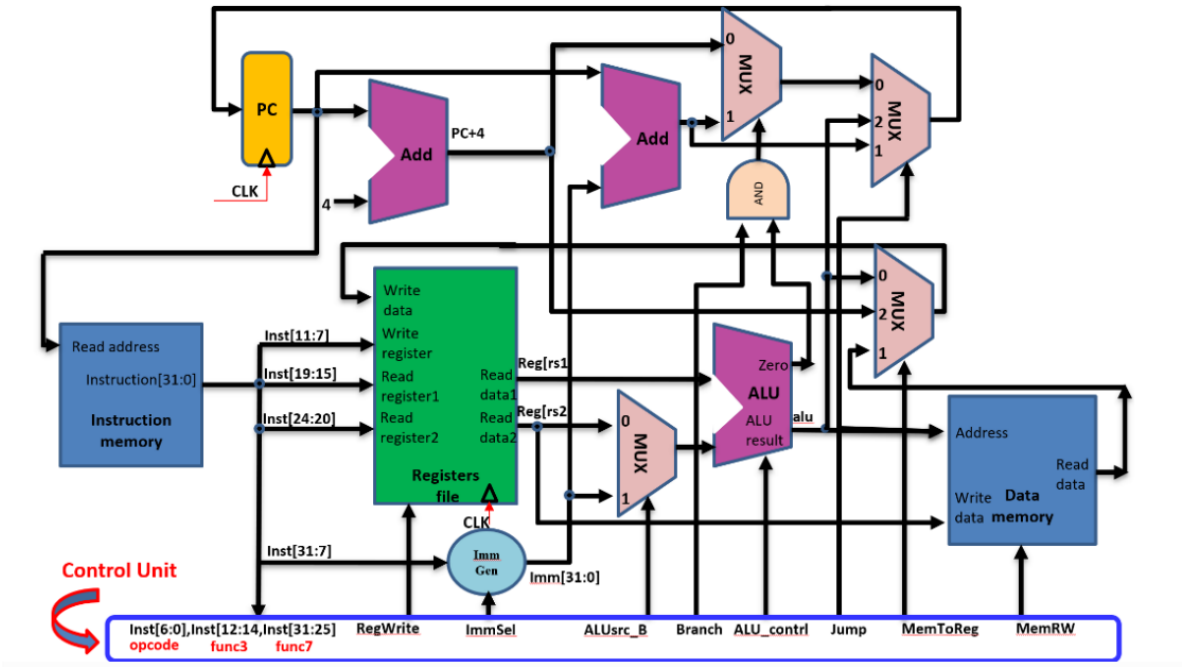
Quesition: Calculate the latency of add, addi, lw, sw, beq, jal.

2. Single-cycle processors are typically limited in their clock speed due to the necessity of completing the longest instruction within one clock cycle, which affects the overall performance scalability of the processor. （T/F）
3. 单周期 CPU 中，以下哪些操作是不能在一个时钟周期内完成的
   A. 从内存里读，并写数据
   B. ALU 计算，并写数据到内存
   C. 更新 PC, 并写数据到内存
   D. 从寄存器堆读值，进行 ALU 计算，并写数据到内存。

4. It is possible to execute the stages of the single cycle data path in parallel to speed up execution of a single instruction. (T/F)
5. For which instructions (if any) is the Imm Gen block on the critical path?

控制信号取值

1. 仍然是以下这张图



Given the control signal as following

	ImmSel
I-type	00
S-type	01
SB-type	10
UJ-type	11

	ALU control
Add	0010
sub	0110
and	0000
or	0001
slt	0111

	MemRW
Mem Read	10
Mem Write	01
No action	00

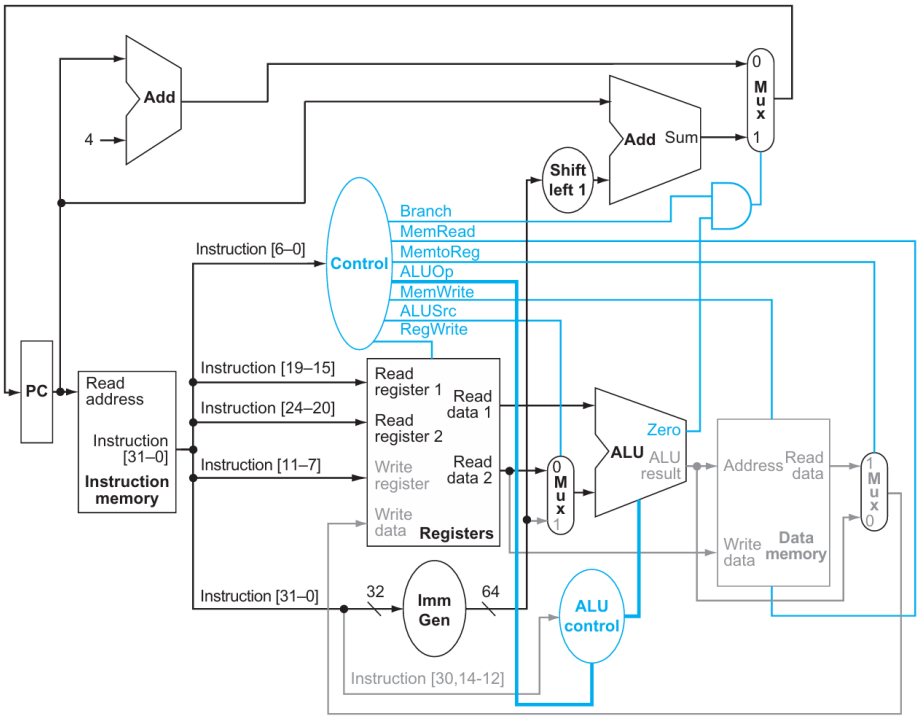
Please given out the control signals

inst	Regwrite	Immsel	ALUsrcB	Branch	ALU control	Jump	MenToReg	MemRW
Jal Label								
LW xd,D(xs)								

2. When silicon chips are fabricated, defects in materials (e.g., silicon) and manufacturing errors can result in defective circuits. A very common defect is for one signal wire to get "broken" and always register a logical 0. This is often called a "stuck-at-0" fault.
    - Which instructions fail to operate correctly if the MemToReg wire is stuck at 0?
    - Which instructions fail to operate correctly if the ALUSrc wire is stuck at 0?

修改元件

1. Examine the difficulty of adding a proposed `lwi.d rd, rs1, rs2 ("Load With Increment")` instruction to RISC-V. Interpretation: `Reg[rd]=Mem[Reg[rs1]+Reg[rs2]]`
    1. Which new functional blocks (if any) do we need for this instruction?
    2. Which existing functional blocks (if any) require modification?
    3. Which new data paths (if any) do we need for this instruction?
    4. What new signals do we need (if any) from the control unit to support this instruction?
2. Examine the difficulty of adding a proposed `swap rs1, rs2` instruction to RISC-V. Interpretation: `Reg[rs2]=Reg[rs1]; Reg[rs1]=Reg[rs2]`
    1. Which new functional blocks (if any) do we need for this instruction?
    2. Which existing functional blocks (if any) require modification?
    3. What new data paths do we need (if any) to support this instruction?
    4. What new signals do we need (if any) from the control unit to support this instruction?
    5. Modify Figure 4.21 to demonstrate an implementation of this new instruction



3. Examine the difficulty of adding a proposed `ss rs1, rs2, imm (Store Sum)` instruction to RISC-V. Interpretation: `Mem[Reg[rs1]]=Reg[rs2]+immediate`

    1. Which new functional blocks (if any) do we need for this instruction?
    2. Which existing functional blocks (if any) require modification?
    3. What new data paths do we need (if any) to support this instruction?
    4. What new signals do we need (if any) from the control unit to support this instruction?
    5. Modify Figure 4.21 to demonstrate an implementation of this new instruction.

中断

1. 关于异常的说法，哪个是不正确的
   A. 进入处理程序前要把原因放入 cause register.
   B. 要把当前指令的地址放到 mepc, 以便处理程序执行结束后返回
   C. 要调到 mtvec 的位置
   D. 处理程序执行结束后要 jalr x0, 0(x1)