外设

存储层级

定义

1. 正确，因为 命中次数断崖式的高

CPI 计算

> 第一题展示存储会造成什么样的等待

1. Instruction cache miss rate is 2%；Data cache miss rate is 4%；CPI without any memory stalls is 2；Miss penalty is 100 cycles；The frequency of all loads and stores in gcc is 36%

   Q: How faster a processor would run with a perfect cache?

   Instruction miss cycles = I×2%×100 =2.00I

   Data miss cycles = I×36%×4%×100 =1.44I

   Total memory-stall cycles= 2.00I+ 1.44I =3.44 I

   CPI with stall = CPI with perfect cache + total memory-stalls = (2 + 3.44)I = 5.44I

2. 200 MHz. 采用 mixed cache. ALU/Logic 35% Load 30% Store 15% Branch 20% cache hit rate 98%, 内存读写 100ns. branch 采用 predict-not-taken. 假设跳转在 3rd 阶段决定。 branch not taken 的比例为 40%, load 后有 50% 的比例会有 load-use hazard. 求 CPI.

$$
\begin{aligned}
&\text{基础：} 1 \\
&\text{指令未命中：} 2\% \times 10^{-7}s \times 200 \times 10^{6}s^{-1} = 0.4 \\
&\text{访存结构冒险：} (15\% + 30\%) \times (1 + 0.4) = 0.63 \\
&\text{分支预测错误：} 20\% \times 3 \times 60\% = 0.36 \\
&load - use\ hazard\text{：} 30\% \times 50\% \times 1 = 0.15 \\
&\text{总计：} 1 + 0.4 + 0.63 + 0.36 + 0.15 = 2.54
\end{aligned}
$$

3. Assuming a base CPI of 1.0 without any memory stalls, what is the total CPI for P1 with the addition of an L2 cache?Assume that P1clock cycle is 0.66ns, L1 miss rate is 8%, L1 hit time is 0.66ns, L2 miss rate is 95%, L2 hit time is 5.94ns, main memory need 70.62ns, 36% instructions need memory access.

$$
\begin{aligned}
L1 - cache &: 1cycle \\
L2 - cache &: \frac{5.94}{0.66} = 9cycles \\
mainmemory &: \frac{70.62}{0.66} = 107cycles \\
totally &: 1 + 36\% \times 1 + 36\% \times 8\% \times 9 + 36\% \times 8\% \times 95\% \times 107 = 4.186
\end{aligned}
$$

虚拟地址

页表大小计算

1. Virtual address 48 bit，DRAM 512GiB，SRAM 256GiB，PageSize 4 KiB，PageEntry 4 bytes 求5并行进程需要多大的PageTable

$$虚拟页数：\frac{2^{48(virtual\ address)}}{4KB(page\ entry)}=2^{36}pages$$

$$一个进程大小是：4B(表项)\times 2^{36}pages=256GB$$

$$5个进程：1280GB$$

过程模拟

Virtual memory uses a page table to track the mapping of virtual addresses to physical addresses. This exercise shows how this table must be updated as addresses are accessed. The following data constitute a stream of virtual byte addresses as seen on a system. Assume 4 KiB pages, a four entry fully associative TLB, and true LRU replacement. If pages must be brought in from disk, increment the next largest page number.

Decimal	4669	2227	13916	34587	48870	12608	49225
hex	0x123d	0x08b3	0x365c	0x871b	0xbee6	0x3140	0xc049

TLB

Valid	Tag	Physical Page Number	Time Since Last Access
1	0xb	12	4
1	0x7	4	1
1	0x3	6	3
0	0x4	9	7

Page table

Index	Valid	Physical Page or in Disk
0	1	5
1	0	Disk
2	0	Disk
3	1	6
4	1	9
5	1	11
6	0	Disk
7	1	4
8	0	Disk
9	0	Disk
a	1	3
b	1	12

- For each access shown above, list whether the access is a hit or miss in the TLB, whether the access is a hit or miss in the page table, whether the access is a page fault, the updated state of the TLB.

  以下仅为参考答案，实际上PF必然PTmiss

  4KB，则offset12位，因此第一个16进制位是page number

Address	Virtual Page	TLB H/M	TLB		
			Valid	Tag	Physical Page
4669 0x123d	1	TLB miss PT hit PF	1	b	12
			1	7	4
			1	3	6
			1 (last access 0)	1	13
2227 0x08b3	0	TLB miss PT hit	1 (last access 1)	0	5
			1	7	4
			1	3	6
			1 (last access 0)	1	13
13916 0x365c	3	TLB miss PT hit	1 (last access 1)	0	5
			1	7	4
			1 (last access 2)	3	6
			1 (last access 0)	1	13
34587 0x871b	8	TLB miss PT hit PF	1 (last access 1)	0	5
			1 (last access 3)	8	14
			1 (last access 2)	3	6
			1 (last access 0)	1	13
48870 0xbee6	b	TLB miss PT hit	1 (last access 1)	0	5
			1 (last access 3)	8	14
			1 (last access 2)	3	6
			1 (last access 4)	b	12
12608 0x3140	3	TLB miss PT hit	1 (last access 1)	0	5
			1 (last access 3)	8	14
			1 (last access 5)	3	6
			1 (last access 4)	b	12
49225 0xc040	c	TLB miss PT hit PF	1 (last access 6)	c	15
			1 (last access 3)	8	14
			1 (last access 5)	3	6
			1 (last access 4)	b	12

- Discuss why a CPU must have a TLB for high performance. How would virtual memory accesses be handled if there were no TLB?

  Without a TLB, almost every memory access would require two accesses to RAM: An access to the page table, followed by an access to the requested data.

稳定性的衡量

1. Mean time between failures (MTBF), mean time to replacement (MTTR), and mean time to failure (MTTF) are useful metrics for evaluating the reliability and availability of a storage resource. Explore these concepts by answering the questions about a device with the following metrics:

MTTF	MTTR
3 years	1 Day

   - Calculate the MTBF for such a device.

     MTBF (Mean Time Between Failures) 平均故障间隔时间= MTTF+ MTTR= 3年零一天

   - Calculate the availability for such a device.

$$= \frac{MTTF}{MTTF + MTTR} = \frac{1095}{1096} = 99.90875912\%$$

- What happens to availability as the MTTR approaches 0? Is this a realistic situation?

  `Availability approaches 1`，随着技术进步是可能很快的更换硬盘的，但是由于文件系统和其他数据很复杂又会导致较难实现

  - What happens to availability as the MTTR gets very high, i.e., a device is difficult to repair? Does this imply the device has low availability?
    - 很大概率是会的，但是如果 MTTF 变得足够大也不一定很低

RAID

1. RAID 中，Rundancy 是作用是什么
   A. 提高速度
   B. 忘了
   C. 检验读写正确性
   D. 提高硬盘的是 reliability

背书题 D

总线

CPU 与外设的交互

1. DMA：数据传输不占用 CPU 时间 → 效率最高。

   Interrupt：CPU 只在 I/O 开始和结束时参与，等待时可执行其他任务 → 效率中等。

   Polling：CPU 持续等待，大量时间被浪费 → 效率最低。

   DMA>Interrupt>Polling
2. **Polling**：不要求并行，反而串行忙等。**Interrupt**：会interrupt。**DMA**：要求并行