外设

存储层级

定义

1. 判断：内存结构中耗时最多的是最上层（L1-cache）

CPI 计算

1. Instruction cache miss rate is 2%；Data cache miss rate is 4%；CPI without any memory stalls is 2；Miss penalty is 100 cycles；The frequency of all loads and stores in gcc is 36%

   Q: How faster a processor would run with a perfect cache?

2. 200 MHz. 采用 mixed cache. ALU/Logic 35% Load 30% Store 15% Branch 20% cache hit rate 98%, 内存读写 100ns. branch 采用 predict-not-taken. 假设跳转在 3rd 阶段决定。 branch not taken 的比例为 40%, load 后有 50% 的比例会有 load-use hazard. 求 CPI.
3. Assuming a base CPI of 1.0 without any memory stalls, what is the total CPI for P1 with the addition of an L2 cache?Assume that P1clock cycle is 0.66ns, L1 miss rate is 8%, L1 hit time is 0.66ns, L2 miss rate is 95%, L2 hit time is 5.94ns, main memory need 70.62ns, 36% instructions need memory access.

虚拟地址

页表大小计算

1. Virtual address 48 bit，DRAM 512GiB，SRAM 256GiB，PageSize 4 KiB，PageEntry 4 bytes 求5并行进程需要多大的PageTable

过程模拟

1. Virtual memory uses a page table to track the mapping of virtual addresses to physical addresses. This exercise shows how this table must be updated as addresses are accessed. The following data constitute a stream of virtual byte addresses as seen on a system. Assume 4 KiB pages, a four entry fully associative TLB, and true LRU replacement. If pages must be brought in
   from disk, increment the next largest page number.

Decimal	4669	2227	13916	34587	48870	12608	49225
hex	0x123d	0x08b3	0x365c	0x871b	0xbee6	0x3140	0xc049

TLB

Valid	Tag	Physical Page Number	Time Since Last Access
1	0xb	12	4
1	0x7	4	1
1	0x3	6	3
0	0x4	9	7

Page table

Index	Valid	Physical Page or in Disk
0	1	5
1	0	Disk
2	0	Disk
3	1	6
4	1	9
5	1	11
6	0	Disk
7	1	4
8	0	Disk
9	0	Disk
a	1	3
b	1	12

- For each access shown above, list whether the access is a hit or miss in the TLB, whether the access is a hit or miss in the page table, whether the access is a page fault, the updated state of the TLB.
- Discuss why a CPU must have a TLB for high performance. How would virtual memory accesses be handled if there were no TLB?

稳定性的衡量

1. Mean time between failures (MTBF), mean time to replacement (MTTR), and mean time to failure (MTTF) are useful metrics for evaluating the reliability and availability of a storage resource. Explore these concepts by answering the questions about a device with the following metrics:

MTTF	MTTR
3 years	1 Day

   - Calculate the MTBF for such a device.
   - Calculate the availability for such a device.
   - What happens to availability as the MTTR approaches 0? Is this a realistic situation?

- What happens to availability as the MTTR gets very high, i.e., a device is difficult to repair? Does this imply the device has low availability?

RAID

1. RAID 中，Rundancy 是作用是什么
   A. 提高速度
   B. 忘了
   C. 检验读写正确性
   D. 提高硬盘的是 reliability

总线

CPU 与外设的交互

1. 对3种I/O方式polling，interupt，DMA据CPU efficiency从高到低排序
2. 在polling、DMA和interruption中，哪种要求processor与IO并行（或者都不需要）