1. Introduction (15%)

1.1 (10%) Consider three processors, A, B and C, which have the following characteristics:

PROCESSOR A	PROCESSOR B	PROCESSOR C
Clock rate: 6 GHz	Clock rate: 3 GHz	Clock rate: 4 GHz
CPI: 1.5	CPI: 0.5	CPI: 2.0

If it takes 10 seconds for Processor A to execute the program, how many instructions and cycles does this program have? How long does it take for Processor B to finish?

A:

1.2 (5%) A computer system has a task that can be divided into two parts: Part A and Part B. Part A takes up 80% of the total time to complete the task, while Part B takes up the remaining 20%. If we can speed up Part A by a factor of 4 and Part B by a factor of 2, what is the overall speedup that we can achieve using Amdahl's law?

A:

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2. Arithmetic for Computer (35%)

2.1 (5%) What is the octal value of `0x20240511`?

A: _____

2.2 (5%) What is the binary value of -219 (using 2's complement)?

A: _____

2.3 (5%) What is the binary bit pattern representation of -20.796875 (using single precision)?

A: _____

2.4 (5%) What is the double precision representation of -20.796875?

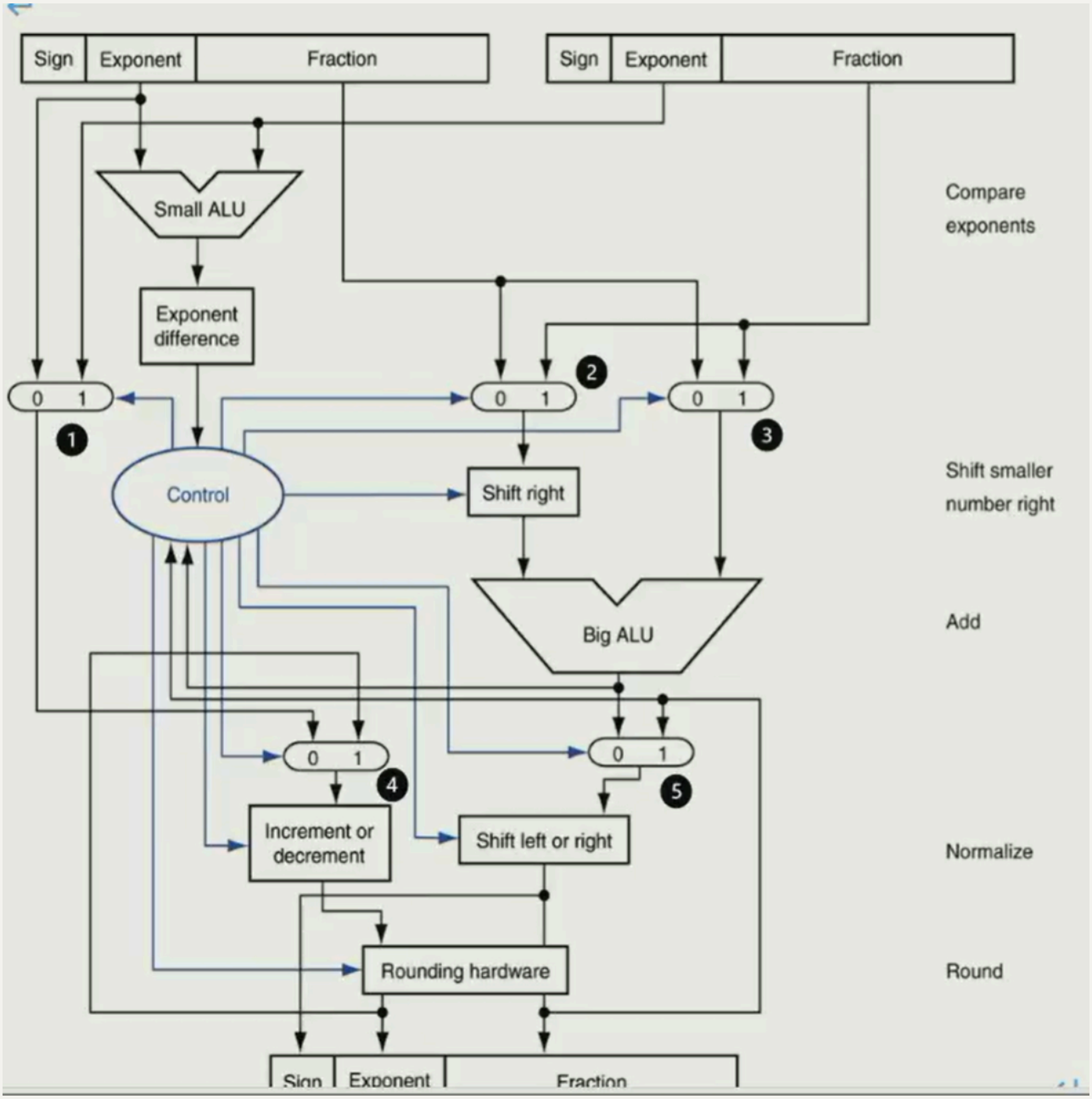
A: _____

2.5 (15%) Floating arithmetic
(Refer to the provided diagram of the floating-point addition unit for part 2)

(1) Calculate $2.6015625 + 5.46875 \times 10^{-2}$ by hand. Assume 1 guard, 1 round bit and 1 sticky bit, and round to the nearest even. Show all the steps, write your answers in single precision floating point format, show all the necessary steps.

(2) What are the control signals for the five MUXs in the provided diagram? Suppose `2.6015625` is placed in the RIGHT side circuit.

A:



3. Instruction (30%)

3.1 (6%) Translate the following two RISC-V assembly codes into binary and hex:

(1) `lw x5, 16(x10)`

A: _____

(2) `bne x4, x5, 50`

A: _____

3.2 (4%) What is the assembly instruction of the following machine code `0x10942C23`?

A: _____

3.3 (10%) Suppose you executed the code below on a version of the single-cycle CPU. All registers are initialized to zero.

```
1  main:  addi x1, x0, 1
2         addi x2, x0, 3
3         ori  x3, x1, 8
4         xor  x4, x3, x2
5
6         sw   x1, 0(x4)
7         and  x2, x2, x4
8         sw   x2, 4(x4)
9         sub  x6, x2, x1
10        bge  x4, x3, L1
11        srli x2, x2, 1
12        jal  x5, L2
13
14 L1:    slli x10, x22, 2
15        add  x10, x10, x4
16        lw   x9, 0(x10)
17        bne  x9, x6, Exit
18        addi x22, x22, 1
19        beq  x0, x0, L1
20
21 L2:    addi x22, x22, 1
22 Exit:
```

After the instructions running, what is the content of register:

- **x4 is ( )**
- **x2 is ( )**
- **x9 is ( )**
- **x22 is ( )**
- **x10 is ( )**

3.4 (10%) Implement the following C code in RISC-V.

```c
#define M 10
void transpose(int A[M][M]) {
    int i, j;
    for (i = 0; i < M; i++) {
        for (j = 0; j < i; j++) {
            int t = A[i][j];
            A[i][j] = A[j][i];
            A[j][i] = t;
        }
    }
}
```

A:

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4. Single cycle processor (20%)

4.1 (10%) Suppose you are designing a single cycle processor that only supports S-type instructions. Draw the most COMPACT processor design below (e.g. no branch modules), including both datapath and control logic.

A: *(Space for drawing)*

4.2 (5%) How many control signals are decoded from the instruction? What are their values for the instruction `sd, x6, 16(x5)`?

A:

4.3 (5%) Suppose you are adding support for R-type instructions to your processor. How many more control signals are decoded from the instruction? What are their values for the instruction `add x1, x2, x3`?

A:
