NMJ31804 – PRINCIPLES OF COMPUTER ARCHITECTURE
Semester 2, 2021/2022

LAB 4: Design of Memory Module RAM and ROM

Task 1:

Integrate all components from pre lab to build a simple system as shown in Figure 9. The input for this system is **reset signal** and **clock signal** and the output is **Data_out**. Connection between components is done using s_Data, s_Address, s_ROM, s_RAM and s_read. Write a Verilog code and simulation result should be as shown in Figure 10.

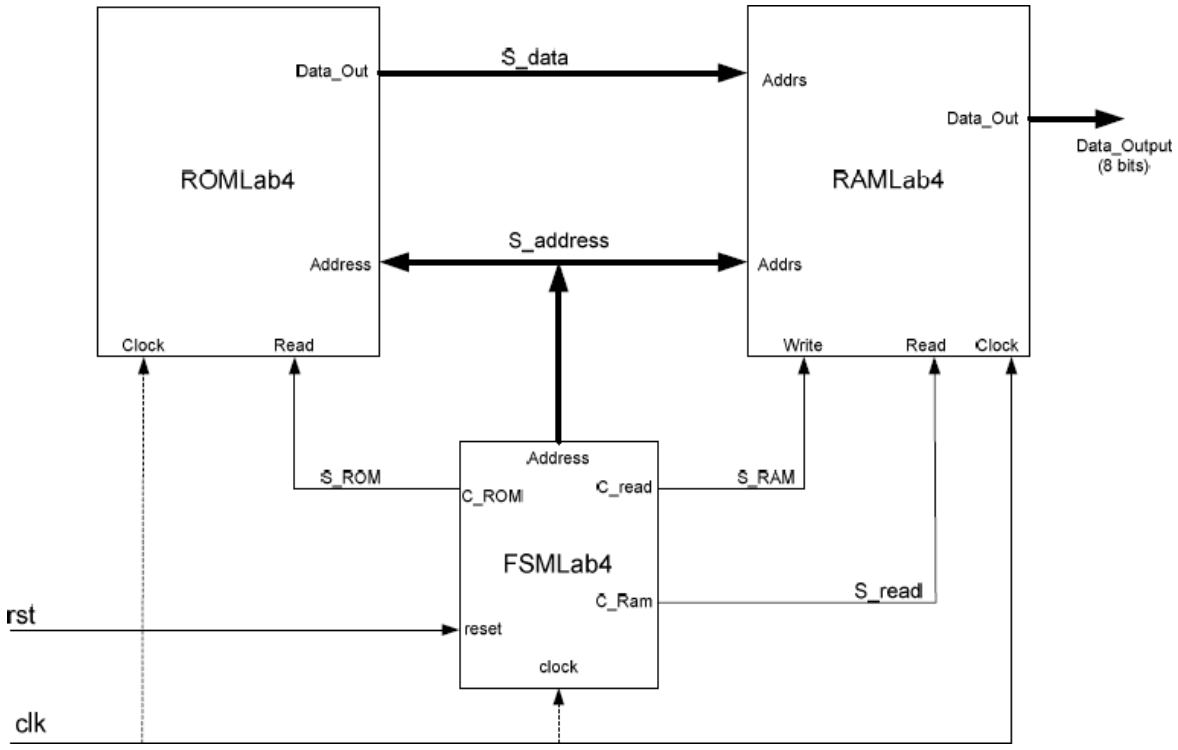

Figure 9: Block Diagram of Overall Components

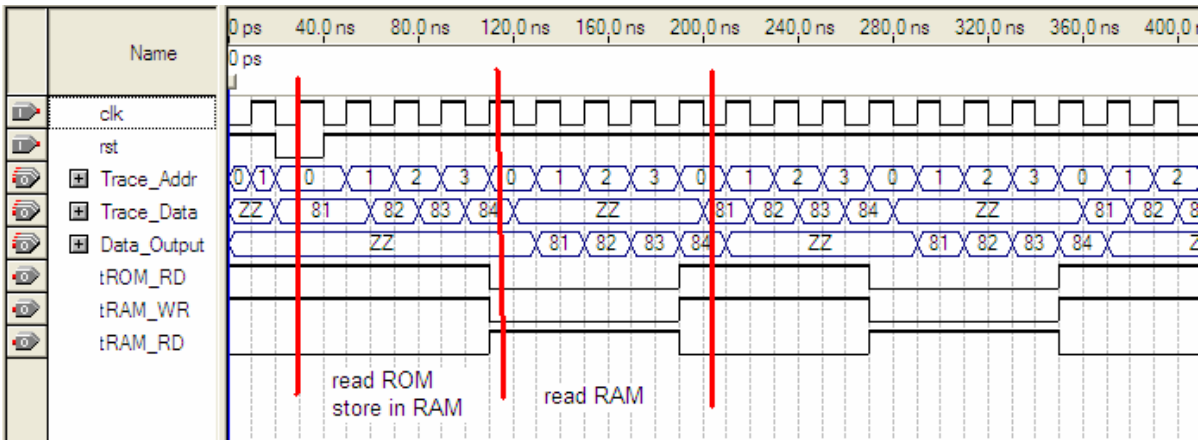

Figure 10: Simulation Result of Overall Components

Task 2:

Write a Verilog code to perform the following function.

Data from ROM1 and ROM2 is added and the result is stored in RAM (refer to Figure 11). You must design each module first and then integrate all modules. Show in detail the flowchart of control unit.

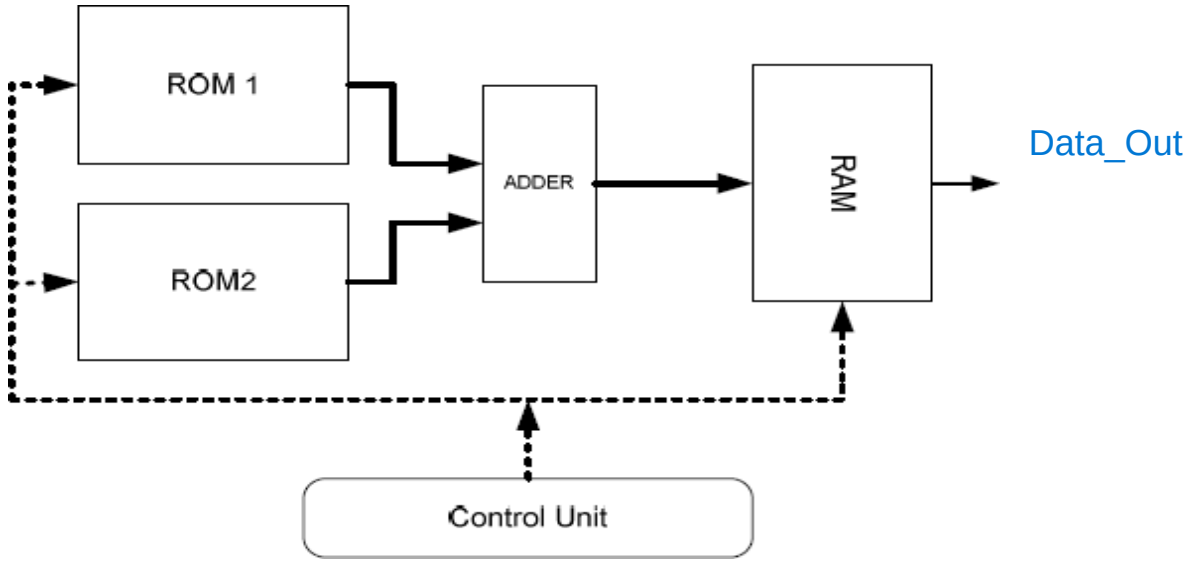

Figure 11: Memory Modules Integration

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