



Exercise 9

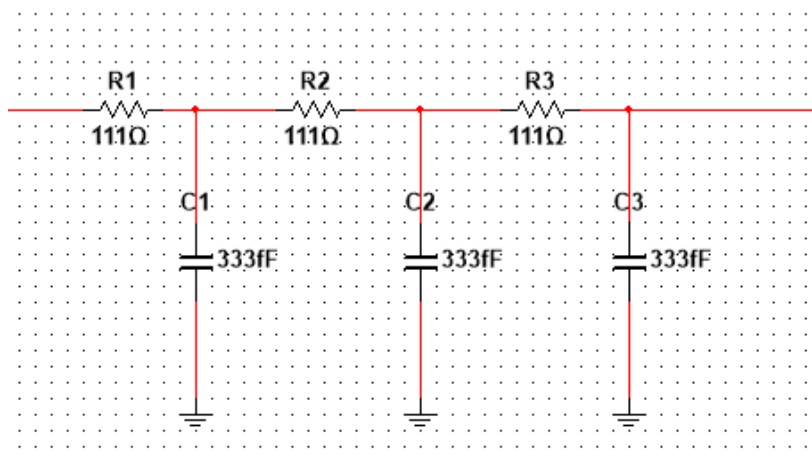
9-1 Consider a 5 mm-long, 4 λ -wide metal2 wire in a 0.6 μm process. The sheet resistance is 0.08 Ω/\square and the capacitance is 0.2 fF/ μm . Construct 3-segment L-model and 3-segment π -model for the wire. (Please present models and calculate delay).

Answer

$$R = R_{\square} \frac{l}{w}$$

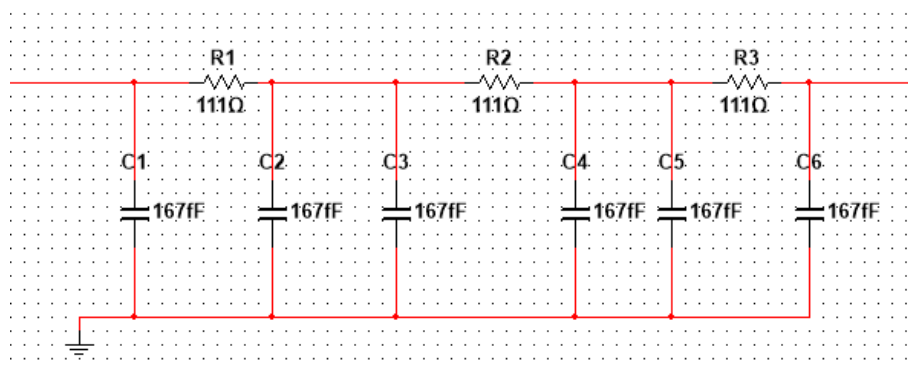
The wire width is 1.2 μm so the wire is 5000 $\mu\text{m}/1.2 \mu\text{m} = 4167$ squares in length

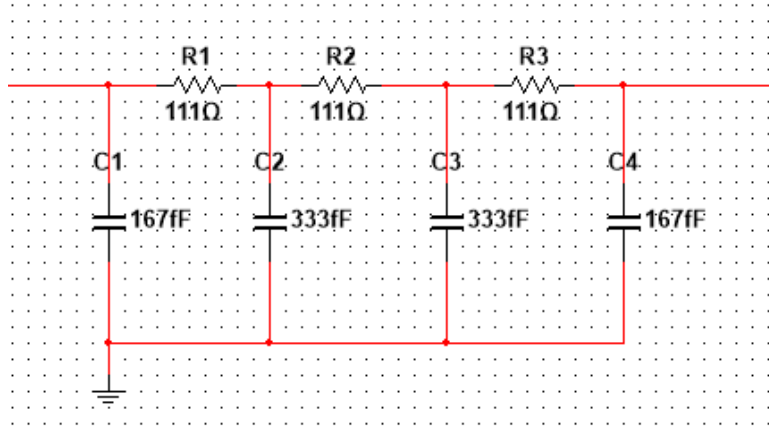
So, the total resistance is $(0.08 \Omega/\text{sq}) \times 4167 \text{ sq} = 333 \Omega$ The total capacitance is $(0.2 \text{ fF}/\mu\text{m}) \times 5000 \mu\text{m} = 1 \text{ pF}$



3-segment L-model

$$\tau = C_1 R_1 + C_2 (R_1 + R_2) + C_3 (R_1 + R_2 + R_3) = 2.22 \times 10^{-10} \text{ s}$$





3-segment π -model

$$\tau = C_2 R_1 + C_3 (R_1 + R_2) + C_4 (R_1 + R_2 + R_3) = 1.67 \times 10^{-10} \text{ s}$$

9-2 Assume an inverter is designed with a PMOS/NMOS ratio of 3.6 and the NMOS transistor is minimum size. ($W = 0.375 \mu\text{m}$, $L = 0.25 \mu\text{m}$, $W/L = 1.5$). $V_M = 1.25 \text{ V}$, $V_{DD} = 2.5 \text{ V}$. Please describe the voltage transfer characteristic and noise margins of CMOS inverter. (use V_{IL} , V_{IH} , NM_H , NM_L and g). The parameters shown in table 9.1.

Table 9.1

	V_{T0} (V)	γ ($\text{V}^{1/2}$)	V_{DSAT} (V)	K ($\mu\text{A}/\text{V}^2$)	λ (V^{-1})
NMOS	0.7	0.45	0.83	134	0.1
PMOS	-0.8	-0.4	-1	-50	-0.2

$$K = \frac{1}{2} \mu C_{ox}$$

Answer

$$I_D(V_M) = K_N \left(\frac{W}{L} \right)_N (V_{GS} - V_{THN})^2 (1 + \lambda_n V_M) = 68.4 \times 10^{-6} \text{ A}$$

$$g = \frac{-1}{I_D(V_M)} \times \frac{k_n \frac{W}{L}_n V_{DSATn} + k_p \frac{W}{L}_p V_{DSATp}}{\lambda_n - \lambda_p} = -24.93$$

$$V_{IH} = V_M - \frac{V_M}{g} = 1.3$$

$$V_{IL} = V_M + \frac{V_{DD} - V_M}{g} = 1.2$$

$$NM_H = V_{DD} - V_{IH} = 1.2 \qquad NM_L = V_{IL} = 1.2$$