EE6610- IC packaging

Assoc. Prof. Poenar Daniel Puiu

3- Multichip & 3D packaging

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3- Multichip & 3D packaging

3.1- Introduction

A multichip module (MCM), or multichip package (MCP), is defined as a single unit ("package") containing 2 or more chips and an interconnection substrate which function together as a system building block. The MCM/MCP must provide the following *functions*:

- *Signal interconnect* & I/O management for the chips contained within the module, as well as *interfacing with the next level system elements*;
- *Thermal management* (typically cooling),
- *Mechanical support*, and
- *Environmental protection*.

MCMs or MCPs are an important technique for IC packaging and associated subsystem and system elements. They *evolved from the earlier traditional* ***hybrid packaging methods***.

The MCPs may be considered as an alternative to an Application Specific Integrated Circuit (ASIC), offering several significant *advantages (compared to CSP/DIL, traditional packaging)*:

- *Lower cost and faster time to market and potential for optimizing performance and functionality.*
- *Significant increase in packaging efficiency by replacing multiple packages with a single package.*
- *Major reduction in overall size and weight.*
- *Improved electrical performance —short interconnects, chips placed closer to each other to enhance signal propagation.*
- *Allows usage of mixed technologies —Si, SiGe, GaAs, etc- to further enhance performance and extend functionality.*
- *Improved reliability —multiple packages eliminated; total number of interconnects significantly reduced.*
- *Cost-effective, particularly at system level.*

Some authors consider that MCP includes the following types of packaging technologies:

a) The Hybrid Circuit (HC) or Hybrid Integrated Circuit (HIC),
b) The Multichip Modules (MCMs),
c) 3-D Packaging, and
d) System in Package (SiP) and System on Package (SoP).

3.1.1- The hybrid IC

A hybrid circuit **is defined as an assembly containing both active semiconductor devices (packaged and unpackaged) and *passive* components (deposited and discrete) interconnected on a common substrate offering a specific circuit function.** The active devices, include diodes, transistors, or integrated circuits, while passive devices are resistors, capacitors, and inductors. The substrate is, e.g., ceramic or Al_2O_3, and with patterned ***thick film*** conductors, resistors and dielectrics.

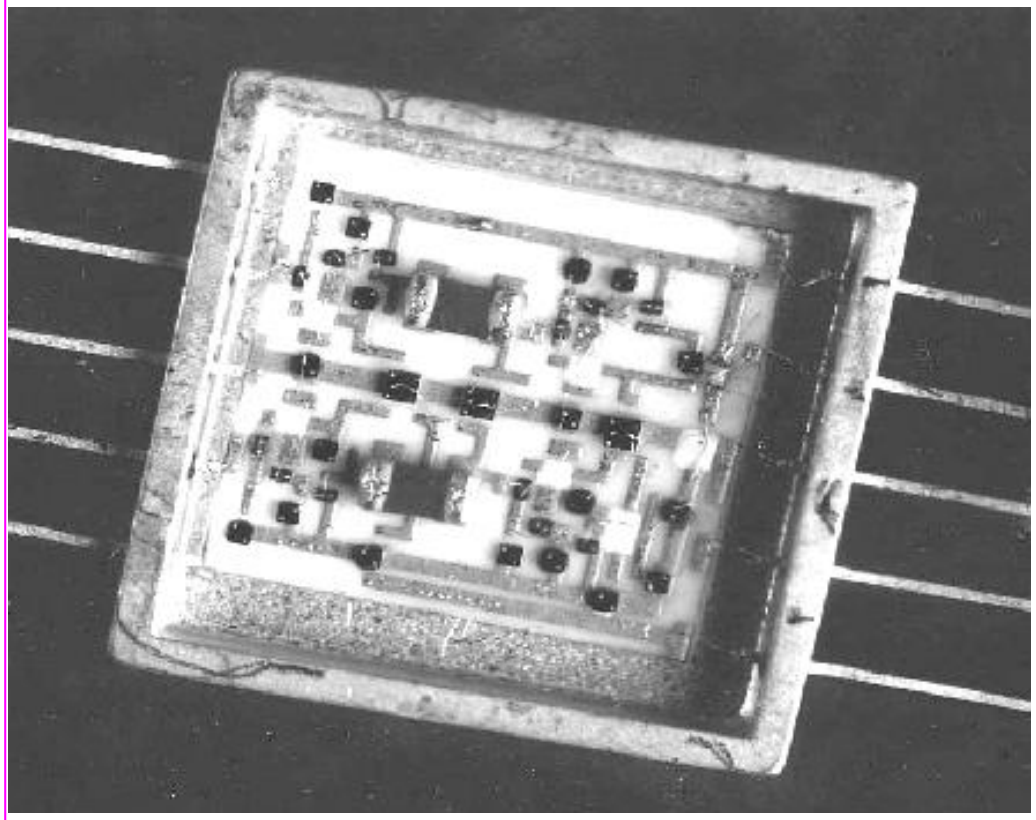


Fig.3.1: Hybrid circuit with transistors and diodes (Circa 1960s)

Fig.3.1 shows an early hybrid circuit (circa '60s) with diodes, transistors and deposited thick film

resistors and discrete capacitors. The active devices were chip and wire assembled to a single level gold conductor deposited on the ceramic substrate and patterned using thick film screen printing. The substrate is shown mounted into a metal package with wires bonded from the substrate I/O pads to the package leads. A metal lid could then be welded in place to provide a hermetic enclosure that allows the assembly to be electrically tested and function in a benign or controlled environment.

When the IC became readily available it was quickly incorporated into the hybrid (Fig.3.2) as the active device replacing the earlier discrete diodes and transistors. The hybrid circuit was the predecessor of the multichip module and ideal for many custom applications not available at the time as a monolithic IC. The hybrid circuit, with addition of the IC, achieved an immediate increase in both functional density and packaging efficiency. With the elimination of multiple packages the potential for improved reliability was an added value.

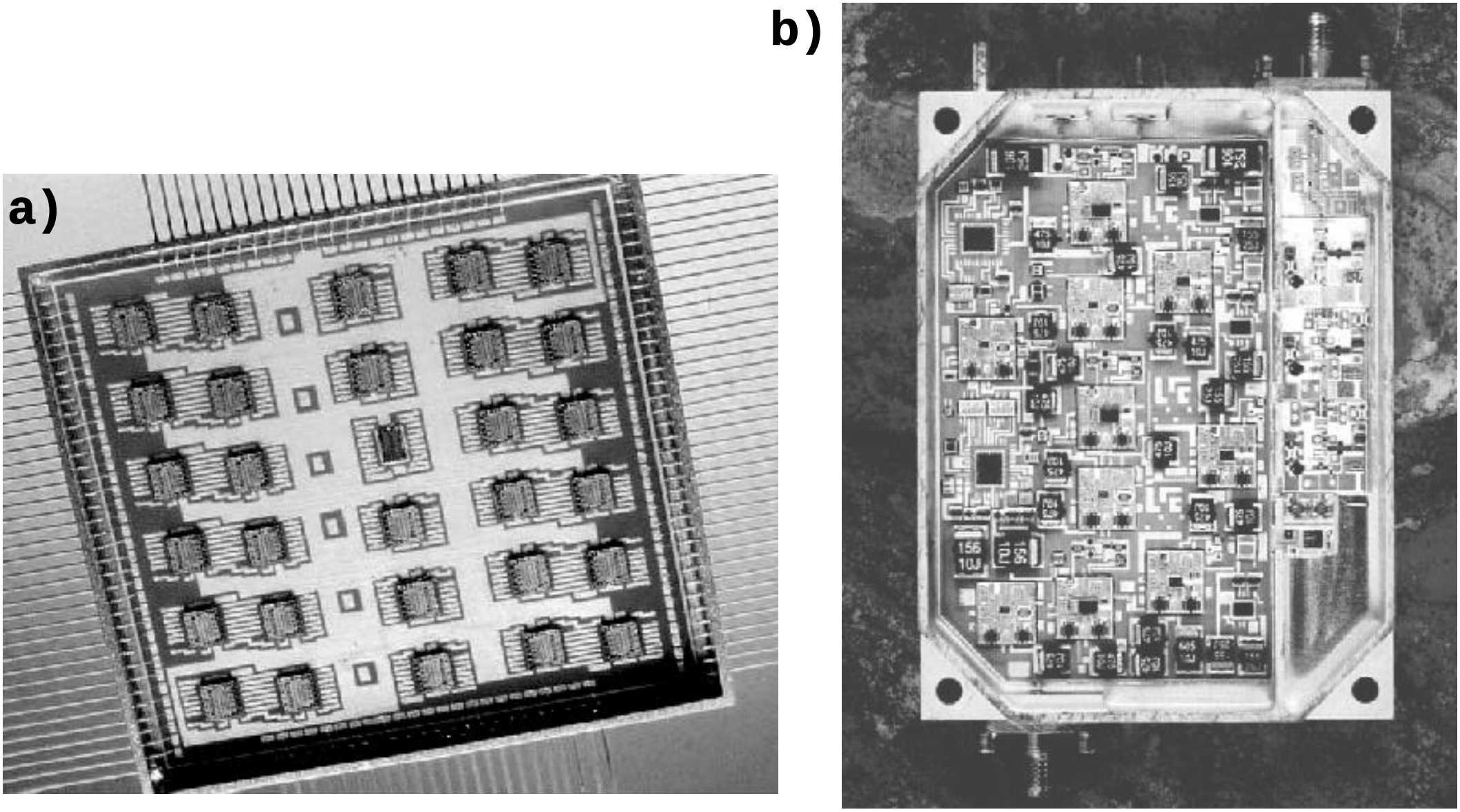


Fig.3.2: a) Multiple ICs on multilevel thick film conductor pattern (circa early 1980s); b) RF/Microwave hybrid circuit

3.2- Features, advantages & disadvantages of MCMs

3.2.1- Main features of MCM

The *main reasons* driving/motivating the development & application of MCMs: *dimensional constraints & increased performance*.

Advantages: Increased chip density with minimum volume and weight than individually packaged parts (single chip packaging). This ↑ *chip density* is *a key factor that sets it apart from its initial hybrid packaging precursor*. *Other benefits:* ↑ reliability & *in some cases* ↓ cost (usually for military & aerospace applications, in which a standard realization with separate components needs to go through tough & complex qualifications for each separate component).

For a package containing multiple chips to be classified as an MCM, the surface area covered by active semiconductor devices (chip covered area A_C) should be equal or greater than 50% of the substrate's (package or carrier) area A_S :

$$A_C \geq 0.5\, A_S \quad (3.1).$$

The ***substrate or carrier is the key element*** in any MCP and especially in the MCM, as *it is the main factor providing most of the previously mentioned functions*. *It is possible to have an interconnecting substrate* (provides electrical interconnections for signal & power supply conductors) *that is different from the mechanical substrate* (provides mainly physical support & thermal dissipation), *as is typically the case in thin-film MCMs*.

Disadvantages:

- *The cost can be higher (especially in low volume production);*
- *↓ yield, especially when not all components can be tested a priori;*
- *The existence of another level of hierarchy can be an added complication & risk in the system development*. Fig.3.3 identifies the hierarchical levels of a complex electronic system, which may need to be realized/miniaturized at MCM level.

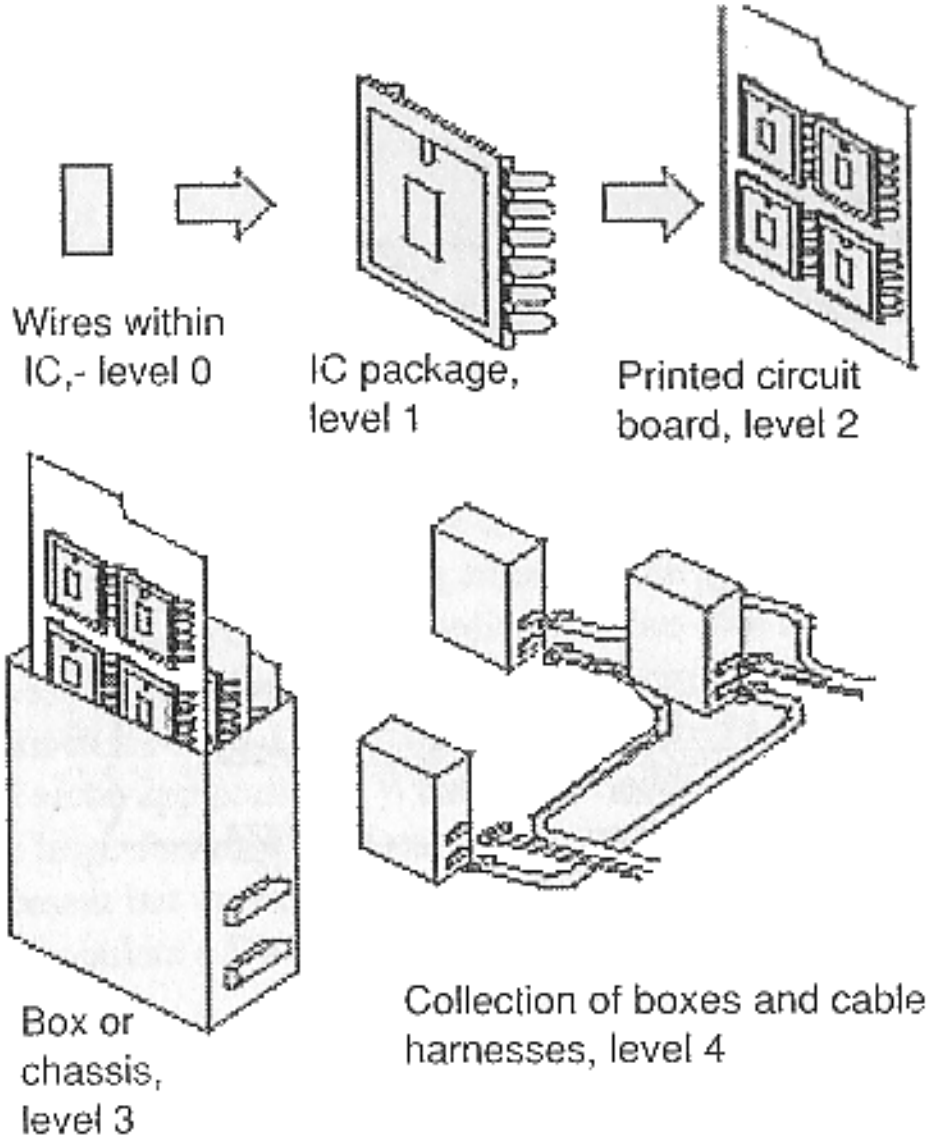


Fig.3.3: Packaging hierarchy of a traditional electronic system realized using discrete components.

Fig.3.4 shows an example of a typical MCM, highlighting clearly that the single most important characteristic of an MCM is the substrate. The package lid used to seal such an assembly is not shown in Fig.3.4. Hermetic sealing is preferred, particularly for aerospace or military applications.

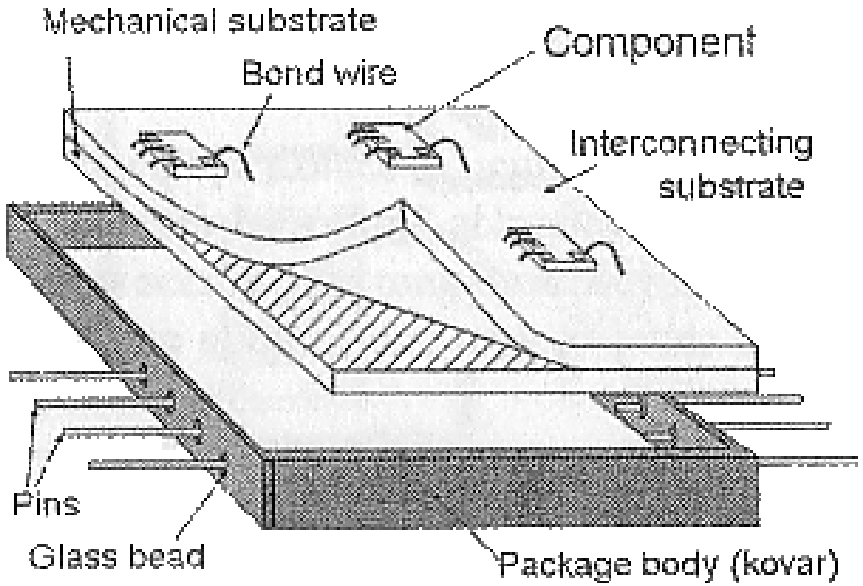
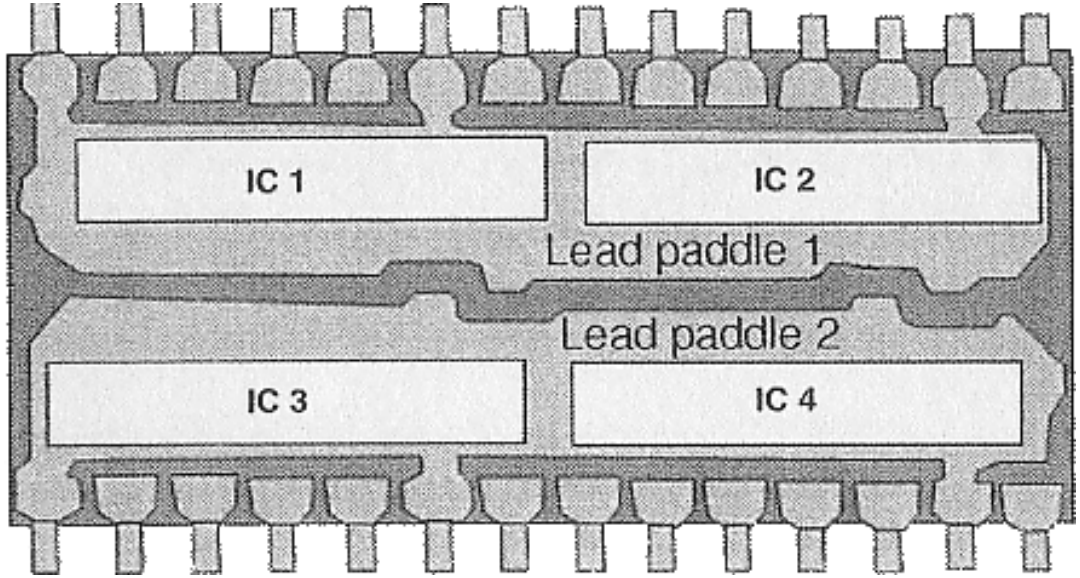


Fig.3.4: Features of a typical MCM.

a)



b)

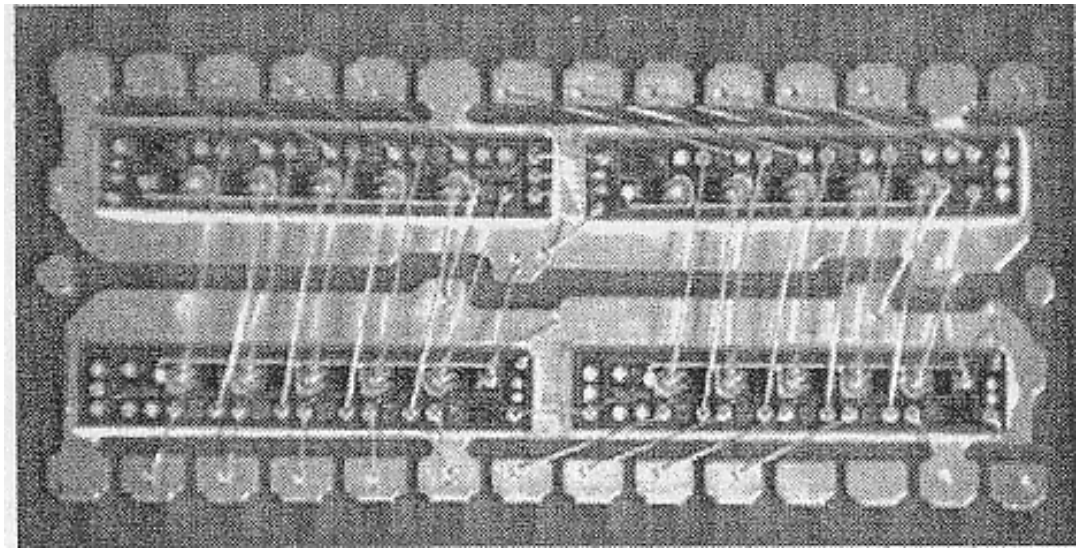


Fig.3.5 illustrates a 4-chip MCP. In fact, most 3D assemblies are die stacks that use such a MCP-based method.

Fig.3.5: Example of a MCP: a) Floorplan with 4 IC dies on 2 electrically isolated lead frame paddles; b) Photo of the real system showing its intrapackage bonding.

There are ***3 main types of MCM substrates***:

*1) Multilayer thin-film structures on semiconductor or ceramic base layers, with **deposited** metal conductors & dielectrics (MCM-Ds);*

*2) Thick-film/**cofired** multilayer ceramic technology (MCM-Cs);*

*3) Organic **laminate** multilayer board structures (MCM-Ls)*, similar to standard printed wiring boards (PWBs), but with denser component placement and greater wiring densities.

As mentioned above and schematically illustrated in Fig.3.6, the MCM provides numerous functions. *In order to be a highly functional MCM, the following criteria must be satisfied:*

a) Chip-to-chip spacing in the MCM must be held to a minimum to minimize signal propagation delays ⇒ the substrate must have *high wiring density* to support the necessary I/O ⇒ conductors must be made of high conductivity metals to ↓ *R*. **In addition**, the traces must be properly designed to *prevent*

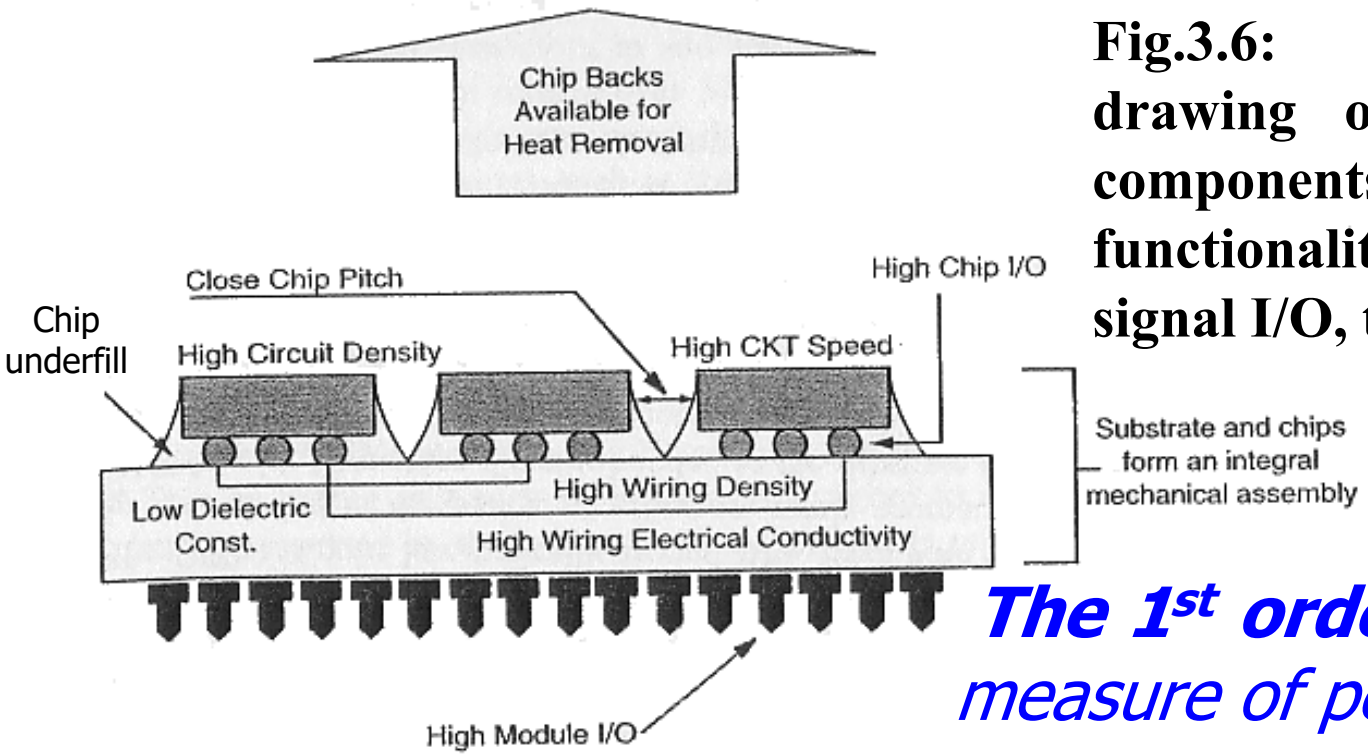


Fig.3.6: Schematic cross-sectional drawing of a MCM, illustrating its components and the various key functionalities that it must provide: signal I/O, thermal management, mechanical support & environmental protection.

The 1st order time constant (*as a measure of performance of the delay****) is:*** $\tau \cong RC = \frac{\rho}{A}\varepsilon_r C_0$ (3.2), where ρ = resistivity of the metal(s) used for interconnections, ε_r = permittivity of the inter-layer dielectric and/or of the substrate (e.g. lower for polyimide than for ceramics: ~3 vs. ~9).

b) The MCM must provide a means of thermal management to limit the junction temperature of the chips at T<85…100°C. This is typically accomplished through:

b.2) Substrate conduction (when chips are mounted to the substrate in the ***face-up configuration***), or

b.3) Heat conduction through the leads (solder balls) in low power applications if the chips are flip-chipped-mounted in a ***face-down configuration*** (as shown in Fig.3.6);

b.3) By using conductive fingers for heat removal in high power applications.

3) The MCM must provide reliable I/O connections to the next level of assembly in the system. Typically, this takes the form of an **interface with a PWB** although direct module interface with external system elements is possible. The number of module I/O is significantly ↓ from the Σ(individual chips I/O numbers).

4) The MCM must provide protection from the environment. Some **technique for sealing the packages**, or at least overcoating/encapsulation of the chips and their interconnects, **must be provided**.

3.2.2- Advantages of MCM

The need for the MCM arises because no single system can be fully integrated in a single chip. However, due to the progress of IC technology continues rapidly, this ultimately may be possible in a near future. At this moment, this cannot be achieved, or it would require a very large chip with very complex technical requirements and, hence, high development and manufacturing costs. Since MCMs use less complex chips and, for the most part, can be repaired, they can be less expensive, and easier and faster to develop. Therefore, MCM will remain the high performance (speed, volume, weight) choice for system packaging in the near future.

***MCMs have 5* major advantages *over individually packaged parts & monolithic systems*:**

1) Higher packaging efficiency (area of chip to area of the board), *due to the fact that the bare chips can be placed much closer together than chips in single chip packages on PCBs (because of the*

wasted space of the packages themselves);

2) Better electrical performance, *due to the shorter distances between chips and, hence, reduced substrate wiring length as well*;

3) Greater reliability *due to reduced number of interconnects between the chip and the board*, and

4) Potential lower cost (in high volume production) *because the individual IC packages are eliminated* $\Rightarrow \downarrow$ *substrate size*.

5) The ability to combine components from divergent processes within a single assembly. However, in practice, ***the objective of mixing technologies can be complicated by special requirements necessary for non-standard structures,*** *e.g. microwave ICs, or microelectromechanical system (MEMS) devices*.

3.2.3- Packaging efficiency

Packaging efficiency is defined as the ratio of the area of all the chips to the area of the MCM substrate, or, for individually packaged

parts, *the area of the system-level board*. Another *alternative names* for packaging efficiency are *'substrate density'* or *'density metric'*.

Traditional single chip packages such as dual in-line packages (DIPs) or quad flat packages (QFPs) require a lot of board real estate due to the packaging size itself and the need to have peripheral leads. Therefore, the board-level efficiency with such packages (DIPs, QFPs) is quite low, typically around 10%. Even with standard ball grid arrays and chip scale packages, the packaging efficiency rarely approaches 50%.

MCMs with bare chips directly bonded to the substrate can be much more efficient, with ***efficiencies approaching 80%***. *The MCM integrates all chip types and required interconnections into a single module together with large numbers of passive devices and other components*. **An integrated packaging structure in which most of the non-standard IC components, e.g. passive devices and specialized RF & microwave devices, are *embedded inside the board*** as thin- or thick-film layers**, thus reserving the top (and bottom) surfaces for the**

large, regularly sized ICs, is called *system-on-package* (SOP). *Its packaging efficiency could approach that of SOC/WSI*.

The ultimate packaging efficiency would be obtained if the entire system were integrated into a single chip, i.e. by SOC/WSI.

The *packaging efficiency of MCMs varies widely:* it is ***the lowest for MCM-L & MCM-C*** and **the highest for MCM-D**. The reason is that packaging efficiency is directly proportional to component I/O# and the wiring density supported by the **substrate**. Thin-film MCMs possess the highest **wiring density**, *measured as* ***length of minimum width track possible per unit area***, and typically provide the highest packaging efficiency because they can interconnect the ICs in the smallest area. Other significant ***benefits*** in addition to size, include ***better electrical performance*** due to shorter wiring length, and ***improved reliability*** due to elimination of one level of interconnect.

Strongly increased packaging densities are achieved using **3D assemblies**. However, in such a case, the ***packaging efficiency***

has to be *re-defined as* the amount of active area in the unit volume [cm^2/cm^3]. Most of current industrial applications usually achieve 5…200 cm^2/cm^3, but max. values of ~1500…2000 cm^2/cm^3 can be reached.

3.2.4- Electrical performance, yield & reliability, and cost of MCMs

Electrical MCM performance

***Fundamental electrical MCM performance can be measured by the* functional throughput rate (FTR)**, *defined as the product*

FTR = (Equivalent nr. of gates per module) × (Max. clock rate f_{MAX}) (3.3).

The maximum clock rate is usually defined as

$$f_{MAX} = 0.25 \cdot t_D \quad (3.4)$$, where

t_D = the delay associated with a typical gate. High-density MCMs can have FTRs in the range 10^8…10^{10} gate-MHz.

Moreover, in high-performance systems, signal-bearing conductors require low latency and distortion to support high clock frequencies. The propagation delay for digital signals can be roughly specified as

$$t_{prop} = t_{flight} + t_{rise} \quad (3.5), \text{ where}$$

t_{flight} is the delay component due to the time of flight: $t_{flight} = l\frac{\sqrt{\varepsilon_0 \varepsilon_r}}{c}$ (3.6), where l= the conductor length, and c= the velocity of light. The other component, the rise time t_{rise}, is roughly given by the product RC and its value can thus be approximated using previous eqn. (3.2). **Hence, one should minimize *l*, *C* and *R* for high digital performance at high frequencies**. However, it must be highlighted that the voltage/supply rails have an **opposite character:** they *benefit* from a very **high *C*** to keep the supply rails free from sudden surges and switching noise, while reducing the A.C. impedance of the grounding system.

Such ***conflicting requirements can be addressed in 2 ways:***

1) Use 2 discrete capacitors next to each active component: one ↓ the A.C. impedance for the RF signal, the other serves as charge storage;

2) Employ an integrated capacitance in the substrate itself.

As will be seen later, *MCM-C layers have capacitance 2...3x*

larger and thus are very suited for the latter method. The **MCM-D support high speed and high density for signal distribution**.

The data processing rate of any complex system (MCM) is heavily influenced by its architecture and techniques, e.g. | | processing. Another measure of performance is the number of millions of instructions per second (MIPS): $Nr.\ of\ MIPS = \frac{10^3}{(cycle\ time)\times(cycles\ per\ instruction)}$ (3.7).

The larger the number of MIPS, the shorter the cycle time and the fewer the number of cycles per instruction must be. However, *for scientific computations that are carried out on vector machines, MIPS is not the most useful measure of performance*. A vector is a collection of N variables, and a single instruction in a vector machine can initiate thousands of floating-point arithmetic operations. *A more appropriate measure is then the **nr. of millions of floating-point logic operations per second (MFLOPS) or megaflops***. Faster machines perform at gigaflops (GFLOPS) and top state-of-the-art computers now approach the teraflops regime.

Yield & Reliability

The overall yield of a multichip assembly is directly related to components simply as $Y = \prod_i y_i$ (3.8), where y_i is the yield of each component.

In assemblies with *N* identical components, module yield is <u>at best</u> y^N. ***Hence, the number of components and the degree to which their yield can be controlled drive the overall yield of MCM assemblies***.

This problem is referred to ***as the known good die (KGD) problem*, and it has often been regarded as a fundamental barrier to the success of MCM approaches**.

Substrate yield is another factor. It is *a function of surface area and the number of layers*. A simple model for the combination of these factors can be postulated as: $Y = \left(\prod_i y_{chip,i} \right) \cdot \left(\prod_j y_{layer,j} \right)^A$ (3.9),

where $y_{chip,i}$ is the yield of a particular component; $y_{layer,j}$ is the yield of a

particular interconnection layer per unit area, and *A* is substrate area.

The yield of modules and substrates is not the only factor in assembly yield; ***even*** perfect ***substrates can suffer yield loss at later stages of assembly***. Fig.3.7 illustrates the yield of an MCM as a function of the number and quality of the ICs used in the module. Even with high-quality chips, or those with a high probability of known good die (KGD) greater than 95%, ***the overall yield can be extremely low for modules containing a large number of chips***. Moreover, the curves were deduced assuming that there are no defects or errors in the substrate and the assembly processes. *The inclusion of such factors would further detract from the yield*.

This makes it necessary, even with strong provisioning for testability, to *introduce schemes for redundancy/defect tolerance/repair*. Thus, ***repairs become critical in large modules containing complex, expensive chips***. Fig.3.8 shows the drastic improvement in yield as a function of the KGD probability & the nr. of repairs for a multi-chip MCM. Notice the positive & significant influence of repairs.

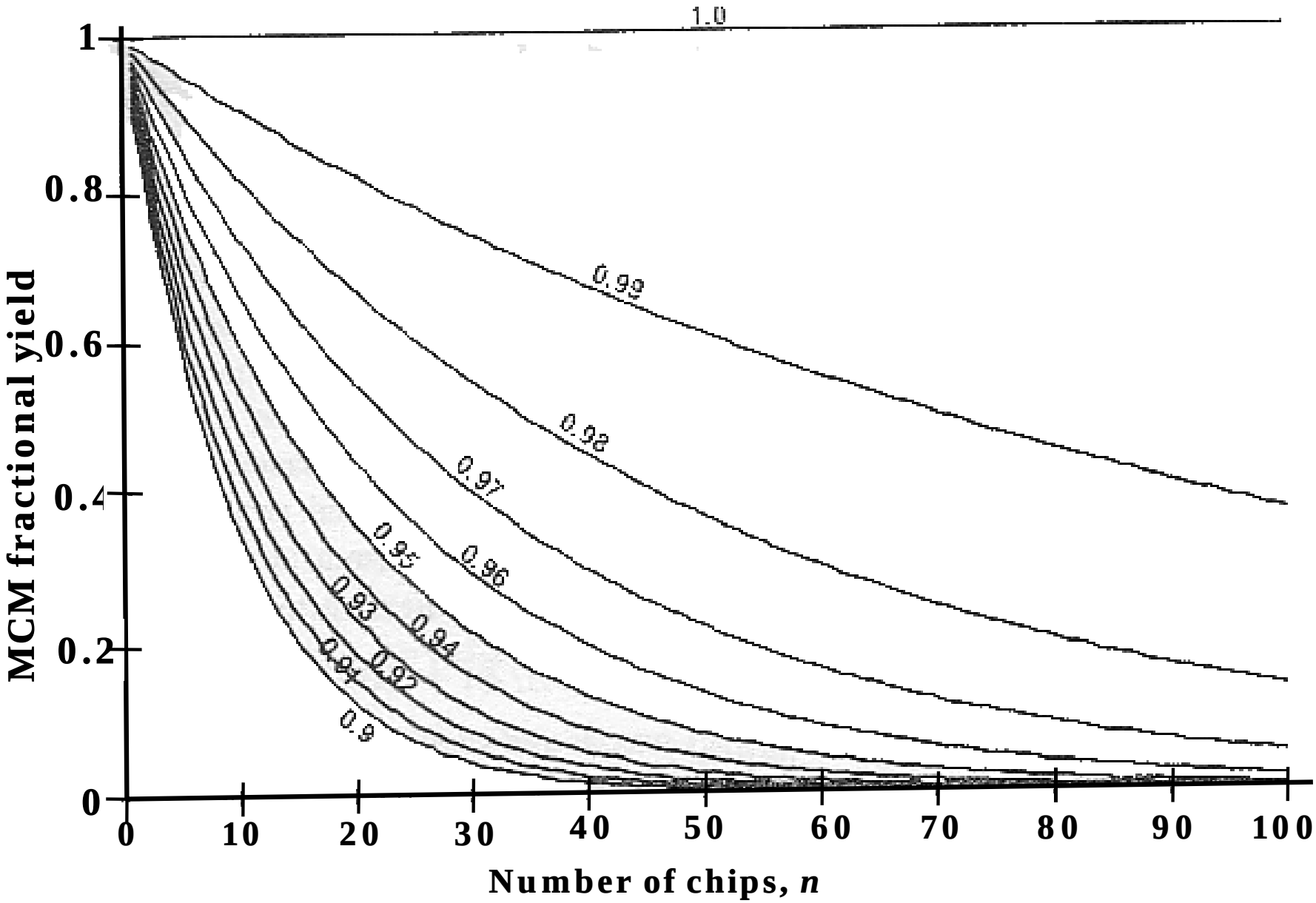


Fig.3.7: MCM fractional yield as a function of the number of chips in the module, for various known good die (KGD) probabilities.

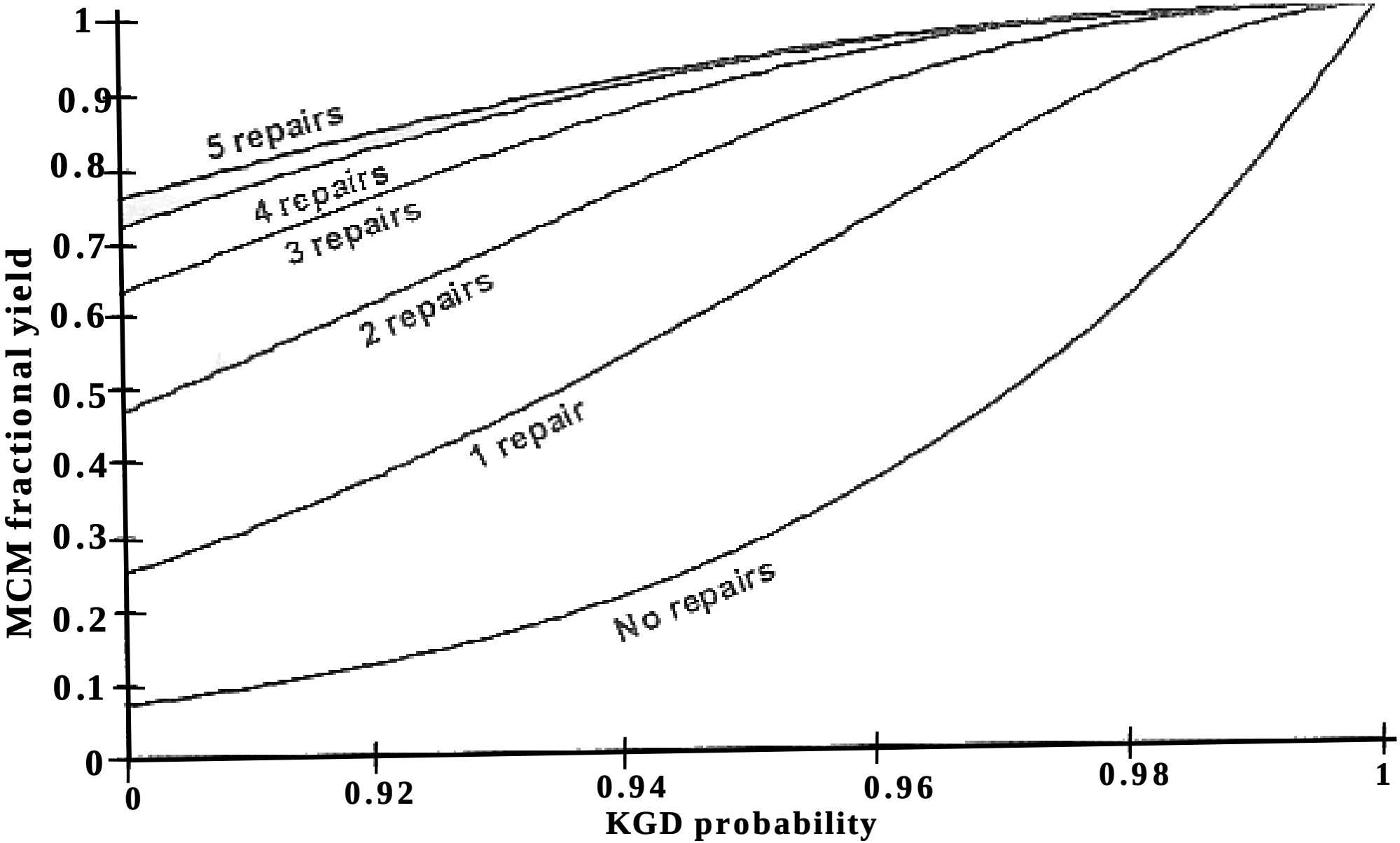


Fig.3.8: MCM fractional yield as a function of the known good die (KGD) probability, for a 25-chip MCM without/with repairs ranges from 0 to 5.

However, ***repair can introduce a tremendous penalty in terms of physical overhead***. Moreover, ***repairability*** in dense MCMs usually requires ***separability*** (the ability to release parts of a tightly fused assembly), which drives contradictory goals. It may be necessary to add margins far in excess of 100% to achieve the level of serviceability required for effective repair.

Reliability *is an essential element, determined by and also determining all MCM design, fabrication, and testing processes*.

Inherently, the MCM packaging operation must be more reliable than the individual ICs that it uses. Such packaging reliability must be designed and built into the product by addressing 3 different key areas:

1) Design for reliability with a minimum number of connections;

2) Construct the module using **6-σ** manufacturing processes;

3) Perform accelerated & other screening tests on the MCM to remove defect-induced failures before the product is shipped.

The *cost* of MCM substrates per unit area is higher because they use the finest feature sizes and other demanding technologies (thin film; multilayer, etc.). However, ***the final cost at system level***, at least theoretically, **should be lower than the alternative single chip package implementation**. This is due to ↓ the number of interconnects and minimizing the actual substrate area & system volume, all facilitated by the very technologies mentioned above.

In quantity, the cost of MCM substrates should be comparable to other substrates supporting single chip packaging because the overall board size (area) required is much, much smaller. *Large area & batch processing can help lower MCM substrate costs*.

3.3- MCMs at system level

The *typical MCM is a subsystem/system which requires multiple adequate engineering solutions for the following design & fabrication aspects:*

1) **Multilevels of the packaging hierarchy**
2) **Electrical design**
3) **Chip-level interconnect**
4) **Module or package-level interconnect**
5) **Heat removal $\Rightarrow$ v. important at chip level**
6) **MCM substrate technologies**
7) **Electrical testing**
8) **MCM wiring and connectivity**
9) **Repair, rework, and change integration**
10) **Module sealing and encapsulation**.

We shall briefly address each of these issues, in the following sub-sections.

Electrical design

The *major electrical design requirement* for MCMs is to *control basic circuit parameters such as resistance, capacitance, and inductance* ⇒ **short signal paths with controlled impedances and low loss**. As the frequency of MCM operation goes up, the need for controlled impedance signal paths becomes increasingly important.

Important ***aspects to be considered***:

- ***Choice of insulating & metallization materials*** *(determine ε & ρ)*

- ***Signal line geometries*** *(interline spacings & distribution and location of power and ground)*.

Sealing & Encapsulation

Hermetic sealing (in ceramic or metal packages) or encapsulation of the MCM is extremely important and can be a major contributor to overall module reliability. *Today, even effective polymer sealing can be*

achieved, provided the polymer coat remains in intimate contact with substrate and chip surfaces, thus preventing liquid water accumulation and subsequent corrosion.

In high-performance, high-value MCMs**, where the module must be repaired rather than discarded, **the encapsulants must be reworkable, i.e. easy to remove, to allow replacement of the malfunctioning chip(s), followed by recoating or re-encapsulation.

Thermal design

As was taught in an earlier part of this course, **heat removal is vital for efficient and reliable operation**. MCM module power dissipations can be up to ~180 W, **but *T* must always be <100°C**.

The actual thermal transfer depends on how the chips are interconnected to the substrate. The heat dissipation for the three most common chip-to-substrate interconnection -wirebonding, flip chip, and tape automated bonding (TAB)- is illustrated in Fig.3.9. *In wirebonding*

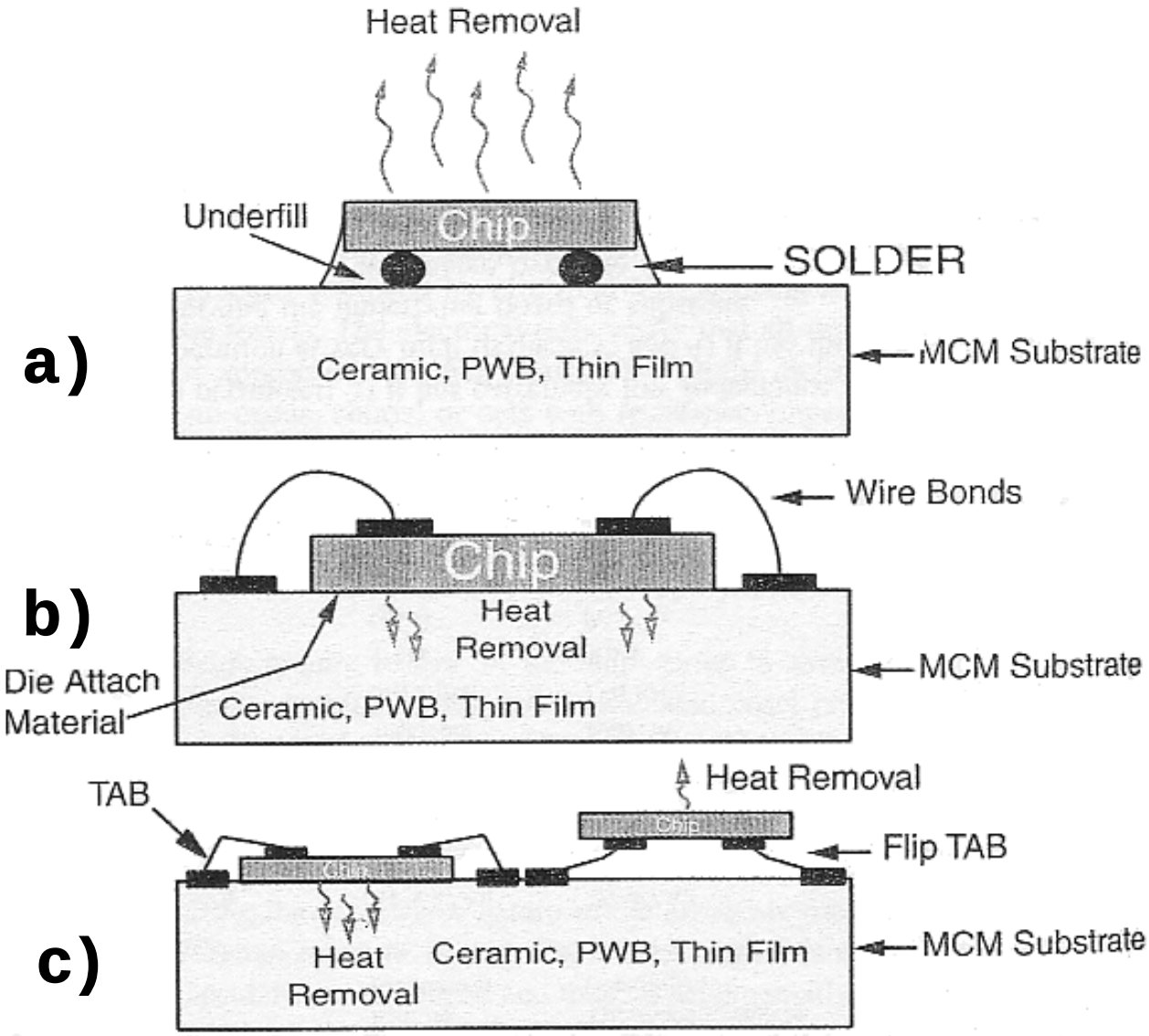


Fig.3.9: Heat dissipation in the 3 main chip interconnection to a MCM substrate: a) Flip-chip; b) Wirebonding; c) TAB.

and standard TAB configurations the heat removal path is directly through the chip's back surface and into the substrate (hence its thermal conductivity is of great importance). *In flip chip and flip TAB, the solder balls or flip TAB leads provide the only substrate contact.*

In the facedown mode, *heat can be easily removed using a metal heat sink* (Al or Cu), ***or cold***

fingers placed ***in contact with the back surface*** and (typically) liquid cooled. *In this case, the removal of heat can be very efficient, handling thermal power densities of up to 100 W/cm^2*.

Electrical Interconnections

Regardless of the interconnection type, the *basic requirements for the interconnect are:*

- *Fatigue and creep resistance*
- *Corrosion resistance*
- *Electromigration resistance*
- *High conductivity*
- *Processing temperature consistent with down-stream heating environments*.

Each interconnection methods has its advantages and disadvantages.

Wirebonding *is the* **dominant form of 1st-level interconnect** because of *its flexibility, low cost, relatively low*

capitalization cost, and ease of use.

Wirebonding is likely to remain the dominant method in the near future ***for all applications that*** *meet the following requirements:*

- *Afford the size perimeter extension for the 2nd bond,*
- *Have a large enough pitch to allow wirebonding, and*
- *Operate at low frequency (<10 GHz).*

Flip chip and TAB have much higher *cost since they require major tooling and capital investment to both produce the bumps and the pre-patterned tape, respectively, and -if necessary- to implement any changes in chip pad geometry*. However, **TAB has one** advantage: the IC is attached to its final lead frame, or inner lead bonding, prior to placement in the package or on the substrate ⇒ ***it can be tested both at speed and temperature in a configuration that is close to its final state, thus, in principle, solving the KGD problem***.

Nevertheless, ***if requirements exceed those listed above for wirebonding, then flip chip is the 2nd interconnect choice*** and its usage is ↑

rapidly worldwide. This is because *flip chip* also has 4 major advantages:

1) The highest number of interconnects per unit area;

2) All the interconnects are contained within the chip area, i.e., there is no *2nd bond or outer lead bond location beyond the chip perimeter*;

3) Extremely low ***Z*** *&* ***C*** *per joint* $\Rightarrow$ operation at very high f; and

4) It has the most robust replacement process for preserving the underlying board or substrate.

MCM connections to system-level boards

Large I/O numbers can only be accomplished with an area array type MCM interconnect, e.g. using pin grid arrays, pad grid arrays, and, more recently, ball grid arrays (BGAs). Hence, the substrate must provide this type of board-level interconnect.

Repair & rework

As was shown in the previous section, the overall yield for large MCMs is low, even if the individual chips have a high KGD probability.

Consequently, *either **MCMs** must be built so inexpensively that they can be discarded, as is usually done with single chip packages*, or they ***must be able to be repaired or reworked***. Additionally, the modules are typically very complex and, they may still need engineering changes before their fabrication is fully completed. *Repair & engineering changes are most often directed at the substrate and its structure*.

Rework generally refers to the need to remove bad chips and replace them with good ones. ***This is done by identifying the bad chips and selectively removing them by a combination of heat & mechanical means***.

Another *example of rework* is related to the necessity of combining the previous two elements (interconnections and the realization of an overlayed system) in complex MCMs. In this case, a complicated overlay pattern, with accurate component alignment is necessary. However, misalignments can occur, either at die placement or after curing, due to the drift in material properties. Such misalignments would compromise the

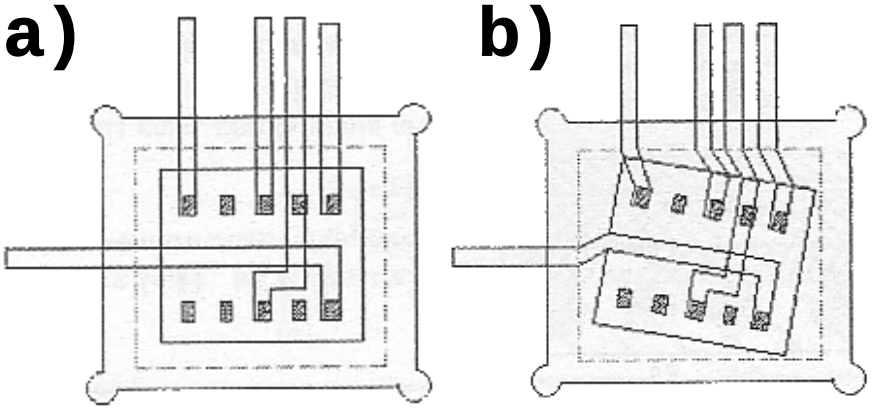


Fig.3.10: Example of 'rework' for dynamic redesign of product manufacturing in order to increase the yield: a) The initial planned/desired alignment and subsequent interconnect pattern to be realized; b) Misaligned die and corrected interconnect by adaptive lithography generated at run time.

functionality of the MCM if the typical fixed patterning is applied. Instead, if the misalignment is detected in due time, rework can be done not by disassembling the processed product but rather by dynamically changing the subsequent steps, in this case using an ***adaptive lithography*** to realize the final conductor patterns (e.g. using direct-write lithography instead of mask-based one). Fig.3.10 exemplifies such a case.

Electrical Testing

Electrical testing is done at several different levels for MCMs:

0a) Ensure that the substrates are defect-free before the assembly process => by design rule checks (DRC), to ensure compatibility with MCM fabrication process, followed by electrical testing;

0b) Testing of the chips prior to assembly;

0c) Visual inspection and destructive physical analysis (DPA) on a lot sample basis;

1) Post-assembly electrical testing of the assembled MCM to ensure a working module, thus validating the defect-free nature of the assembly process and certifying the results of chip (KGD) and substrate testing.

Additionally, testing must also find the defective chips on non-working products. This is a key element necessary for the repair process.

3.4- Types of MCM substrates/processes

As was already mentioned in the previous section, there are ***3 main types of MCMs***:

- ***MCM-L****s, based on organic laminate technology;*
- ***MCM-C****s, thick-film or cofired ceramic technology; and*
- ***MCM-D****s, deposited thin-film multilayers*.

Each type of MCM has its own features and importance.

3.4.1- MCM-L

MCM-L is ***derived from conventional PWB technology***, but ***differs*** *from as it makes use of the following processes:*

i) Photolithography (to fabricate small feature sizes) ***and accurate placement of components***;

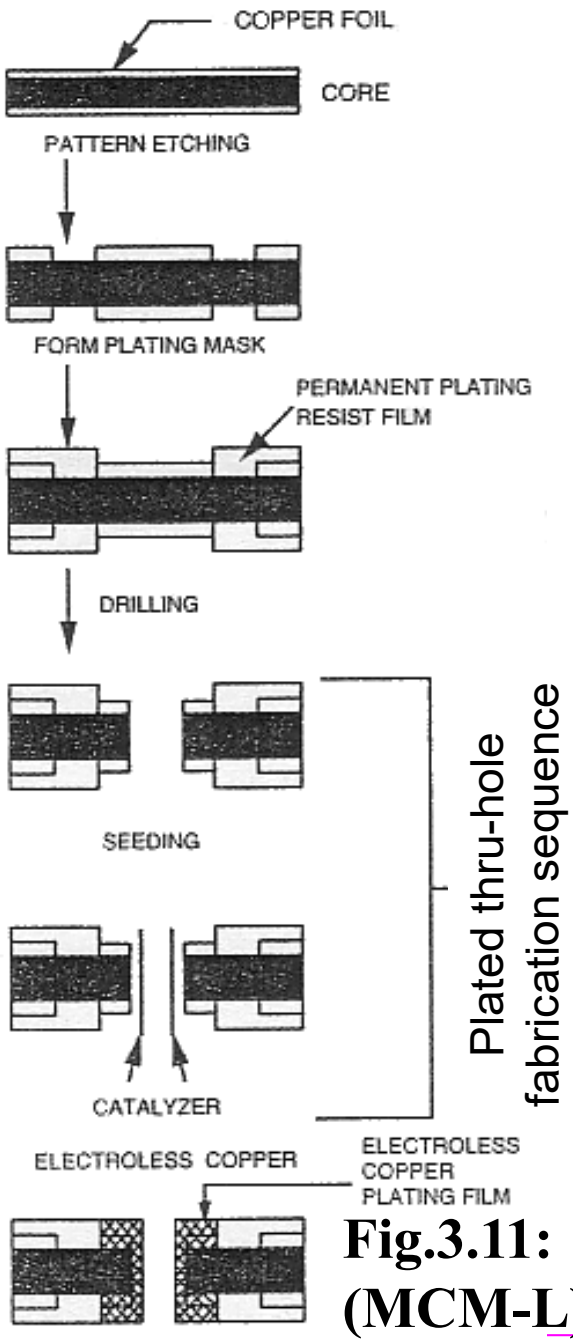
ii) Surface mount technology (SMT), with bare dies interconnected with wirebonds or flip chip processes, instead of standard packaged-part soldering.

MCM-L is similar to what once was called hybrid microelectronics with ***two notable exceptions***:

1) The **substrate is a laminated organic material** rather than ceramic or silicon, and

2) **The module package need not be hermetically sealed.**

MCM-L provides the lowest density of the three major MCM technologies and is usually the least expensive to implement. MCM-L is also known as chip-on-board (COB).



MCM-L technology uses Cu traces separated by fiber glass-reinforced organic laminates (the most common), with plated through-holes or vias interconnecting the layers. A typical ***fabrication sequence*** is shown in Fig.3.11. *Compared with conventional PWBs,* ***it boasts:***

a) Smaller feature size;

b) Allows the incorporation of vias that extend only partly through the board (blind vias) as well as those that connect between layers entirely within the board (buried vias). The use of both types of vias greatly ↑ wiring density of components that can be connected on the board.

There are **3 types of laminated (MCM-L) substrates: *rigid, flex,*** and ***rigid-flex***.

Fig.3.11: Schematic representation of a standard printed wiring board (MCM-L) fabrication sequence.

Rigid MCM-L substrates *are typically made of epoxy-based polymer resin dielectrics, reinforced with fiberglass*. Other reinforcing materials include quartz, Kevlar, polyimide, or Teflon. ***Polyimide*** *provides excellent stability and a low* ε_r*, thus assuring excellent signal propagation and high frequency performance*.

Two types of dielectric layers are used in a typical MCM-L: **cores** *and* **prepregs**. *The* ***core material*** *is delivered from the manufacturer fully cured and usually clad with Cu on both sides*. *The as-received prepreg material is* **partially cured** *and is used as a* ***bonding agent*** between core layers. ***Problem of these dielectrics:*** *CTE mismatch with ICs*.

Both the cores and prepregs are typically fiber reinforced. *If the* **dielectric layers** *have* ***no reinforcing fibers****, the resulting laminate in thin layers is quite flexible, leading to the name flexible or* ***flex circuits***. Combining both types of laminates into a single board structure yields an MCM-L substrate called **rigid-flex**.

There are ***5 basic process steps*** *in the manufacture of MCM-L substrates:*

1) Select the appropriate core and prepreg layers *to meet the electrical and mechanical performance criteria.*

2) Photolithographic patterning and etching of the Cu conductors *on the core layers.*

3) Drilling of vias *(blind, buried, or full through-holes).*

4) Lamination of the cores *to each other using the prepreg layers.* Multiple laminations are usually required to form blind and buried vias. If the board only has plated through-holes, then a single lamination step is usually possible with post-lamination via drilling.

5) Plating of drilled holes *in single layers* (buried vias), *partially through several laminated layers* (blind vias), *and holes going all the way through the board* (plated through-holes as used in PWBs).

Three **key operations** are ***vital for the optimal realization & functionality of MCM-L***: *Inner layer processing, Via formation & Surface layer finishing*.

The treatment of Cu surface layers defines a major difference between PWBs and MCM-Ls. Conventional PWBs are made for surface mounting or the through-hole soldering of leaded packaged components. The surface pads are typically solder plated with PbSn solder, which is suitable for mass surface mount reflow or the wave soldering of through-hole devices. MCM-L substrates potentially require the selective plating of several metals, including Au for wirebonding, PbSn solder for chip components & TAB leads, and hard wear-resistant Au for edge connectors.

The board can be populated only with ICs, or with both active and passive components, and even with other MCMs in some complex cases. Once populated, the MCM-L uses organic coatings (glob top) *to protect the chips and their bonds as well as the components and the entire board*.

Advanced MCM-L substrates: The **major limitation** of standard MCM-L is the ***lack of wiring density required to meet the routing and I/O requirements***. This is mainly due to the need for the plated through-hole vias produced by mechanical drilling. In a typical PWB, the

drilled holes are relatively large (nominally 12-15 mils = 300-475 μm) with large cover pads. Moreover, the cost of hole drilling ↑ quasi-exponentially as the size of the via ↓.

The loss of this much wiring density cannot be tolerated for high performance applications. ***The solution*** *is a new and emerging innovative technology, called* ***surface laminar circuits (SLC)****, which can provide high wiring density at low cost*. **SLC** is very simple in concept, the basis of which is to ***use low-cost materials such as epoxy, or polyimide, and Cu metallization,*** which are already used in both conventional PWB and MCM-D construction, ***but apply them together as thin films over large board areas***. The concept is shown in Fig.3.12 for a ball grid array (BGA) with a hybrid or built-up substrate.

It can be seen that the built-up **SLC has a two-part structure**:

a) A Cu-clad epoxy-glass (FR-4) carrier substrate with plated & plugged through-holes;

b) Alternating layers of photo-imageable dielectric coating (epoxy

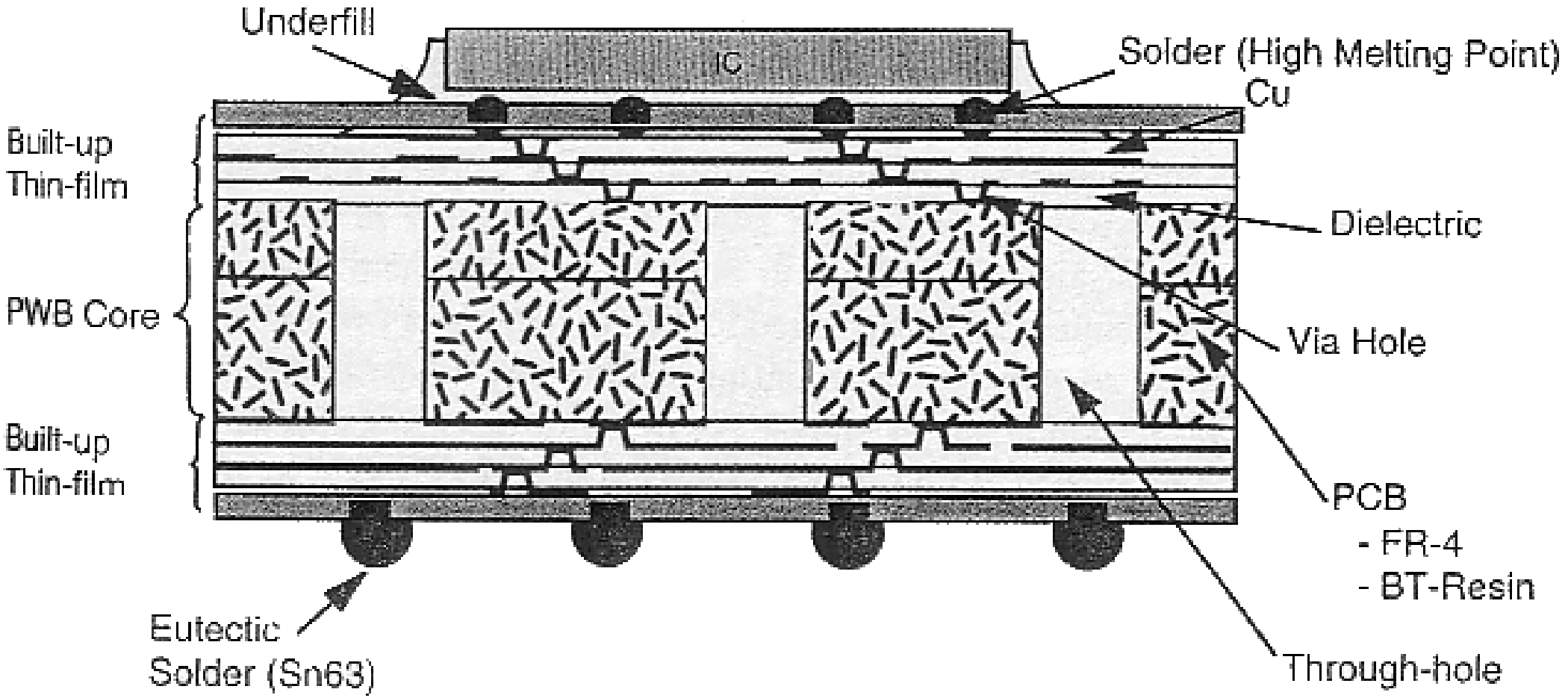


Fig.3.12: Schematic representation of a SLC type of MCM-L.

or polyimide) & Cu (deposition or plated) thin films. Interconnection between wiring planes is done by via holes produced in the photo-imageable dielectric layer by UV exposure and subsequent developing.

Key advantages of the SLC type of MCM-L technology:

1) Greater wiring density due to elimination of drilled through-holes (except in the core);

2) Capability to support very high device I/O densities;

3) More flexible design options for EMI shielding than with MCM-D technology alone;

4) Usage flexibility for any conventional interconnect technology (wirebonding, TAB, and flip-chip);

5) Easily up-scalable (more layers and/or cores could be stacked).

3.4.2- MCM-C

MCM-C is similar to, and evolved from, the ***older ceramic thick-film hybrid circuits***, *in which* ***multilayer circuitry is*** **screen printed** *onto a rigid ceramic substrate (Al_2O_3 ; $\varepsilon_r > 9$). Printed layers alternate between metal traces and dielectrics, with metal-filled "vias" to interconnect layers*.

A true MCM has only bare ICs and, perhaps, some passive chip components or occasional specialized packaged parts on its surface. The packaging density –as was shown by eqn. (3.1)– is proportional to the fraction of the substrate area occupied by ICs, but is limited by via size and alignment difficulties when screen-printing several layers, which become less planar as the number of layers increases.

The MCM-C substrates appeared in response to the need for increased packaging density and enhanced performance. ***Density was increased by shrinking the size of features, such as the vias used***.

In the *thick-film process, the dielectric layers are screen-printed and subsequent layers are built on top of the previous one(s) like a stack of bricks. Screen-printing can produce minimal feature*

alternate and ***more advanced ceramic processing method is called*** **cofired technology**. ***The main difference*** between conventional thick-film and cofired ceramic processes ***is the nature of the dielectric***.

The basic **cofired ceramic process steps** are:

0) The dielectric layers are sheets of unfired ceramic, called green state ceramic, or *green tape* if the layers are tape cast.

1) Each sheet is separately patterned with its metal conductor traces;

2) Vias (200 μm or smaller) are mechanically punched or laser machined into each individual unfired ceramic layer, then filled with conducting paste.

3) Each conductor layer is printed on its own slice of **unfired** ***ceramic***

⇒ 2 benefits: ***a)*** ↓ **in line and space sizes;**

b) **Significantly smoother surface than thick-film ceramic**

⇒ the screen emulsion seals it during the printing ⇒ pattern integrity.

4) Collate, stack & align together all sheets, like pages a book, before

laminating all of them together.

5) Finally, the entire stack is being fired, usually in 2 steps:

5.a) Pre-fire @ ~800°C: to remove organic binders;

5.b) Fire (@ higher temeprature).

Since all of the circuit features are now created on unfired ceramic, they undergo identical shrinkage of about 15-20% when fired, that is, **all the layers are fired at once**, hence the name "cofired" for this technology.

Two types of such technologies can be distinguished: A) High temperature, and B) Low temperature cofired ceramic (HTCC & LTCC).

Features of the **HTCC technology**:

A.1) T= 1400...1600°C;

A.2) Utilizes primarily **alumina with small amounts of glass and various organic components as green sheet** ceramic layers;

A.3) Because of the high temperatures, the **conductors must be realized using refractory metals (W, Mo)** mixed with alumina and small amounts of glass (4-11%) $\Rightarrow$ high ρ.

Features of the **LTCC technology**:

B.1) Utilizes ceramic layers containing ***large amounts of glass***. ***Incorporating glass within the ceramic*** has further crucial beneficial effects ⇒

B.2) T= 800…1000°C

B.3) Lowers ε_r = about half that of alumina ⇒ *improved performance at high frequencies*,

B.4) CTE v. close to that of Si & GaAs

B.4) Higher conductivity metals can be used (Cu & Au); however

B.5) Thermal conductivity significantly ↓ when compared to that of an HTCC module.

Additionally, other *points of concern are:*

C.1) The individual unfired ceramic layers are flexible and can be cut or torn, but unlike paper, they are somewhat brittle and can fracture if the stresses are too great ⇒ ***care must be taken in the layout for placing vias and limiting the total area of opening***

(max.40% of total area);

C2) Balanced distribution of metal-covered areas in the layout, is important for two reasons:

i) The metal shrinks at a different rate than the ceramic during/after firing (CTE difference);

ii) The mechanical strength of the fired metal is lower than that of the fired ceramic.

To ensure uniform shrinkage and mechanical integrity, the design should strive to maintain the same cross-sectional metal content across the substrate. Individual layers can be "unbalanced" as long as the sum of all the layers provides a reasonably overall even distribution of metal. Taking appropriate care, ceramic cofired technology substrates can be made with as many as 100 layers, each with 70- to 90-µm vias.

The introduction of photo-printable thick-film pastes enables to further ↓ feature size down to **75 µm** and eliminate screen patterning. In this process, the

conductor and dielectric pastes are photosensitive. They are applied to the entire substrate and after drying, are exposed through a photomask to UV light and subsequently processed like in any photolitho method.

3.4.3- MCM-D

In MCM-Ds, **both the metal and dielectric layers are sequentially deposited as thin-films, and patterned photolithographically**. ***Features:***

i) Yields the highest circuit density (feature size can be <10 μm, which which is an order of magnitude smaller than either MCM-L or non-photodelineated MCM-C);

ii) The most process-intensive and expensive MCM technology *(Fabrication process similar to that used in the manufacture of ICs, employing thin film deposition and patterning all features photolithographically)*. Although MCM-Ds tend to be expensive per unit area, they typically use much less area for a given circuit and thus can

cost competitive, especially in large volumes.

The substrate base layer or carrier must be very smooth and flat. Silicon wafers are mostly used, *because they are readily available, very smooth and flat, and relatively low cost, and, more importantly, they match the CTE of various layers and of other chips*. ***This Si base is merely a platform; no devices are realized in it, as opposed to ICs***. In the future, however, active & passive components, will be integrated into this base.

Materials used:

- Dielectrics: Spin-coated **polymers** (polyimide, BCB) and **CVD** silicon oxides, nitrides or oxynitrides.

- Metals: usually sputterred **Cu, Al, or Au**.

Spin-coating of polyimide is done in several steps. Initially, an aminosilane solution is spun onto the surface and baked to provide a monolayer that increases the adhesion of the polyamic acid precursor. Then, to ensure a defect-free dielectric layer and to ↑ the degree of planarization,

a second coat of polyamic acid precursor is applied and soft-baked. The complete curing process entails further heating up to a peak temperature of 350-400ºC, which provides enough thermal energy to crosslink the polymer and form a true polyimide. The vias are formed by RIE in an O_2 plasma using a patterned metal mask.

The ***weakest link*** in the MCM-D substrate fabrication process is ***forming the dielectric***. This is because it is ***difficult to create*** *large planes of defect-free polymer films, especially* ***pinhole-free ones***. *Consequently, a* ***major concern*** *in a substrate design is the* ***amount of crossover area*** **= the area created whenever the metal on top of a given dielectric layer crosses over any metal below it**.

Progress in MCM-D technology will not likely focus on further shrinking of feature sizes to ↑ packaging density, but rather on ↓ the relatively high cost by ↑ yield.

As a special case, it is worth highlighting the General Electric (GE)

high-density interconnect (HDI) process as an unusual representative of the MCM-D class (about HDI, see again Section 2.2.3 and Fig.2.10). The typical process flow is illustrated in Fig.3.13. *The process integrates ICs and other components face up into the* ***recesses*** *of a planarizing mechanical substrate (Fig.3.13-a) made of ceramic, glass, metal, or plastic. The recesses are, in this case, preformed and must be accurate within ~10* ***μm*** *so that all components, after placement (die attach), create a nominally planar assembly (Fig.3.13-b). The MCM-D interconnect system is created after this step. It is initiated by laminating a glue-clad Kapton sheet (Fig.3.13-c), that had initially been cured, laser drilled to form vias, and then metallized. The metal (Ti-Cu-Ti) is then patterned and etched to form a patterned single layer. The lamination, drilling, metallization, patterning, and etch steps are repeated as required to create a finished, interconnected substrate (Fig.3.13-d).*

Formation of a patterned overlay system is complicated by many factors. One important factor is component alignment, which can change

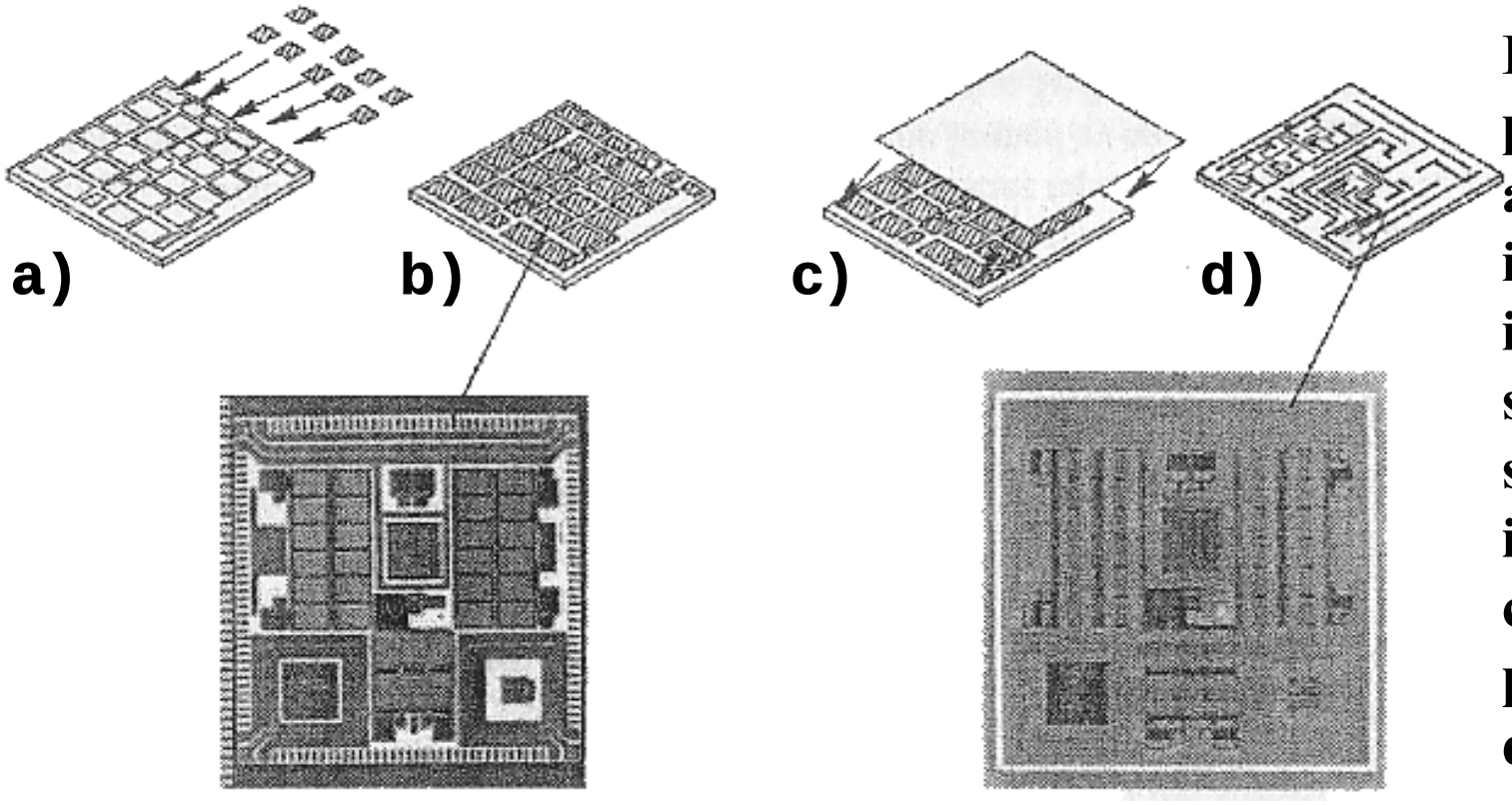


Fig.3.13: Simplified HDI process flow: a) Introduce components into recesses embossed into the mechanical substrate; b) Planar substrate with integrated components, c) Formation of patterned overlay, and d) Completed HDI substrate.

even after placement due to drift in the curing steps associated with die attach. To combat this problem, GE's HDI process employed a novel solution, the adaptive lithography system that was mentioned earlier.

Consequently, we can summarize in the following Table 3.1 the main features of all types of MCM implementations:

Technology	Advantages	Disadvantages
MCM-D	- Highest density - Lowest ε_r (2.5…4) - Very good CTE matching (2…3×10^{-6} /°C) - Low dielectric dissipation factor* (~0.2…0.6% for organic diel.on Si)	- High cost - Limited nr. of layers - Complex processing - Difficulty in creating large areas of pinhole-free dielectric layers - **Highest dissipation factor (3…30%) for inorganic diel. on Si**
MCM-C	- Low dissipation factor (0.1…1%) - Reasonable CTE matching (3…7×10^{-6} /°C) - Max. nr. of layers - Robust	- **Highest ε_r (5…10)** - Medium cost - Medium density
MCM-L	- Low ε_r (3…5) - Lowest cost - Simplest processing - Robust	- **High dissipation factor** (~1…3%) - High CTE (>10^{-5} /°C) - **Lowest density**

Table 3.1: Quick comparison between the various types of MCMs

*= The ***dissipation factor DF*** **is defined as the ratio of a capacitor's equivalent series resistance (*R*) to its capacitive reactance (X_c)**:

$$DF = \frac{R}{X_C} \times 100 = \omega RC \times 100 \quad [\%] \qquad (3.10).$$

Since the loss in a capacitor can also be expressed using the **loss tangent** $\tan\delta = \frac{\sigma}{\omega\varepsilon}$, where $\varepsilon = \varepsilon_0\varepsilon_r$ is the permittivity and σ is the conductivity of the capacitor's dielectric material, and, after some simple calculations it can be quickly deduced that $DF = \frac{1}{\tan\delta}$ (3.11).

From Table 3.1 it can be seen that ***comparisons*** *between various MCM-based technologies or specific implementations are done comparing the values of the following parameters as judging criteria*:

- Dielectric constant ε_r of the substrate and its loss of tangent δ (or dissipation factor), e.g. at 1 MHz;
- CTE & thermal conductivity κ;
- Metals & metallization systems used for interconnections