EE6610- IC packaging

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3- Multichip & 3D packaging (continued)

3.5- Complex assembly structures and 3D systems

- 3.5.1- Substrate configurations
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3.6- MCM wiring design

3.5- Complex assembly structures and 3D systems

3.5.1- Substrate configurations

***The relationship of components to substrates in an MCM defines a* substrate arrangement *or* substrate configuration**. *A number of potential substrate configurations are shown in Fig.3.14*.

Substrates can be used in a manner **similar to PWBs**, in which *components are mounted onto the assembly. Such configurations are referred to as* ***patterned substrate approaches*** (Fig.3.14-a is a particular example illustrating distinct interconnecting and mechanical substrates).

A variation of this configuration, sometimes used for power devices, *is referred to* as the ***recessed patterned substrate*** and is shown in Fig.3.14-b. In this case, *access holes are formed through the interconnecting substrate*, resulting in *a more intimate substrate contact* and, therefore, *lower thermal resistance*.

A fundamentally different substrate configuration results when the

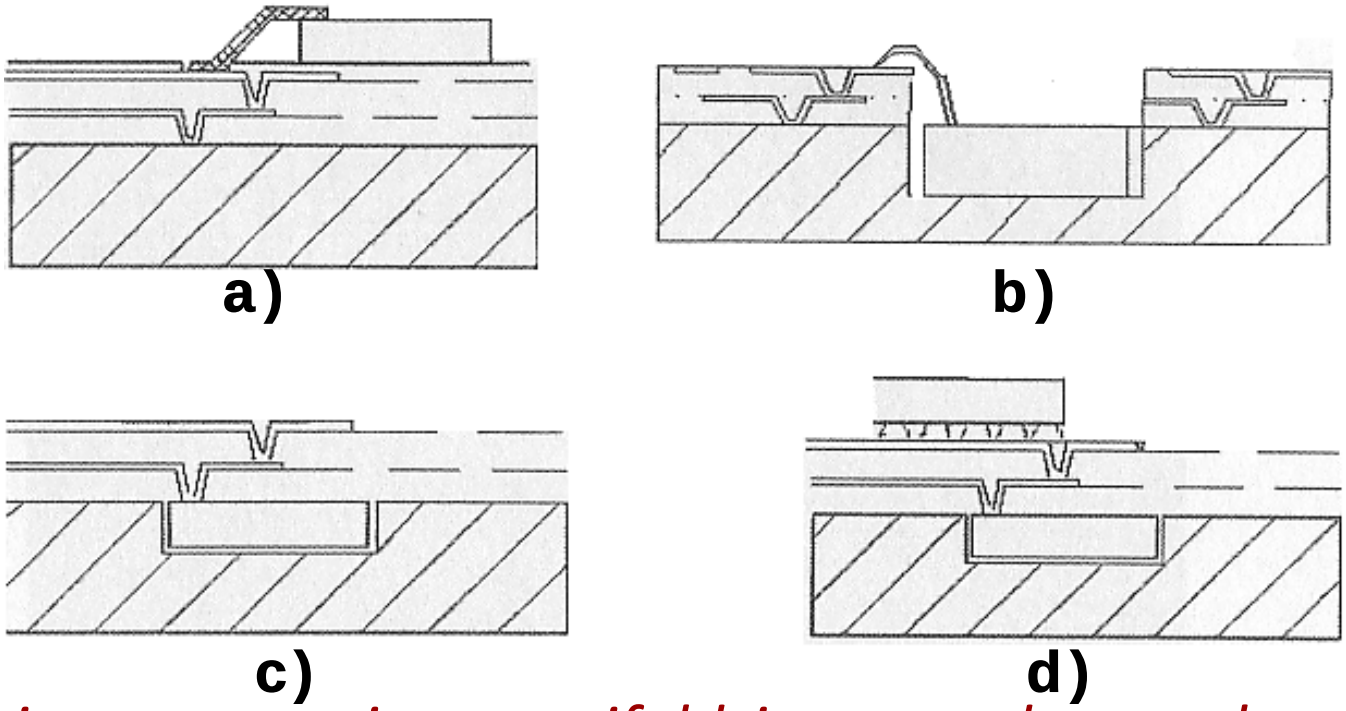


Fig.3.14: MCM substrate configurations:

a) Patterned substrate;
b) Recessed patterned substrate;
c) Patterned overlay;
d) Combination.

interconnection manifold is created over the substrate that contains the components, as shown in Fig.3.14-c. This approach *is referred to* **as patterned overlay**. In this case, components are recessed into a planarized substrate, which serves as a starting surface onto which multiple levels of interconnects are created.

The ***component-attach or element-attach approaches are defined as the explicit schemes for which components are mechanically and electrically attached to the substrate***. The relevant approaches which can

be used are: wirebonding, TAB & flip-TAB, flip-chip, patterned overlay and with conductive adhesives. The first ones were already presented in the previous lessons. We shall briefly present here only the last ones.

The patterned overlay *defines interconnects metallurgically joined to component bond pads as part of the intrinsic process used to form interconnects*. *Thus, both the substrate and the chip attachment approach are defined simultaneously*. Chip scale-packaging approaches employ a similar method, namely wafer-level packaging. ***One difference between wafer-level approaches and more generalized patterned overlay approaches is that the former is applied to entire wafers, as opposed to heterogeneous arrangements of individual components***.

The use of **conductive adhesives** permits **rapid attachment of components to substrates at low temperatures**. ***In conductive adhesives, conductive particles are loaded into a polymer matrix, which, upon curing, forms a conductive bridge***. *The technique is commonly applied in low-cost, low-performance*

applications. Recently, the technique has been used in much more complex assemblies, such as the attachment of grid array assemblies to substrates. At present, the *approach appears to be improving the capability to interconnect tight-pitch assemblies with high yield*, but it is presently still limited to applications at or above 0.5 mm center-to-center pitch.

3.5.2- Package body styles

A final package, however simple or complex, represents the transitional structures between the MCM and the board (or other higher level assembly) into which it integrates. The spatial efficiency in package body styles can impact on the effectiveness of MCM approaches if improved performance is desired. Fig.3.15 shows a few examples of package body styles. In Fig.3.15-a it can be seen that the substrates can be strategically engineered to provide component mounting surfaces on both sides for at least the MCM-C and MCM-L approaches. In general, integral package constructions (where the substrate and the package structures are

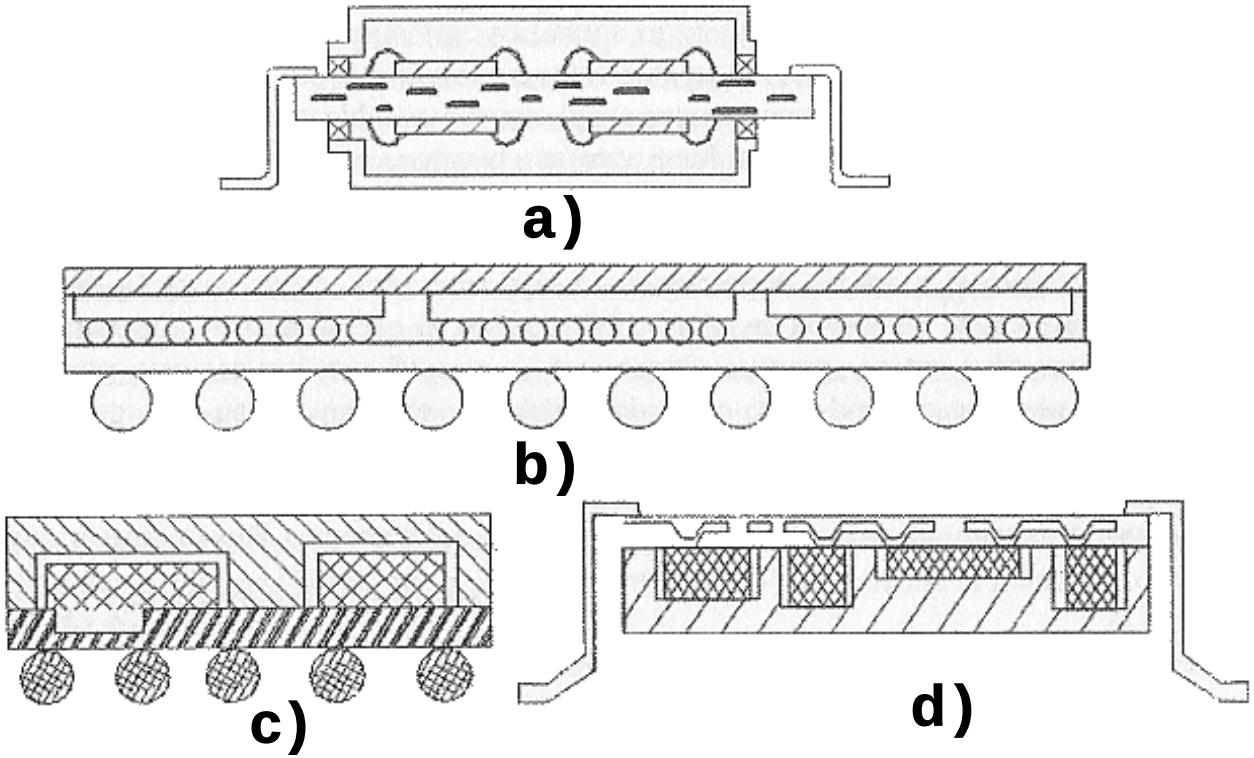


Fig.3.15: Examples of package body styles:

a) **Double-sided MCM-C quad-flat package;**
b) **Flip-chip patterned substrate BGA;**
c) **Patterned overlay BGA;**
d) **Patterned overlay quad-flat package .**

combined) are preferred. Fig.3.13-a achieves a higher component density by using both sides of a substrate for components and by employing an integral package construction. Both of these objectives are difficult to achieve in MCM-D approaches. Fig.3.15-b is just an extension of common BGA packages, while Fig.s. 3.15-c & -d show the extension of a patterned overlay structure for a BGA attachment, and for converting a patterned overlay MCM into an integral surface-mount package.

3.5.3- 3D systems

Planar MCM approaches are limited in that, even when chips are placed in a perfect tile (no gaps between any chip), *the highest density achievable is a single circuit layer*. Obviously, *3D integration and/or 3D packaging become necessary in order to further obtain significant improvement in density and to enable further* ***significant*** *increase in performance & functionality.* 3D integration of ICs is beyond the scope of this course. Here we shall focus only on 3D packaging.

3D packaging can be defined as ***any technology that stacks semiconductor elements on top of each other*** AND ***utilizes vertical interconnects between the elements***. 3D packaging enables to build up electronic systems with:

- Higher functionality
- Higher density of interchip interconnects
- Lower volume
- Lower high-volume manufacturing cost
- Lower electrical parasitics of interconnects

The 3D packaging approaches can be divided into **stacking** and **folding** approaches.

In stacking approaches, ***a number of planar elements are placed one on top of another***, *as in a stack of playing cards*. In this case, the word "element" can refer to:

1) Individual ICs,
2) MCM substrates, or
3) Packages containing ICs or MCMs.

A somewhat different classification highlights that 3D packaging can be obtained by:

- **Stacking of packaged dies** (package on package) (Fig. 3.16),
- **Stacking of dies, chip to chip** (3D-Packaging) (Fig. 3.17),
- **Wafer level 3D integration** (3D-WL), chip to wafer, wafer to wafer

Table 3.2 compares characteristic features of 3D-packaging (which is also illustrated schematically in Fig.3.18) with 3D-WL packaging.

In **folding approaches**, ***one can fold a planar assembly with a flexible substrate into a more compact shape***.

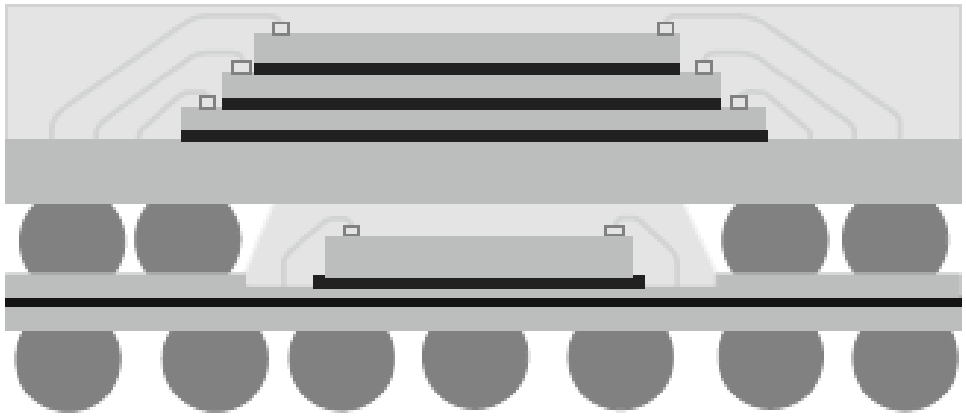
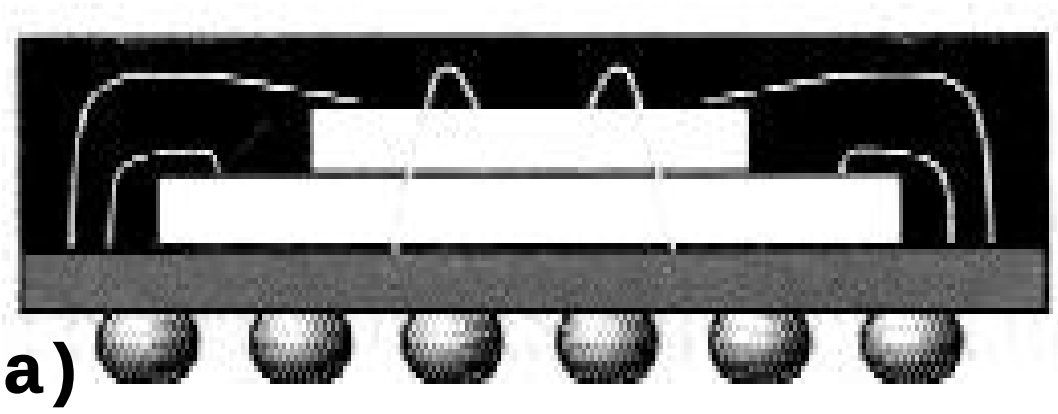
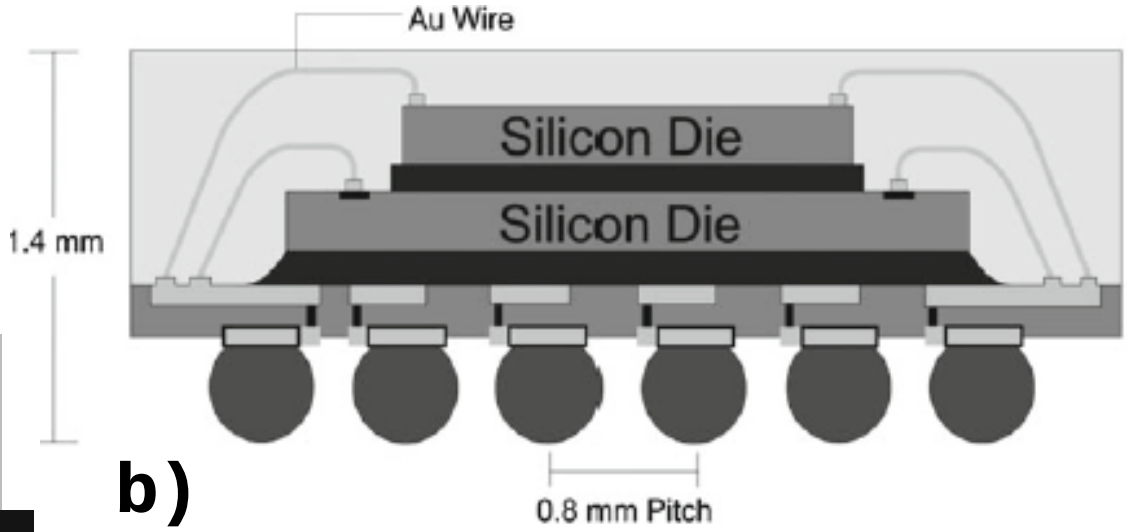


Fig.3.16: Package-on-package





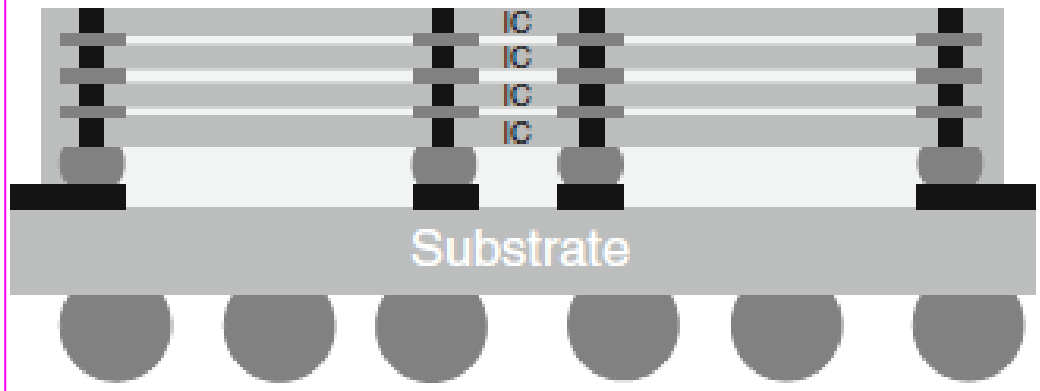


Fig.3.18: 3D-WL integration

Fig.3.17: Representation by different authors of the same type of structure, but under 2 different names: a) Stacked die packaging; b) 3D-packaging.

Technology	*3D packaging*	*3D-WL integration*
Infrastructure	Packaging, Bond wires,	Foundry
3D interconnect	Flip Chip (FC)	Through Si vias (TSVs)
Active layer thickness	>50 μm	<50 μm
I/O density (cm^{-2})	10^4–10^5	10^5–10^8

Table 3.2: Features of 3D integration/packaging.

Fig.3.19 illustrates how a 3D design stacks multiple ***tiers***, *composed of active* devices (transistors, etc.) and their respective interconnect layers, atop each other. Vertical connections of the various tiers are realized by so-called *inter-tier vias*, often realized as through-silicon vias (TSVs).

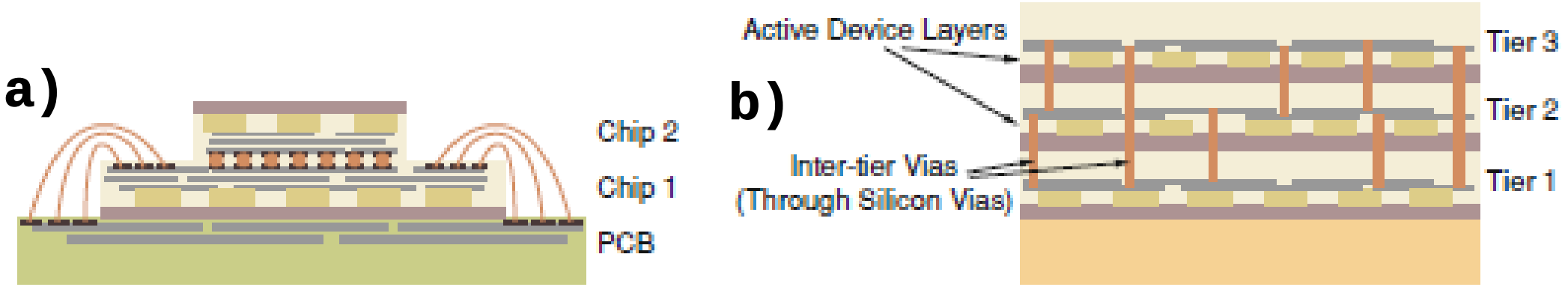


Fig.3.19: Schematics of 3D designs: a) 3D packages, and b) 3D ICs

Fig.3.19–a shows the stacking of various chips/die. **Such an arrangement is often called *3D package***. Fig.3.19–b shows **3D integration of multiple functional levels *on the same chip* and connected mainly using TSVs, and commonly referred to as** 3D **ICs.**

While 3D packages allow the vertical integration of various heterogeneous technologies, 3D integrated circuits enable denser circuits due to smaller distances between active devices in the third dimension.

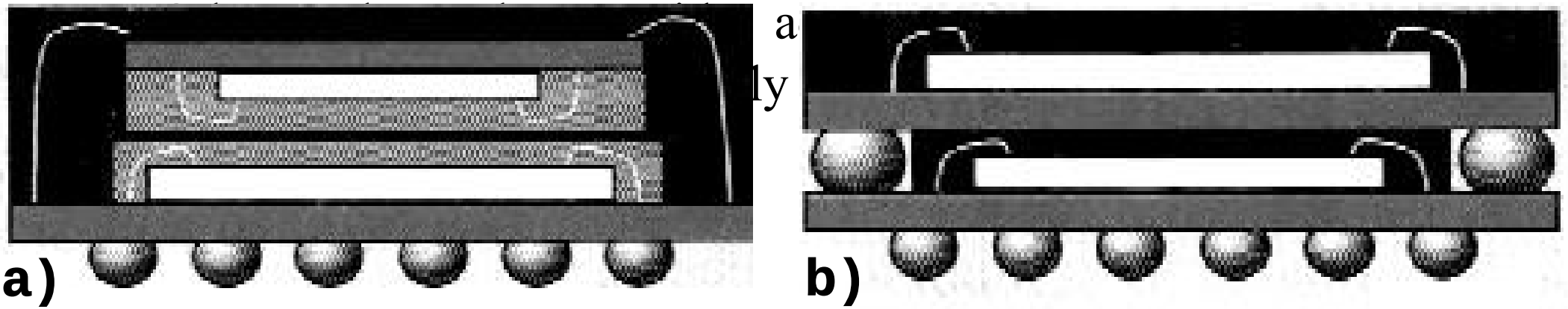


Fig.3.20: 3D IC Stacking Options: a) Package-in-Package (PIP) stacking; b) Package-On-Package (POP) stacking

Another 3-D approach is from Irvine Sensor called ***Neo-stack***™. The patented process features stacked layers each containing one or more devices and a flex (polyimide) film supported conductor interconnect. Fig.s 3.21-a and -b are schematic cross-sections of a single die layer and a multi-die layer respectively. Note that all circuitry terminates at the edges of the flex film. The individual layers following stacking (lamination) are accessed by way of a vertical interconnect. ***Neo-stack***™ uses only fully tested die to enhance yields and thus avoids the need for any rework.

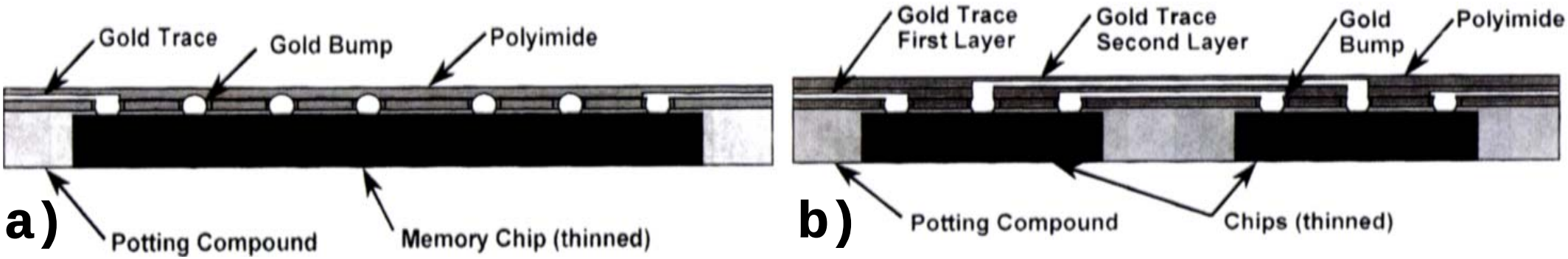


Fig.3.21: a) Single Chip *Neo-Stack*™ inner layer; b) Multichip Inner Layer.

Challenges & disadvantages of 3D integration/packaging:

A) The high density of consumed power can offset the advantages of this technology due to the degradation of performance and reliability. It is obvious that the thermal management will become more challenging if many 2D chips are integrated by 3D stacking.

In particular *the heat transfer is becoming a limiting factor due to the low thermal conductivities of the dielectric layers between the dies.*

B) A 2nd limiting factor arises from the yield of untested dies combined in a 3D-WL package. The so-called "known good dies" problem has a big influence on the cost structure for this type of packages.

When combining *n untested dies from* wafers with a die yield y_i ,*if the yield of the stacking process is* y_S , *then the overall yield of the stacked package* y_{3D} *will be:*

$$y_{3D} = \prod_{i=1}^{n} y_i \cdot y_S^{n-1} \qquad (3.12)$$

3.5.3.1- Through Si via (TSV) technology

Through silicon vias (TSVs) are the key feature in 3D-WL integration. *The size of the TSV is substantially* smaller *than a wire bond or a solder bump.*

The TSV technology consists of *wafer thinning, wafer "drilling", via oxidation for electrical insulation and via filling with conductive material.*

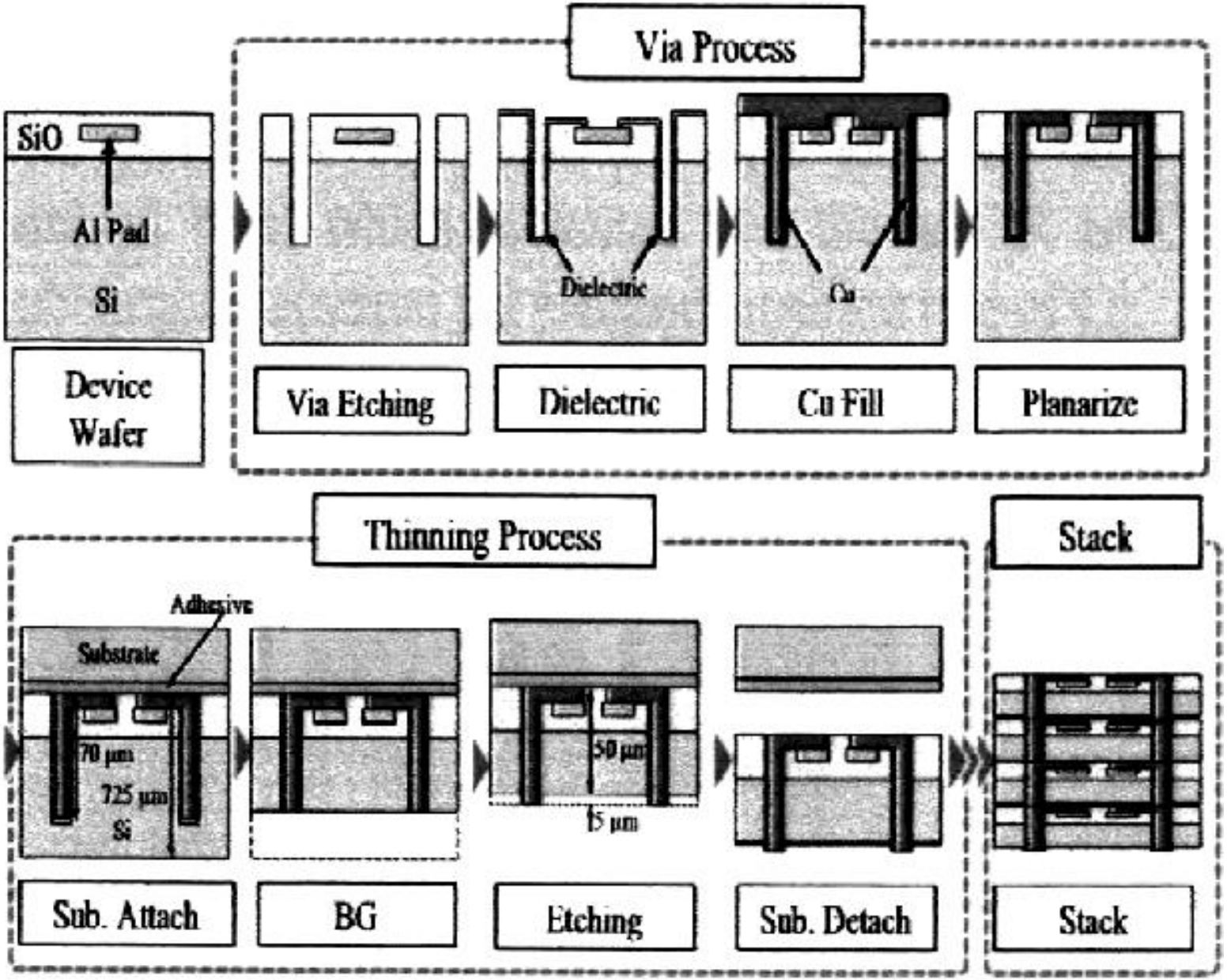
TSVs can be realized using two technologies: plasma etching or laser drilling. TSVs are mainly fabricated by plasma etching in Si using the Bosch process, which applies a repetition of via wall passivation & dry etching the bottom of the vias.

The **aspect ratio (*thickness of die to diameter of via*)** of TSVs is limited due to the limitations of the via filling technologies. Fine-pitch plasma etched TSVs are filled with Cu or W; laser drilled vias can be filled with conductive paste & other materials.

The TSV process starts with the reactive etching of the Si substrate

(DRIE) to form the via. The etching is anisotropic resulting in extremely straight sidewalls. This is followed by the deposition of a dielectric layer (SiO_2), then a conductive seed layer (TiN/Cu), followed by electroplating Cu to fill in the via. Typical dimensions for a through-via is 10 μm on a side. A graphic description of the process is presented in Fig.3.22.

Following via formation, there is a wafer thinning operation using chemo-mechanical polishing (CMP). The thinned wafer is now ready for the stacking or bonding process. The wafer bonding is a critical step in the stacking process. Precision alignment of wafer to wafer is required and must be maintained during the actual bonding process that involves application of heat and pressure. Fig.3.23 is a schematic representation of die vertically interconnected and bonded using Cu-Sn-Cu eutectic for attachment. Highlighted are the various materials and interfaces. Note that in this example the via fill metal is tungsten, W.



Note:
BG = Backside grinding

Fig.3.22: Vertical 3D integration using TSV & die-to-die stacking process.

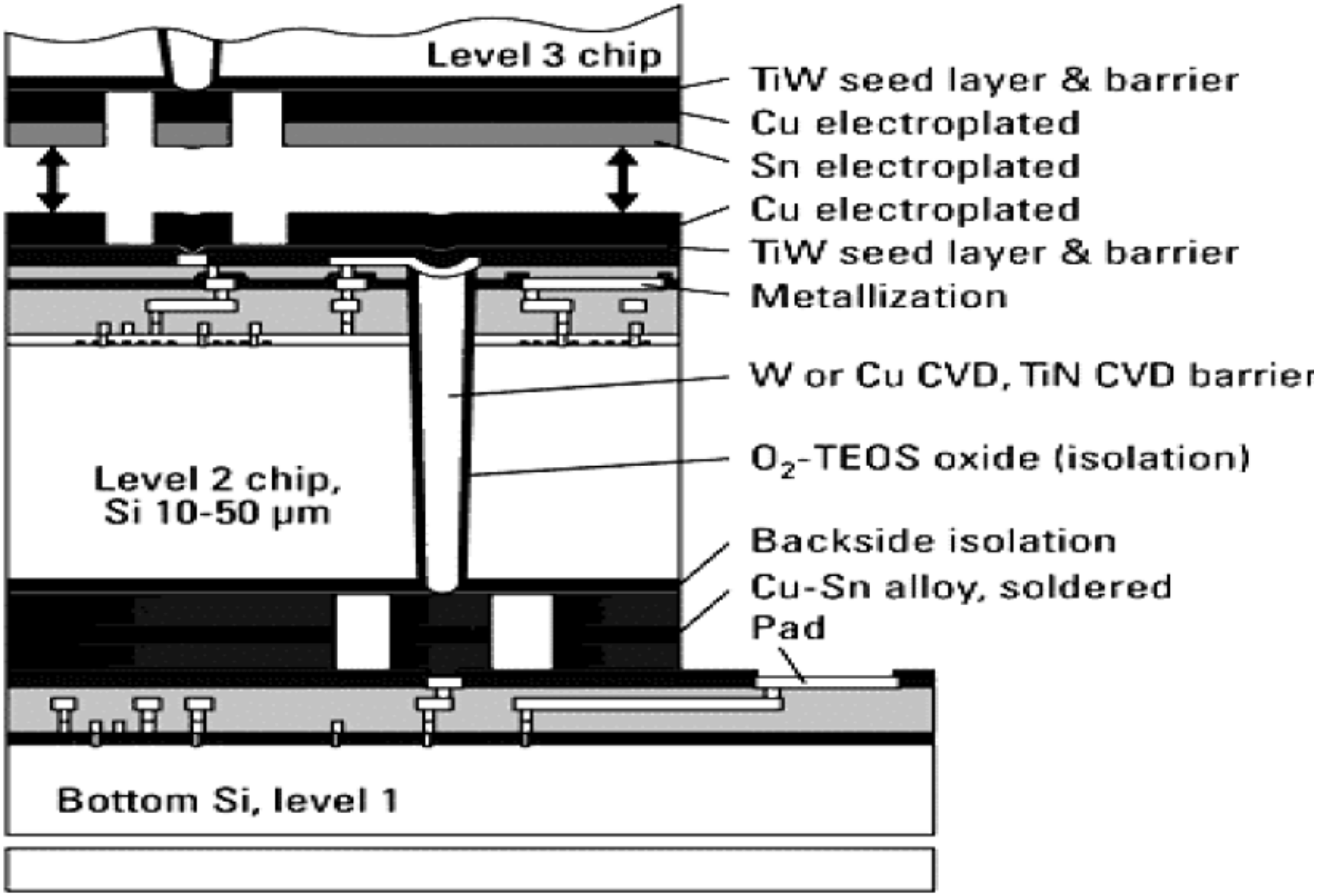


Fig.3.23: Zoom in of a schematic cross-section of vertically interconnected stacked dies.

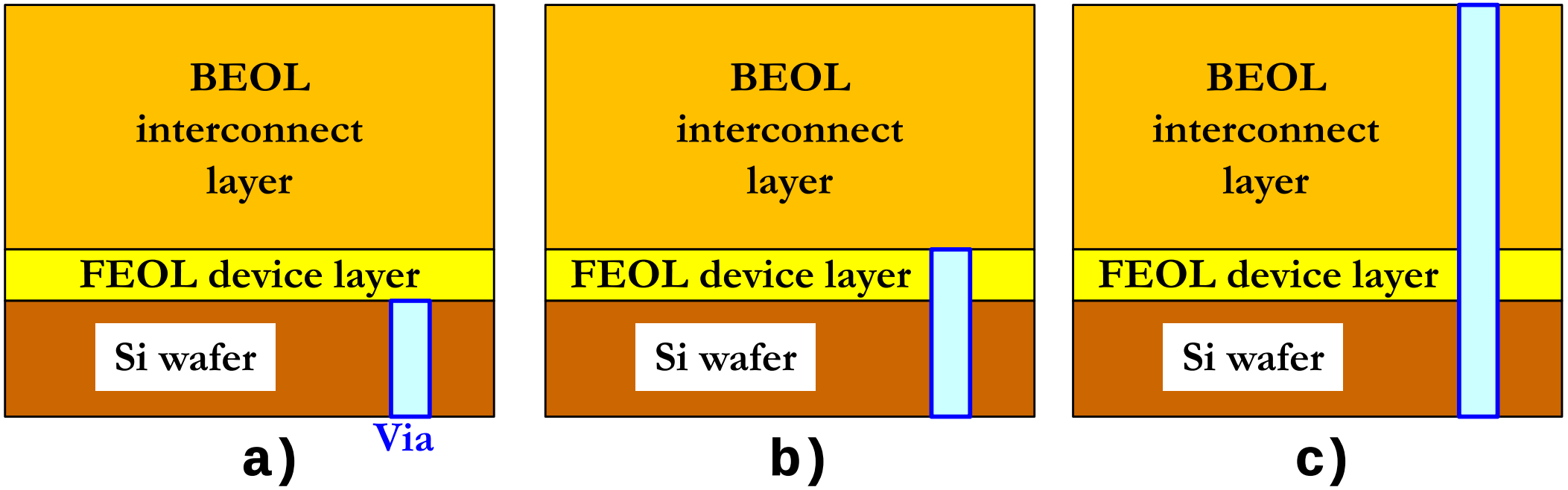


Fig.3.24: The 3 types of via technologies: a) Via first, b) Via middle; c) Via last. BEOL = Back End Of Line; FEOL = Front End Of Line

The process flow for fine pitch via can be configured as via-first, via middle or as via-last process, (Fig.3.24).

The small sizes of TSV enable a higher interconnect density and exhibit lower signal delay and lower power consumption. Table 3.3 compares parasitic parameters of TSV contacts with those for wirebonding and flip-chip (FC) contacts.

	Wirebonding	FC contact	TSV contact
Resistance	122 mΩ	1.2 mΩ	1.7 mΩ
Capacitance	25 fF	<1 fF	-
Inductance	2.6 nH	0.2 nH	0.05 nH
Pitch	100 µm	200 µm	4 µm

Table 3.3: Comparison of parasitic parameters for different interconnect technologies

3.5.3.2- 3D die assembly technologies

Technologies for 3D assembly are still very challenging. There are **different approaches to arrange semiconductor dies in a vertical stack,** such as ***chip-to-chip assembly, chip-to-wafer assembly or as wafer-to-wafer assembly***.

The key assembly processes for 3D packaging by die-stacking are:

- Wafer thinning and singulation,
- Handling of thin dies, and
- Low temperature bonding technologies for TSVs.

After wafer processing the wafers have to be diced into individual dies, usually by mechanical sawing. Beforehand the wafers are mounted on a tape frame. The "dicing before-grinding process" (Fig.3.25) is in use for minimizing the backside chipping of thinned wafers. The wafers are only partially diced and the singulation occurs after backgrinding.

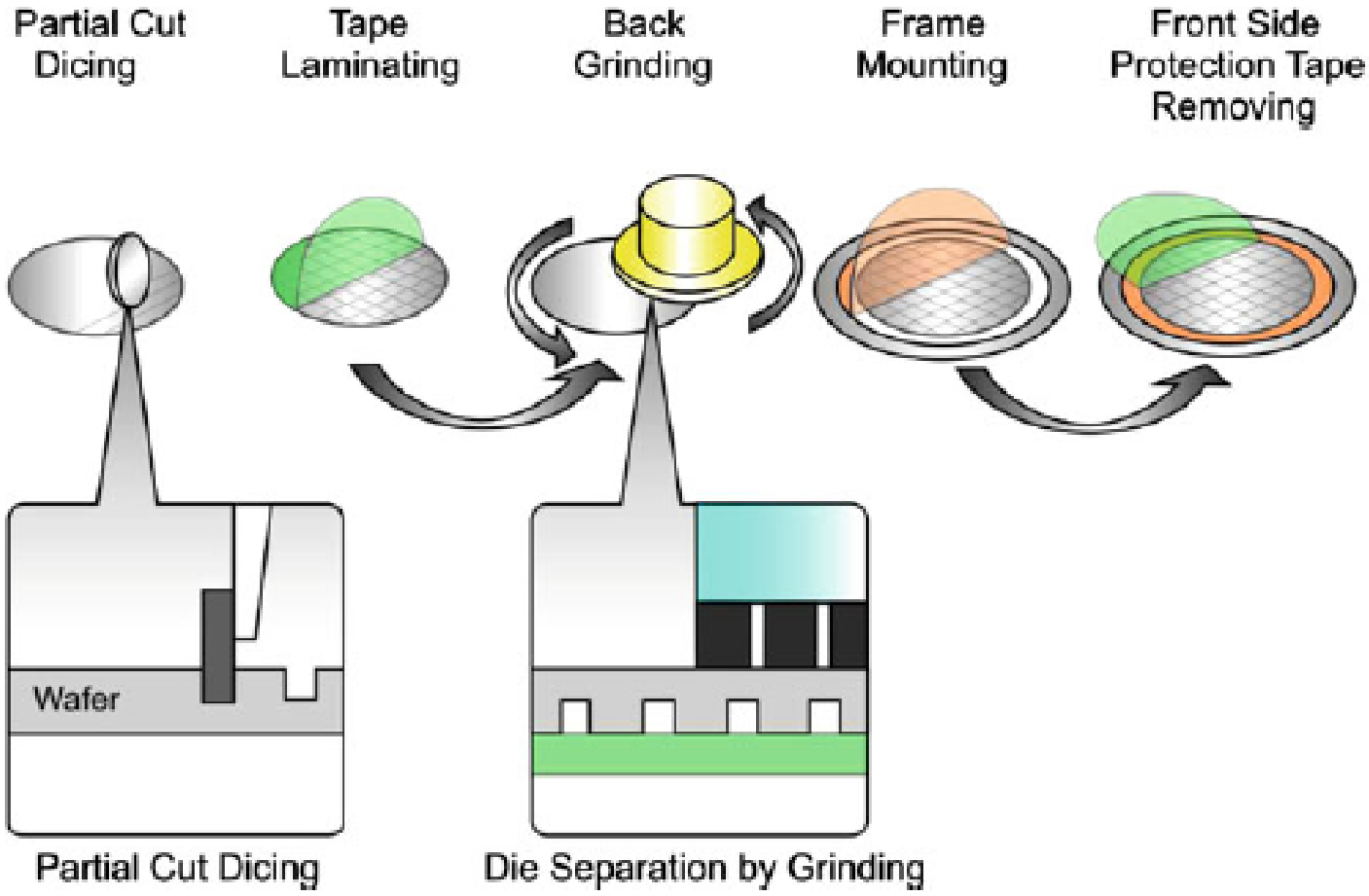


Fig.3.25: Dicing-before-grinding process for singulation

Another key element is ensuring safe handling of wafers for other microelectronic device fabrication processes like chemical–mechanical polishing (CMP), lithography, wet etching, vacuum deposition, plasma processing or backgrinding. *For this purpose rigid substrates are used, mostly made out of silicon or glass*. After completing all required processes the handle substrate has to be removed from the device wafer and will be supported by tape frames for dicing or later for die to wafer bonding.

Subsequent key processes are the **assembly and the bonding** *either as* ***die-to-wafer*** *or as* ***wafer-to-wafer***. **The alignment accuracy for these processes is a challenge and will limit the number of TSV to TSV interconnects.**

Die-to-wafer bonding permits the integration of dies from different wafers and allows the assembly of "known good dies" to "known good receiver dies", which is a great economic advantage.

Bonding processes for 3D-integration are still under investigation. Technologies for bonding play a significant role for achieving the desired

functional performance, the reliability and low cost for the stacks. Two approaches are favored:

- The solder-based bonding uses the solid-liquid interdiffusion (SLID) of Cu with a thin layer of Sn. SLID is applying a soft-soldering material with a low melting temperature resulting in a high-melting and brittle joint, formed by intermetallic compounds (IMC). The difference between the low melting temperature of the solder material and the melting temperature of IMCs allows a sequential multilevel chip stacking at low process temperatures without remelting of joints.
- Cu-to-Cu bonding can be performed as surface activated Cu bonding at room temperature or as thermal compression bonding which is more spread in 3D integration. Cu pads demand uniform height and smooth and free of oxides surfaces. The bonding process has to be arranged in a vacuum chamber by application of high contact pressure and temperatures up to 350^{o}C for 2 hrs.

3.5.4- MCM Stacks

Advantage: *Compared to die stacks, collections of components of dissimilar size and process can be readily cointegrated*. One example of an MCM stacking method is illustrated in Fig.3.26, based on a set of identically sized MCM-C substrates in which conductors are patterned on the top and bottom surfaces with land grid arrays. Compliant interposers are introduced in the borders of each MCM to connect signals vertically.

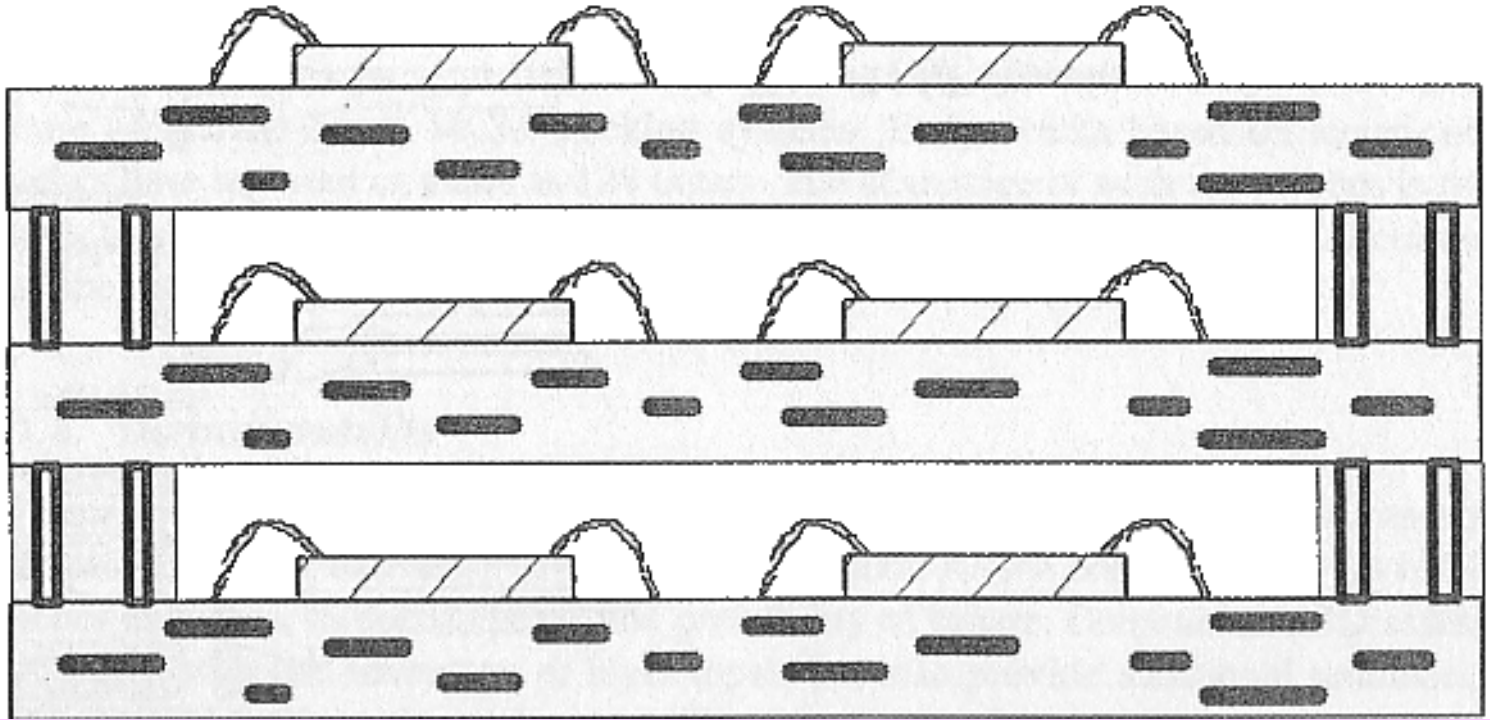


Fig.3.26: Example of a MCM-C stack that uses interposers.

Patterned overlay approaches are particularly suited for 3D assemblies, *since the component layers of the stack are planar*. The 3D HDI is such a process. Its flow and a typical example module are shown in Fig.3.27, in which more planar modules are combined to form a stack. The process used to form these layers is similar to GE's HDI shown earlier in Fig.3.13, only that the **substrates must contain edge conductors**, either built into the substrate or added through a special metallization process. This modification then permits ***to interconnect the set of stacked modules using an edge overlay system***. Additionally, the

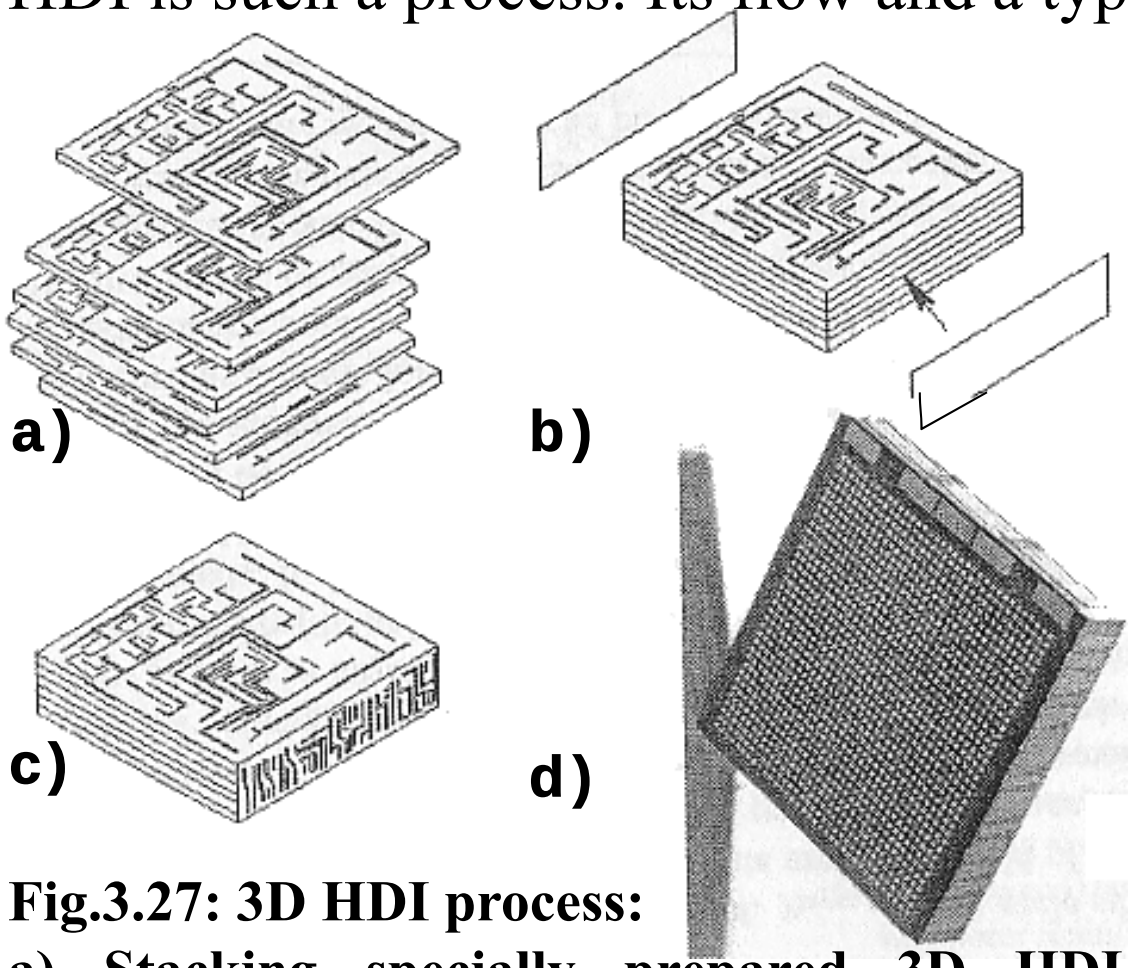


Fig.3.27: 3D HDI process: a) Stacking specially prepared 3D HDI layers; b) Edge overlays formed, c) Finished stack; d) Example of a 4-layer HDI module.

individual substrate edges are now interconnecting components (adaptive lithography again can play an important role in maintaining alignment during fabrication). Once again, Kapton is laminated to the assembly (Fig. 3.27-b) and patterned to create the interconnections between layers (Fig. 3.27-c). A typical module built this way is shown in Fig. 3.27-d.

A still ***more advanced 3D example*** is the so-called **highly integrated packaging and processing (HIPP)**. *It combines a number of special MCM assemblies that are called* ***segments in pairs***. These segments contain MCMs, are patterned with land grid arrays (LGAs), and are jacketed by efficient thermal management structures. *The segment pairs are sandwiched onto thin multilayer printed wiring structures to form a clamshell*. The sandwich employs interposers to ensure a uniformly compliant (positive) contact between each of the conductors on the mated LGAs. *A number of such clamshells can be efficiently stacked and then combined with separate dedicated wiring board structures for power and signal distribution*.

3.5.5- Folding approaches

Folding creates 3D assemblies by converting planar assemblies to 3D through. *This is done with individual dies using an oversized patterned overlay*. ***By extending the overlay beyond the floorplan of an individual component, a "flap" is formed by the excess, which can be folded around the body of the die***. If the flap is patterned, it can be used to produce a convenient connection surface for another similarly patterned component. This arrangement then creates another method for vertical signal transport and any stacking approach (e.g. as shown in Fig.A.4 in **Appendix 3 after L3b**) can be employed. Another method involving folding produces a planar floorplan of components that is simply folded into a 3D assembly. Advantage: *Folded assemblies eliminate some process steps and complexities associated with stacking and connecting the various levels of a 3D system*.

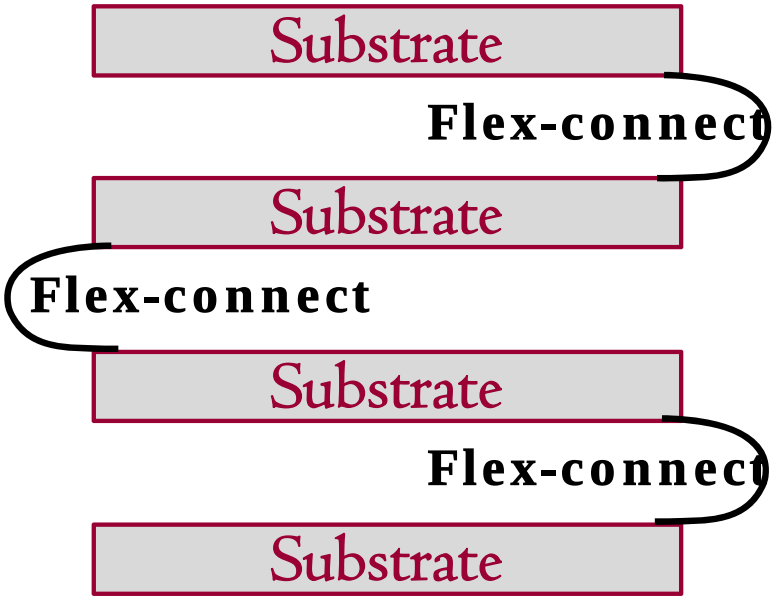


Fig.3.28: Folded flex-based MCM.

3.6- MCM wiring design

The **design of a multichip module** is a complex process that must **consider multiple requirements**: ***electrical function (schematic), final size and weight, environmental performance, and reliability***.

The *size* of the overall MCM substrate is *determined by the physical chip size, the interconnect perimeter, the wiring density, and other physical constraints (e.g. portability)*.

In order to determine the basic size possible, a wireability analysis must be performed. **The objective of a wireability analysis is to determine, *before detailed design and layout,* the ability to route a substrate**. *Wiring analysis can predict the number of layers required to wire the components for a particular circuit design and may also be a useful tool for estimating substrate cost*.

The **basic concepts** in a wireability analysis are ***wiring demand, wiring capacity, average wire length,*** and ***connectivity***.

The wiring demand *D* is the amount of wiring required to

interconnect a given circuit.

The wiring capability C is the amount of wiring available for interconnection. These two parameters are related through the equation: $D = \varepsilon \cdot C$ (3.13), where

ε = the wiring efficiency; typically, it is in the 30-70% range and is a function of a number of factors, such as routing algorithm efficiency and area removed by via occlusion.

Additionally, one can also define a **wiring density** or **wiring capacity** of MCM substrates. *It is a measure of the amount of physical wiring that is maximally available to interconnect components together, and is generally specified in terms of unit length per unit area*. The **total wiring capacity** C_T, which is *a function of the* ***minimum signal lines center-to-center pitch P_S*** **that can be fabricated on a given MCM substrate technology**, is usually normalized to a given square area, such as the **size of the pitch P_P of the packaged part or**

bare chip attached to the MCM (*also called wiring efficiency***)**. In this case, *neglecting via holes and through-holes*, for N_T signal layers (i.e. wiring layers), the total wiring capacity C_T is given by: $C_T = \frac{P_P \cdot N_T}{P_S}$ (3.14).

Generally, substrates with higher wiring capacities are capable of accommodating more complex assemblies. MCPs and stacked packages have no wiring capacity. They must rely on arrangements where the proximity of pads on dissimilar dies is sufficient to permit completion of intra-package connections.

To calculate the wiring demand ***D***, the **average length per interconnection** $\overline{L}$ must be estimated. *This length between any two points (1 and 2) is* ***not*** *a direct route*, since alternate layers of signal line are usually routed in *x* and *y* orthogonal channels, or 'streets'. The ***average wiring path length*** is *sometimes referred to as the* **Manhattan length**, which is given by: $\overline{L} = |x_1 - x_2| + |y_1 - y_2|$ (3.15).

The wiring demand D is then simply

$$D = N_{PP} \cdot \bar{L} \qquad (3.16), \text{ where}$$

N_{PP} is the number of pin-to-pin connections.

If considering that, for an average number of pins per net area N_{AP} there are $(N_{AP} - 1)/N_{AP}$ number of wires, then for a given number inputs and outputs N_{IO}, the wiring demand D is:

$$D = N_{IO} \cdot \bar{L} \cdot \frac{N_{AP} - 1}{N_{AP}} \qquad (3.17).$$

To estimate $\bar{L}$, assuming that the chips on an MCM substrate interact with either their nearest neighbors or their next nearest neighbors yields an average length given by $L = 1.5P_P$ (3.18'), but a more general approximation is $\bar{L} = 0.77P_P \cdot N_C^{0.245}$ (3.18''), where N_C is the number of chips to be interconnected.

Estimating the wiring demand in the **absence of a preliminary layout** *uses* ***Rent's Rule:*** $N_{IO} = a \cdot g^b$ (3.19), where N_{IO} = the number of inputs and outputs for the chip, package, or substrate; g = the number of fundamental circuits (gates) contained within the chip, package, or substrate; a = **the Rent's coefficient *or the average number of connections per circuit I/O***, and b =the Rent's exponent ($0<b<1$). Approximate Rent's Rule exponents and coefficients for various devices and systems are given in Table 3.4.

Rent's Rule is especially useful in determining required circuit density and optimal device placement for a particular circuit design. **The total number of gates (or circuits) *G* on an MCM containing an arbitrary number of circuits (chips),** can be found from the relation:

$$G = \sum_{i=1}^{m} N_i g_i \qquad (3.20), \text{ where}$$

N_i is the number of type i components, g_i is the number of gates in the i^{th} component type, and m is the number of different devices. ***This expression***

Device/System	***a***	***b***
Dynamic Random Access Memory (RAM)	6.2	0.085
Static RAM (SRAM)	6	0.12
Microprocessors	0.82	0.45
Random Logic (gate arrays)	1.9	0.5
Computer Systems	2.5	0.6
Chip/Model Level	1.4	0.63
Board/ System Level	82	0.25

Table 3.4: The coefficients and exponents for Rent's rule for various device & system technologies.

assumes that all of the individual circuits or components have the same Rent's relationship. Then **the total package I/O count N_{IO},** assuming *no interaction between the circuits of different types* (a worst-case wiring scenario), is given by: $N_{IO} = a \cdot G^b$ (3.21).

Although originally Rent's rule was informally documented as an empirical observation to certain types of circuit modules in computer

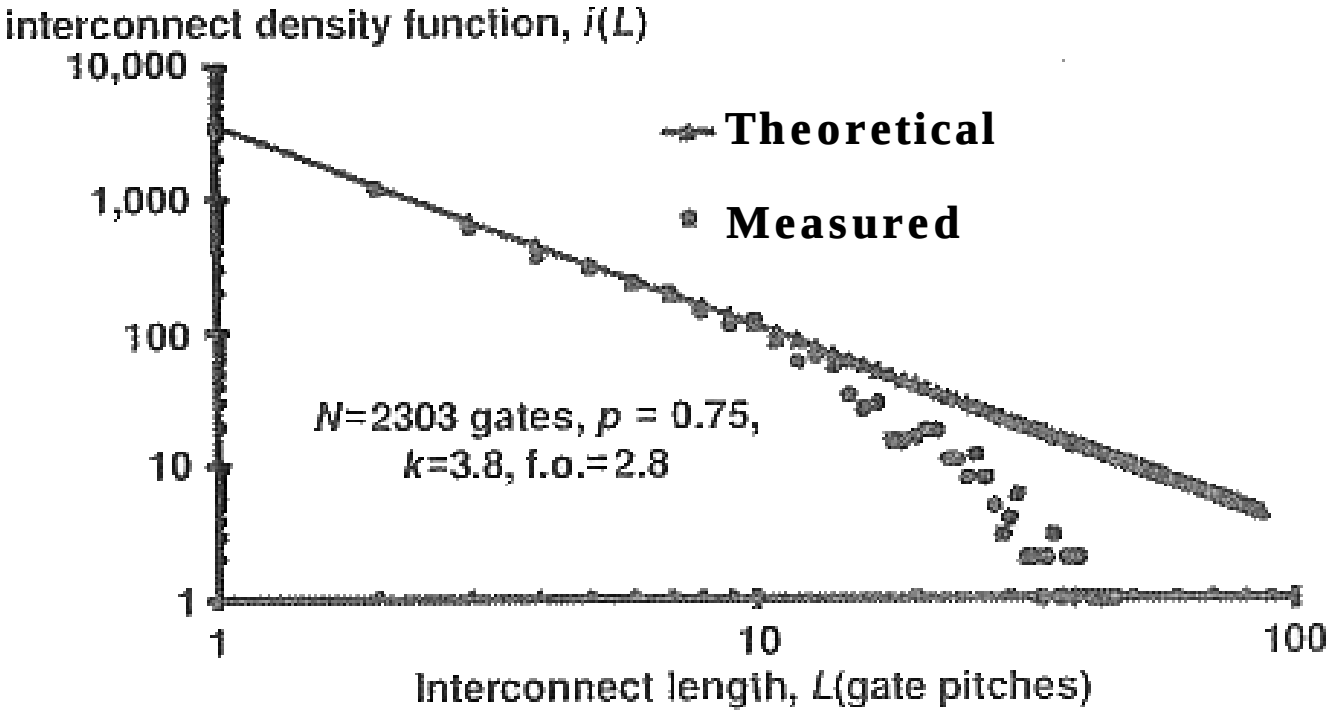


Fig.3.29: Interconnect length distribution in a typical modern VLSI IC.

systems in the early 1960s, it has been found to be germane to most of the recursive elements in a hierarchy such as that shown in Fig.3.3. For example, using Rent's rule, an analytic distribution of interconnection lengths in integrated circuits was found, which is compared in Fig.3.29 against a typical distribution in an actual IC.

Rent's rule demonstrates the importance of power law relationships in understanding certain aspects of packaging complexity, but it requires

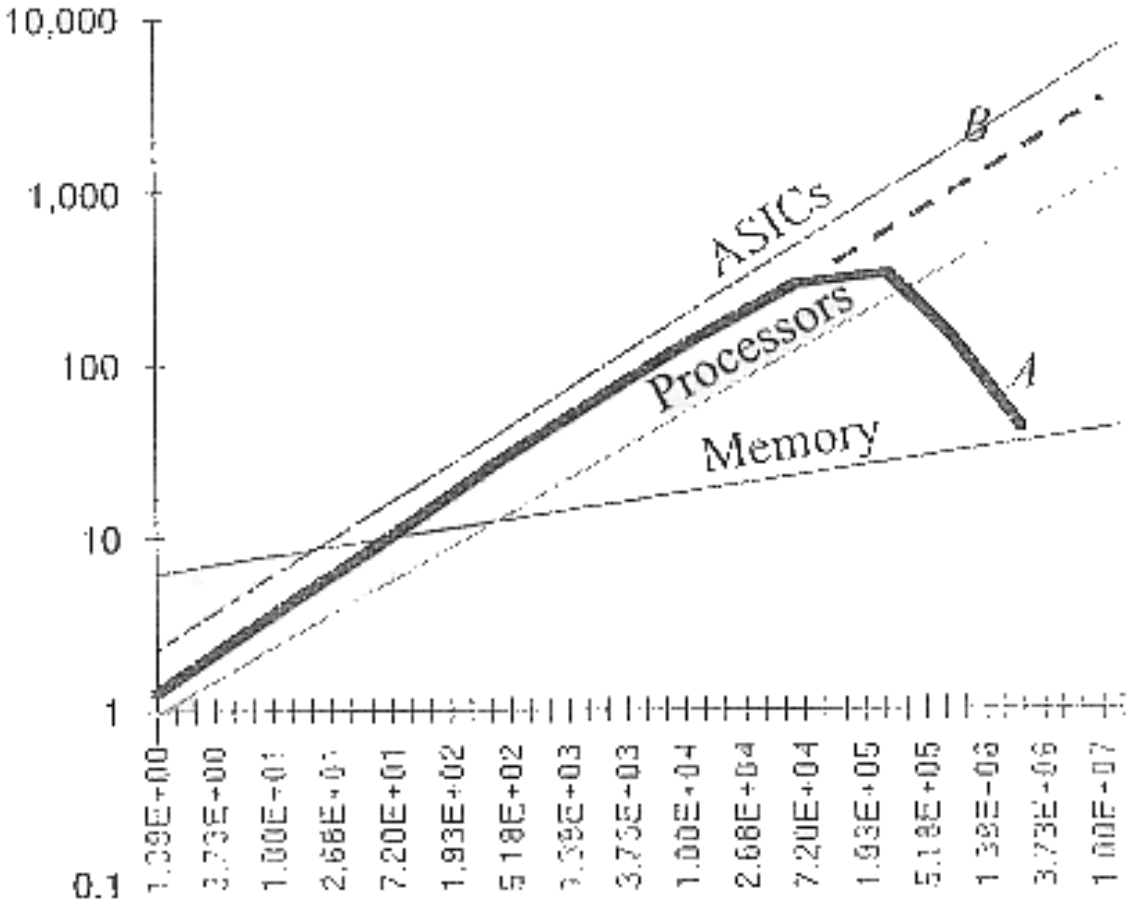


Fig.3.30: Rent's rule for different component types & system classes:
A- dimensionally constrained,
B- performance constrained.

careful interpretation. For example, it explains the **steady** ↑ ***in I/O numbers for complex ICs as gate counts have also*** ↑ ***according to Moore's law***. This growth rate in I/O numbers depends on component type, as suggested in Fig.3.30. *Different types of components have different Rent's exponents*. Regular structures, such as memories, possess a low

Rent's exponent and, therefore, have a very slow growth in I/O. On the other hand, processors and complex application-specific integrated circuits (ASICs) lack such regularity in structure and, therefore, drive higher I/O for a comparable number of gates.

It has been reported that the *Rent's exponent of many electronic systems falls in the range* $0.65 < b < 0.75$. **This range for Rent's exponent becomes problematic for 2D systems**, however, ***as the complexity of systems increases***.

It is straightforward to show this by comparison to an arbitrarily large 2D system. Assume that a large 2D system is divided into 4 equal square partitions, with pins spaced equidistant in each partition. Assume each partition has t pins. For each $k \times k$ arrangement of t-pin blocks, Rent's rule takes the form

$$4\left(\frac{1}{4}k\right)t = t\left(k^2\right)^b \qquad (3.22).$$

Since Rent's rule applies recursively, we observe that each partition has t pins and there are k^2 partitions. By definition, there are t pins per

block. Since only the blocks on the perimeter contribute to the global I/O count, the exposed partitions contribute one of four edges, and the global system has 4 edges. Obviously, the only solution for arbitrarily large k is given in the limit b= 0.5, corresponding to the maximal b in infinite 2D systems. For 3D systems, it can be shown that the resulting value is b= 2/3, which closely corresponds to the previously observed range for most real-world systems.

The analysis of real systems, which may contain mixtures of circuit types each having a different local b, is not so easily captured by a single power law expression. In this case *a heterogeneous Rent's rule expression has to be developed & used in order to deal with such mixtures*. *Cases are easily contrived, however, where monotonic increases in gate count do not result in monotonic increases in I/O*.

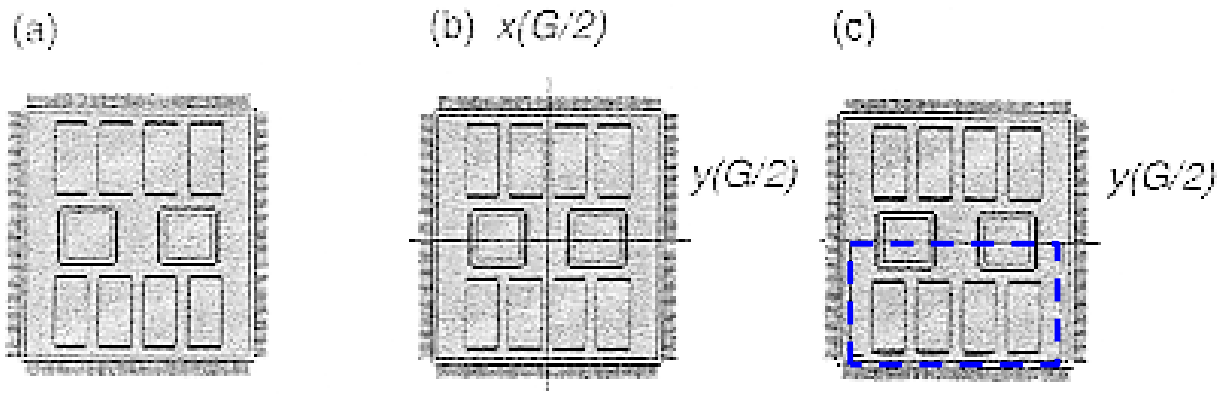


Fig.3.31: Circuit example for Rent's rule to estimate the nr. of multichip module package leads: a) Basic MCM; b) Imaginary dividing lines such that half of the logic gates fall on either side of the two lines; c) Imaginary box incorporating half of the total number of logic gates

Example: Consider the circuit shown in Fig.3.31, which contains two gate array devices with 5000 gates each and eight 64-MB static random access memory (SRAM) chips. In order to design correctly the substrate for this MCM, estimate the maximum wiring, i.e. the number of leads on each side, required by this four-sided MCM (with inputs and outputs on all sides).

Solution: Table 3.4 gives the values a= 1.9 *and* b= 0.5 for gate arrays

$\Rightarrow$ using eqn. (3.19) with g= 5000, the number of I/Os for each gate array chip is: $N_{IO\text{-}g.a.chip} = 1.9 \cdot (5000)^{0.5} = 134$ *each.*

At the same time, Table 3.4 gives the values $a = 6$ *and* $b = 0.12$ *for SRAM. We also know that a kilobit is* $1\ \text{kb} = 2^{10}$ *bits, hence a* $1\ \text{Mbit} = 2^{20}$ *bits, and since bytes -**not** bits- are involved, one must also multiply with 8. Therefore, for the 64 MB capacity we have* $g_{SRAM} = 64 \times 8 \times 2^{20}$, *and using eqn. (3.19) the number of each SRAM chip I/Os results as* $N_{IO\text{-}SRAM} = 6 \cdot (536870912)^{0.12} = 67$ *each.*

However, since each type of circuit has a different Rent's exponent, it is necessary to bring them to a common denominator, so to speak, i.e. to find a single equivalent g value by considering all chips to be of t*he same type, so they can have the same Rent's exponent and coefficient. (Otherwise we cannot apply later eqn. (3.20) to find out the value of* G*). Since SRAMs are predominant, let's 'convert' the* g *for the gate array chips. This can be done by considering & solving eqn. (3.19) for a SRAM using the* $N_{IO\text{-}g.a.}$*:*

$$a_{SRAM} \cdot g_{g.a.equiv-as-SRAM}^{b_{SRAM}} = N_{IO-g.a.} \Leftrightarrow \log g_{g.a.equiv-as-SRAM} = \frac{\log N_{IO-g.a.} - \log a_{SRAM}}{b_{SRAM}}$$

In this case we get

$$\log g_{g.a.equiv-as-SRAM} = \frac{\log 134 - \log 6}{0.12} = 11.2412 \Rightarrow g_{g.a.equiv-as-SRAM} = 10^{11.2412}\ !$$

which is obviously impossibly large!!! This means that our mathematical equivalation is not correct, or at least is not in the right direction. Noticing that the large value of g_{equiv} *is ultimately due to the small value of* b, *let's try the opposite conversion, i.e. to consider that all chips would be 'equivalated' as gate arrays (*a=1.9, b=0.5*). In this case we need to 'convert' SRAMs into g.a-s. The equation remains principially the same, only the subscripts change correspondingly:*

$$\log g_{SRAMequiv-as.g.a.} = \frac{\log N_{IO-SRAM} - \log a_{g.a.}}{b_{g.a.}} = \frac{\log 67 - \log 1.9}{0.5} \Rightarrow g_{SRAMequiv-as-g.a.} = 10^{3.0946} = 1,243$$

We can now apply eqn. (3.20) to find the total number of equivalent logic gates G:

$$G = \sum_{i=1}^{m} N_i g_i$$

for which we have, for i=1 (gate arrays), N_1= 2, and g_1= 5,000 , *while for*

i=2 (SRAM equiv. as g.a.) $N_2 = 8$, *and* $g_2 = 1{,}243$, *resulting in*

$$G = 2\times5{,}000 + 8\times1243 = 19{,}944.$$

Then, the estimated total number of package leads can be calculated from eqn. (3.21): $N_{IO\text{-}tot\text{-}MCM} = 1.9\cdot(19{,}944)^{0.5} = 268$ *leads in total, for the entire MCM* => 67 *leads on each side*.

In the previous example, *the* ***maximum number of wires crossing a horizontal line*** *can also be estimated*. It is ***assumed*** that the **maximum number of vertically traveling leads will occur at the coordinate point where there are *G/2* gates above the line and *G/2* gates below the line**. The horizontal and vertical coordinates of this point will be given by *y*(*G*/2) and x(*G*/2), respectively (see Fig.3.31-b & -c). *To estimate the number of leads whose wires will cross this horizontal line, an imaginary box is placed around the lower portion of the circuit*, as shown in Fig.3.31-c. Using Rent's Rule, the number of leads *N* whose wires will exit this imaginary box is given by:

$$N = a\left(\frac{G}{2}\right)^b = \frac{N_{IO}}{2^b} \qquad (3.23).$$

Also, it is *assumed that the number of leads going to the package I/O pins located below this line will not affect the wire congestion in the vertical direction*. Similarly, *the number of package leads must be reduced by a factor of* $1-(N'_{IO}/N_{IO})$, where N'_{IO} = the number of package leads available to the $G/2$ circuits without crossing over the imaginary line $y(G/2)$. Thus, the ***maximum number of vertically going leads*** is given by:

$$N_h = \frac{N_{IO}}{2^b}\cdot\left(1-\frac{N'_{IO}}{N_{IO}}\right) \qquad (3.24).$$

The ***number of wires crossing that horizontal line is***:

$$W_h = a\cdot N_h \qquad (3.25).$$

For the previous example, $N'_{IO} = N_{IO}/2 = 134 \Rightarrow$ eqn.(3.24) for this case becomes

$$N_h = \frac{N_{IO}}{2^b} \cdot \left(1 - \frac{1}{2}\right) = \frac{N_{IO}}{2^{b+1}} = \frac{268}{2^{1.5}} \approx 95$$

Hence, assuming an average of a=1.9 leads per max. number of vertically travelling wires that cross the horizontal line $y(G/2)$, the number of wires crossing it will be $W_h = a \cdot N_h = 1.9 \cdot 95 \approx 180$.

By symmetry, in this particular example, max. number of horizontally travelling wires that cross the vertical line $x(G/2)$ will also be 180, resulting in a grand total of 360 wires.

If the MCM substrate is 1.5 in. × 1.5 in. and the line-to-line pitch is 10 mils, then the wiring capacity is 150 wires per layer, neglecting vias and keep-out areas. However, assuming a 50% routing efficiency, the actual wiring capacity is 75 wires. Thus, for our total of 360 wires per layer, about 5 signal layers would be required to route this design.

However, we should highlight that for signal wiring even more layers need to be added than those suggested by the above analysis. **Conductors to distribute power and ground planes to control**

impedance must be included. *A rule of thumb is to add a power layer & a ground layer for every 4-5 signal layers*, with all MCMs having at least one power layer and one ground layer. *Other requirements* (electromagnetic interference shielding, impedance control, etc.) *may dictate the use of even* ***more*** *ground planes*.

Generally speaking, ↑ **the level of integration determines an inherent ↑ in the number of layers, with resulting disadvantageous consequences: high L & Z ⇒ ↑ noise and operating f_{MAX} , ↑ complexity (more vias & more layers, to be fabricated with better accuracy and ↓ feature size) ⇒ ↑ cost and ↓ overall reliability**.

Requirements related to the spacing of the I/Os on the chip also exist. If the spacing of the wires on the MCM metallization layout is larger than the I/O spacing on the chip, then it is difficult or impossible to fit wires in the pin pattern, thus causing a major increase in the number of board layers to get 100% connectivity.