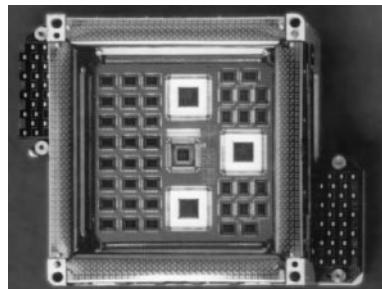

12 MULTICHIP MODULES (MCMs)

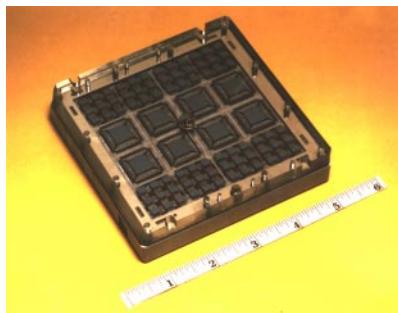
HISTORICAL PERSPECTIVE

Virtually every large computer manufacturer, telecommunications products manufacturer, high volume consumer electronics manufacturer and aerospace products manufacturer is working on or considering designs that include multichip modules. There has been a dramatic increase in activity over the last five years, with entire conferences being dedicated to multichip modules. MCMs have gone through three phases in their growth.

Phase one was the widespread use in mainframe and super computer products. Some examples of MCMs used for these high-end applications are shown in Figure 12-1. The primary driving force was performance. These systems were predominately ECL based, with relatively low integration levels. The MCM implementation allowed the "re-integration" of the LSI chips into VLSI modules, while keeping the wiring delays small.

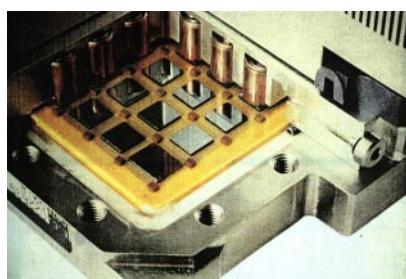


Source: DEC



Source: Motorola/Siemens

Source: ICE, "Roadmaps of Packaging Technology"



Source: IBM

22555

Figure 12-1. Early MCMs in ECL Mainframe Computers in the Mid 1980's

Using a conventional single chip package and circuit board interconnect strategy, the package and interconnects took up over 50% of the timing budget. Decreases in the chip delays could not have much impact on system performance without a significant decrease in the interconnect delays as well.

The use of MCMs reduced the interconnect delays significantly. This is shown in Figure 12-2 comparing the delays in the IBM 3033 with a CPU using single chip packages and four circuit boards, and the IBM 3081, the first mainframe that used the Thermal Conduction Module (TCM). An example of this first large volume application of MCMs for IBM is shown in Figure 12-3. The use of an MCM cut the CPU from four boards to one board and the wiring delays from 28nsec to 9nsec.

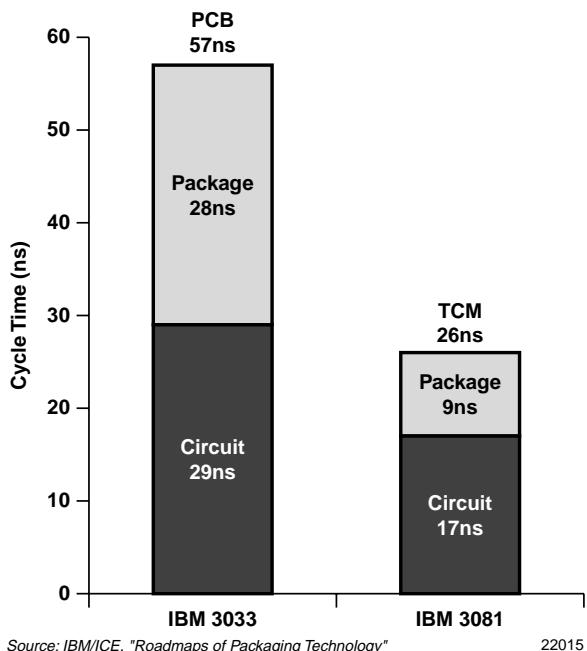
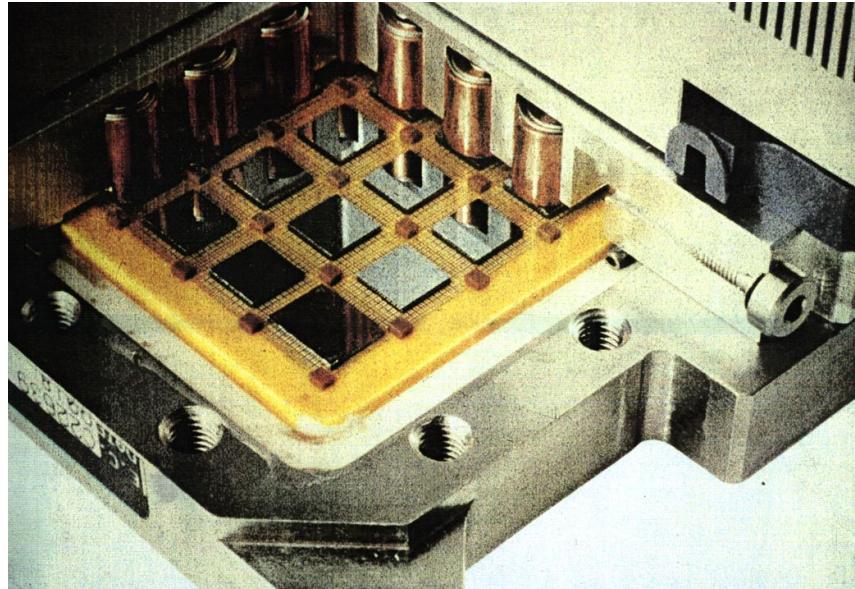


Figure 12-2. IBM Case Study: Wiring Delays as a Fraction of Total Delays

The cost of being one of the first to implement MCMs in production was not cheap. IBM invested \$1B in their cofired ceramic packaging facility. DEC invested over \$600M in their thin film line. Some estimates of the investment for other MCM substrate technologies are listed in Figure 12-4.

Phase two was the exploration of MCM technologies and the building of an infant infrastructure by the visionaries and champions of a merchant MCM industry. The attention focused on MCMs stimulated the end users to work through scenarios of product applications and technology implementations to find the most cost effective matches.



Source: IBM/ICE, "Roadmaps of Packaging Technology"

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Figure 12-3. IBM TCM with Flip Chip on Cofired Ceramic Substrate

COMPANY	TECHNOLOGY	YEARS	DOLLARS TO MANUFACTURING
IBM	Complete Multilayer Cofired MCM	10	1B
DEC	Complete Thin-Film MCM	6	600M
Siemens	Complete PWB-Based MCM	5	250M
AT&T	Complete Thin-Film, Si-on-Si, Flip-Chip MCM	5	200M (development only)
Raychem	Thin-Film, Si, Ceramic Substrates Only	6	70M (low-volume prototypes)
Alcoa	Thin-Film, Si, Ceramic, Cofired Ceramic Substrates	6	200M (production)

Source: ICE, "Roadmaps of Packaging Technology"

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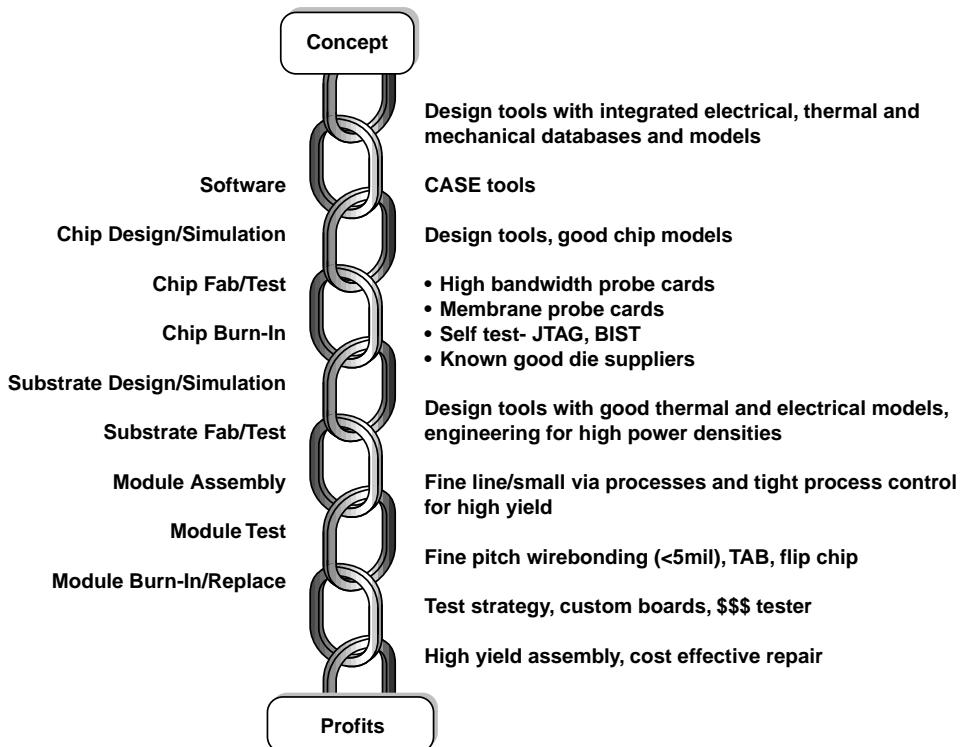
Figure 12-4. Estimated Costs of Developing High-Density Packaging

Many of these early pioneers had their start in large system companies. This was a period of high expectations being set. The belief was, "...if we build it, they will come". If there were a viable thin film substrate based technology, for example, companies would flock to incorporate it into their products.

MCMs were viewed as taking over all of packaging. The single chip package was declared dead. Thin film MCMs were projected to revolutionize the electronics industry. Everyone was talking about their commitment to MCMs. Using the word MCM in a company's product literature gave the company an association with leading edge and state of the art.

A number of start-ups were funded with venture capital money in order to be positioned to participate in this coming revolution. Some of the visionary companies which did not survive the shake-up include Polycon, Advanced Packaging Systems, ISA, Polylithics, Alcoa Microelectronics, TI's HDI and Pacific Microelectronics Center.

A common perception was that thin film multilayer substrates were the optimum substrate solution for MCMs. Having a substrate technology was often confused with having an MCM solution, however. In fact, the substrate was only one link in the chain required to successfully and economically implement an MCM product. Figure 12-5 illustrates the other pieces that were discovered to be needed. The attention focused on these other aspects stimulated the growth of an MCM merchant infrastructure.

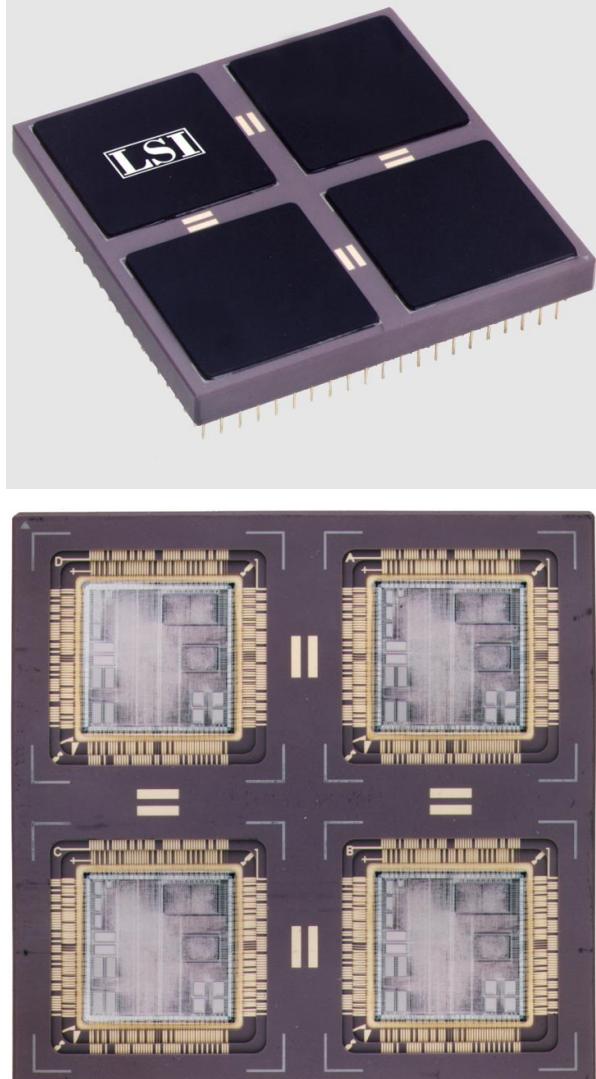


Source: ICE, "Roadmaps of Packaging Technology"

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Figure 12-5. The MCM Infrastructure

End users of everything from computers to consumer products, such as Sun, Silicon Graphics, Apple Computers, LSI Logic and Kodak, had designed and built a number of prototype MCMs to evaluate the vendor base, technology options and cost/performance benefits to MCMs. A few of these designs actually went into limited production. Figure 12-6 is an example of a four chip graphics controller module LSI Logic fabricated for SGI, currently in production.



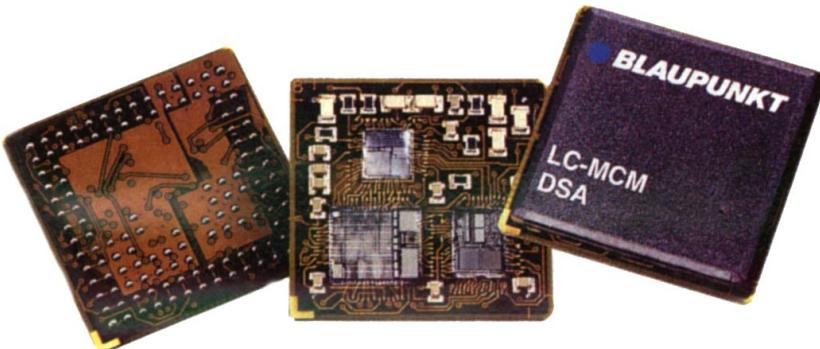
Courtesy of LSI Logic
Source: ICE, "Roadmaps of Packaging Technology"

22343

Figure 12-6. LSI Logic MCM-C

Out of this phase of vision (or hype) has arisen the third phase—the establishment of a strong merchant infrastructure and the introduction of MCM designs that are in volume production, spanning the range from high end computer to low end consumer products. It is principally the portable and wireless consumer products that have fueled this third wave of application and integration of MCMs.

All the attention placed on MCMs over the last ten years has resulted in the identification of some of the market niches where MCM solutions make sense. A few examples of modules in production are shown in Figures 12-7 and 12-8.



Source: Blaupunkt/ICE, "Roadmaps of Packaging Technology"

22029

Figure 12-7. Low Cost Four Layer MCM-PBGA Controller



Courtesy of S-MOS/ICE, "Roadmaps of Packaging Technology"

22005

Figure 12-8. Cardio Chip on Board Module, x86 Module

Through the pioneering efforts of the early visionary individuals and companies and stimulated by strong competition from off shore vendors, multichip modules are today moving into volume production in the merchant world. The MCM market is estimated to be between \$1B and \$3B by the year 2000, with a projected growth rate on the order of 20%. Some examples of the market forecasts are shown in Figures 12-9 and 12-10.

Year	Revenues (\$M)	Revenue Growth (%)
1988	182.5	—
1989	217.1	18.9
1990	259.8	19.7
1991	312.0	20.1
1992	375.7	20.4
1993	453.1	20.6
1994	547.2	20.8
1995	660.4	20.7
1996	788.5	19.4
1997	926.2	17.5
1998	1,067.6	15.3

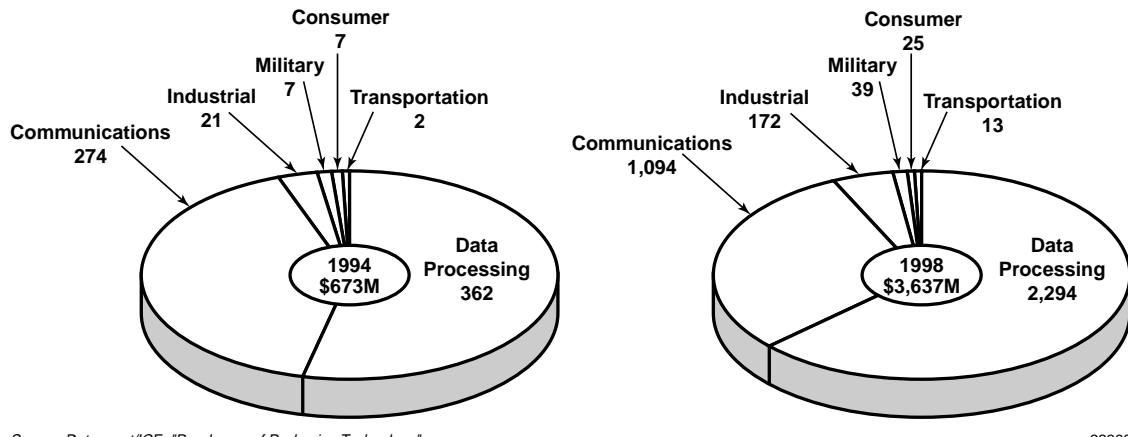
**Compound Annual Growth Rate
(1991-1998): 19.2%**

Note: All figures are rounded

Source: Frost and Sullivan Market Intelligence/
ICE, "Roadmaps of Packaging Technology"

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Figure 12-9. MCM Market World Revenue Forecasts 1988-1998 (In Millions of Dollars)



Source: Dataquest/ICE, "Roadmaps of Packaging Technology"

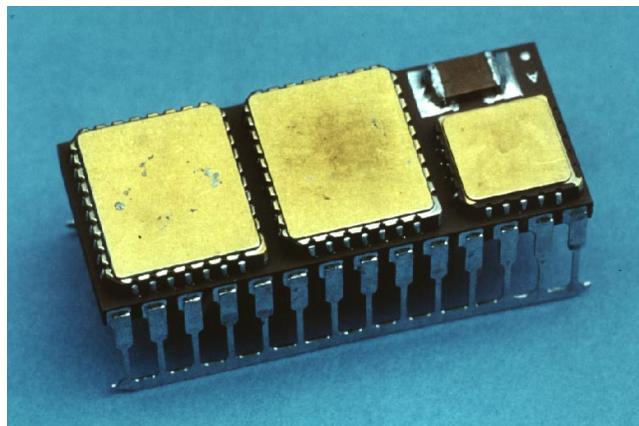
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Figure 12-10. MCM Revenue in North America (\$M)

WHAT IS AN MCM?

The term multichip module (MCM) has been in use for at least 25 years. However, the term refers to a constantly moving target. In the industry today, there is still ambiguity about what constitutes an MCM.

There has been a tendency to take advantage of the current high-tech marketing hype associated with the label MCM and call any functional collection of chips on a single substrate an MCM. For example, the modules shown in Figure 12-11 have been called MCMs even though they consist of packaged die mounted on a substrate.



Source: ICE, "Roadmaps of Packaging Technology"

15767A

Figure 12-11. Dual In-Line Module

Some modules have been a “tour-de-force” in package engineering, such as the modules used by NEC in the SX-X and Fujitsu in the VP2000. The NEC modules use substrates of cofired ceramic with thin-film, copper-polyimide multilayers on top. The Fujitsu substrates have 61 layers of low-temperature cofired ceramic glass with copper traces. Yet, in both applications, the chips are packaged in single-chip micropackages.

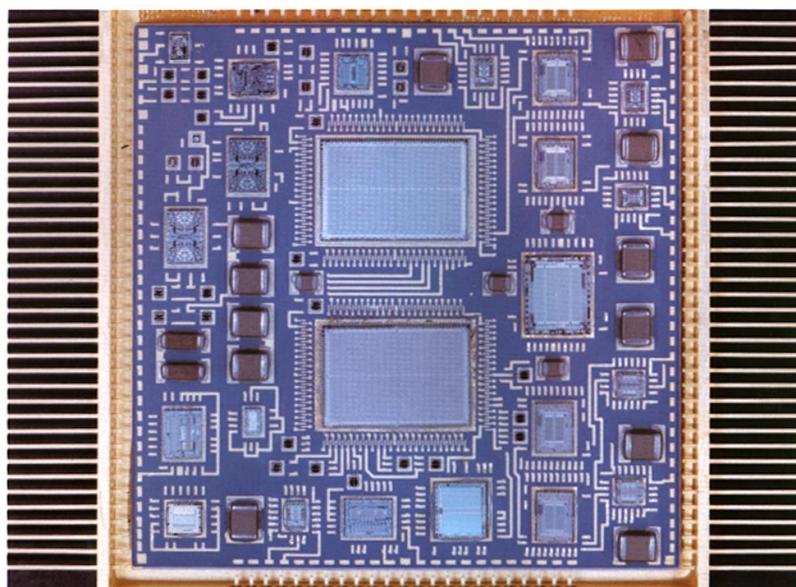
The generally accepted definition of an MCM is a collection of more than one bare die on a common substrate. All modules meeting this condition share the same common issues associated with using bare dice, using a substrate with fine surface features for chip interconnection and interfacing to the next level.

Even so, there is ambiguity in this definition—what is the accepted definition of a bare die? The Motorola MCAIII and MCAIV devices are offered as epoxy-encapsulated dice on TAB carriers. The only difference between this configuration and a 25mil pitch leadless plastic TapePak™ pack-

age is the outer pitch of the leads. Is a chip on a TAB carrier a “bare” die or a packaged die? When mounted on a thin-film interconnect substrate, as DEC did in the VAX 9000, is the module a multichip module? In most cases, modules with TAB are considered MCMs. Handling the tape carrier package (TCP) requires special care, the outer lead pitch is typically 10mil or less and requires a higher density interconnect substrate than traditional boards.

Based on this definition, the evolving four families of MCMs include:

Hybrids: traditional thick film substrates with typically small die and low density of interconnect, with an external form factor that is a custom leaded hermetic can. An example of a hybrid is shown in Figure 12-12.

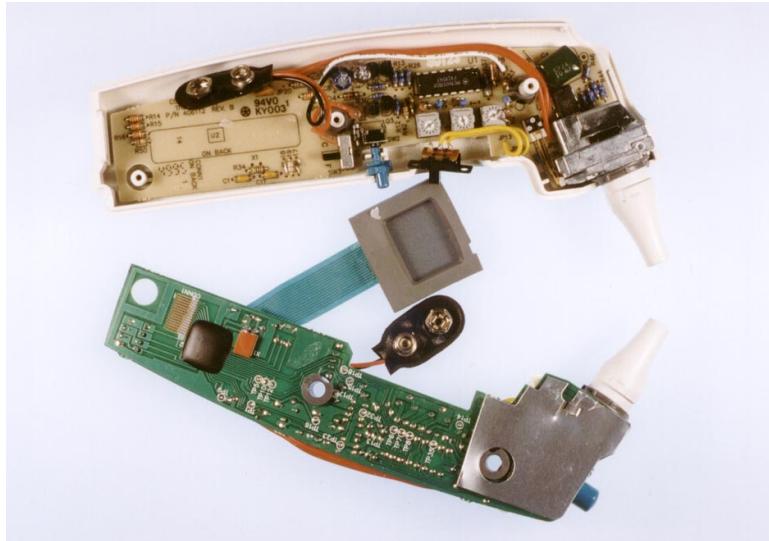


Source: Boeing Microelectronics/ICE, "Roadmaps of Packaging Technology"

22563

Figure 12-12. Rocket Control and Monitoring Hybrid

Chip on Board (COB): bare dice on organic laminate substrates, such as FR4, along with other SMT devices, both packaged devices and discrete components. The form factor is typically a small daughter card, such as PC cards, smart cards, and small motherboards. The dice can be wirebonded and called COB, or flip chip attached and called DCA (direct chip attach) or TAB mounted. Examples are shown in Figures 12-13 and 12-14.



Courtesy of Flextronics/ICE, "Roadmaps of Packaging Technology"

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Figure 12-13. Thermoscan Instant Thermometer

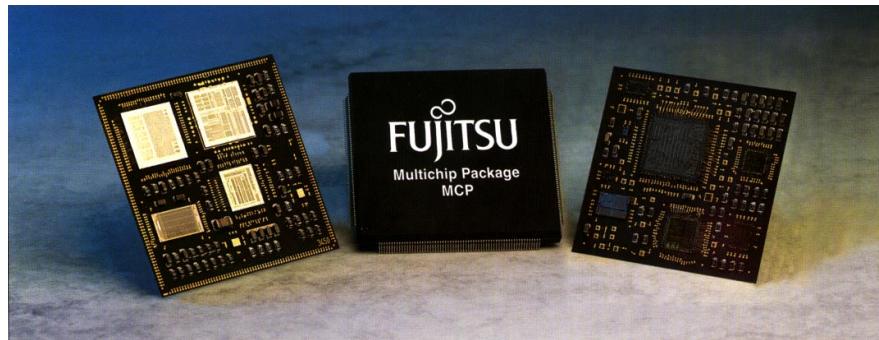


Courtesy of Flextronics/ICE, "Roadmaps of Packaging Technology"

22008

Figure 12-14. Close Up of the Encapsulated Chip-On-Board

Few Chip Packages or Multi Chip Packages (MCPs): a small module that has an external form factor that matches a single chip package, and typically two to five bare dice. The dice can be attached using wirebonds, flip chip attach or TAB. The external form factor can be leaded as a PQFP, PGA or BGA. Once packaged, the MCP is handled just like a single chip package. The end user never needs to know if a single chip or multiple chips are inside the package. An example is shown in Figure 12-15.

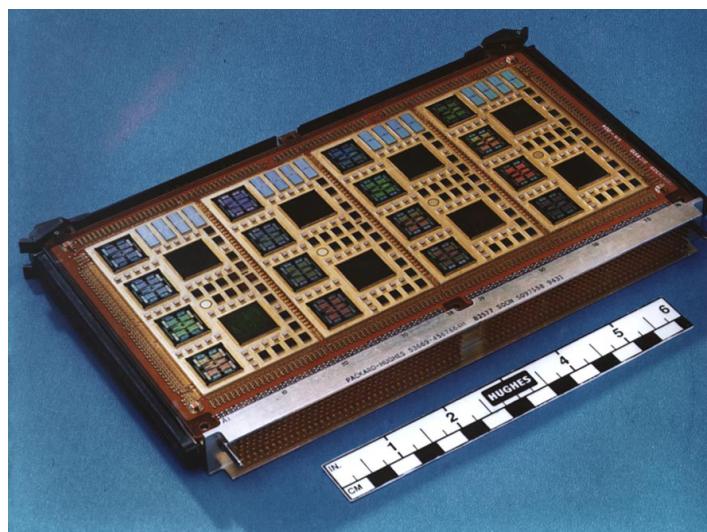


Source: Fujitsu/ICE, "Roadmaps of Packaging Technology"

22057

Figure 12-15. Wireless Module in a Multichip Package (MCP)

High end MCMs: This includes large, high density substrates with many chips as used in mainframes and large military hybrids that have multiple high density dice and a custom form factor. An example is shown in Figure 12-16.



Courtesy of Hughes Microelectronics/Source: ICE, "Roadmaps of Packaging Technology"

22562

Figure 12-16. High Performance Avionics Controller with Four Thin Film MCMs Mounted on One Card

All MCMs currently in production now, or being planned in the near term fit into one of these four categories.

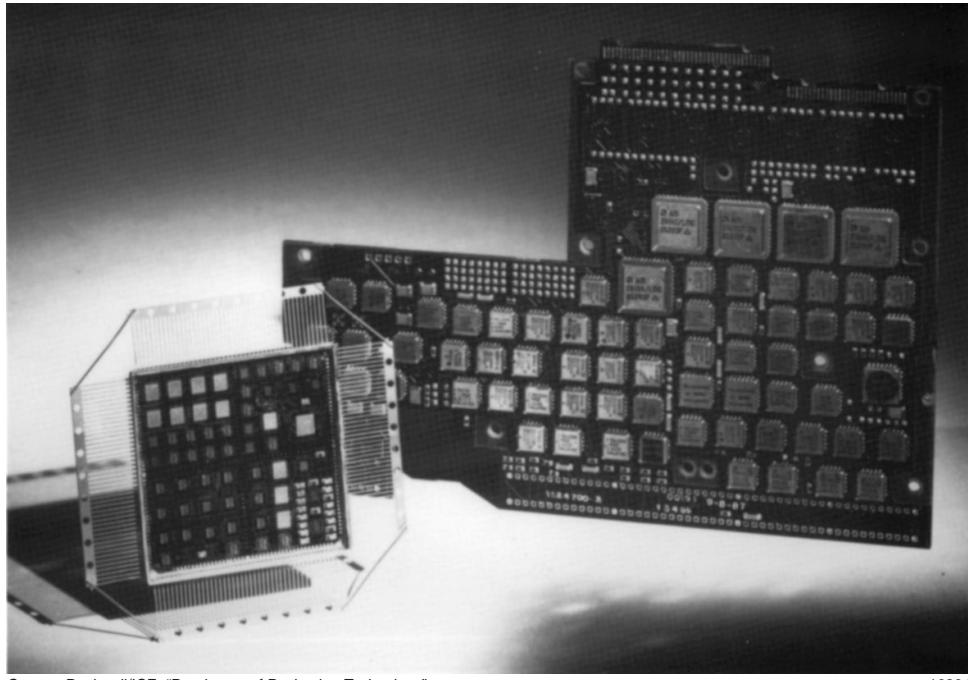
WHY MCMs

Among these four families of MCMs, there is one common feature that drives their use: the single chip package is eliminated. This one change allows for three potential gains over the conventional approach of single chip packages on circuit boards:

- Smaller size and less weight
- Higher performance
- Lower cost

One or more of these reasons plays a role in every application of MCM in production today.

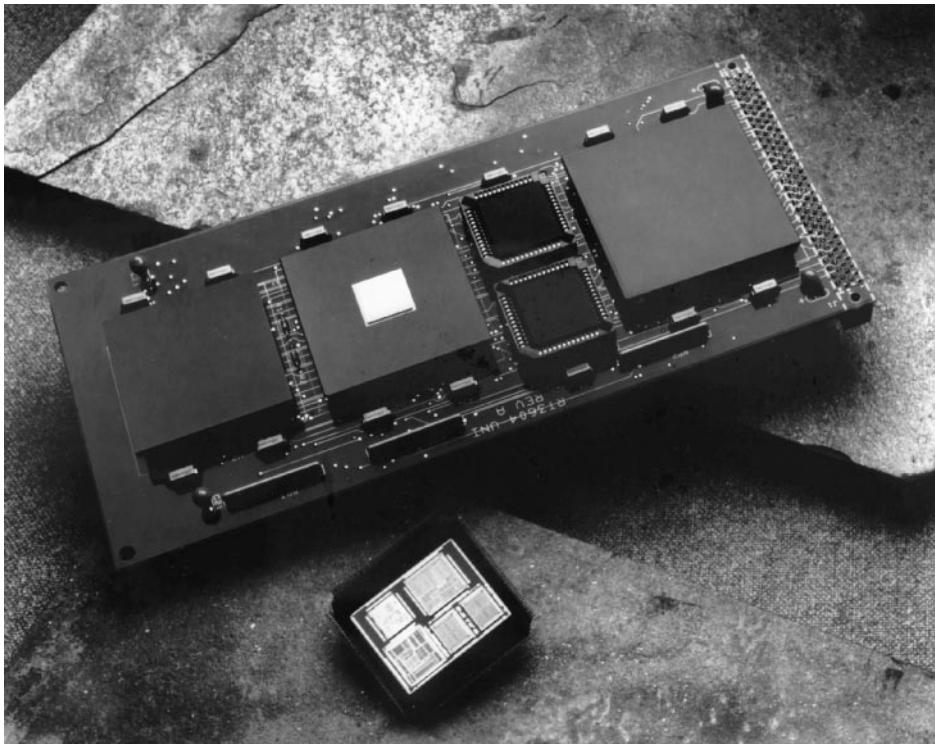
The size reduction possible with an MCM implementation is graphically apparent when two identical designs are compared, a conventional and an MCM. Figures 12-17, 12-18, 12-19, 12-20, and 12-21 show direct comparisons between single-chip packages on a substrate and the same chip set in an MCM.



Source: Rockwell/ICE, "Roadmaps of Packaging Technology"

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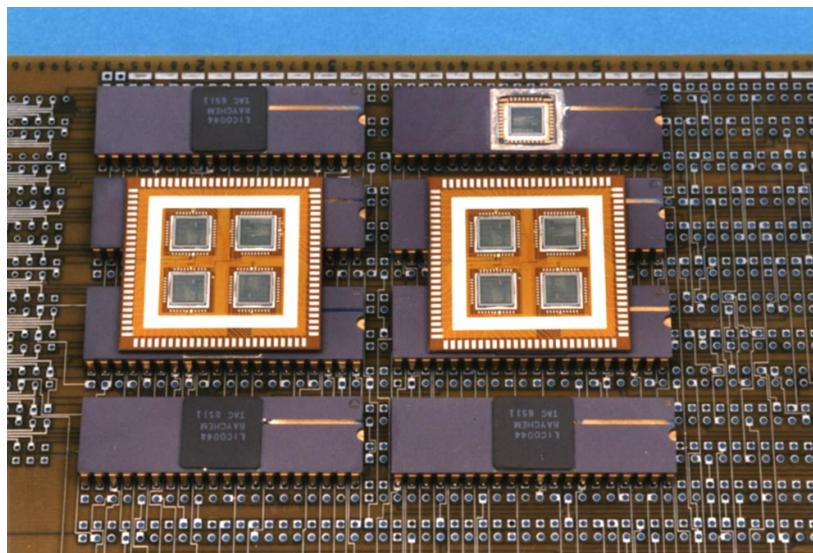
Figure 12-17. Conventional Board and Equivalent MCM



Source: nChip/ICE, "Roadmaps of Packaging Technology"

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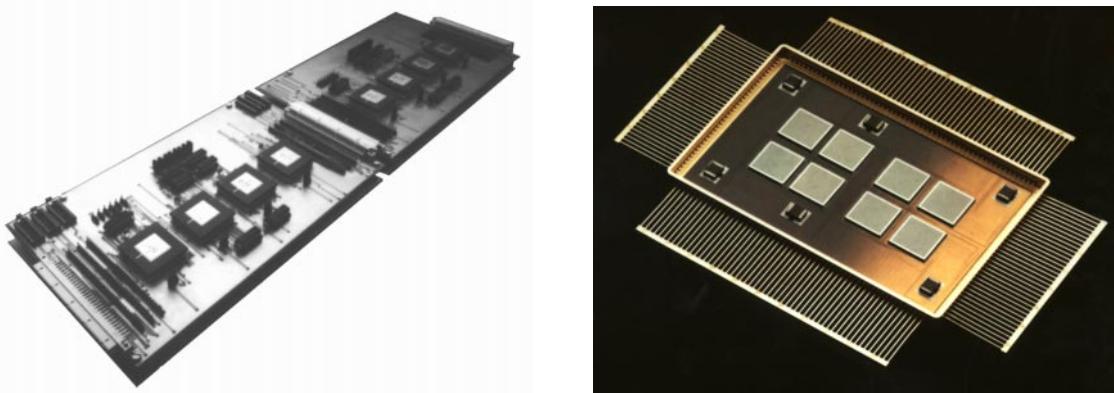
Figure 12-18. Comparison of Conventional and MCM RISC Microprocessor Chip Sets



Source: Advanced Packaging Systems/ICE, "Roadmaps of Packaging Technology"

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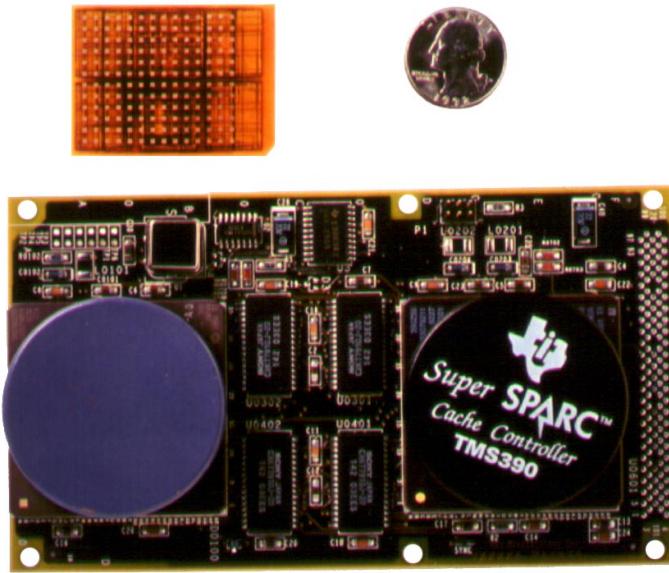
Figure 12-19. Thin-Film Multichip Modules and Equivalent Single-Chip Packages



Source: Pacific Microelectronics Center/ICE, "Roadmaps of Packaging Technology"

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Figure 12-20. Comparison of Conventional DSP Board and Equivalent MCM

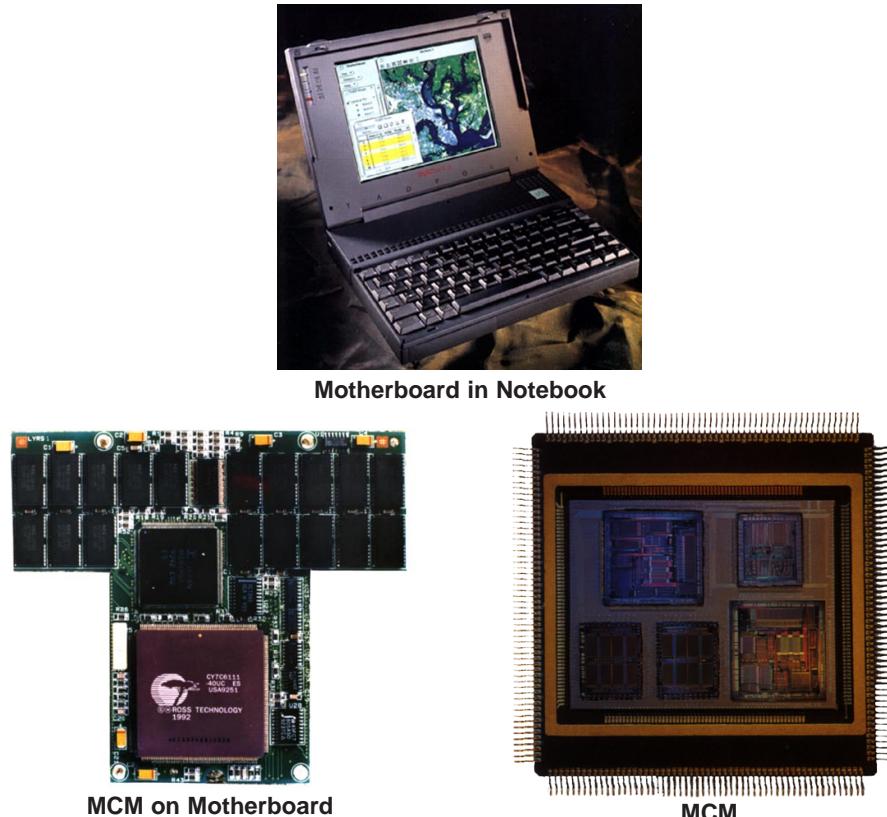


Courtesy of Sun/ICE, "Roadmaps of Packaging Technology"

22010

Figure 12-21. SuperSPARC Module in Conventional Form Factor and Integrated as a Chips First Module

Portable applications, especially notebook computers, camera and telephone applications are the primary drivers for smaller size. Figure 12-22 illustrates the size reduction possible using an MCM in a notebook application. These applications have fueled the growth in particular of the MCP style. Figure 12-23 is an example of a four chip module that was designed for use in a hard disk drive in a PC-card format, where space was at a significant premium. In these applications, a small premium in price was worth the added value of smaller size. Typically laptops are priced at a 20% premium over their comparable desktop versions.



Source: Tadpole/nCHIP/ROSS/ICE, "Roadmaps of Packaging Technology"

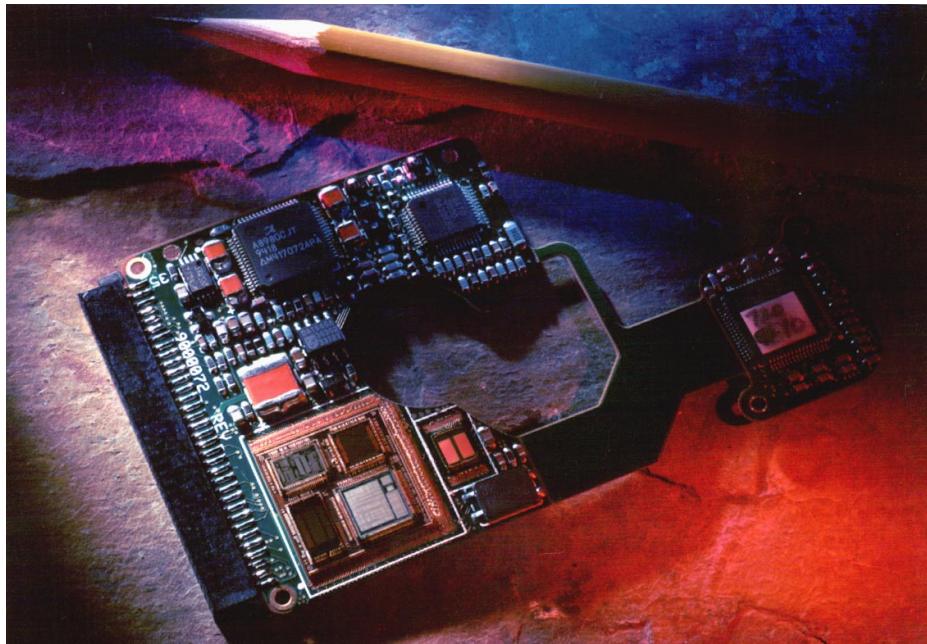
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Figure 12-22. SPARCbook 2 Notebook Computer

In addition to physical size, there is a reduction in:

- The weight of the system
- The total interconnect length
- The total interconnect capacitance
- The switching power dissipation
- The critical net wiring delay
- The electrical noise generated

Of course, an already released product will seldom be redesigned into an MCM unless it enables a new form factor for the product or significant cost reduction. Some of the examples of systems converted to MCMs shown above were developed as evaluation and demonstration vehicles. In practice, it will be the next generation product that will be designed with a new technology. This adds confusion and can be misleading when comparing the current generation product in conventional technology with a next generation product in a new technology.



Courtesy of MMS/ICE, "Roadmaps of Packaging Technology"

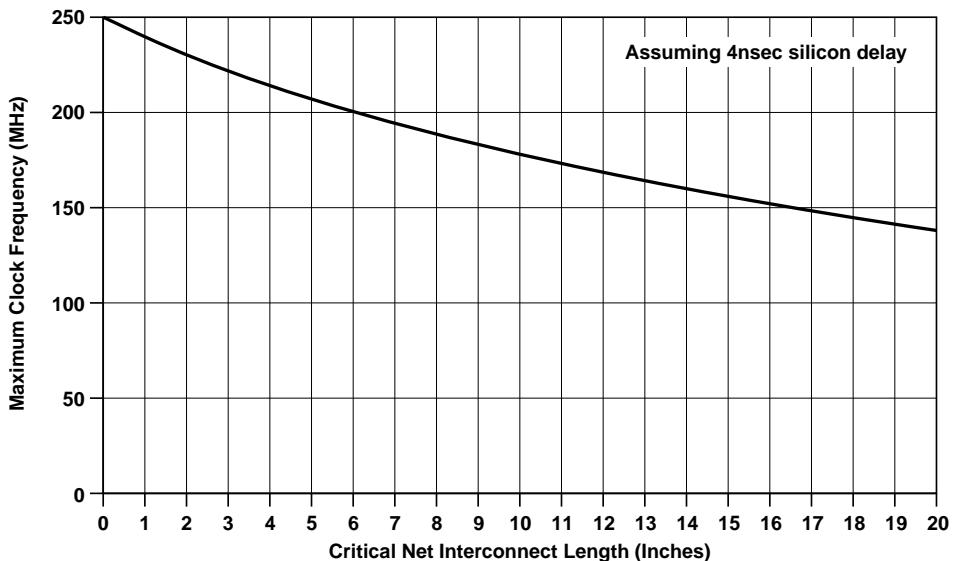
22035

Figure 12-23. Disk Drive Controller Card with Small MCM

The performance of a system can be increased by an MCM implementation only if critical nets exist between chips. If the clock frequency is limited by propagation delays within the core of the chip, no amount of packaging innovations will increase the clock frequency. However, if wiring delays influence the clock frequency, then the delays can be reduced by a factor of 3-10, simply based on interconnect length reductions.

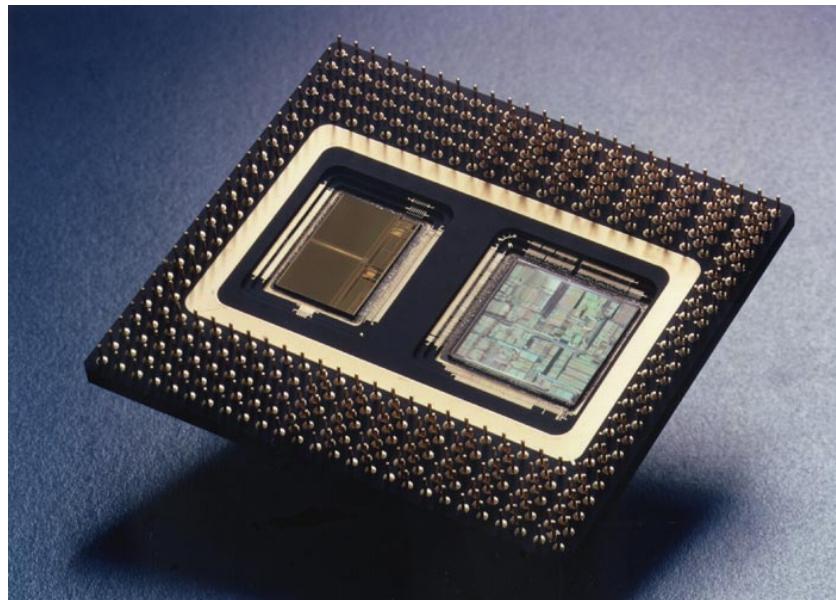
For example, if the on-chip delays are 4nsec, the influence of the wiring delays can be calculated assuming a wiring delay of 160psec/in. The resulting clock frequency for the system is shown in Figure 12-24. An effective interconnect length of 12 inches in a conventional approach results in a clock frequency of 160MHz. If an MCM implementation drops the interconnect lengths to 2 inches, the clock frequency can be increased to 230MHz. This was the motivation of Intel to use an MCM for the Pentium Pro, shown in Figure 12-25. The proximity of the L2 cache to the CPU allows a 200MHz clock frequency.

Another performance benefit that may be gained in an MCM approach over a conventional approach is the reduction in switching noise. This arises from two sources. The output load capacitance a driver sees will be lower on an MCM with shorter interconnects. Lower load capacitance means less charge is switched, which means less dI/dt .



Source: ICE, "Roadmaps of Packaging Technology"

22558

Figure 12-24. Interconnect Limited Clock Frequency

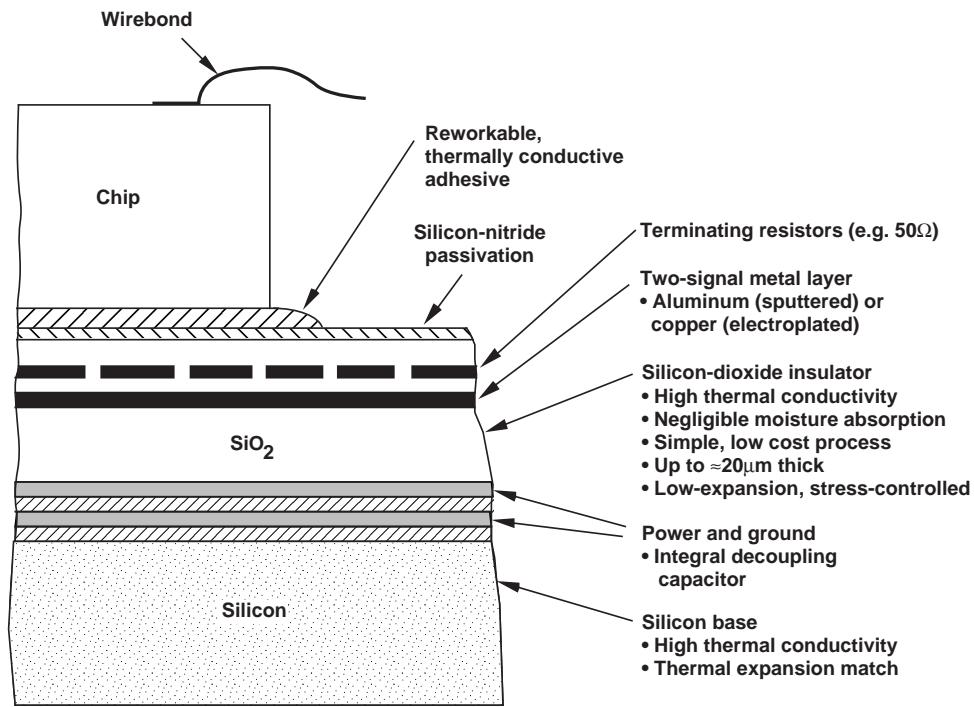
Source: Intel/ICE, "Roadmaps of Packaging Technology"

20116

Figure 12-25. Pentium Pro Processor

Secondly, the bond leads can be kept shorter on an MCM if the substrate used has fine lines and microvias. This will decrease the lead inductance and the switching noise. The lowest inductance is possible using flip chip. An additional benefit to flip chip is the opportunity to add more power and ground pins to the chip, decreasing the effective inductance even more.

An added feature in some technologies is integrated low-inductance decoupling capacitors, possibly built into the substrate as thin-film capacitors. An example is shown in Figure 12-26. If switching noise is reduced, it is not necessary to select the long slew rate option offered on virtually all gate arrays, and higher bandwidths can be used.



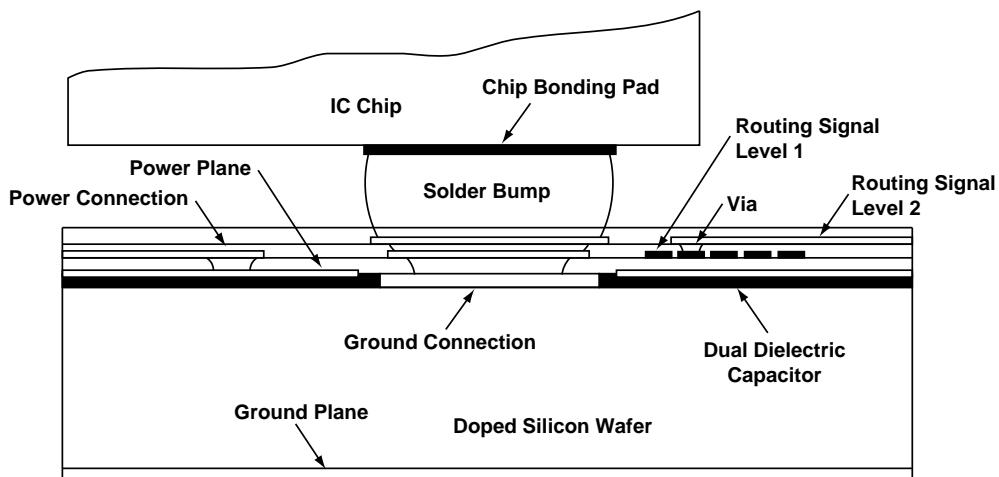
Source: nChip/ICE, "Roadmaps of Packaging Technology"

16218A

Figure 12-26. nCHIP Silicon Circuit Board

The combination of C4 chip bonding, ground and power planes, and integrated thin-film decoupling capacitors offers a nearly ideal electrical environment. An example of AT&T's version of this design is shown in Figure 12-27. Of course, these features can be incorporated in single chip packages as well, as pointed out in previous chapters.

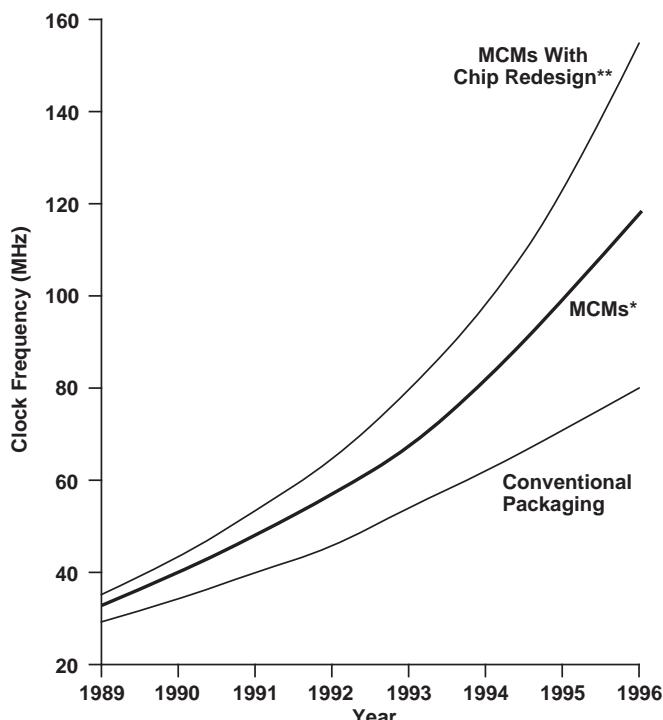
Currently, all gate arrays use output drive buffers that have larger current drive capabilities than the internal gates, and longer propagation delays. For example, the internal gate delay for LSI Logic 0.7 micron CMOS gate arrays is less than 0.5nsec. The delay for off-chip drivers is 1.4nsec for the fastest, able to drive a 15pF load. The output buffer to drive an MCM internal net could be reduced in size and offer a lower gate delay. For example, a typical net, one inch long, may have a capacitance of only 4pF. With a chip redesigned for lower capacitive loads, there may be an additional increase in speed. A study by nCHIP, shown in Figure 12-28, illustrates this possibility.



Source: AT&T/ICE, "Roadmaps of Packaging Technology"

11913

Figure 12-27. Interconnect Substrate and IC Chips



* Assumes a 4ns gain.

** Assumes a 6ns gain.

Source: nChip/ICE, "Roadmaps of Packaging Technology"

16217

Figure 12-28. Microprocessor Performance

In summary, the features of an MCM that offer enhanced electrical performance are:

- Smaller wiring delays through shorter lengths
- Shorter driver delays through less capacitive loading, leading to faster buffers
- Lower switching noise due to small bonding parasitic paths
- Lower propagation noise due to controlled impedance interconnects

There is heat dissipated, P_{AC} , whenever an interconnect capacitance is charged and discharged. The lower the capacitance that is continually charged and discharged per clock cycle, the lower the switching power dissipation. The advantages MCMs offer are lower interconnect capacitance and an ensuing lower AC power dissipation.

The total power dissipated in the output buffer resulting from the need to drive a length of interconnect, L_{trace} , is:

$$P_{AC} = C_L L_{trace} V^2 F_{clock}$$

If there are 300 nets in a PWB-based circuit, for example, with a typical net length of three inches, the total length of the traces will be 900 inches. At 4pF/in, 50MHz, and a 5 volt swing, the total power dissipation will be:

$$\begin{aligned} P_{AC} &= 4\text{pF/inch} \times 900 \text{ inches} \times (5\text{V})^2 \times 50\text{MHz} \\ &= 4.5 \text{ watts} \end{aligned}$$

This same system, packaged in an MCM with interconnect lengths reduced by 70 percent will have a power dissipation of 1.35 watts.

If the PWB and MCM systems were both operated at 100MHz, the difference in power dissipation between them would be over six watts. This is significant in portable applications.

MCM TECHNOLOGIES

Popular Approaches

The technologies available to build MCMs have already been described. The building blocks are the die attach methods of wirebond, flip chip and TAB, and the substrate technologies of thick film ceramic, cofired ceramic, organic laminate and thin film multilayer materials. The outer form factors for modules span the range of peripherally leaded packages, PGAs, BGAs, daughter cards with connectors, and motherboards. Figure 12-29 summarizes these choices.

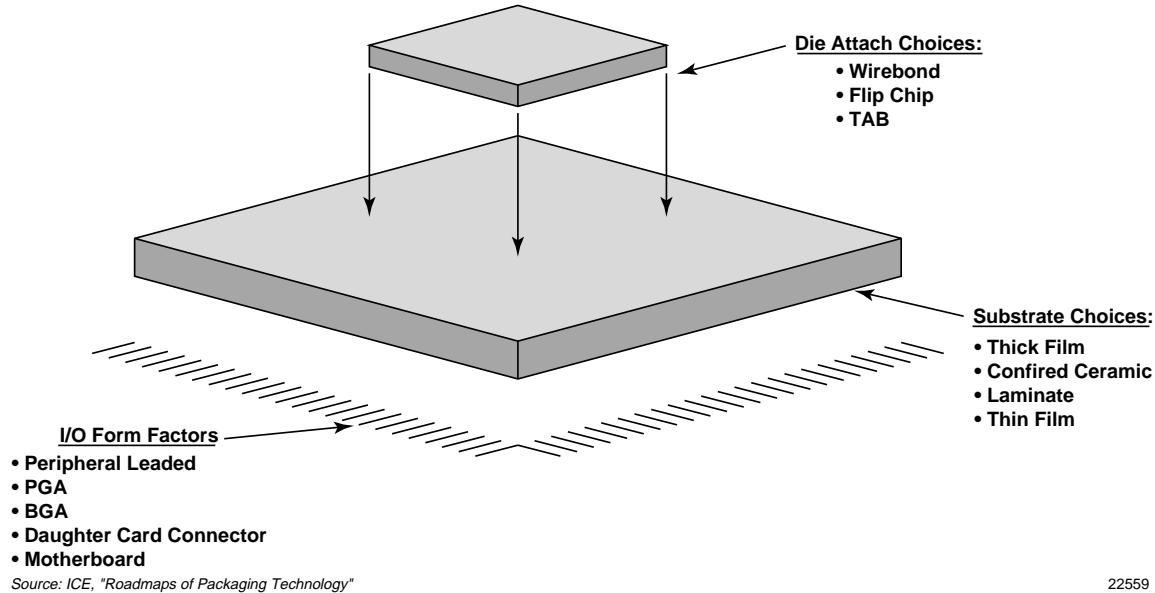


Figure 12-29. MCM Form Factor Options

There has been a tendency of associating the substrate choice with the type of MCM. The following classifications have been introduced by the IPC:

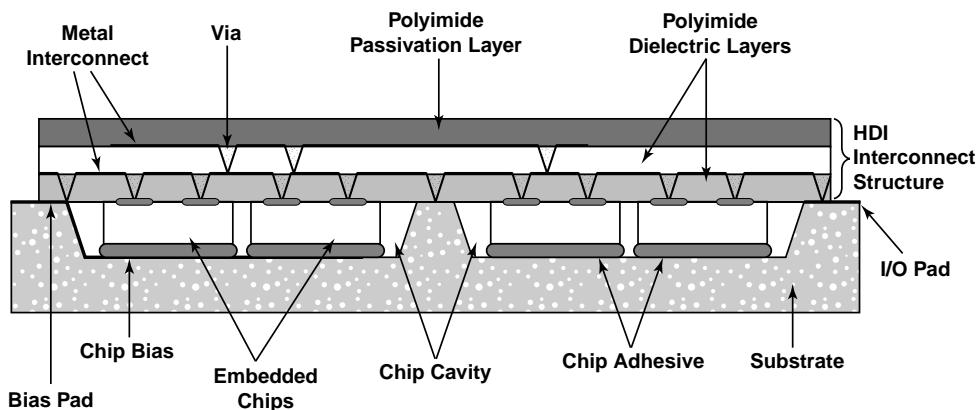
- MCM-L: using a laminate substrate such as FR4
- MCM-C: using a cofired ceramic substrate, either HTCC or LTCC, but not thick film
- MCM-D: using a thin film, multilayer, deposited substrate, with substrates of silicon, ceramic or aluminum
- MCM-C/D: using a multilayer cofired ceramic base with thin film built on top
- MCM-L/D: using a laminate base, with thin film built on top—sometimes referring to BUM substrates
- Silicon on silicon: using a silicon substrate and thin film multilayer interconnects

Because of the hype associated with the term MCM, many substrate vendors will advertise that they build MCMs, when in fact they fabricate cofired ceramic substrates, or just high density circuit boards or thick film substrates. The term MCM-L in particular is ambiguously used in the industry. It is generally associated with substrates that have finer features than conventional boards, typically at 5mil line and space or finer. However, there is no special distinction between the technology of an MCM-L substrate and a conventional laminate substrate. As BUM technology becomes more widely available, it will initially be used almost exclusively for bare die single chip or MCM applications, and subsequently migrate to conventional single chip package on board applications.

Chips First

There is another unique approach to fabricating MCMs in addition to those listed above. All traditional MCM designs take a previously fabricated substrate and attach chips to it as the last step. This is termed chips last. The alternative is to start with the chips first, and build the interconnects on top of them. The technique was pioneered by GE Corporate R&D. Though there have been a number of other attempts at commercializing the technique by TI, ISA and Polylithics, only GE currently provides merchant service in this area. Recently, the GE R&D group was acquired by Lockheed Martin, which is continuing the technology offering. The chips first technology also goes by the term HDI.

Figure 12-30 show a cross section of a completed chips first module. The starting point is a substrate that can be either an inert slab like ceramic, or a multilayer FR4 substrate with interconnects. Die are mounted on the substrate, active side up, and placed as closely together as possible. This can be achieved with virtually no gap. The die are adhesively attached to the substrate, with their active surfaces all on the same level to within 10 microns of each other.



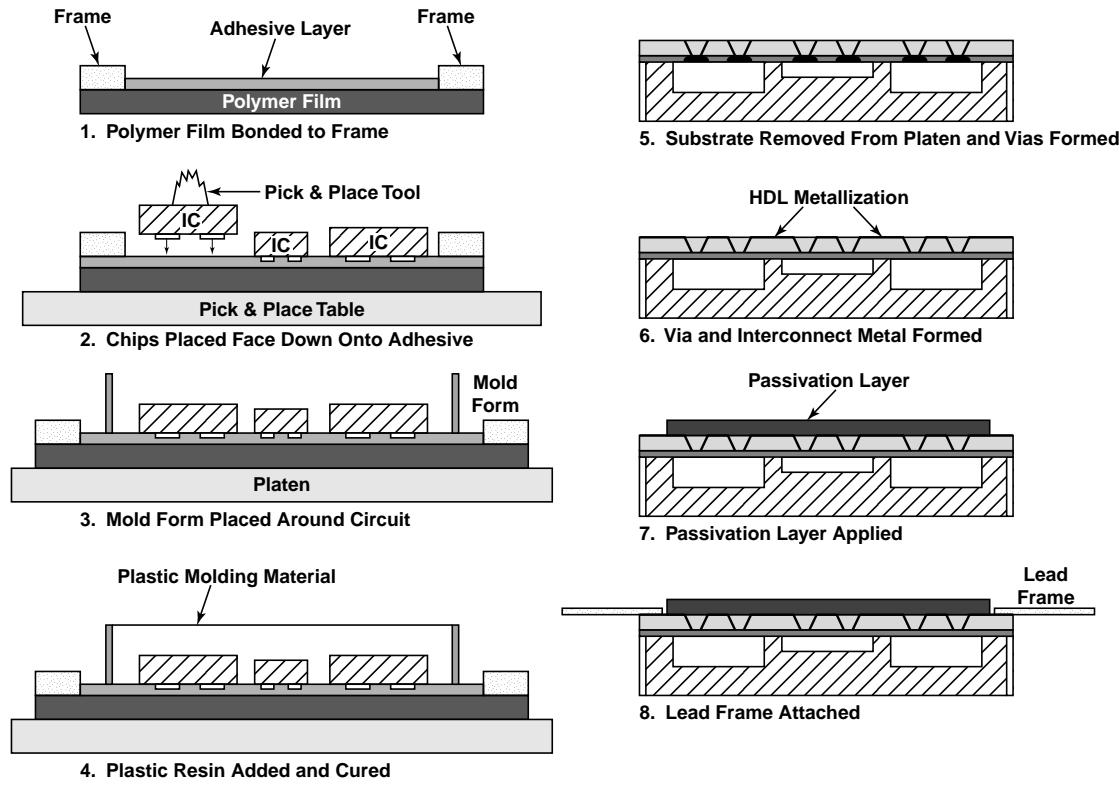
Source: GE-Lockheed Martin/ICE, "Roadmaps to Packaging Technology"

22018

Figure 12-30. HDI Chips First Module Cross Section

Alternatively, the die can be mounted pads down on an adhesive layer, and potted in place with a molding compound. The module can then be flipped over, with the top of the adhesive layer exposed. This is illustrated in Figure 12-31.

In either case, the top of the die now become the base substrate upon which the multilayer interconnect will be built up using a sequential process.



Source: GE-Lockheed Martin/ICE, "Roadmaps of Packaging Technology"

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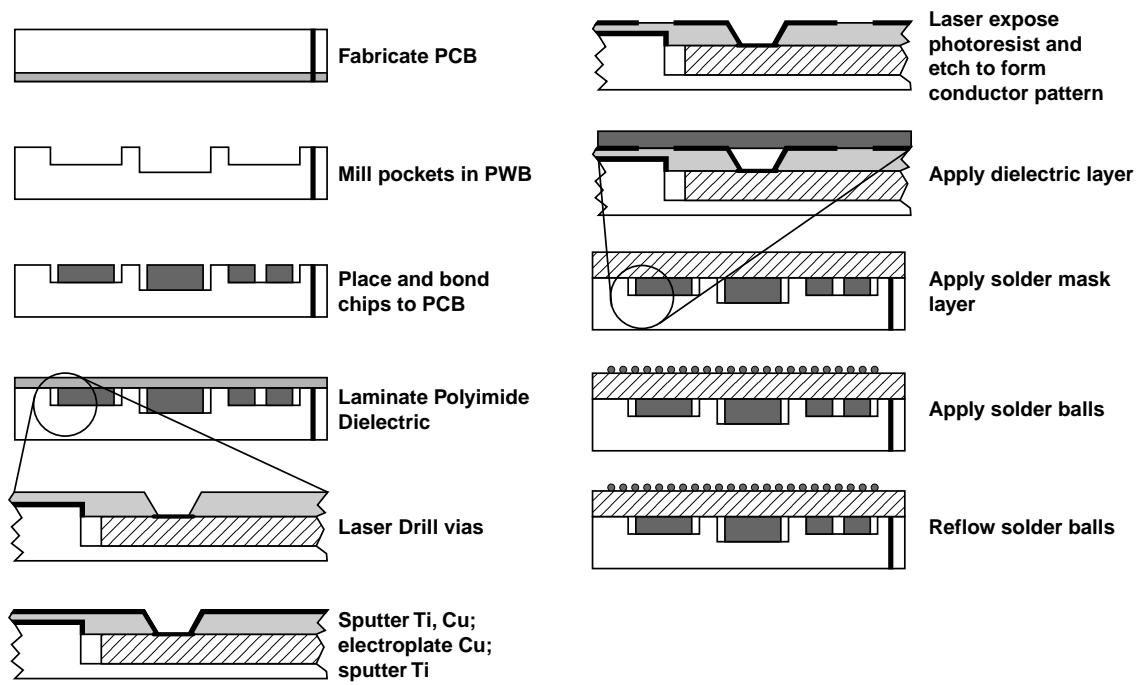
Figure 12-31. Plastic Encapsulated HDI Process Flow

Various approaches have been attempted to achieve a lowest cost process. A typical process is shown in Figure 12-32. Dielectric layers are laminated or spun on. A copper layer is sputtered on and via holes are opened up in photoresist. These holes are used as masks for laser drilling of the holes. The holes are then plated and traces patterned. A new dielectric layer is applied, and the process continues. Structures with up to five metal layers have been built. An example of the cross section of the interconnect is shown in Figure 12-33.

The top surface can be used for pads to either a peripheral leadframe, a pad grid array or a BGA. An example of a chips first module from TI with a BGA footprint is shown in Figure 12-34.

Chips first technology allows the highest packaging density, flip chip performance, no special preparation of the die before dicing and excellent opportunity for thermal management off the back side of the die. An example of a chips first Sparc Module fabricated on an aluminum nitride substrate is shown in Figure 12-35.

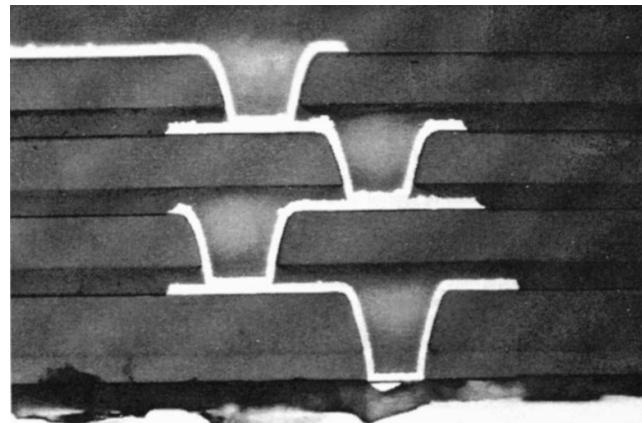
This technology truly is the re-integration of discrete die back into an integration level comparable to wafer scale integration.



Source: TI/ICE, "Roadmaps of Packaging Technology"

22017

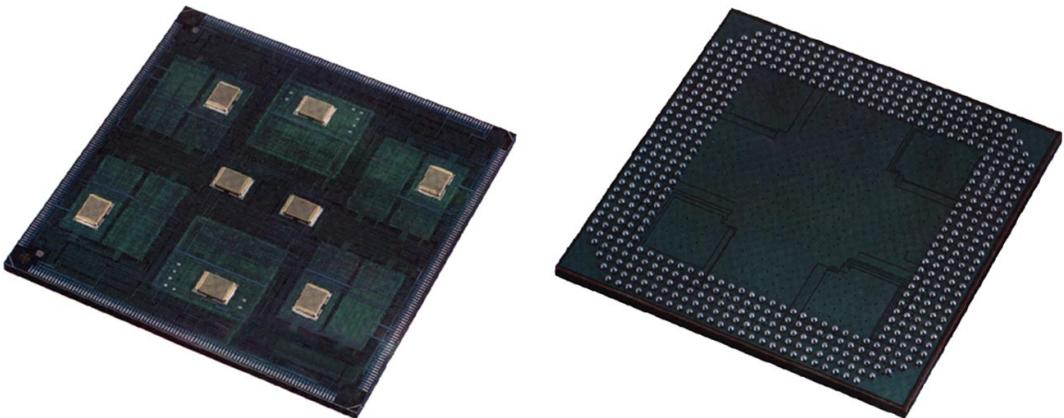
Figure 12-32. MCM HDI Process Flow



Source: GE Corp. R&D/ICE, "Roadmaps of Packaging Technology"

22202

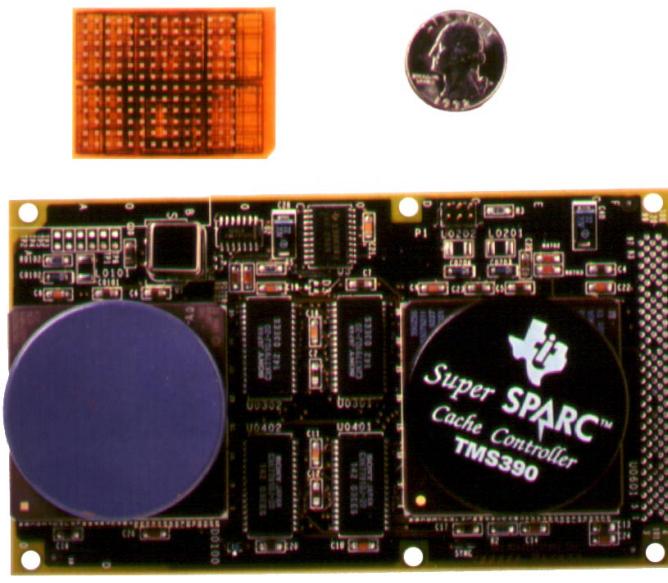
Figure 12-33. Cross Section of Multilaminated HDI Structure (1mil Vias)



Source: TI/ICE, "Roadmaps of Packaging Technology"

22049

Figure 12-34. Chip First Module with BGA Footprint



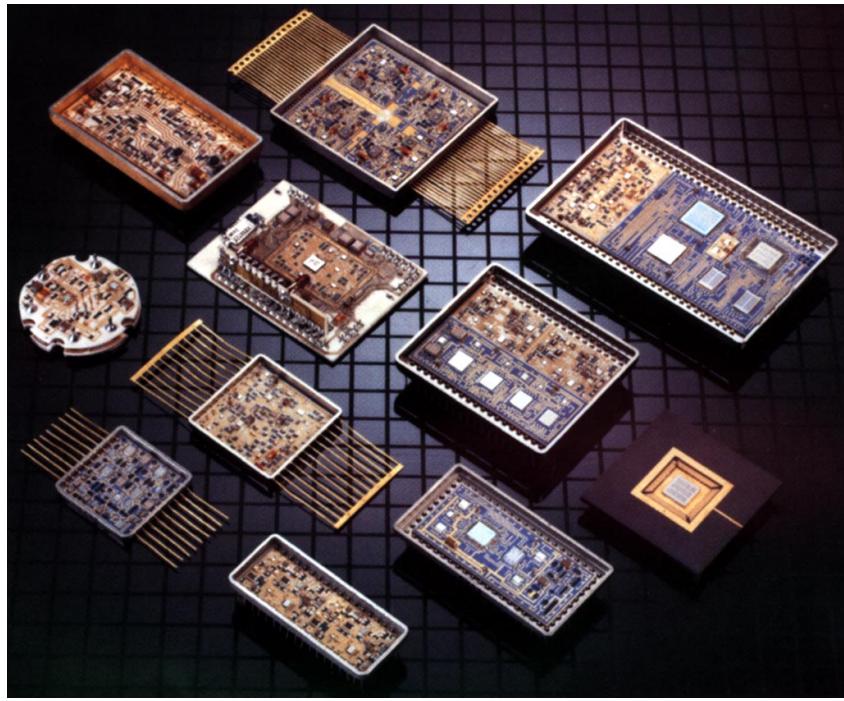
Courtesy of Sun/ICE, "Roadmaps of Packaging Technology"

22010

Figure 12-35. SuperSPARC Module in Conventional Form Factor and Integrated as a Chips First Module

Hybrids

The oldest MCM implementation is hybrids. They are traditionally low pin count die, mounted on thick film ceramic substrates, using gold wirebonding. The hybrid is typically hermetically sealed in a metal can with glass/Kovar feedthroughs. Some examples of typical hybrids are shown in Figure 12-36.



Source: AEROFLEX/ICE, "Roadmaps of Packaging Technology"

22040

Figure 12-36. Typical Thick Film Hybrids form Aeroflex

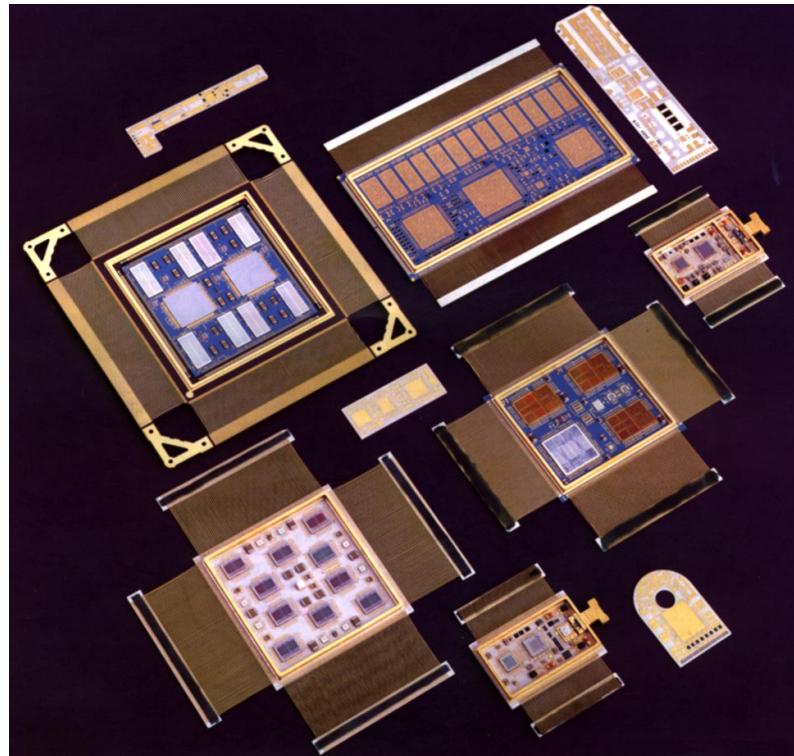
Hybrids have advanced and evolved considerably since these early days. The term is still generally associated with MCMs that use thick film substrates, but the level of complexity has increased. Figure 12-37 is an example of complex hybrids.

Many low end applications of MCMs that are not performance driven, but cost driven, use thick film hybrids. In cost sensitive applications, the die are small, the layer count is low and the die are commonly glob topped, and not hermetically sealed. The first digital watches used hybrid technology. An example of an early watch is shown in Figure 12-38.

A chief advantage of hybrid technology is that there is a well established infrastructure of small to medium sized companies experienced in the die acquisition, handling, wirebonding, assembly and fabrication of the thick film substrates. A single hybrid house can take complete responsibility for delivering a fully assembled and tested MCM. This is a strong factor in the vendor selection process.

Chip on Board

Chip on Board has also been around for a long time. It was largely enabled by the introduction of electronic grade polymers that can glob top encapsulate the die and protect them from the environment. An example of the glob top process for COB is shown in Figure 12-39.



Source: CTS Microelectronics/ICE, "Roadmaps of Packaging Technology"

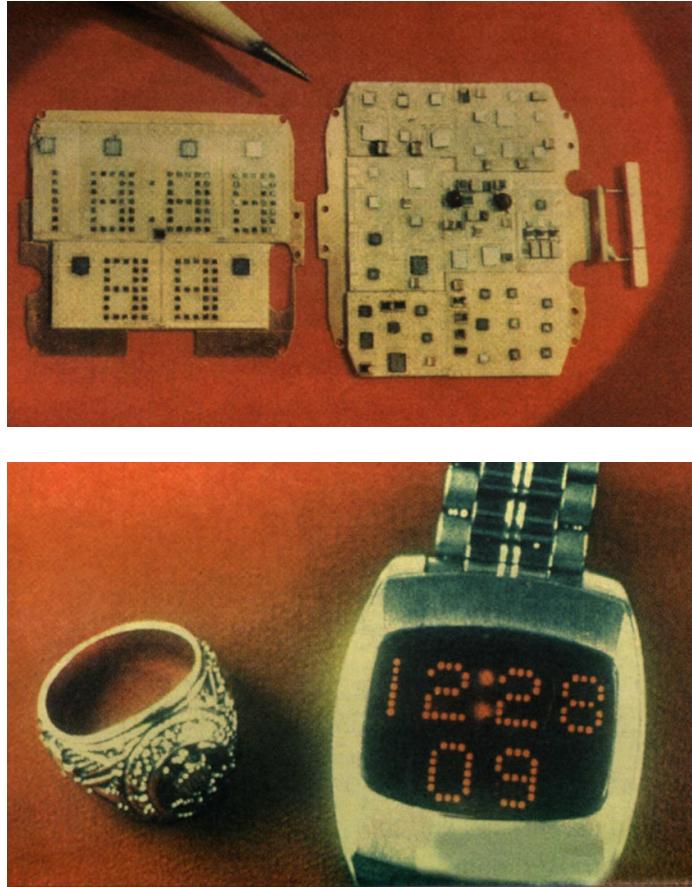
22039

Figure 12-37. High Density Thick Film Hybrids

COB uses a conventional circuit board: a substrate with gold typically on the pads. Features are typically on the order of 5mil lines and spaces, to give an effective pitch of 10mil to the die bonding pads. However, with memory, or smaller dice, courser features are often used.

The chief distinguishing feature of a COB design is that it contains a mix of conventional single chip packages and other discretes along with the bare dice. It is not cost effective to use a high density interconnect substrate technology for the entire board because most of the board area with conventional components is not able to take advantage of the enhanced performance.

After the other surface mount components are attached and wave or reflow soldered to the boards, the bare die are adhesively attached with silver filled epoxy. The chip pads are then aluminum wedge wirebonded to the pads on the board. The pitch can be as fine as 5mil lines and spaces. After test, the chips are encapsulated with a protective epoxy.



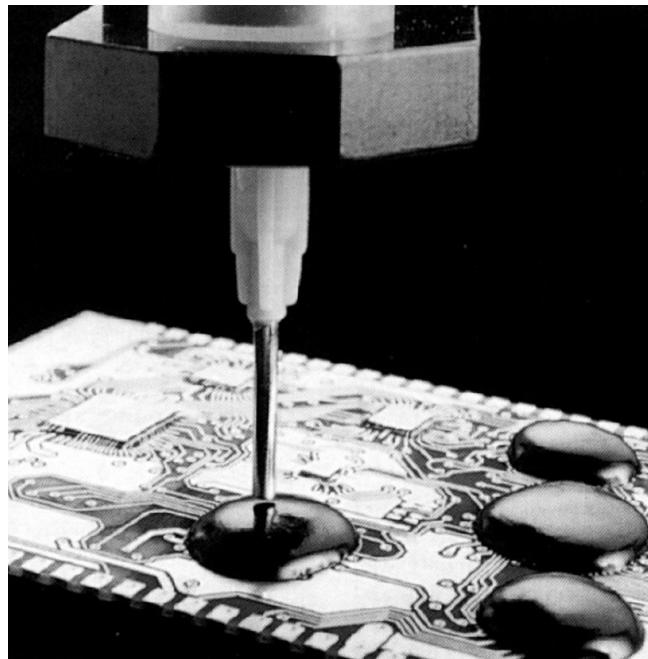
Source: Electronic Engineering Times/ICE, "Roadmaps of Packaging Technology"

22406

Figure 12-38. The First Digital Watch Using Hybrid Technology

Chip on board is used in cost sensitive applications, most commonly watches and consumer products, where size is a premium and there is value in eliminating a few of the packages. An example of the COB application for a hand held PDA is shown in Figure 12-40. The smallest handheld phones are partially enabled by the use of COB. Cellular phone applications, in particular, are strongly weight sensitive. The elimination of the package by the use of COB helps decrease the product weight. This is shown in Figures 12-41 and 12-42.

COB applications range in substrate size from large motherboards to small daughter cards. An example of three bare dice, mounted to the motherboard of a Poquet Computer is shown in Figure 12-43. This is a less common form factor.



Source: Dexter/ICE, "Roadmaps of Packaging Technology"

22013

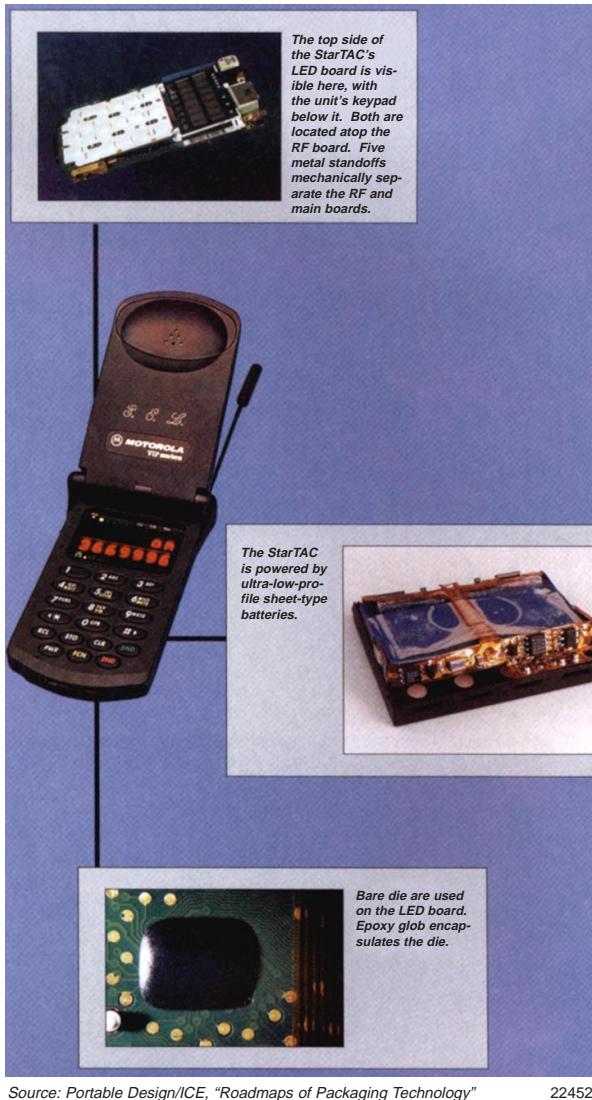
Figure 12-39. Liquid Epoxy Encapsulation of Bare Die



Courtesy of Franklin Electronic Publishing/ICE, "Roadmaps of Packaging Technology"

22014

Figure 12-40. Franklin's Handheld Databases with COB Dice

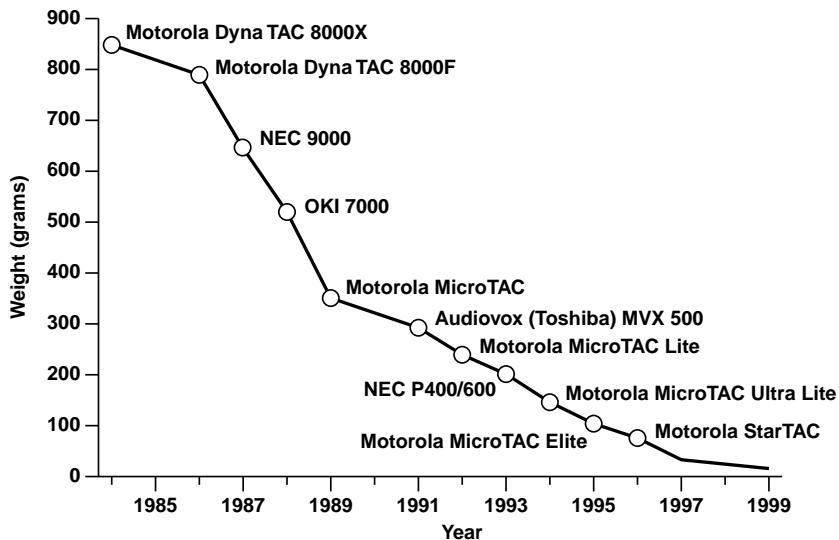


Source: Portable Design/ICE, "Roadmaps of Packaging Technology"

22452

Figure 12-41. Motorola StarTAC Cellular Phone

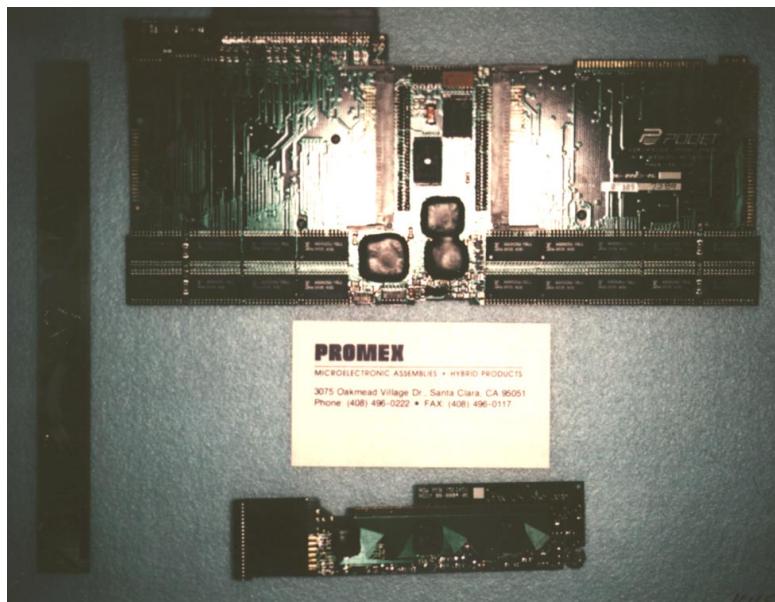
LSI Logic introduced their Ngine module as a daughter card with three bare dice mounted as COB. This module was a MIPS RISC processor module. Figure 12-44 is an example of the module. Two of the dice dissipate over 3 watts and required mounting on a heat spreader. After all the conventional components are mounted to the board, the die are attached and wirebonded to the pads on the substrate. The module is tested and if it passes, the chips are glob topped. If a bad die is found, it is removed and a new one placed.



Source: Herschel Shosteck/ICE, "Roadmaps of Packaging Technology"

22423

Figure 12-42. Weight is a Strong Driving Force for Cellular Phones

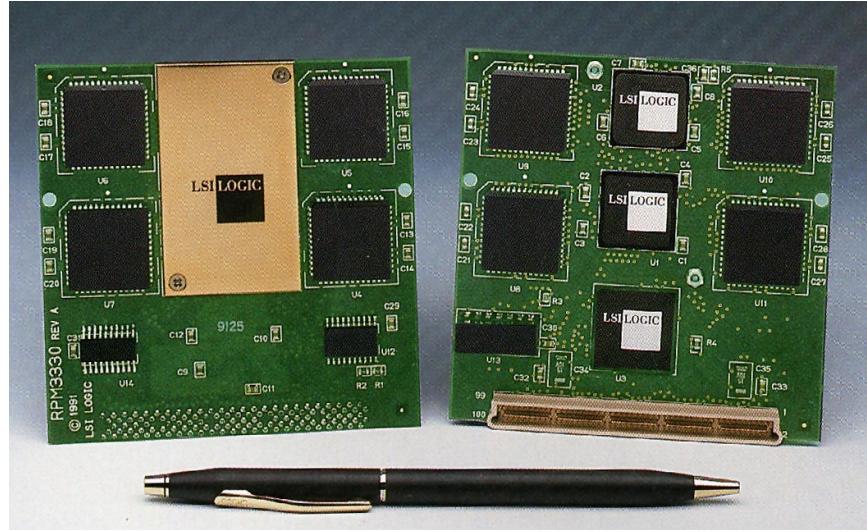


Source: Promex/ICE, "Roadmaps of Packaging Technology"

16115

Figure 12-43. The Poquet Computer Motherboard: COB, Through-Hole and Surface Mount

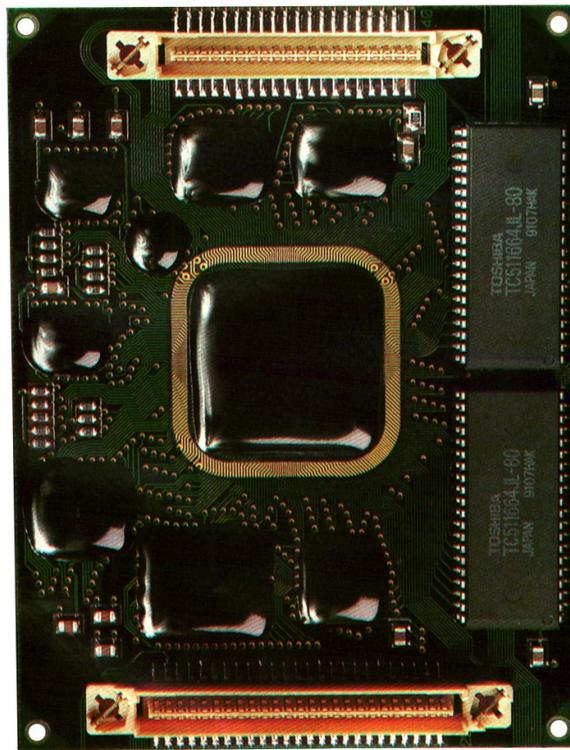
Typically, COB is used for small substrates, with a standard interface to the next level. A popular use for COB modules is embedded applications, such as laptops and PDAs, where a microprocessor and support chips are interconnected. Figure 12-45 is an example of a VGA subsystem for a laptop. The large chip in the center is an ASIC controller with various peripheral interface chips around it.



Source: LSI Logic/ICE, "Roadmaps of Packaging Technology"

22046

Figure 12-44. RPM3330 MIPS Nengine Module with Three COB Dice

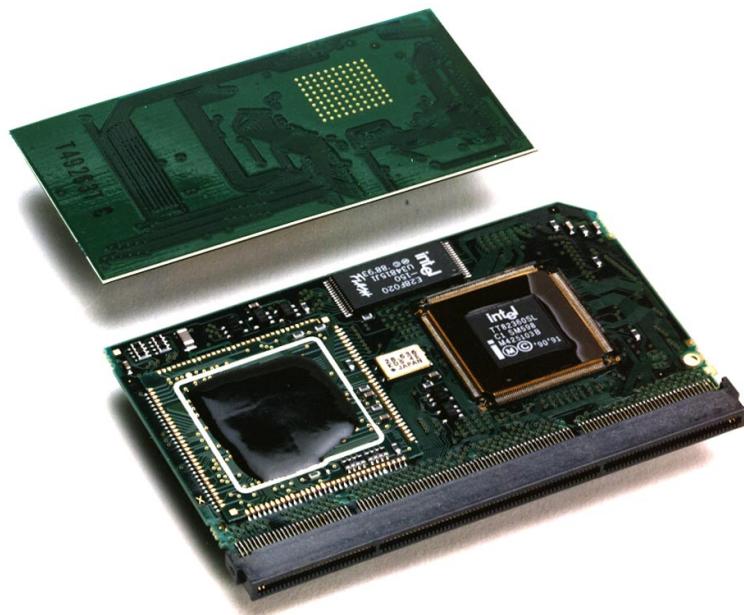


Source: Electronic Packaging & Production/
ICE, "Roadmaps of Packaging Technology"

22020

Figure 12-45. Complete VGA Subsystem with COB

The CARDIO format from S-MOS has been applied to a variety of portable computer applications. Examples are shown in Figure 12-46. Both COB and TAB on board are used, depending on the availability of the microprocessor. These cards use both the 386 and 486 processors. Figure 12-47 is an example of a CARDIO module mounted in a small handheld PDA.



Courtesy of S-MOS/ICE, "Roadmaps of Packaging Technology"

22007

Figure 12-46. CARDIO Module with COB and TAB on Board

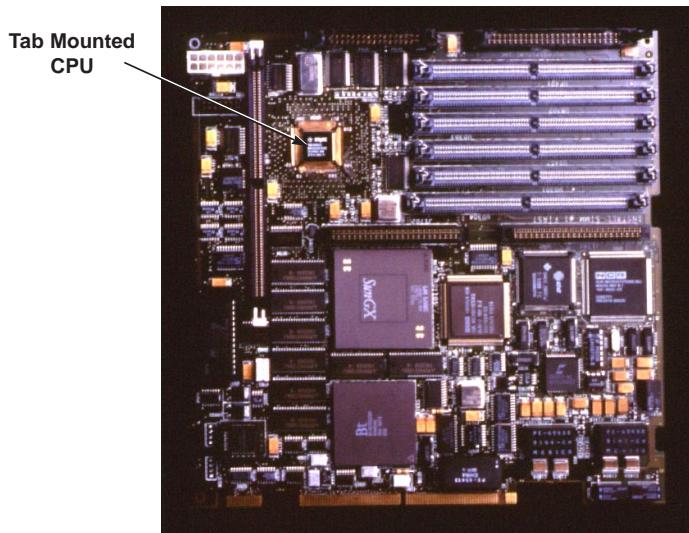


Source: S-MOS Systems/ICE, "Roadmaps of Packaging Technology"

22021

Figure 12-47. Melard "Ranger" Portable Workstation with S-MOS CARDIO Module

TAB on board is commonly used in the assembly of laptops off shore, but is not commonly used in the U.S. An exception is the motherboards used by Sun Microsystems for their low end MicroSparc workstations. An example of the motherboard with the CPU as TAB on board is shown in Figure 12-48.



Source: Sun Microsystem/
ICE, "Roadmaps of Packaging Technology"

22390

Figure 12-48. MicroSparc Motherboard Showing TAB-On-Board Processor

Two form factors have become popular in the last few years that take advantage of COB technologies, PC-Cards and Smart cards.

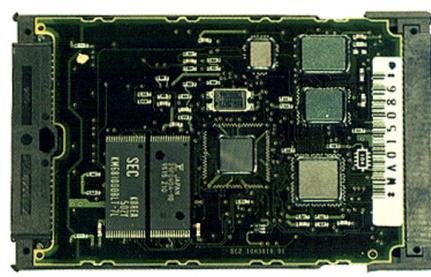
The PCMCIA (personal computer memory card international association) form factor was standardized originally for memory add-ons for small computers or hand held devices. It has since been renamed the PC-Card standard, reflecting its much broader uses. The PC-Card is used for solid state and hard drive memory, communications interfaces and embedded controllers. Though most of the units in production use individually packaged devices, there are examples with one or more bare die.

Figure 12-49 are examples of a PC-card communications products with one or more chips flip chip mounted to the laminate card and underfilled. This is usually referred to as direct chip attach or DCA. Figure 12-50 is another example of a PC card, with both COB and DCA.



**Small Module with Two
FC DCA Mounted Chips**

Source: IBM



**Wireless Modem PCMCIA Card with Five
DCA Chips**

Source: IBM

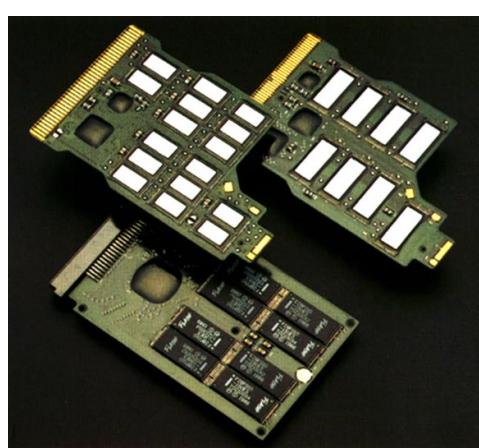


**PC-Card with Single
DCA Chip**

Source: Celestica

22578

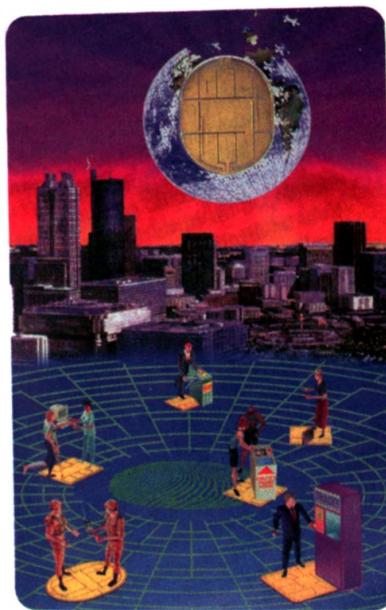
Figure 12-49. PC-Card Communications Products



Source: Ibiden/ICE, "Roadmaps of Packaging Technology" 22190

Figure 12-50. Memory Cards with COB and FC on Laminate Substrate

The smart card is a credit card sized module that has memory and microprocessor chips embedded inside. An example of a smart card used in the 1996 Summer Olympics in Atlanta is shown in Figure 12-51. The gold circle in the upper center of the card is the inserted module containing a microcontroller and memory chip, both as bare die, mounted on a section of double sided FR4 substrate. The gold pads on the bottom of the FR4 are for contacting the chips with a card reader. The small, thin module is inserted in a molded cavity in the card. This assembly operation is shown in Figure 12-52.



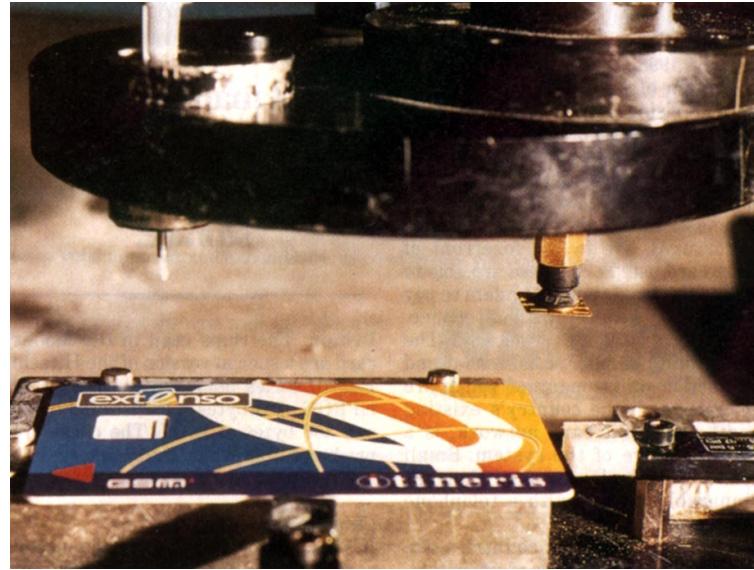
Source: *Scientific American/*
ICE, "Roadmaps of Packaging Technology"

Figure 12-51. Smart Card Used in the '96 Olympics

The applications for these cards range from "electronic money" to health databases to ID cards. The market estimated by Motorola for smart cards is \$800M, as shown in Figure 12-53. Another analysis projects a market size of double this estimate, to over \$1.8B by the year 2000, as shown in Figure 12-54.

Few Chip Modules: MCP

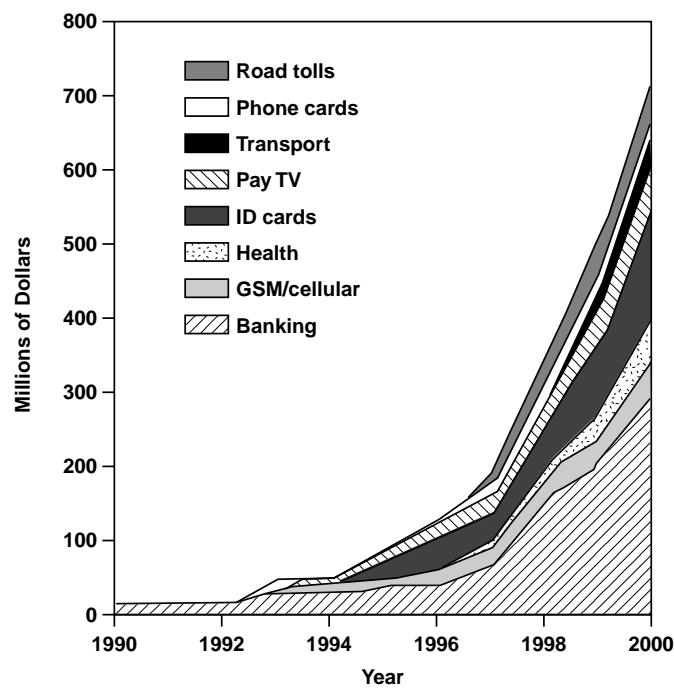
A new term has arisen to describe the potentially largest market segment for MCMs. This MCM has an outer form factor that is identical to an existing single chip package form factor. Since the body size is relatively small, not many chips will fit in the package. These modules have been called "few chip modules" or multichip packages (MCPs).



Source: Semiconductor International/ICE, "Roadmaps of Packaging Technology"

22051

Figure 12-52. Inserting a Smart Card Chip into a Card



Source: Motorola/ICE, "Roadmaps of Packaging Technology"

22016

Figure 12-53. Projected Market Opportunities for Smart Cards

Item	1989 (\$M)	1994 (\$M)	2000 (\$M)	Percent Annual Growth	
				94/89	00/94
U.S. Smart Card Products Demand	78	215	1,750	22.5	41.8
Transaction Processing	3	20	650	46.1	78.6
Automatic ID & Security	29	75	525	20.9	38.3
Communications	—	5	200	—	84.9
Health Care	—	5	75	—	57.0
Education & Institutional	2	15	50	49.6	22.2
Public Sector	43	85	200	14.6	15.3
Multifunctional & Other	1	10	50	58.5	30.8

Source: The Freedonia Group Inc./ICE, "Roadmaps of Packaging Technology"

22048

Figure 12-54. U.S. Markets for Smart Card Products

Importantly, MCPs are different from other MCMs. The use of a standard package format to house the MCM makes their use transparent to the end user and the assembly infrastructure. Once encapsulated, the user never needs to know whether there is one or many chips inside the package. It also makes it easier for the MCM vendor to offer standard products. There are millions of MCPs in production per month: Fujitsu alone ships 15 million units per month for laptop and PDA applications.

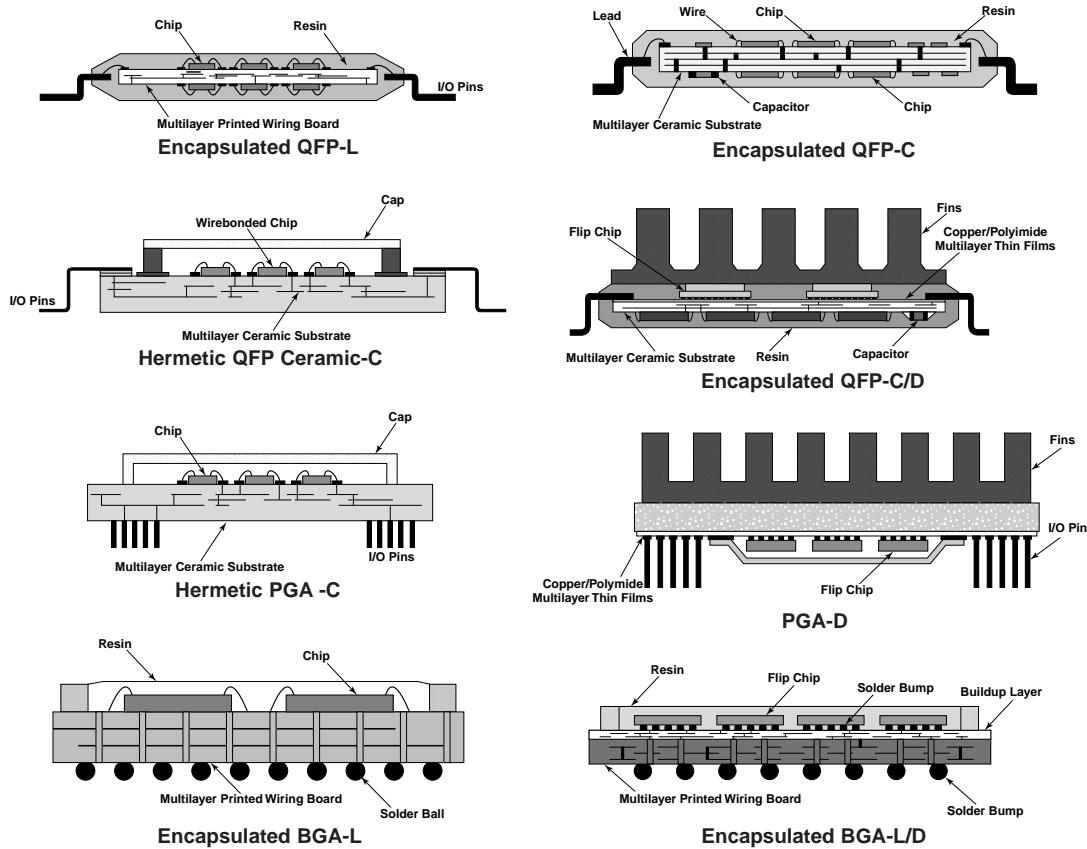
MCP output formats that are in volume production today include QFP, PGA and BGA. The substrates used on the inside include MCM-D, MCM-L and MCM-C. Die attach methods are wire-bond, flip chip and TAB. Completed modules have been fabricated and shipped in every possible combination of these technology choices. Figure 12-55 is a schematic demonstrating the various types of modules that are possible.

There are three application markets for MCPs—customized modules fabricated specific to a customer's requirements, standard memory modules and standard processor modules.

An early two chip MCM was fabricated by Hestia in the early 1990s from a conventional four layer FR4 board, shown in Figure 12-56. It used two bonding shelves for one die to reduce the need for fine lines. The leadframe was silver filled epoxy bonded to the peripheral pads on the substrate with an epoxy ring over the joint to provide mechanical strength.

An example of a power management unit for laptops from Appian Technology is shown in Figure 12-57. The four die are mounted as COB, with a PGA format on the bottom. When the epoxy lid is placed on top, it looks like a standard single chip PGA package.

AT&T shipped MCPs using their PolyHIC process. Built on a ceramic substrate, the metallization was thin film copper with a photo-imageable triazine as the dielectric. An example of an AT&T MCP is shown in Figure 12-58.



Source: Fujitsu/ICE, "Roadmaps of Packaging Technology"

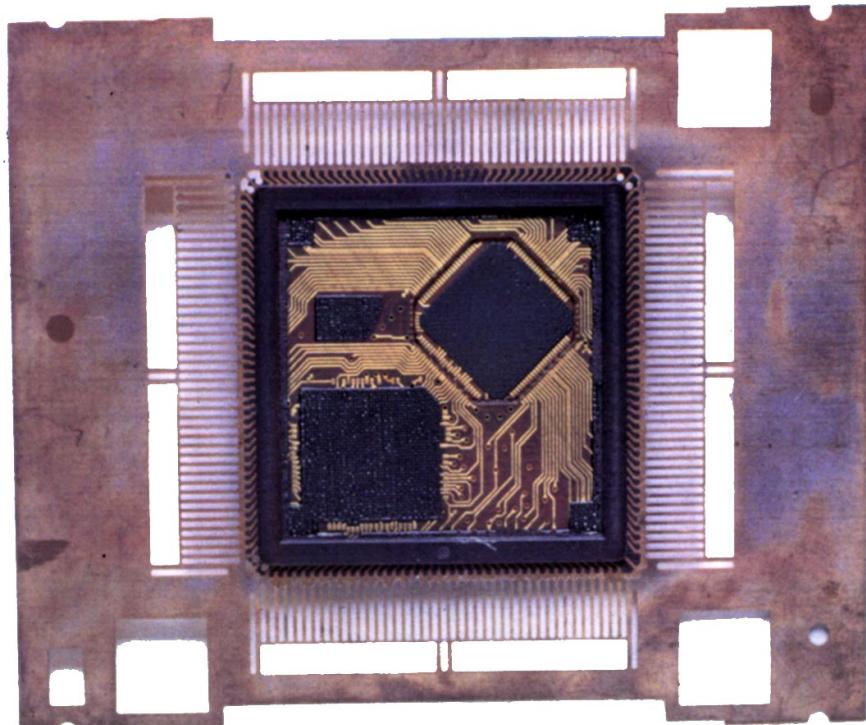
22579

Figure 12-55. Cross Sections of Various MCP Form Factors

An example of an MCP with flip chip die attach and a BGA footprint is shown in Figure 12-59. The two layer substrates are fabricated in panels, and the assembly operations are handled in strips. In this example, the die have area array eutectic solder balls. They are aligned and reflowed to the substrate, tested and underfilled. A cap is then molded over the die to provide mechanical and environmental protection. Finally, the solder balls are placed on the bottom side of the package and reflowed in place.

Fabricated in a similar manner, a wirebond BGA MCP is shown in Figure 12-60. The BGA footprint is becoming a popular format for MCPs.

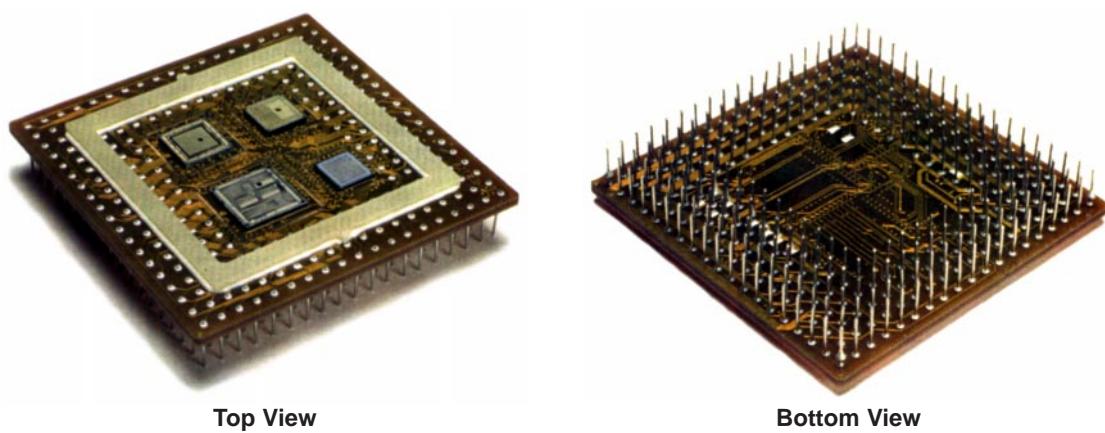
Another market segment for MCPs is the memory market. MMS has introduced their ChipFrame product line as a family of standard SRAM modules. The substrate is a four layer thin film on aluminum base, with the die wirebonded to the substrate and a leadframe silver filled epoxy attached to the perimeter. The entire module is then molded to look like a PQFP. Figure 12-61 is an example of the substrate with the devices bonded, before leadframe attach and molding.



Source: Hestia/ICE, "Roadmaps of Packaging Technology"

22054

Figure 12-56. Low Cost Two Chip Module With PQFP Form Factor



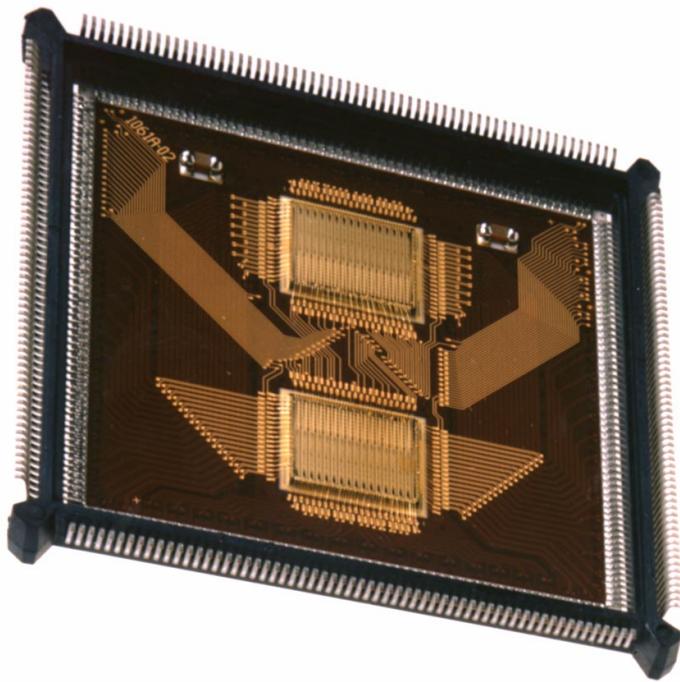
Top View

Bottom View

Source: Appian Technology/ICE, "Roadmaps of Packaging Technology"

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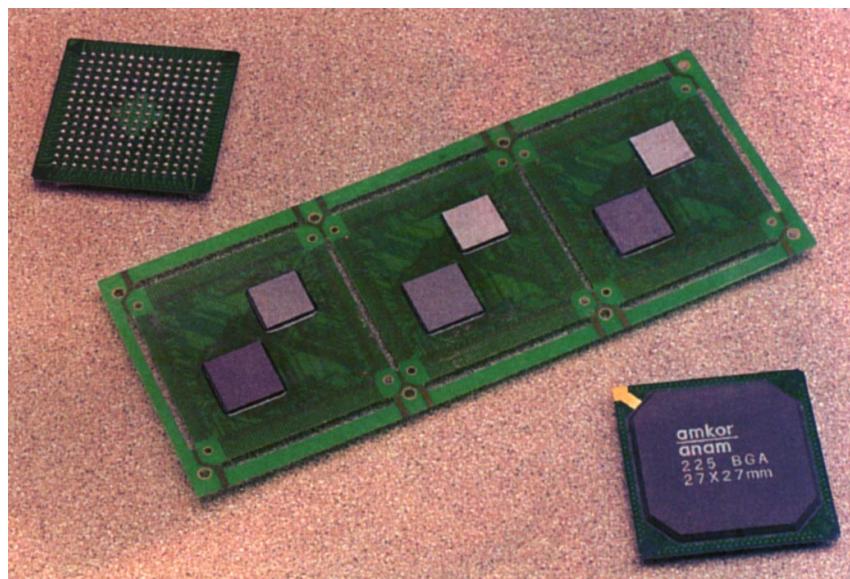
Figure 12-57. Power Controller for Laptops



Courtesy of AT&T Network Systems
Source: ICE, "Roadmaps of Packaging Technology"

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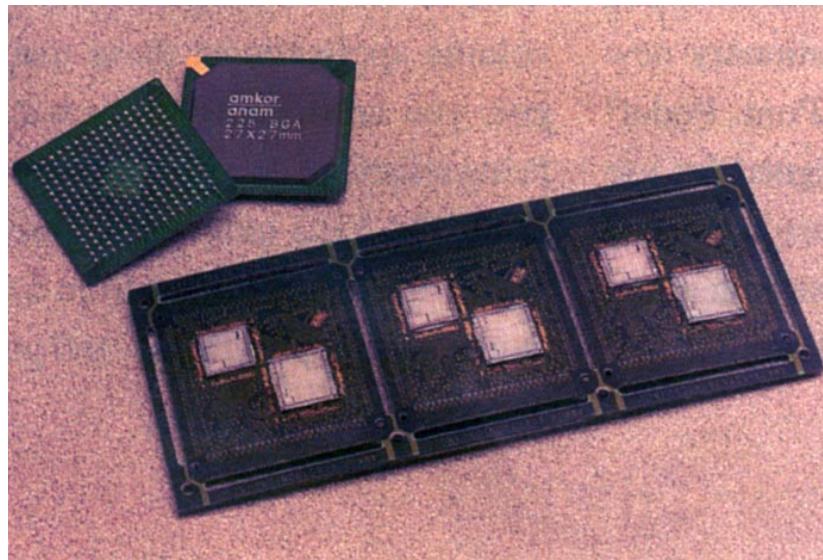
Figure 12-58. AT&T's PolyHIC MCM



Source: Amkor/ICE, "Roadmaps of Packaging Technology"

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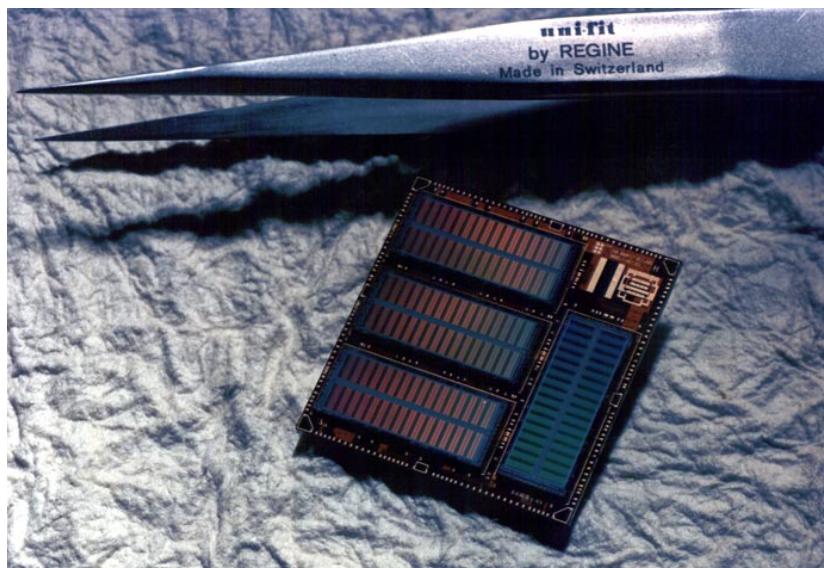
Figure 12-59. FC-DCA with PBGA Form Factor



Source: Amkor/ICE, "Roadmaps of Packaging Technology"

22028

Figure 12-60. COB MCM with PBGA From Factor



Source: MMS/ICE, "Roadmaps of Packaging Technology"

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Figure 12-61. ChipFrame Module Before Leadframe Attach and Encapsulation

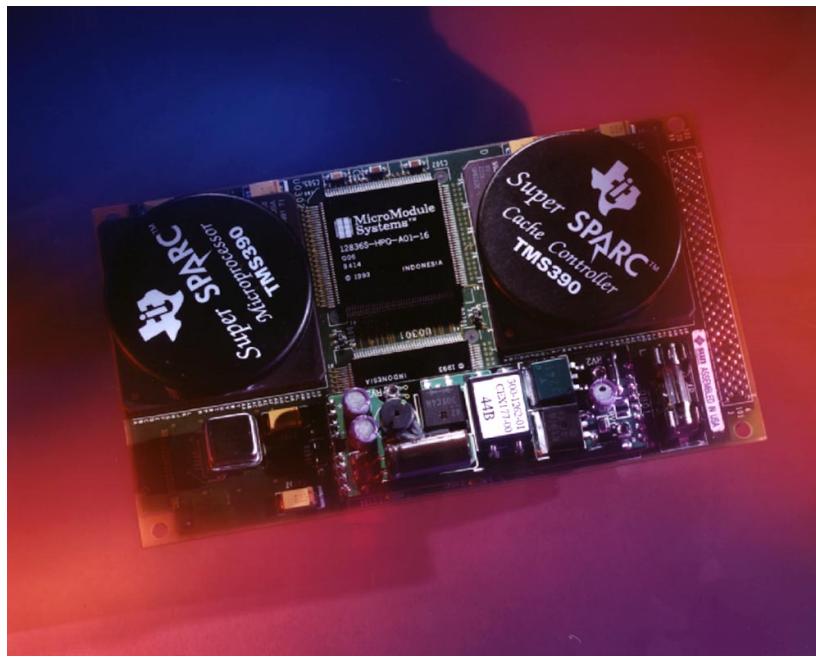
An example of this four chip memory module is shown in Figure 12-62 after leadframe attach and molding. These modules are used in the Sun Microsystems SuperSparc Xbus modules to provide 2Mbytes of cache SRAM on each processor card. An example of the Super Sparc module is shown in Figure 12-63. There are two ChipFrame MCPs on each side of the card. This was the very first MCM shipped by Sun Microsystems in a volume application.



Courtesy of MicroModule Systems/Source: ICE, "Roadmaps of Packaging Technology"

22056

Figure 12-62. ChipFrame Package Consisting of Four SRAM Chips



Courtesy of MMS/Source: ICE, "Roadmaps of Packaging Technology"

22055

Figure 12-63. Four ChipFrame Packages Mounted on a 2 Megabyte SuperSPARC Module

One of the early focuses of MCMs was for microprocessors. Processor modules remain an important market segment. Both RISC and x86 based processors are shipped in MCP formats. Unisys has used MCP modules for processors and memory before they were called MCPs. An example of a family of cofired ceramic MCPs is shown in Figure 12-64, composed of an ASIC and its memory.

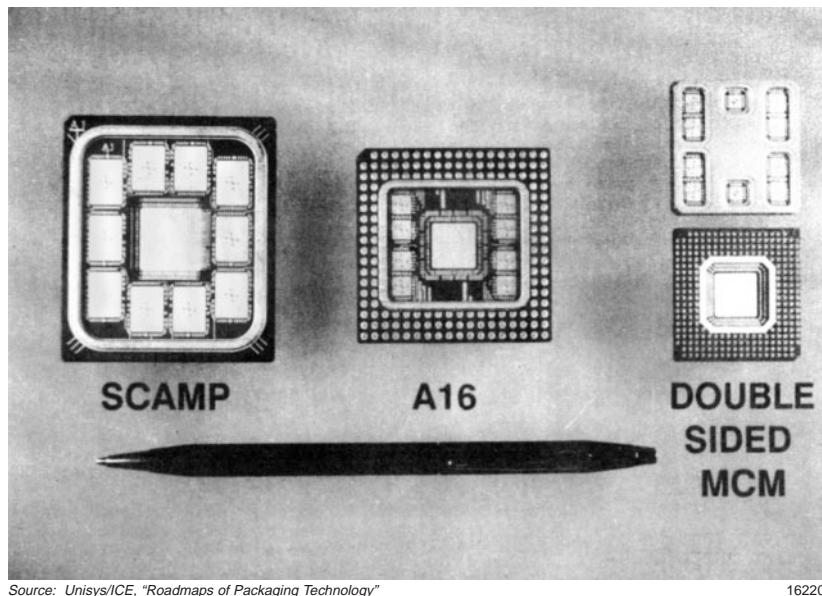
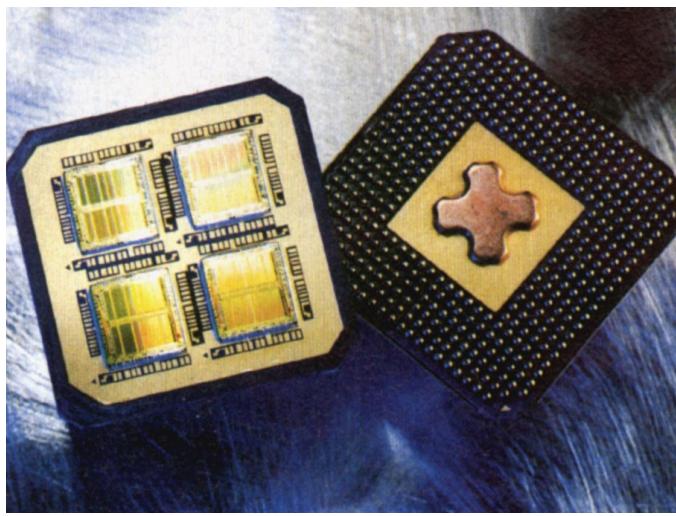


Figure 12-64. Cofired Ceramic Multichip Modules From Unisys

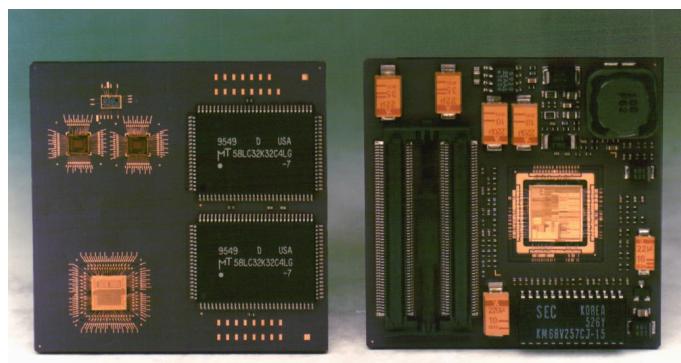
Motorola began shipping dual processor 88110 modules with two processors and on board SRAM cache in 1993, packaged in a ceramic BGA module. An example is shown in Figure 12-65.



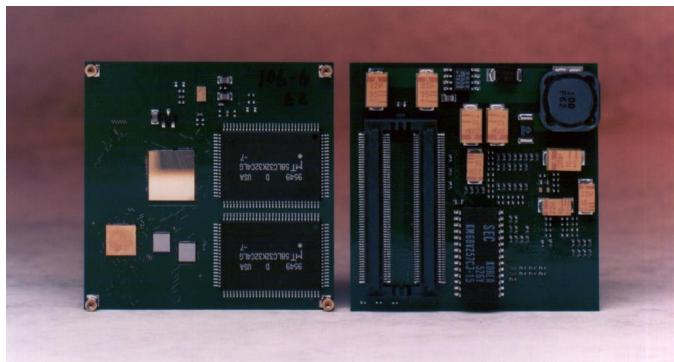
Source: Motorola/ICE, "Roadmaps of Packaging" 22058

Figure 12-65. Dual 88110 Processor Modules in Ceramic BGA

Fujitsu has offered Pentium modules for notebook applications in both ceramic and laminate configurations. An example of each version is shown in Figure 12-66. The laminate version uses flip chip attach with Fujitsu's BIT assembly process, described in Chapter 9. To implement this approach required the use of BUM technology in the laminate substrate. In order to get to market quickly, before the BUM technology was released to manufacture, a ceramic version of the module was built and shipped. Die were wirebonded on both sides. Both versions of the module are currently in production.



MCM-C Upgradable System for Pentium-Based Notebooks



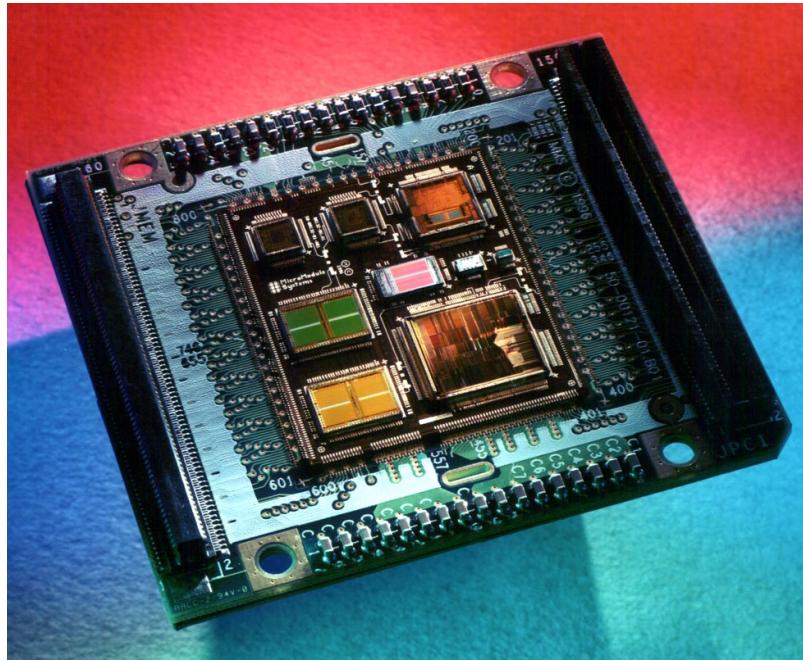
MCM-L Upgradable System for Pentium-Based Notebooks

Source: Fujitsu/ICE, "Roadmaps of Packaging Technology"

22580

Figure 12-66. Pentium Modules From Fujitsu

MMS has been shipping their Spectrum series of CPU modules since 1994. An example of the Gemini CPU module consisting of a Pentium processor, with power management chip set, 256K of L2 cache, Tag SRAM and temperature sensor, is shown in Figure 12-67. The substrate is the MMS multilayer thin film substrate on an aluminum base. It is mounted and wirebonded to an FR4 frame to connect to a surface mount connector. After assembly, a lid is sealed over the top of the thin film module. With a metal base, the thermal management is excellent. From junction to case, the thermal resistance is only 1.2°C/watt.



Courtesy of MicroModule Systems/ICE, "Roadmaps of Packaging Technology"

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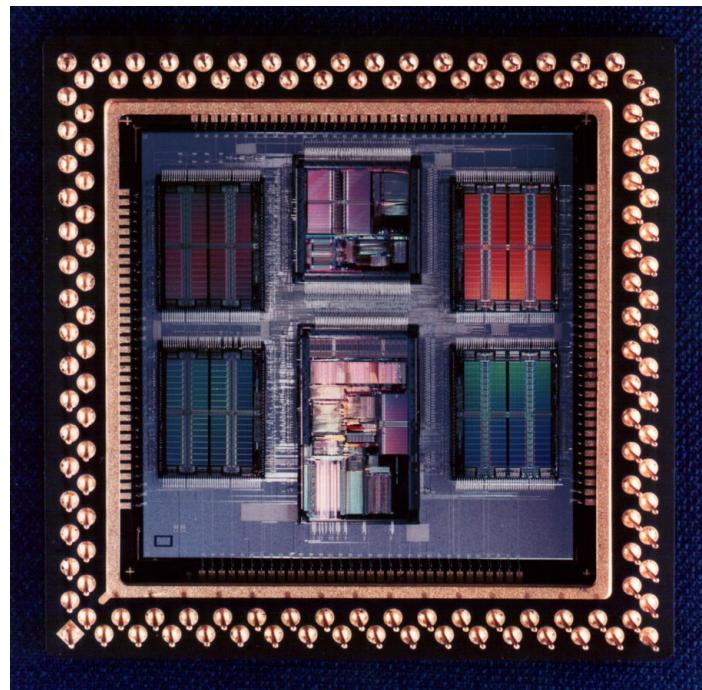
Figure 12-67. MMS Spectrum CPU Family Gemini Notebook CPU Module

Ross Technologies has been shipping Sparc modules in MCP packages into laptops since 1992, and into Sun workstations and others since 1994. An example of their module, containing a SuperSparc processor, a memory management unit and four SRAMs is shown in Figure 12-68. The substrate is a thin film, aluminum/SiO₂ (on silicon) substrate from nCHIP, mounted in a cofired ceramic package, with a PGA footprint. This small form factor allows a dual processor to fit on one Mbus module. The first units were used in tadpole laptops, as previously described.

Advanced version of this MCP use flip chip die attach, and under filling, on a thin film substrate. An example is shown in Figure 12-69. Above about 100MHz, the clock frequency is improved by the use of the MCP over the conventional single chip package. Modules from Ross operate above 166MHz with the fastest die.

As part of Sun's evaluation effort, other technologies were used to fabricate the same SuperSparc chip set in an MCP. Figure 12-70 is an example of a cofired ceramic version fabricated by Alcoa Microelectronics, showing the composite pieces and the assembled MCP.

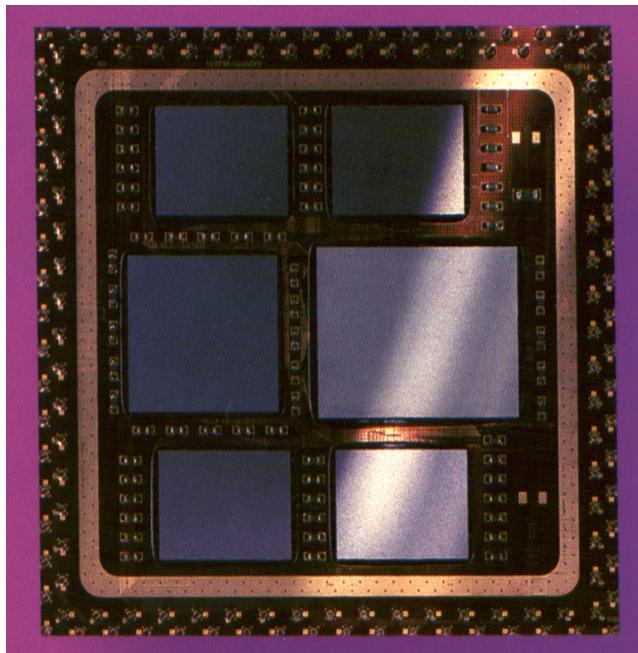
IBM has recently offered their cofired ceramics technology as an alternative for MCP modules. Their MCP modules use a multilayer cofired ceramic base, with layers of copper/polyimide thin film on top. The die are most commonly flip chip attached. The footprint out the bottom is a PGA, though BGA is also offered. An example of the module is shown in Figure 12-71.



Courtesy of nChip/ICE, "Roadmaps of Packaging Technology"

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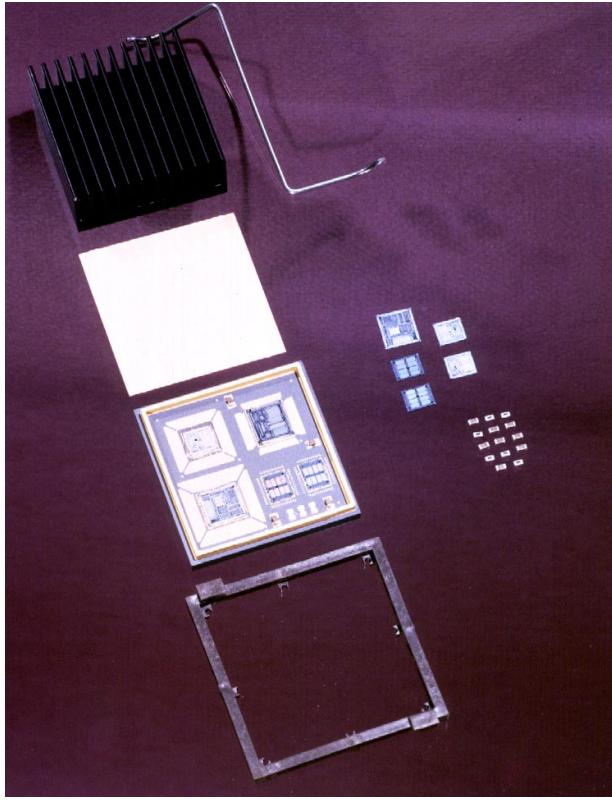
Figure 12-68. Ross hyperSPARC™ Module With Wirebonded Die on a Chip Substrate



Source: ROSS Technology/ICE, "Roadmaps of Packaging Technology"

22032

Figure 12-69. Ross hyperSPARC™ Module With FC on Thin Film



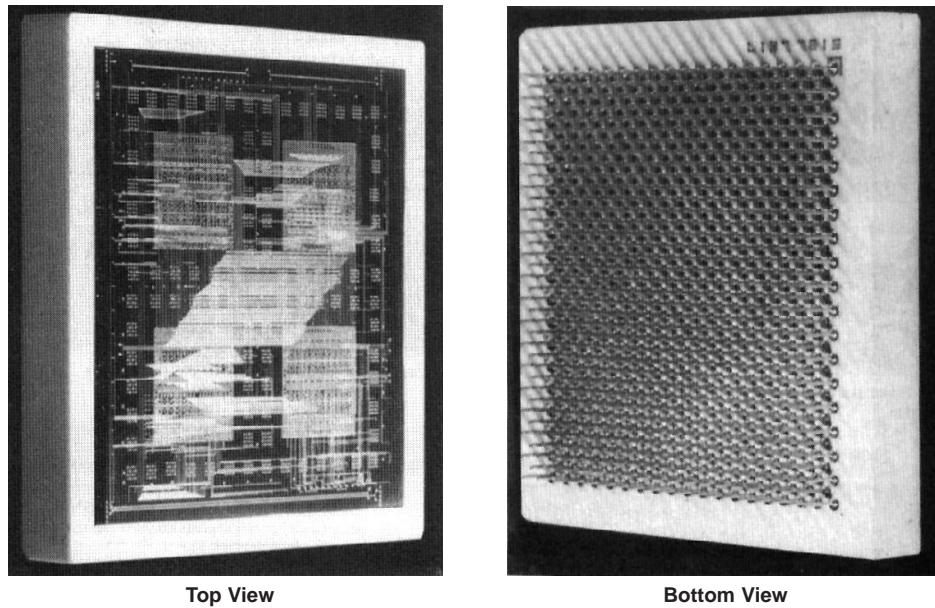
Source: Alcoa Microelectronics/ICE, "Roadmaps of Packaging Technology" 22038

Figure 12-70. Cofired Ceramic Version of SuperSPARC Chip Set Showing the Components Before Assembly

One of the more advanced MCP modules is used by HAL Computers as their CPU module. It is a thin film substrate with polyimide and copper metallization, built on cofired ceramic with flip chip die attach. The chips are bonded using Fujitsu's BIT process. A heatsink is attached to the back of the substrate to draw the heat out, and the ceramic module has a PGA form factor that plugs into a motherboard. An example of this MCP is shown in Figure 12-72.

High End CPU Modules

At the high end of the MCM spectrum is the largest and most complex MCMs that resemble daughter cards in size. These have traditionally been used for the CPU of mainframes and supercomputers. The IBM 3081 and 9000 are of this generation. These modules typically require the highest interconnect densities. An example of the cross section of the IBM 9000 module with 61 layers of low temperature cofired ceramic topped with one layer of thin film, polyimide, with flip chip on top is shown in Figure 12-73.



Source: IEEE Transactions on Components, Packaging, Applications and Processes
for High Performance Packaging/ICE, "Roadmaps of Packaging Technology"

22508

Figure 12-71. IBM MCM

Another example of a high end MCM is shown in Figure 12-74. It is a flight control processor used in space flight applications. It is 2 inches x 4 inches, mounted in a cofired aluminum nitride package, with 442 peripheral leads. The substrate is nCHIP's thin film aluminum SiO_2 on silicon, and the die are wirebonded.

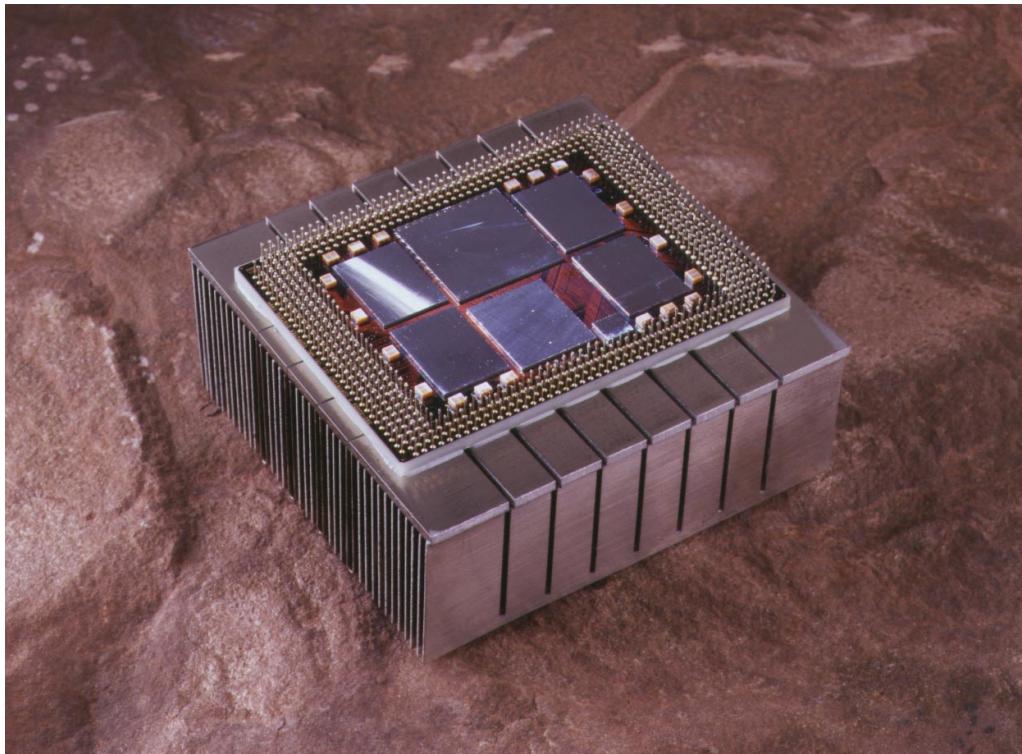
All high end MCMs use either thin film multilayer or a combination of thin film on top of cofired ceramic, because of the higher interconnect densities required for a larger number of die, each with a large pin count.

WHICH MCM TECHNOLOGY IS THE RIGHT ONE?

Why are there so many MCM options to choose from? The answer is that each small variation, from each different vendor has a different cost-performance-risk-schedule trade-off for the combination of application, chip supplier, chip assembler, substrate fabricator, module assembler and end user.

Price is a strong component in the substrate selection process. There is a general price distinction among the three popular approaches of laminate, cofired ceramic and thin film. Raytheon conducted a study comparing the quoted prices to fabricate a substrate to accommodate 19 chips and 53 passives with 529 I/O in a PGA footprint. The module, when fabricated in MCM-L, was 18 layers and 6.6cm x 6.6cm. The results of the price survey are shown in Figure 12-75. MCM-L was

chosen because of its lower cost. This price trend is indicative of the relative pricing for the substrate technologies: MCM-D will be more expensive than a comparable MCM-C substrate, which is more expensive than an equivalent MCM-L substrate.



Courtesy of Hal Computers/ICE, "Roadmaps of Packaging Technology"

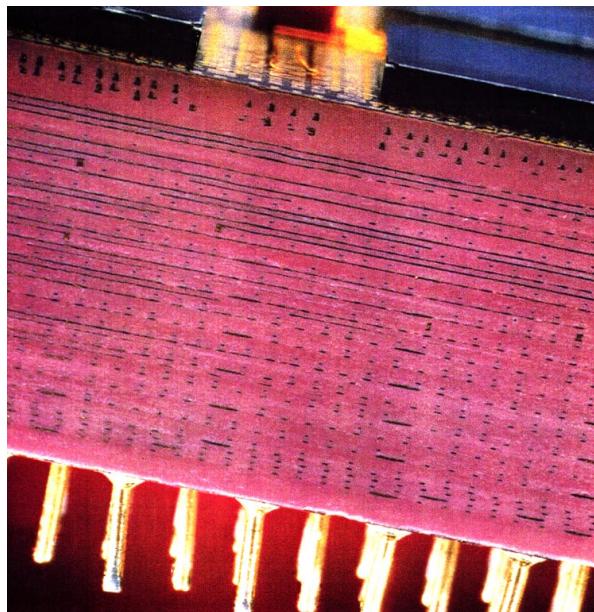
22201

Figure 12-72. CPU Module of HAL Computer with FC on Thin Film

In addition to basic substrate price, each of the MCM families reviewed above will have slightly different weighing factors for the other important factors for the substrate technologies of: thick film, conventional laminate, BUM, cofired ceramic (both HTCC and LTCC), and thin film, as well as combinations such as MCM-D/C and MCM D/L.

For hermetic hybrids, thick film will continue to be used. As LTCC becomes more popular, and the capability is more commonly found, some of the higher layer count thick film designs will be switched over to LTCC. For non hermetic hybrids, thick film ceramic and conventional laminate will be candidates for the substrates. As the layer count increases above four, laminate and LTCC will become lower cost candidate technologies than thick film.

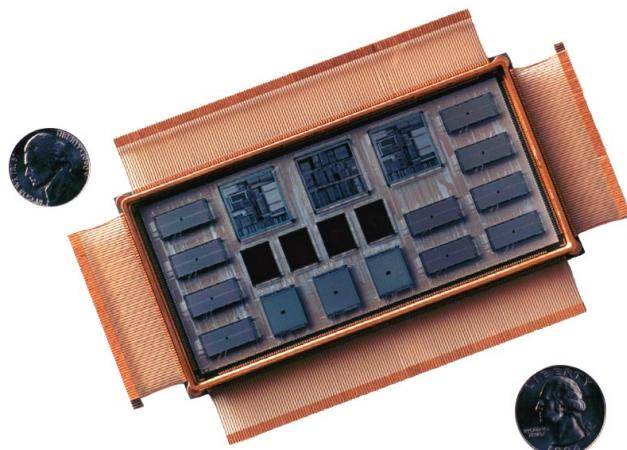
For COB, conventional laminate technology will be the substrate of choice. This is driven by cost. When conventional laminate is not able to meet the interconnect needs, the choices will be opened up to BUM.



Source: IBM/ICE, "Roadmaps of Packaging Technology"

22392

Figure 12-73. Cross Section of 52 Layer Cordierite Substrate With 1 Layer Thin Film-Polyimide on Top



Courtesy of nChip/ICE, "Roadmaps of Packaging Technology"

22036

Figure 12-74. Space Flight Computer Module Designed Jointly by TRW and JPL and Built by nCHIP

For MCPs, all four technologies are viable candidates. Two parameters will determine if a substrate can meet the interconnect needs, the via density and the interconnect density. Among the substrate technologies, there are multiple choices between thin film, cofired ceramic and BUM, in being able to provide the via densities needed for all forms of bare dice. Each of these technologies allow microvias. Figure 12-76 illustrates the via densities available for different via pitches and the requirements needed for packaged, wirebonded and flip chip devices just for pad escapes.

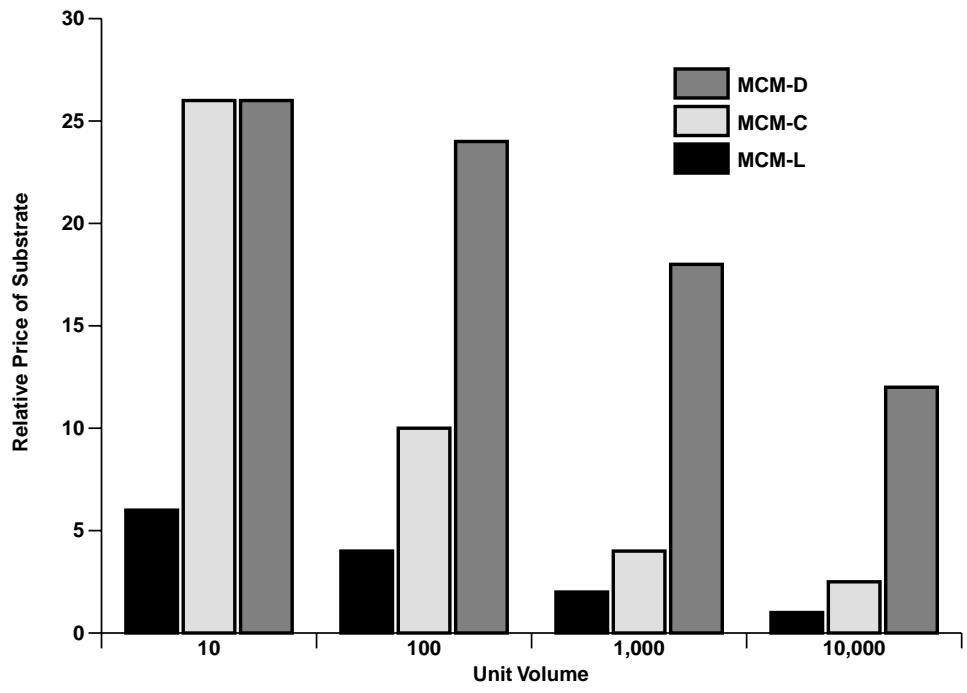


Figure 12-75. Relative Prices for the Same Module in Three Substrate Technologies

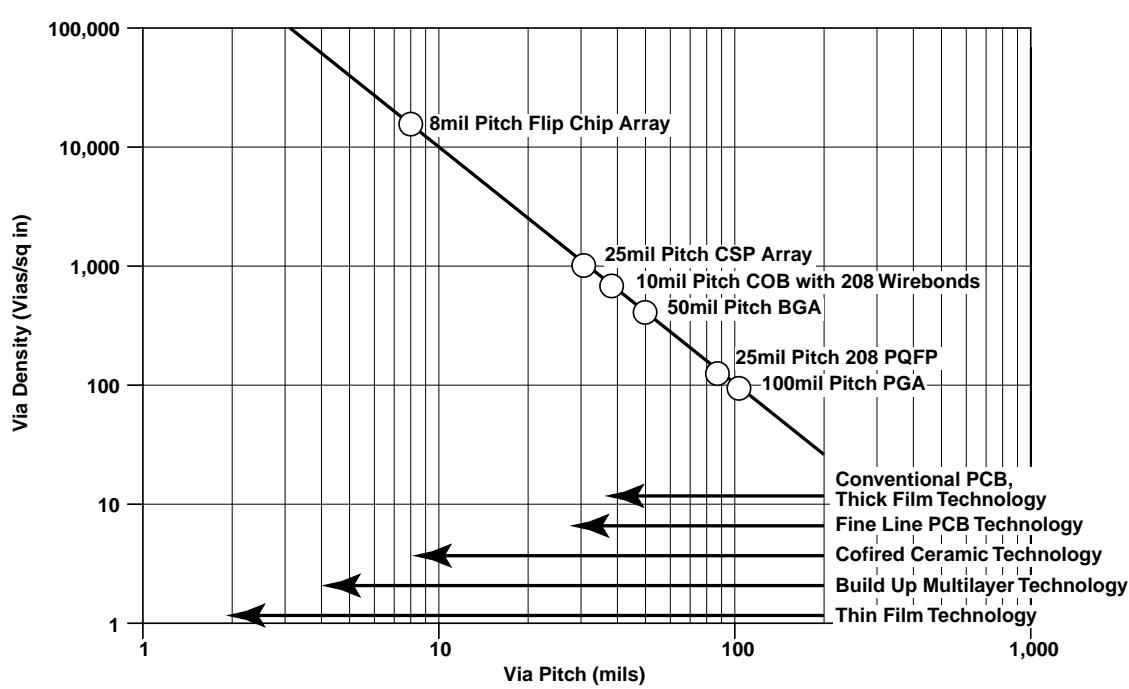


Figure 12-76. Via Density Needs and Capabilities

Conventional mechanically drilled vias at 30mil centers would not be able to handle the tight pitches required for high pin count flip chip. However, for many applications of COB and wire-bonded devices, it is perfectly adequate.

The interconnect density available is determined by the linewidth. In cofired ceramic, both HTCC and LTCC, this is limited by the screen printing process to about 8mil centers. For BUM, this is a moving target, and the distinction between BUM and thin film begins to blur below 2mil pitch. For most MCPs, the interconnect density with BUM, cofired and thin film is adequate, and each of these are candidate substrates.

For the high end MCM, where extremely high interconnect densities are required, mixed technology substrates of cofired ceramic with thin film on top, or BUM with thin film on top, or just thin film alone are the candidate substrates.

However, what the end user buys is more than just MCM substrates at some price. It is a complete module, with a delivery schedule at some degree of risk to consider. Determining the right balance of risk and reward, dollar price, and schedule/price is a very personal decision, with many right answers.

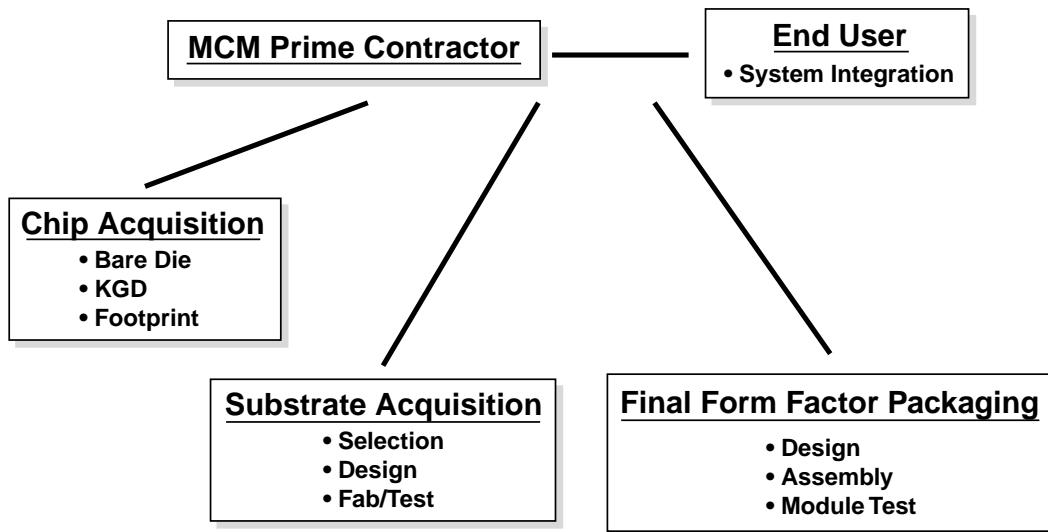
Likewise, the variety of MCM solutions available in the merchant market place is due to the different mix of vendors and the historical path each company took to get to their current portfolio of technology options. A key element to this third phase of the MCM industry is that the current successful surviving vendors are MCM solution providers.

THE MCM VENDOR BASE

There are five functions that must be performed to create and implement an MCM product:

- module design
- chip fab, chip acquisition
- substrate fab
- chip assembly, final module assembly and test
- purchase and integration into the system by the end user

From the end user's perspective, it is not so much a choice of technologies that influence the module decision, as it is the selection of vendors. One organization must own the MCM design and act as prime contractor. The role of the prime contractor and the end user is shown in Figure 12-77. There are two options—either the end user acts as prime contractor, or another vendor takes full responsibility.



Source: ICE, "Roadmaps of Packaging Technology"

22567

Figure 12-77. Roles of Prime Contractor and End Users in MCM Production

In the first case, the end user is the prime contractor. They are in control of the design of the module and the selection of the vendors for the chips, the substrates and the assembly. In the early days of MCMs, this was the only choice if an end user did not have MCM technology in house. Few vendors were willing to accept overall responsibility for the final MCM. Not many companies integrated MCMs into their products because of this, except vertically integrated companies that had significant in house expertise, such as Hughes, Motorola, Honeywell, IBM, DEC, NEC, Fujitsu, Toshiba, Sharp, Ericsson, and SGS Thompson.

The second type of vendor-customer relationship is when another party takes responsibility for the final MCM. The second party can be the ASIC supplier, the substrate supplier, the assembler, or the design house. There are successful examples of each of these structures in use today.

For example, LSI logic has supplied MCMs to their customers using their own chips. The four chip graphics controller for SGI, is an example. The design was done by the end user and LSI. The chips were fabricated by LSI Logic. The substrate supplier was Kyocera. LSI Logic performed the chip assembly and delivered fully tested MCMs to SGI in a PGA format. SGI used their contract assemblers, such as Solelectron, to perform the assembly into motherboards, along with the conventional components.

Companies that call themselves MCM vendors have evolved from three different sources. First are the previous vertically integrated system companies that have turned some of their internal resources into merchant services. Examples are IBM, Fujitsu, Toshiba, Lucent Technologies, Unisys, SGS Thompson, Hughes, TI, and Motorola.

The next ancestor of MCM vendors are the prior hybrid assembly houses, which had experience in assembly of bare die to thick film substrates. With the addition of LTCC substrates and purchasing laminates from external PCB vendor, former hybrid suppliers have redefined themselves as MCM vendors.

Finally, of the numerous thin film multilayer start up pioneering companies, only two remain: MMS and nCHIP. These companies were able to survive because they accepted the responsibility for the complete assembly of modules as well as substrates.

In addition to the historical vendors, there are two new types of MCM providers that are emerging in the industry today. Seeing the need for “integrators” in the industry, vendors who have traditionally owned a piece of the MCM food chain have taken over the whole pie. InterChip Corp. was formed to take responsibility for the delivery of MCMs by supplying the design expertise and acting as prime contractor, working with the chip suppliers, the substrate vendors and the assembly houses as subcontractors. A number of the contract assembly houses with expertise in handling bare dice as COB have also moved into the full service MCM business, such as Celestica, Solelectron and Nextek.

THE MAIN CHALLENGE: KNOWN GOOD DIE

MCMs did not become the vehicle that made single chip packages obsolete. They did not take over all of electronics. However, they represent over a \$1B market today, and the market is growing faster than the industry as a whole, as the infrastructure matures. It used to be the main barriers were:

- design tools
- affordable substrates
- availability of known good bare die
- assembly vendors
- thermal management schemes

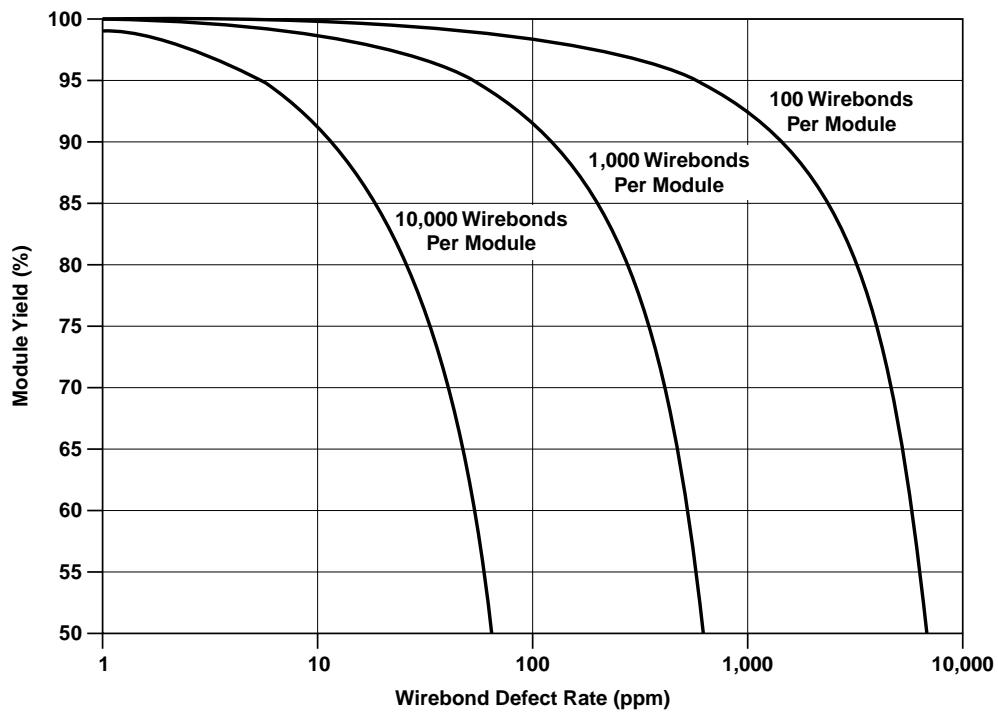
Over the last five years, as the MCM infrastructure has matured, each of these barriers have eased. Today, the most significant barrier is still the widespread availability of known good die (KGD) at reasonable cost.

Why KGD?

The final yield of an MCM depends on two leading terms, the assembly yield, Y_{assembly} , and the die yield, Y_{die} . For a module with N_{bond} wirebonds, and a defect rate, in ppm, of DR, the assembly yield is given by:

$$Y_{\text{assembly}} = (1 - DR)^{N_{\text{bond}}}$$

This is shown graphically in Figure 12-78. For high volume wirebonding operations, the wirebond yield is 10-100ppm. The yield is enhanced if all the bonding surfaces are UV or plasma cleaned prior to bonding. In a module with four die, each with 300 I/O, for example, there might be 1,200 wirebonds. For a defect rate of 100ppm, the module assembly yield would be 89%. If the defect rate were improved to 10ppm, the assembly yield would be 99%. With conventional techniques, and attention to detail, it is possible to reach high module yield assembly operations.



Source: ICE, "Roadmaps of Packaging Technology"

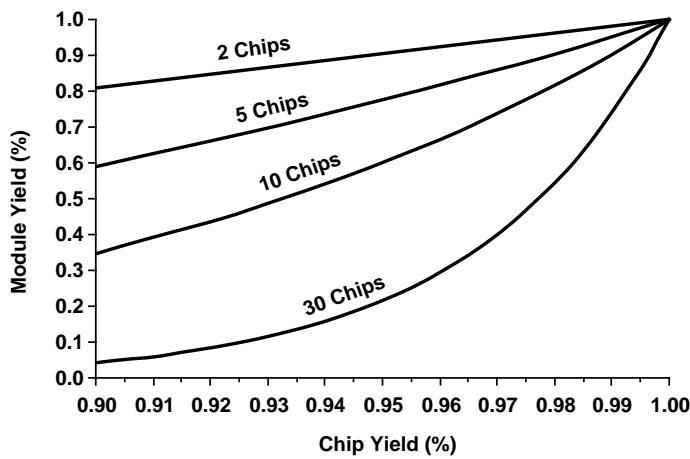
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Figure 12-78. Module Yield From Wirebond Assembly Defects Only

The yield due to the quality of the die is related to the chip yield, Y_{chip} , and the number of dice in the module, N_{chip} . The module yield, is given by:

$$Y_{\text{module}} = Y_{\text{chip}}^{N_{\text{chip}}}$$

This is plotted in Figure 12-79. For example, in a four chip module, if the die quality is 95% good, the expected module yield will be 81%. If the chip yield is 99%, the module yield would be 96%. For modules with a large number of die, starting with known good die is essential to maintaining acceptable module yield.



Source: ICE, "Roadmaps of Packaging Technology"

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Figure 12-79. Module Yield for Multichip Modules

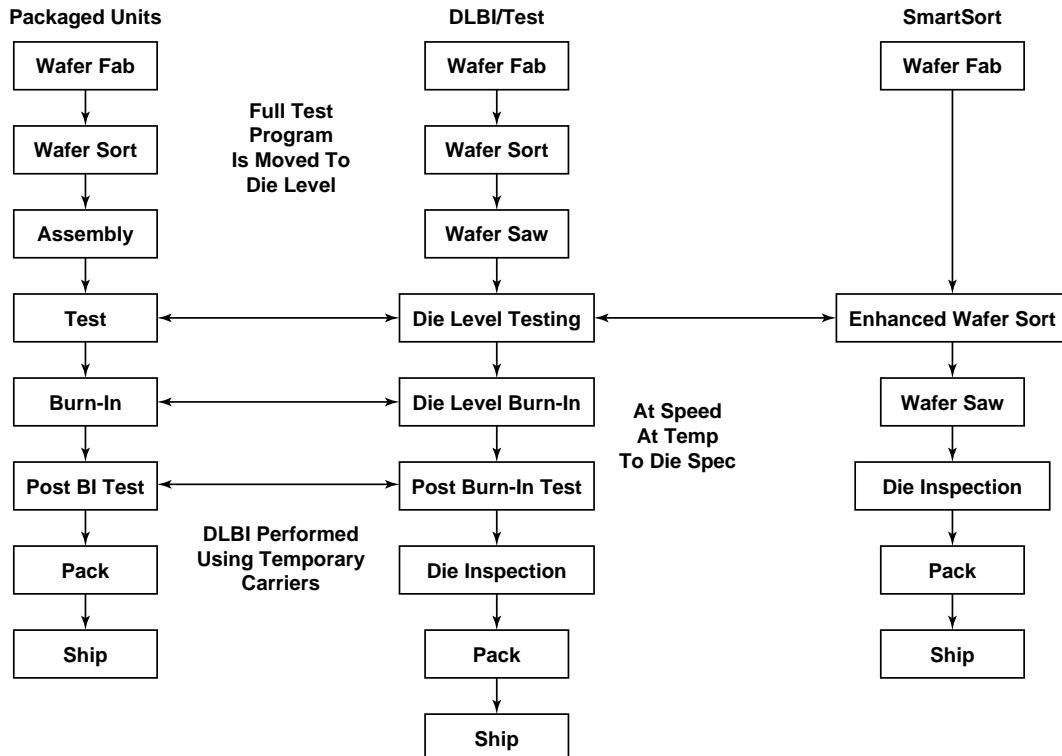
There is no such thing as a “perfect die”. Once assembled into a system, a die may be unacceptable due to four reasons:

- it has a killer defect and is not functional
- it does not have enough design margin and fails at a speed, temperature or voltage corner
- it falls out due to infant mortality, during burn-in
- it fails in the operation of the system with a fault that was not screened for (test escape)

In the conventional back-end assembly process sequence for packaged die, shown in Figure 12-80, tests are performed to catch the first three problems. There is always the possibility of a test escape, due to the limited test coverage possible given the size of ASICs. For example, a typical high end digital tester will run about 100 million test vectors on a chip. When a processor boots up UNIX, there are about 3 billion vectors run on the chip. When qualifying a new chip, the test vectors are constantly updated to catch newly identified failure modes. One of the characteristics of a mature chip is excellent test vector coverage.

The accepted definition of known good die (KGD) varies through the industry. Intel has established a definition of KGD as “...equivalent to or better than the corresponding package parts in terms of electrical and reliability performance”. Even this definition is ambiguous. It does not necessarily mean burn-in has been performed. After all, not all die need to be burned-in to achieve a high yield.

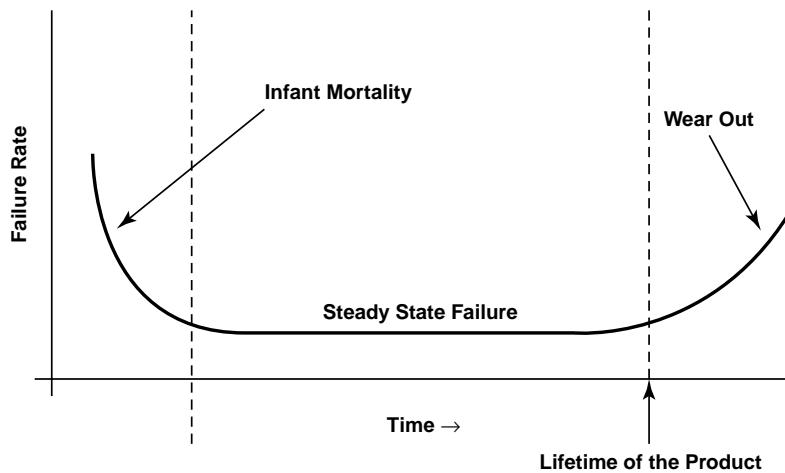
Burn-in is an accelerated way of screening out potentially weak chips. The failure rate for a collection of chips, in general, follows a bath tub shaped curve. An example is shown in Figure 12-81.



Source: Intel/ICE, "Roadmaps of Packaging Technology"

22369

Figure 12-80. Test Flow Comparison



Source: ICE, "Roadmaps of Packaging Technology"

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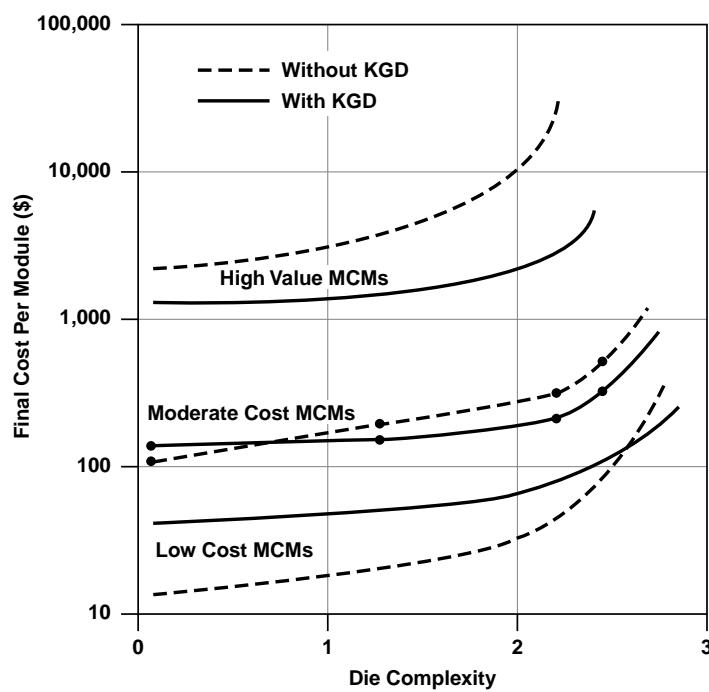
Figure 12-81. Failure Rate for Chips

There is an initial high failure rate. This is due to weak links or latent defects created during the manufacturing process. After an initial period of normal operation, typically less than three months, most of the weak links that are going to fail have failed. The failure rate remains more or less constant over the life of the product thereafter. At some point, the failure rate begins to increase again, due to wear out. The onset of wear out defines the life of the product.

The hope is that the failure rate of the weak links will be accelerated at elevated temperatures. By stressing parts at temperatures from 85°C to 125°C for 24 to 96 hours, many weak links will fail and be screened out, while not substantially accelerating the failure of normally robust parts.

The typical failure rate from burn-in is about 5% for new IC processes. If each failure is analyzed, the cause of failure identified, and the process modified to eliminate the production of the weak link, the failure rate from burn-in, or infant mortality, can be reduced by an order of magnitude. In a mature process, the failure rate can be less than 0.5%.

Die fabricated on a mature process line can routinely attain less than 0.5% burn-in drop out rate. If the burn-in costs are included, it might be more expensive to use burned-in die from a mature line for an MCM. Figure 12-82 illustrates this point. Since added testing will increase the cost of the bare die, to achieve the optimum MCM yielded cost may require different verified quality levels for the bare die.



Source: Rockwell Defense Electronics/ICE, "Roadmaps of Packaging Technology"

22370

Figure 12-82. Estimates of Final Module Costs (Including Replacement of Defective ICs)

For example, when the MCM uses many leading edge, high value die, the added costs of burn-in will result in a lower cost yielded module. However, for a few chip module, with mature die, the added cost of burn-in may not return much value to the yielded module, but increases the cost.

The “goodness” of the die required for the most cost effective MCM will vary depending on the complexity of the module and the maturity of the die manufacturing processes.

Though the standards for the quality of the die vary from vendor to vendor, four general categories are emerging.

- Level 1 is at-speed probed good die, typically with a visual inspection
- Level 2 is at-speed and hot chuck probed die
- Level 3 is with additional burn-in
- Level 4 is full testing to 100% of the data sheet specifications

Elmo Semiconductor, a distributor of known good die, offers a much tighter test specification, shown in Figure 12-83 as level 5. Even with the wide variation in the industry on what constitutes a KGD, there is an increasing number of vendors, both IC manufacturers and third party distributors that are now offering KGD. Figure 12-84 lists some of the current vendors.

Level 1	Level 2	Level 3	Level 4	Level 5
<ul style="list-style-type: none"> • Wafer Probe • Visual Inspection • Package Sample • Bondability Test • Electrical Test 	<ul style="list-style-type: none"> • Std/Hot Wafer Probe • Visual Inspection • Package Sample • Bondability Test • Electrical Test 	<ul style="list-style-type: none"> • Std/Hot Wafer Probe • Visual Inspection • Package Sample • Bondability Test • Thermal Cycling • Interim Electrical Test • Burn-In • Electrical Test 	<ul style="list-style-type: none"> • Std/Hot Wafer Probe • SPC Probe • Visual Inspection • SEM Analysis • Package Sample • Bondability Test • Thermal Cycling • Interim Electrical Test • Burn-In • Electrical Test • Life Test 	<ul style="list-style-type: none"> • Wafer Probe • Visual Inspection • Elmo KGD • Coating Process • Visual Inspection • KGD Contact • Assembly • Bondability Test • Thermal Cycling • Interim Electrical Test • Burn-In • Electrical Test • Die Removal • Visual Inspection

Notes:

- Inspection and test methods consistent with MIL-STD-750/883 methods
- Wafer Probe method (Std. or Hot Probe) depending on device type/design

Source: Elmo Semiconductor/ICE, "Roadmaps of Packaging Technology"

22387

Figure 12-83. KGD Categories Used by Elmo Semiconductor

Company	Functional and DC Parametric Test	At-Speed and At-Temperature Test	Full KGD With Burn-In
Advanced Micro Devices	x	x	
Allegro Microsystems	x		
American Microsystems	x	x	
Analog Devices	x	x	
Calogic	x		
Chip Express	x		
Chip Supply	x	x	x
Cypress Semiconductor	x	x	
Device Engineering	x	x	
Elmo Semiconductor	x	x	x
Eltek Semiconductor	x		
Harris Semiconductor			x
IBM Microelectronics	x		x
Integrated Device Technology	x		x
Intel		x	x
LSI Logic	x		
Micron Semiconductor	x	x	x
Minco Technology Labs	x		
Motorola	x	x	x
National Semiconductor	x	x	x
Rood Testhouse	x	x	x
Semi Dice	x		
SGS-Thomson	x	x	
Texas Instruments	x	x	x
Vitesse Semiconductor	x	x	
VLSI Technology	x	x	

Source: EP&P/ICE, "Roadmaps of Packaging Technology"

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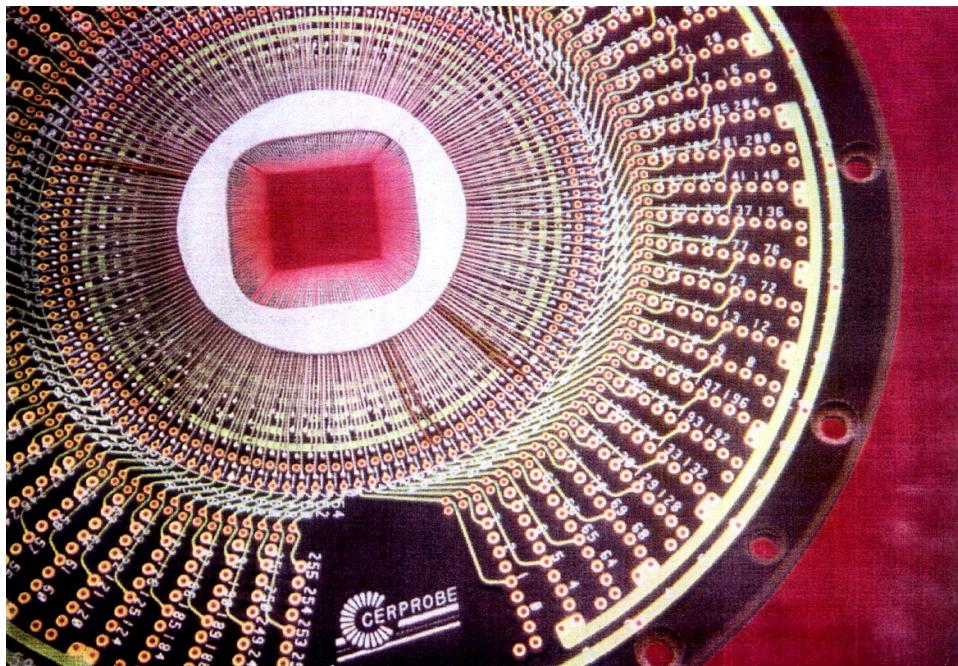
Figure 12-84. Bare Die Suppliers

As the specifications for KGD standardize and the technologies to implement them move up the learning curve, the price adders from KGD will converge. Currently, there is wide variation among suppliers for KGD. National Semiconductor and Samsung offer some die at lower price than the packaged units, from 0.8x to 1.2x. Intel offers KGD at parity to the packaged die prices as part of their SmartDie program. Most other suppliers, especially distributors, offer 1.5 to 5x premiums for the extra effort of acquiring, specifying, testing and sometimes burning in the bare dice. Key enablers to even faster proliferation of MCMs is decreasing the cost of KGD and increasing the number of suppliers.

Probed Good Die

At-speed wafer probing has had to keep up with the advances in increasing pin count, increasing clock frequency, and the transition to finer pitch peripheral pads or area array pads.

The traditional method of testing die on a wafer is with a needle probe card, shown in Figure 12-85. Each needle that touches a bonding pad terminates on a lead on the probe card which eventually connects to a driver circuit on the tester. Though the chip is less than an inch on a side, the test equipment to drive the test vectors may take up a large part of a room. Figure 12-86 is an example of large tester.



Courtesy of Cerpobe/ICE, "Roadmaps of Packaging Technology"

22375

Figure 12-85. Conventional, 500 Pin High Speed, Epoxy Ring Probe Card

The needle probe card has significant limitations as pin count increases, speed increases and pitch decreases. The most significant innovation in probe cards has been the membrane probe card, pioneered by HP, Hughes, Probe Technology and Micro Module Systems. An example of a membrane probe card for testing a peripheral die is shown in Figure 12-87.

In its typical configuration, the membrane is composed of from one to four layers of copper polyimide, fabricated in the same way as a thin film MCM substrate, with the interconnect layers lifted from the silicon or aluminum base. At the center of the membrane is a pad array in the mirror image of the chip that is to be probed. This can be peripheral or area array. The pads fan out to

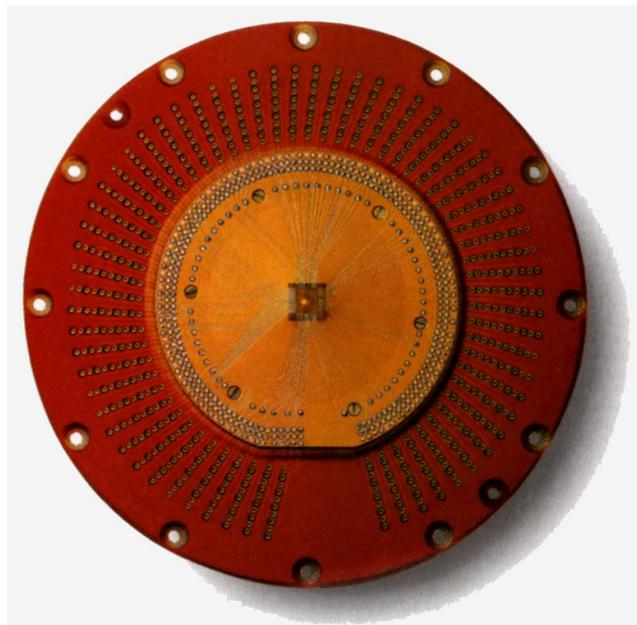
the edge of membrane to contact points that connect to pins on the probe station on a courser grid, typically 50mil centers. An example of a membrane probe from MMS, designed to probe area array pads, is shown in Figure 12-88.



Source: Unisys/ICE, "Roadmaps of Packaging Technology"

22384

Figure 12-86. State of the Art Test Equipment to Test a Single Die



Source: Packard-Hughes/
ICE, "Roadmaps of Packaging Technology"

22374

Figure 12-87. Packard-Hughes IC Membrane Test Probe



Source: Micro Module Systems/
ICE, "Roadmaps of Packaging Technology"

22378

Figure 12-88. Test-Frame Membrane Probe Card for Area Array Chips

By using multiple planes in the membrane, low inductance power and ground distribution can be implemented, with controlled impedance traces directly to the chip pads. The probe card can provide a better electrical environment than the chip's environment in the MCM.

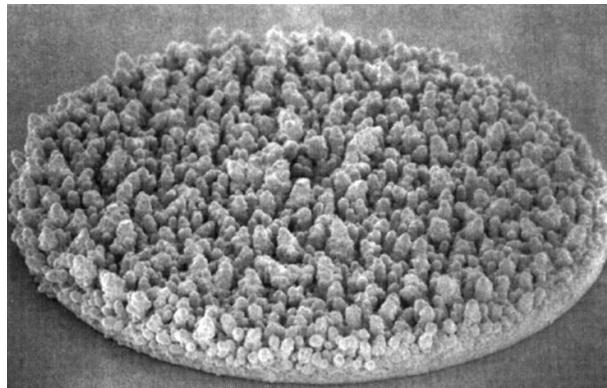
One of the challenges of probing the aluminum pads on bare die is making reliable contact, especially after repeated touch downs on adjacent die. Normally, high pressure is needed to break through the thin oxide layer on the pad. With conventional needle probe cards, the pressure is created by compliance in the cantilevered needles and a scrubbing action of the tungsten tip moving a few tenths of a mil over the surface of the pad.

For membrane probe cards, various other tricks have been developed. The pressure is applied either by an elastomer contact pressing the membrane against the wafer under test, or by air pressure in a small cap on top of the membrane. The actual contacting surface is typically a raised button of gold plated nickel. IBM has developed a process of plating dendrites of palladium on a pad. An example of these dendrites, typically 1mil high, is shown in Figure 12-89. These sharp points can be very effective at punching through the oxide layers of pads. Alternatively, sharp tips can be plated up on the ends of the traces on the membrane probe cards, as shown in Figure 12-90.

Burn-In Carriers

When burn-in is required, additional fixturing is needed. There are three methods in use for bare die burn-in:

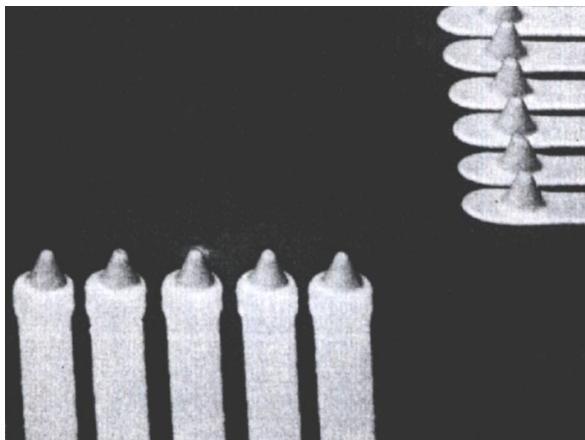
- a fixture for an individual die
- a temporary package for an individual die
- a temporary fixture to probe an entire wafer during burn-in



Source: IBM/ICE, "Roadmaps of Packaging Technology"

22386

Figure 12-89. SEM Photograph of Palladium Dendrites on a Pad



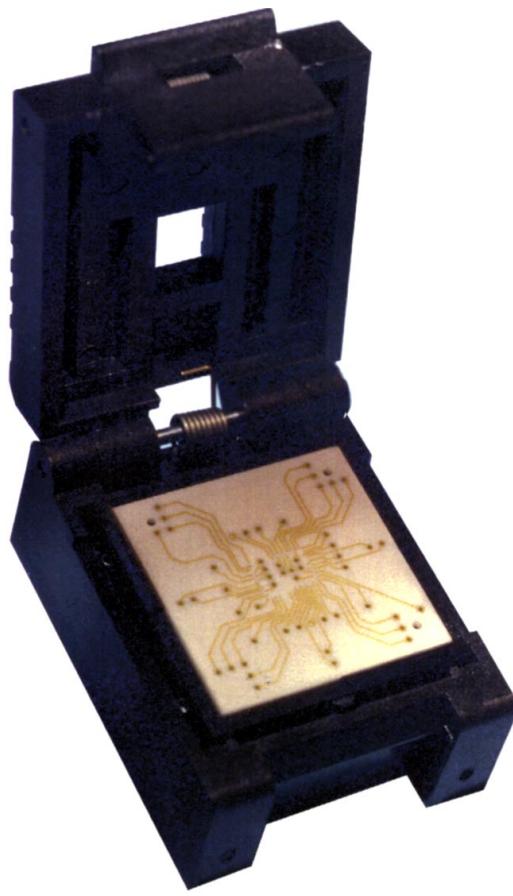
Source: Electronic Design/ICE, "Roadmaps of Packaging Technology"

22422

Figure 12-90. Plated Tips on the Ends of Leads of a Probe Card

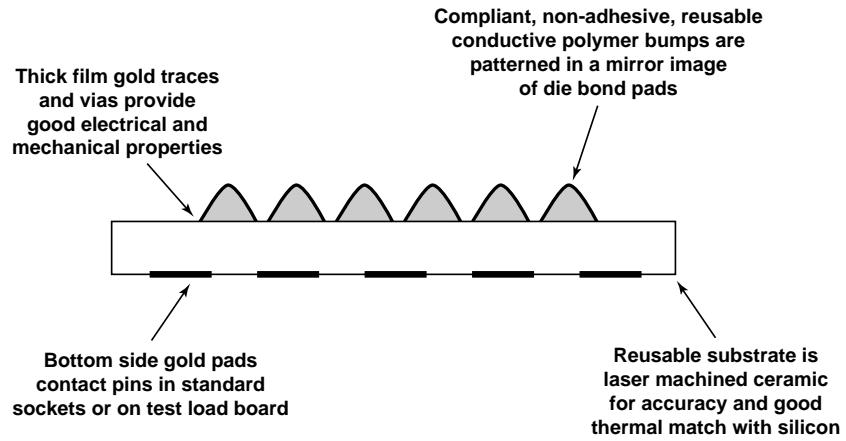
Fixtures for individual die typically consist of a substrate with fine line traces that fan out from the die pads to the periphery where conventionally spaced pins can be mated. In addition, the mechanical fixturing is provided to hold the die against the probe pads in a socket on a load board during the burn-in process.

An example of the EPIK System fixture from EPI, is shown in Figure 12-91. A ceramic substrate with thick film metallization and laser drilled through holes is the base to which a die is flip mounted. Small compliant polymer bumps are screen printed with Epoxy Technology conductive polymer on the ceramic substrate. These bumps provide the compliance and pressure to break through the oxide. A thermo-electric cooler against the back side of the die can also perform in situ burn-in. These features are shown in Figures 12-92 and 12-93.



Source: EPI Technologies/ICE, "Roadmaps of Packaging Technology" 22381

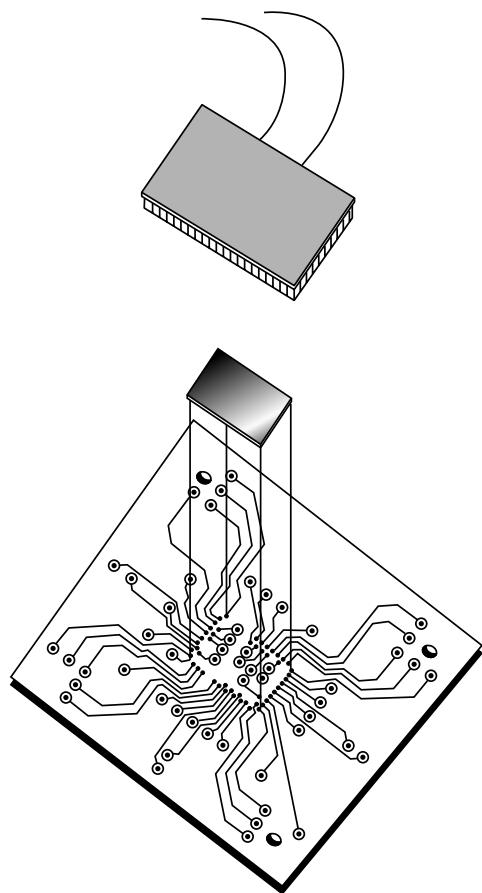
Figure 12-91. EPIK System With Ceramic Substrate in a Standard BGA Burn-In Socket



Source: EPI Technologies/ICE, "Roadmaps of Packaging Technology"

22383

Figure 12-92. Detail of Substrate



Source: EPI Technologies/
ICE, "Roadmaps of Packaging Technology"

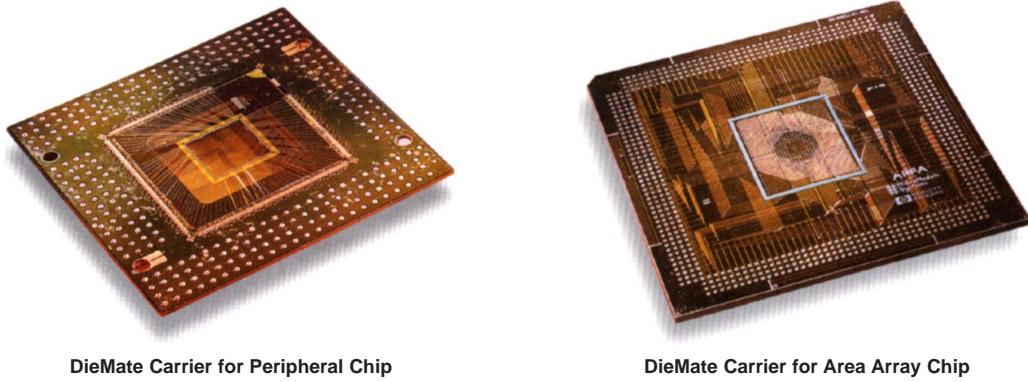
22382

Figure 12-93. Thermoelectric Cooler (TEC) for Temperature Testing

TI and MMS have formed a joint product line that leverages TI's test and burn-in fixture experience with the substrate experience of MMS. An example of the Test Frame substrate from MMS for both a peripheral chip and an area array chip is shown in Figure 12-94. These frames are mounted in burn-in sockets with the die pressing against the pads. A cap is spring loaded to apply a controlled contact force. This assembly is shown in Figure 12-95.

In the DieMate system, automated pick and place equipment can be used to load bare die into the sockets of the load board. This is shown in Figure 12-96. Intel uses the DieMate system in their KGD program, called SmartDie.

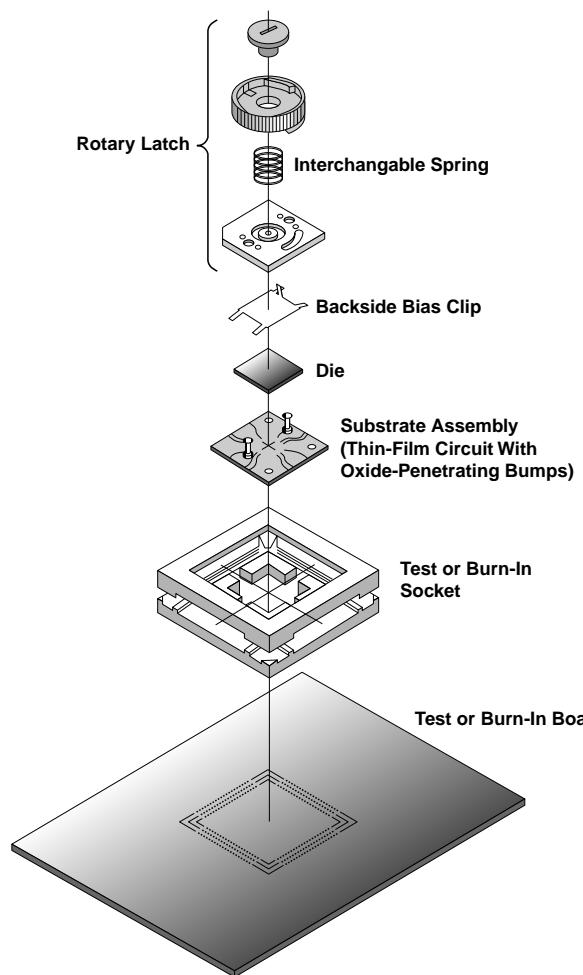
Another approach to fixturing the bare die is to use a conventional ceramic package and a weak bond. This method is used by MCNC in their BATS (Burn in And Test Socket) program and Chip Supply, among others. This general technique is called a temporary package. The approach of MCNC is especially well suited for flip chip with solder bumps.



Source: Micro Module Systems/ICE, "Roadmaps of Packaging Technology"

22581

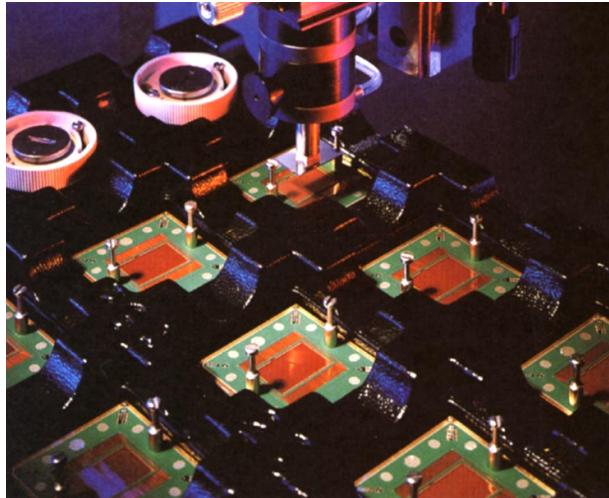
Figure 12-94. DieMate Carriers



Source: Computer Design/ICE, "Roadmaps of Packaging Technology"

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Figure 12-95. DieMate Carrier-and-Socket Burn-In System



Source: Micro Module Systems/
ICE, "Roadmaps of Packaging Technology"

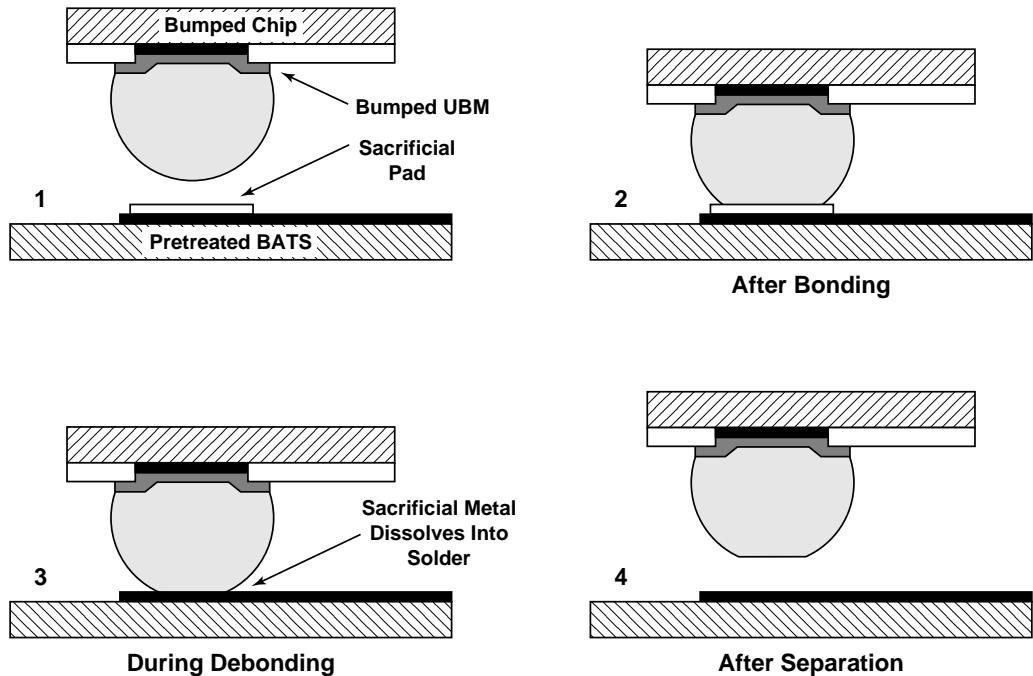
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Figure 12-96. DieMate Carrier Assembly Using a Modified Flip Chip Bonder

A substrate with solderable pads and a fan out to peripheral leads is used to solder attach the chip. However, only a thin layer of a solderable metal is on the pads. The metal under the pad is a non-wetting metal. The chip makes an initial solder contact with the pad and stays attached through burn-in. To remove the chip, the solder is reflowed and heated for a few minutes, enough time for the solderable metal to dissolve in the solder ball, and the solder ball to de-wet. This is illustrated in Figure 12-97. Though MCNC has kept their process proprietary, it could be implemented with aluminum pads having a thin flash of gold on top, for example. The flash of gold would have to be redeposited after each use.

In the case of Chip Supply, a weak wirebond is used to bond the die pad to a conventional ceramic package. The bonding conditions are purposefully non-optimized so the bond is weak and can be pulled off the die after the completion of burn-in. In this way, the chips are assembled into ceramic packages and placed in sockets in load boards and burned in normally. After burn-in and test, good die are removed from the temporary package by pulling up the wirebonds. A similar method is used by Elmo Semiconductors.

If an entire wafer could be burned in at once, without first dicing into chips, there might be significant cost savings by reducing the handling. This intriguing possibility has motivated a number of designs for wafer scale burn-in. In order to contact all the die pads on a wafer, the probe card must closely match the TCE of Silicon. If an 8 inch wafer is aligned to the probe card at ambient temperature, and then heated to 125°C, a TCE difference of 5ppm will result in a misalignment of 4mils, equivalent to one pad slip. A reasonable candidate for the probe card is another silicon wafer.



Source: MCNC/ICE, "Roadmaps of Packaging Technology"

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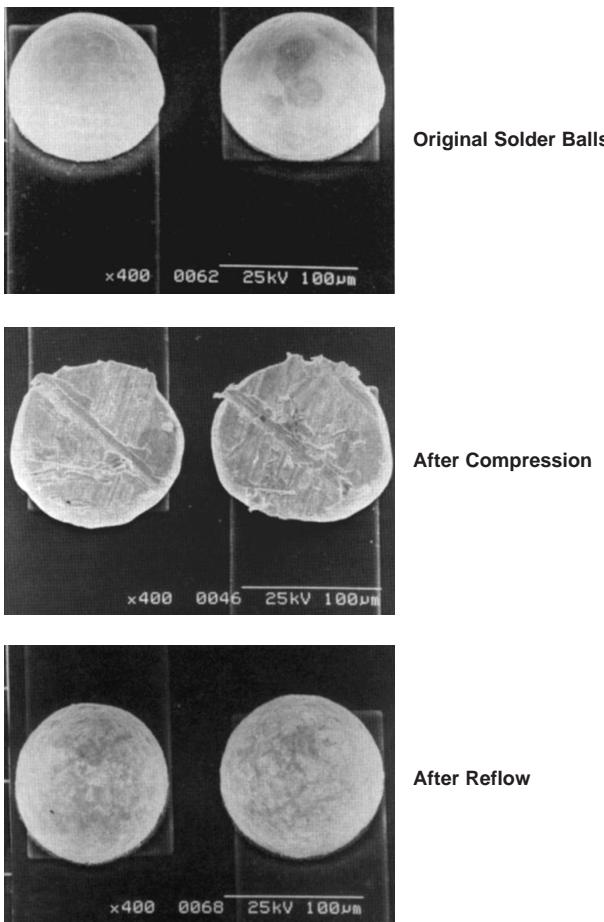
Figure 12-97. The BATS Process

nCHIP has demonstrated a silicon interconnect substrate probe card with a mirror image of the pads on the wafer to be probed. Solder balls on the probe card are used to contact the pads on the wafer. The two wafers are aligned and pressed together. At the 125°C burn-in temperature the solder balls deform and take up any noncompliance. After the wafer probe card is removed, the solder balls can be reformed again by normal reflow and reused. An example of the solder ball deformation and reformation is shown in Figure 12-98. nCHIP has demonstrated this silicon wafer probe card for memory die.

Shipping and Handling

The last step before shipping out the door is packaging the bare die for shipment. There are five methods that are either currently used or proposed:

- Gel-Pak containers
- wafers on tape
- packaged die
- waffle pack
- tape and reel



Source: nCHIP/ICE, "Roadmaps of Packaging Technology"

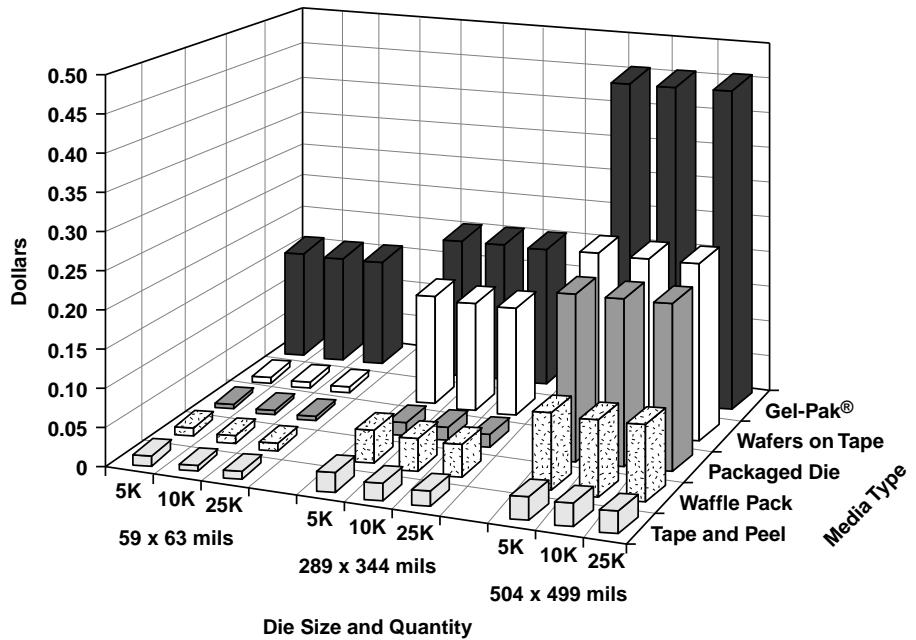
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Figure 12-98. Effect on Solder Bumps From Wafer Level Burn-In

Figure 12-99 displays the relative costs for these methods, for different die sizes. The cost adder to the die is less than \$0.3, except for Gel-Pak. Gel-Pak containers cost approximately \$0.5 per die, assuming that the containers are not reused. If the containers are recycled back to the vendor, the cost of Gel-Pak can easily reach the \$0.1 range per die. Intel ships all their die in Gel-Pak containers, and are experimenting with tape and reel. In high volume, tape and reel offers the lowest cost shipping option. An example of both is shown in Figure 12-100. The above methods will become more common place as MCM applications proliferate.

WHERE IS WAFER SCALE INTEGRATION?

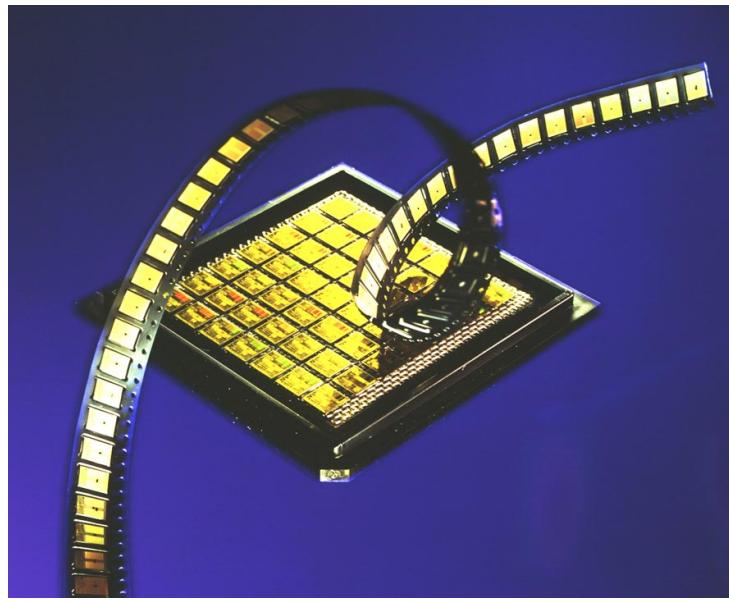
All the advantages of high end MCMs should be realizable with Wafer Scale Integration (WSI). By keeping the chips embedded in the wafer and arranging all the interchip routing as part of the chip's multilayer metalization, very compact packaging should be possible. No added assembly would be necessary. The fundamental problems with this approach, however, are yield and cost.



Source: National Semiconductor/ICE, "Roadmaps of Packaging Technology"

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Figure 12-99. Cost Per Die – Shipping Media Comparison



Courtesy of Intel/Source: ICE, "Roadmaps of Packaging Technology"

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Figure 12-100. Bare Die Shipped as Smart Die in Gel-Pak and Tape and Reel

There will always be a tendency toward more functions (or transistors) per die. Figure 12-101 illustrates the driving forces affecting the optimum size of a die. Lower cost achieved by mask level integration of transistors allows a lower cost per gate than assembling components diced from a wafer. However, as the number of gates increases, the yield goes down and the cost per function begins to rise. The optimum die size that balances integration and yield is constantly moving upward. This trend can be seen in Figure 12-102.

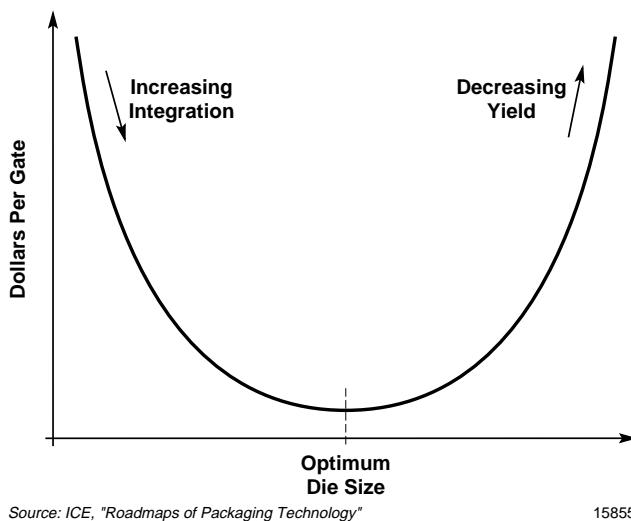


Figure 12-101. Where is Wafer Scale Integration?

If projected ahead, a 4Gbit DRAM chip will be a few inches on a side. Figure 12-103 is an example of one of the first working prototypes of the 4 Gbit DRAM from NEC. This may be a glimpse of possible chip size in the future.

For random logic wafers, as compared to memory wafers, significant challenges exist for the design of the entire wafer, especially if it involves redundancy, self test and self rerouting.

Large gate arrays currently require 4-6 metal layers for on-chip routing. A high-density WSI wafer may require a total of 8-10 metal layers. The final interconnect would have to achieve extremely high yield, because the value of a good wafer at the seventh or eighth metal layer is very high.

A cost effective strategy to approach the potential density of WSI is to always use the optimum size die and reconstruct the wafer with tested good dice. This approach, termed "Wafer Scale Reconstruction" or WASER, by Hughes Aircraft Company, is exactly the approach that MCMs enable.

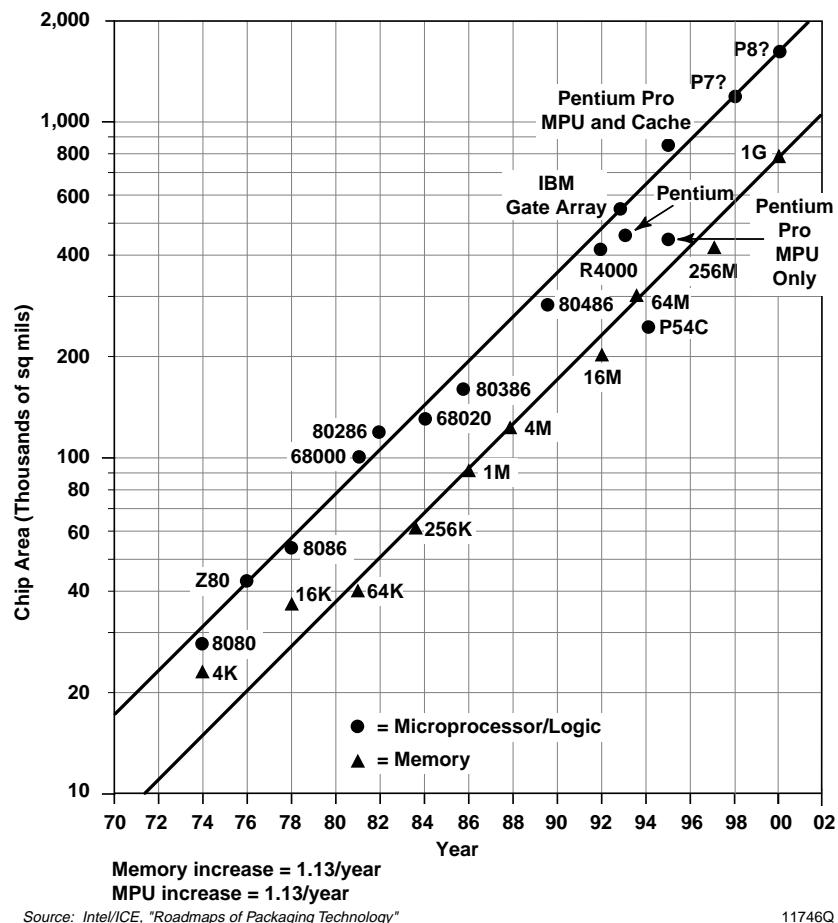
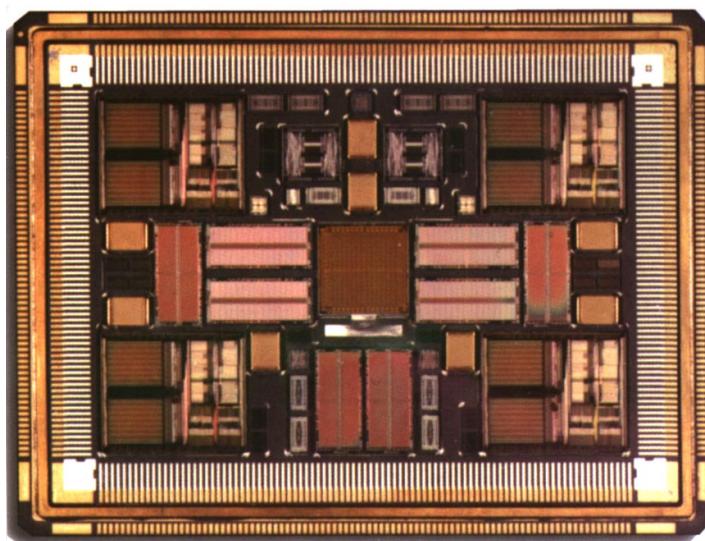


Figure 12-102. IC Die Size Trends



Figure 12-103. A 4Gbit DRAM

Substrates with interconnect only are fabricated in a process optimized for substrates, then tested and repaired as needed. Chips with an optimized size are manufactured in a process optimized for chips and are supplied tested. The chips are bonded closely together on the substrate. The result is a reconstructed wafer, but with components manufactured using the most cost effective processes. This approach takes advantage of the largest dice available today. An example of the reconstruction of wafer scale densities is shown in Figure 12-104. This is a tiled array of chips assembled using the GE HDI process.



Source: Lockheed Martin/ICE, "Roadmaps of Packaging Technology"

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Figure 12-104. Tiled Chips in an MCM with Near Wafer Scale Integration Density

The added feature of WASER is the ability to combine device technologies. The chips can be individually optimized for logic function, memory, "processing" (as in DSP and MPUs) and cost. Such integration, after all, is the real objective of using MCMs, in general.

