

# Table of Contents

<b>Acronyms</b>	<b>ii</b>
<b>Symbols</b>	<b>iii</b>
<b>1 Introduction</b>	<b>1</b>
1.1 Background . . . . .	1
1.2 Motivation . . . . .	3
1.3 Objectives and Specifications . . . . .	3
1.4 Major contribution of the Dissertation . . . . .	3
1.5 Organisation of the Dissertation . . . . .	3
<b>2 Methodology</b>	<b>4</b>
2.1 Package Style . . . . .	4
2.2 Wiring . . . . .	6
2.3 Substrate . . . . .	8
<b>References</b>	<b>10</b>

# Acronyms

<b>NN</b>	Neural Network
<b>ML</b>	Machine Learning
<b>DL</b>	Deep Learning
<b>FCN</b>	Fully Convolutional Network
<b>CNN</b>	Convolutional Neural Network
<b>RCNN</b>	Region Based Convolutional Neural Network
<b>DCNN</b>	Deep Convolutional Neural Network

# Symbols

$\Pi$  An Pi Symbol  
 $\beta$  An Beta Symbol  
 $\sigma$  An Sigma Symbol  
 $\alpha$  Another Alpha Symbol

# Chapter 1

## Introduction

The first chapter of the dissertation is almost invariably the Introduction. Generally, its purpose is to lead the readers into the problem you intend to attack in the project, to set the scene. The main points here consist of the background to the problem and your motivation in solving it. This then leads into the objectives and the scope of the project. It is good to conclude your Introduction with a section on the layout of the dissertation. It prepares the readers for what is to come

### 1.1 Background

Background goes here. Also you can put in some references .

Here is a sample of table in Table 1.1

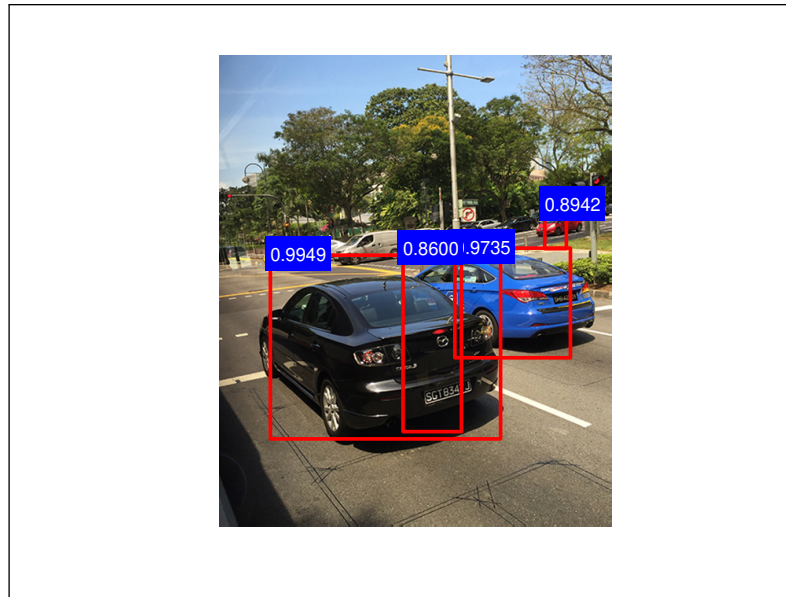
**Table 1.1: A table without vertical lines.**

	Treatment A	Treatment B
John Smith	1	2
Jane Doe	–	3
Mary Johnson	4	5

Use `\newpage` to force start a new page.

Also can try to refer to this image in Figure 1.1. Notice that the .eps and .pdf format vector graphs are favoured, because:

1. they can be zoomed-in to check the detail.
2. text in such formats are search-able.



**Figure 1.1: Bounding-box example of cars.**

Try to insert a math equation as in Equation 1.1. If you wanna try the in-line mathematical, here is a sample  $\alpha = \pi \cdot \frac{1}{\Theta}$ .

$$e^{ix} = \cos x + i \sin x \tag{1.1}$$

Also here is a sample for footnote and hyperlink url<sup>1</sup>.

When mention some file formats can use music.mp3, latex.pdf, etc.

If there are any update of the dissertation standard, or you want to contribute

---

<sup>1</sup><https://github.com/doem97>

to the NTU-EEE-MSc-Dissertation-Template project too, kindly send an E-mail to me. Thank you :)

## **1.2 Motivation**

## **1.3 Objectives and Specifications**

## **1.4 Major contribution of the Dissertation**

## **1.5 Organisation of the Dissertation**

# **Chapter 2**

## **Methodology**

After an introduction on the development history and a brief on design criteria, this chapter focuses on specific components. For the rest of this chapter, the analysis of MCM will go deeper into explanations for key MCM design methodologies, thus giving a detailed view on MCM design.

### **2.1 Package Style**

assembly techniques (surface mount, chip and wire) 9.11 p.223

Assembly, the macro arrangement of MCM structure, determines existences of specific components. After several decades of MCM development, various methods of assembly have been implemented, with costs and performances ranging from low to high.

Traditionally, industrial attention has been paid on the surface-mount assembly method, which provides a considerable performance with the lowest cost. This technique solders pre-packages components onto intended substrates to form the overall module. Many package styles can be categorized as this method: SIP, DIP, etc.

To integrate circuits and components onto the substrate via epoxy attachment and wire bonding provides another method with higher density as well as a very low interconnect electronic circuit parasitics. This is called the chip-and-wire assembly, and it can be implemented through various package styles, e.g., epoxy seal, metal package.

The above techniques can also be applied at the same time to form a hybrid package. [1]

Three main methods for IC die attachment are provided in current industries: wirebond, flip chip and TAB. [2]

Regarding to the thermal design mentioned in the previous part, it's important to take the heat spreader into consideration.

e.g.

- Epoxied directly to the BeCu heat spreader through a cutout in the board
- Epoxied to the head spreader, through a cutout, via a thermally conductive submount, to electrically isolate the die from the heat spreader

The package style of an MCM should be designed according to its practical usage. Major considerations towards the design scheme should include and should not be limited to: on the frontend, the general function, purpose, interconnects, testability, available assembly techniques, active elements configurations; on the backend, placement, routing, via minimization, tree searching, layer estimation, potential failure risks, reliability.

Hence, during the design flow, careful attention must be paid on the arrangements of these technologies, so that appropriate ones can be applied on appropriate places. [3]



## 2.2 Wiring

Wiring in MCM supports one of its critical functions: to provide both signal interconnects for the chips within the package and an interface between the module itself and the outer environment. In current industrial applications, there are three mainstream metals for MCM wiring fabrication: Al (aluminum), Cu (copper) and Au (gold).

1. Al is well known for its low fabrication cost and a proper oxidization resistivity. It's easy to sputter and evaporate Al onto the intended surface, but the difficulty in electropolation limits its flexibility.
2. Cu has a significantly larger conductivity and a better electromigration resistivity compared with Al, and it's also very flexible in deposition methods. However, oxidization on the surface of copper makes it hard to adhere to other materials, especially dielectrics and other wires.
3. Au has the highest conductivity among these materials, making it very suitable for thin-film fabrication. What's more, it has a fairly good deposition method flexibility, though its adhesion is poor so that a Ti or Ti/W layer is always needed. Another critical shortcoming is its high cost.

Directly related to the wiring fabrication, the conductor materials should be determined in accordance with the design, electrical requirements and process requirements. Among numerous properties of a given material, conductivity and reliability are the most important towards fulfilling the specification. [3]

*There are also other various types of wiring materials...*

*In the previous chapter, a key considerations for wiring design has been introduced: the wiring density. In the design flow of an MCM, the need to determine its*

size usually leads to a *wireability analysis*.

A wireability analysis includes considerations about three parameters of this design: *wiring demand* (D), *wiring capacity* (C), *average wire length* and *connectivity*.

The wiring demand refers to the required amount of wiring for a given circuit's interconnection, while the wiring capacity indicates the maximum available amount. The relationship between them can be expressed as follows:

$$D = \varepsilon C \quad (2.1)$$

where  $\varepsilon$  stands for the wiring efficiency with a circuit specified typical value between 30% to 70%. Neglecting via and through holes, the total wiring capacity  $C_T$  can be described through the following equation, for a given MCM:

$$C_T = \frac{P_P \times N_T}{P_S} \quad (2.2)$$

where  $P_S$  is the minimum signal line pitch;  $P_P$  is the pitch size;  $N_T$  is the number of wiring layers.

The calculation of wiring demand, on the other hand, the average length per interconnection  $\bar{L}$ , or the Manhattan length, should be estimated beforehand. A classical estimation method by Rickert is

$$\bar{L} = 0.77 P_P N_C^{0.245} \quad (2.3)$$

where  $N_C$  is the number of chips to be interconnected. [4]

The number of I/O pins is another crucial parameter in the design stage of an MCM. The well-known Rent's Rule gives a very useful estimation on this

$$N_{IO} = ag^b \quad (2.4)$$

In the above equation, if a specific chip is given,  $N_{IO}$  is its anticipated number of I/Os;  $g$  is its number of gates;  $a$  and  $b$  are the average connection number per I/O, or the Rent's coefficient, and the Rent's exponent respectively. [5]  $a$  and  $b$  are determined empirically and several typical values are given below. [6]

**Table 2.1: Rent's coefficients and exponents for specific devices/systems**

Type	Rent's coefficient, $a$	Rent's exponent, $b$
DRAM	6.20	0.085
SRAM	6.00	0.120
Microprocessors	0.82	0.450
Random Logi	1.90	0.500
Computer Systems	2.50	0.600

*Also, emphasize their importance*

chip and wire assembly

## 2.3 Substrate

The whole chapter 9 [3]

For any packaging design, the substrate influences almost every part of its overall performance.

C: thick-film, HTCC, LTCC. D: inorganic dielectrics on Si, organic dielectric on Si. L: laminated board

substrate technologies (how to carry dies) 9.10 p.220 [3]

## References

- [1] James J Licari. *Hybrid microcircuit technology handbook: materials, processes, design, testing and production*. Elsevier, 1998.
- [2] Eric Bogatin, Dick Potter, and Laura Peters. *Roadmaps of packaging technology*. Integrated Circuit Engineering Scottsdale, 1997.
- [3] Wai-Kai Chen. *The VLSI Handbook, Second Edition (Electrical Engineering Handbook)*. CRC Press, Inc., USA, 2006.
- [4] Robert G Rickert. Design trade-offs. In *Electronics Materials Handbook vol. I Packaging*, pages 18–24. ASM Int., 1989.
- [5] Bernard S Landman and Roy L Russo. On a pin versus block relationship for partitions of logic graphs. *IEEE Transactions on computers*, 100(12):1469–1479, 1971.
- [6] Rao R Tummala et al. *Fundamentals of microsystems packaging*. McGraw-Hill New York, 2001.