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# Chapter 1

# History and Criteria

Multi-Chip-Modules have been around since the early 1970s and 1980s mainly used in IBM mainframes first as memory and then for thermal conduction, but have been much wider use in the 1990s. This is an important engineering enhancement that allows the miniaturization of electronic components while improving performance.

## 1.1 MCM Used in Early Stage

Multi-Chip-Modules was first introduced into bubble memory in the 1970s. Bubble memory is a type of non-volatile computer memory that uses a thin film of a magnetic material to hold small magnetized areas, known as bubbles or domains, each storing one bit of data. The magnetic material is arranged into parallel tracks and the bubbles can form a serial of '1' and '0' under the control of external field. To increase the density of bubble memories, memory chips were assembled in multilayer stack. This is the original form of MCM. However, the lack of stability and its non-moving characteristics made it obsolete and finally replaced by other memories in 1990s. The idea of MCM was reserved and was used in later technologies.

MCM was also used in mainframe computer packaging. In the 1980s, MCM substrate was first used in this area in the form of Thermal Conduction Module(TCM) which was introduced by IBM. The usage of MCM was not only aim to integrate more chips together, but also to optimize the power distribution, interconnection and cooling. Figure 1.1 shows an exploded view of a water-cooled TCM substrate. [1] From the 1980s to 1990s, IBM TCM technology updated two generations, Alumina-Mo Ceramic MCM and Glass-ceramic copper Ceramic MCM. The third generation will move towards more layers, more I/Os and thinner.

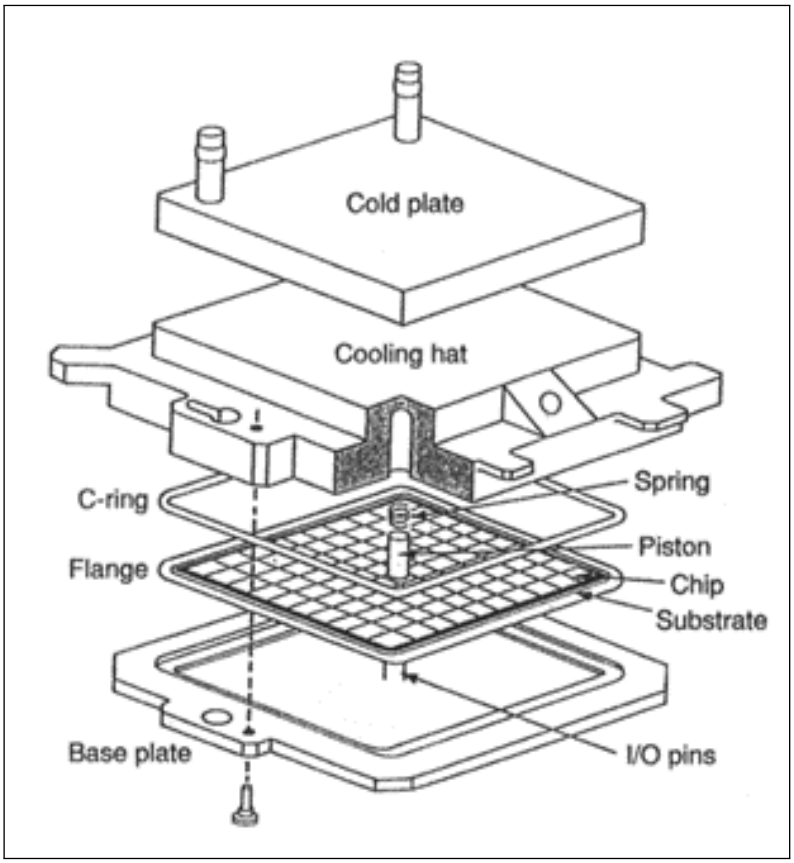


**Figure 1.1: Exploded view of a water-cooled TCM substrate.(Ref. [1], Fig. 13.3 )**

The multilayer ceramic approach derived from TCM was then used to enhance the strength, increase electrical transition speed and reduce the cost of the module. Superconducting multilayer multichip module arises at the right moment. In the 1990s, StratEdge Corporation cooperated with TRW Superconductive Electronic Research Group to provide high performance multichip modules using

high-temperature superconductors. [2] Superconducting MCMs were verified to have the performance of high speed, low capacitive impedance, low input-output mismatch and less cable losses. These characteristics were important for developing MCMs in the next several decades.

## 1.2 Recent Situation

Intel also tried several times on the technology of MCM in order to realize the dual-core processor. In 2005, Pentium D, a type of processor in 8xx and 9xx formats, was first introduced during the Intel Developer Forum (IDF). There were two processor die named "Cedar Mill" being integrated inside one Pentium D. At the same time, AMD also released its first dual-core processor, Opteron, in April, 2005. However, AMD made it dual-core in the level of raw wafer and made no use of MCM. Although multi-core can be realized in the absence of MCM packaging technology, MCM packaging can better promote product renewal. For example, the first quad-core processor was manufactured using bare die integration and MCM integration simultaneously.

Nowadays, MCM packaging technology is gradually well developed and has a good application in various fields. In addition to the core processor, GPU, DRAM, etc., are also using MCM technology. We can summarize the development history of so many years and draw the conclusion from the following aspects:

1. Higher inter-chip transmission efficiency. Intel Pentium D and IBM both used MCM technology for efficiency. Efficiency is first, then integration.

2. Higher integration and the race of multi-core. In order to speed up the updating, Intel not only used the multi-core integration of raw wafer, the

technique of MCM packaging was also developed and used.

3. Flexible and accelerated development. To some extent, MCM packaging can make up for the lack of wafer processing development. Multi-core processor, for example, can be fabricated on wafer level or integrated during packaging, which allows companies to launch products in a more flexible way.

## 1.3 Dielectrics

Polymeric dielectrics have been widely accepted as materials of choice for inter-layer dielectrics in MCMs [3]. The higher the dielectric constant of polymeric dielectric is, the higher packaging densities will be achieved. On the contrary, lower or non-uniform dielectric constant will exhibit the characteristic of weaken signal level and cause energy loss. In this case, non-uniform means the dielectric constant varies at different frequency electromagnetic sine wave. If the signal is made up of wave forms of multiple frequencies, the dielectric constant under each component frequencies should take into consideration. In addition, crosstalk also need to be examined. The dielectric constant between two signal lines plays an important role in this case. If the dielectric constant of the material is low enough, the signal lines can be placed very closely.

In the multilevel thin film structures, there are at least two signal layers which can influence each other during the operation. A dielectric layer is a must to serve as an inter-layer to minimize the crosstalk. More specifically, the expected dielectric constant of the dielectric layer should range from 2 to 3.5 and does not vary significantly with frequency (on the order of 0.1) for many of the polymeric dielectrics used in electronic packaging.

## 1.4 Thermal Design

Temperature is one of the most important player in MCMs as well as other chips. However, it is hard to define the thermal property using only few parameters. All that is wanted is a more suitable working environment for chips and improve the reliability of MCMs.

There are still some important parameters or concepts need to be mentioned. First is thermal paths. It is obvious that MCMs temperature can be effected by internal and external factors. The internal thermal path is directly formed by the structure itself and heat can transfer from the inside to the outside though it. Also, external temperature and heat dissipation are important but not decide by MCMs. Usually, thermal design follows the experiments and simulations. The experiments gives a briefly direction for the thermal design and computer simulation provide a more specific module to illustrate the thermal path better. Second, heat transfer mechanisms. There are three types of heat transfer: conduction, convection and radiation. The heat conduction is defined by the Fourier cooling law which provide a connection between energy, temperature and parameters of chips. Convection and radiation heat transfer is decide by the external factors such as heat dissipation materials and air or fluid velocity. The last is thermal coupling. In most cases, chips are assembled on the motherboard or PCB board and then installed inside certain cages or on shelves. If there are multiple boards connected to only one backplane, the thermal conduction can be huge and the heat transmission rate is too limited from the plane to the ambient to sustain the significant heat generation. Frames or enclosures are designed to deal with the thermal coupling.

There are several thermal control methods could be used for MCMs. Material property improvement is the most effective way to deal with thermal problems. If the thermal resistance can be reduced by changing materials, the heat will

spread more quickly and leave MCMs operating in a lower temperature. However, this approach is constrained by a number of factors. So, people come up with other ideas such as backside cooling. A metal mount is usually attached at the backside of MCMs to transfer heat to the ambient more efficiently. Then, many methods, natural convection, forced convection, liquid immersion, etc. can be applied to cool the chip down.

## 1.5 Electrical Design

There are a set of electrical parameters to be considered during the fabrication of MCMs, such as delay, noise, reflection, crosstalk, line losses, loading effect and so on. The final objective of the electrical design of MCM is to produce a layout which is a description of the artwork used to make the masks to be applied in MCM production. [4]

With the aid of computers, we can follow the process shown in Figure 1.2 to prepare the layout of MCMs. Start with timing design and then fulfill the requirements of net delay. After MCM placement and routing there is a process of back annotate. Finally, the simulation of timing verification and signal integrity will give out the result of the layout assessment.

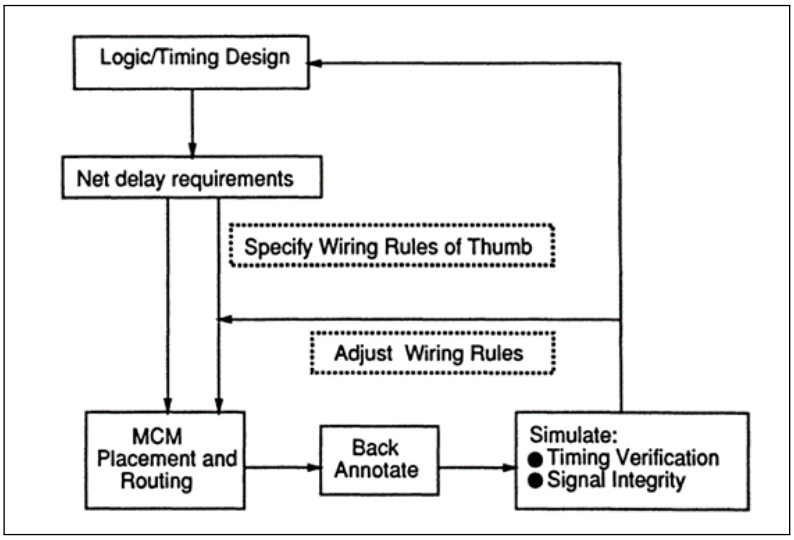


**Figure 1.2: The steps in producing an MCM layout.(Ref. [4], Fig. 11.22 )**

About the noise control, noise on data signal lines can be fixed to some extent but excess noise on clock lines should be eliminated. The delay on the data path is contributed by the impedance and the length of the line as well as the properties of dielectric layers. A short path and low line resistance would be preferred to minimize the internal delay. Reflection and crosstalk also need to be treated well which involves carefully design of the layout and interconnections. Delay and noise have great influence on chip performance and can be reduced by using MCM technology. So, MCM packaging is a comprehensive technology which needs to take into account many electrical properties.

# Chapter 2

# Methodology

After an introduction on the development history and a brief on design criteria, this chapter focuses on specific components. For the rest of this chapter, the analysis of MCM will go deeper into explanations for key MCM design methodologies, thus giving a detailed view on MCM design.

## 2.1 Package Style

Assembly, the macro arrangement of MCM structure, determines existances of specific conponents. After several decades of MCM development, various methods of assembly have been implemented, with costs and performances ranging from low to high.

Traditionally, industrial attention has been paid on the surface-mount assembly method, which provides a considerable performance with the lowest cost. This technique solders pre-packages components onto intended substrates to form the overall module. Many package styles can be categorized as this method: SIP, DIP, etc.

To integrate circuits and components onto the substrate via expoxy attachment

and wire bonding provides another method with higher density as well as a very low interconnect electronic circuit parasitics. This is called the chip-and-wire assembly, and it can be implemented through various package styles, e.g., epoxy seal, metal package.

The above techniques can also be applied at the same time to form a hybrid package. [5]

Three main methods for IC die attachment are provided in current industries: wirebond, flip chip and TAB. [6]

Regarding to the thermal design mentioned in the previous part, it's important to take the heat spreader into consideration, e.g.

• Epoxied directly to the BeCu heat spreader through a cutout in the board
• Epoxied to the head spreader, through a cutout, via a thermally conductive submount, to electrically isolate the die from the heat spreader

The package style of an MCM should be designed according to its practical usage. Major considerations towards the design scheme should include and should not be limited to: on the frontend, the general function, purpose, interconnects, testability, available assembly techniques, active elements configurations; on the backend, placement, routing, via minimization, tree searching, layer estimation, potential failure risks, reliability.

Hence, during the design flow, careful attention must be paid on the arrangements of these technologies, so that appropriate ones can be applied on appropriate places. [7]

## 2.2 Wiring

Wiring in MCM supports one of its critical funcitons: to provide both signal interconnects for the chips within the package and an interface between the module itself and the outer environment. In current industrial applications, there are three mainstream metals for MCM wiring fabrication: Al (aluminum), Cu (copper) and Au (gold).

1. Al is well known for its low fabrication cost and a proper oxidization resistivity. It's easy to sputter and evaporate Al onto the intended surface, but the difficulty in electropolation limits its flexibility.
2. Cu has a significantly larger conductivity and a better electromigration resistivity compared with Al, and it's also very flexible in deposition methods. However, oxidization on the surface of copper makes it hard to adhere to other materials, especially dielectrics and other wires.
3. Au has the highest conductivity among these materials, making it very suitable for thin-film fabrication. What's more, it has a faily good deposition method flexibility, though its adhesion is poor so that a Ti or Ti/W layer is always needed. Another critical shortcoming is its high cost.

Directly related to the wiring fabrication, the conductor materials should be determined in accordance with the design, electrical requirements and process requirements. Among numerous properties of a given material, conductivity and reliability are the most important towards fulfilling the specification. [7]

In the design flow of an MCM, the need to determine MCM size usually leads to a *wireability analysis*.

A wireability analysis includes considerations about three parameters of this de-

sign: *wiring demand* (D), *wiring capacity* (C), *average wire length* and *connectivity*.

The wiring demand refers to the required amount of wiring for a given circuit's interconnection, while the wiring capacity indicates the maximum available amount. The relationship between them can be expressed as follows:

$$D = \varepsilon C \tag{2.1}$$

where $\varepsilon$ stands for the wiring efficiency with a circuit specified typical value between 30% to 70%. Neglecting via and through holes, the total wiring capacity $C_T$ can be described through the following equation, for a given MCM:

$$C_T = \frac{P_P \times N_T}{P_S} \tag{2.2}$$

where $P_S$ is the mininum signal line pitch; $P_P$ is the pitch size; $N_T$ is the number of wiring layers.

The calculation of wiring demand, on the other hand, the average length per interconnection $\overline{L}$, or the Manhattan length, should be estimated beforehand. A classical estimation method by Rickert is

$$\overline{L} = 0.77 P_P N_C^{0.245} \tag{2.3}$$

where $N_C$ is the number of chips to be interconnected. [8]

The number of I/O pins is another crucial parameter in the design stage of an

MCM. The well-known Rent's Rule gives a very useful estimation on this

$$N_{IO} = ag^b \tag{2.4}$$

In the above equation, if a specific chip is given, $N_{IO}$ is its anticipated number of I/Os; $g$ is its number of gates; $a$ and $b$ are the average connection number per I/O, or the Rent's coefficient, and the Rent's exponent respectively. [9] $a$ and $b$ are determined emperically and several typical values are given below. [10]

**Table 2.1: Rent's coefficients and exponents for specific devices/systems**

| Type | Rent's coefficient, $a$ | Rent's exponent, $b$ |
|---|---|---|
| DRAM | 6.20 | 0.085 |
| SRAM | 6.00 | 0.120 |
| Microprocessors | 0.82 | 0.450 |
| Random Logi | 1.90 | 0.500 |
| Computer Systems | 2.50 | 0.600 |

## 2.3 Substrate

The whole chapter 9 [7]

For any packaging design, the substrate influences almost every part of its overall performance, and as a fact determines the type of the MCM package. In this part, the substrate material and the substrate configuration are introduced, which as two crucial concepts lead to the next chapter's introduction on basic fabrication processes.

MCM-L uses plastic laminate as the substrate, imitating properties of PWBs. (chen2006vlsi, 9.2.1)

MCM-C adopts think-film substrate, or ceramic technologies, including high-temperature cofired ceramic (HTCC) and low-temperature cofired ceramic (LTCC).

MCM-D, the advanced ones compared with the other two categories, uses inorganic dielectrics or organic polymers as the thin-film substrate.

Thin-film packages have evolved to a much greater extent with polymeric materials. The capability offered by polymers include a lower dielectric constant, the ability to form thicker layers with higher speeds, and lower cost of deposition. Polymer dielectrics have been used as insulating layers in recent microelectronics packaging.

The thin-film substrate must have a flat and polished surface in order to build upon. The substrate should be inert to the process chemicals, gas atmospheres, and temperatures used during the fabrication of the interconnect. Mechanical properties are particularly important because the substrate must be strong enough to withstand handling, thermal cycling, and shock. The substrate must also meet certain CTE constraints because it is in contact with very large silicon chips on one side and with the package on the other side [11,12]. Thermal conductivity is another important aspect when heat-generating, closely spaced chips need that eat conducting medium. It is informative to state that high-density, large-area processing has generated interest in glass as a carrier material.

Substrates can be used in a manner similar to PWBs, in which components are mounted onto the assembly. Such configurations are referred to as patterned substrate approaches (Fig.3.14-a is a particular example illustrating distinct interconnecting and mechanical substrates).

A variation of this configuration, sometimes used for power devices, is referred to as the recessed patterned substrate and is shown in Fig.3.14-b. In this case, access holes are formed through the interconnecting substrate, resulting in a

more intimate substrate contact and, therefore, lower thermal resistance.

A fundamentally different substrate configuration results when the interconnection manifold is created over the substrate that contains the components, as shown in Fig.3.14-c. This approach is referred to as patterned overlay. In this case, components are recessed into a planarized substrate, which serves as a starting surface onto which multiple levels of interconnects are created.

The component-attach or element-attach approaches are defined as the explicit schemes for which components are mechanically and electrically attached to the substrate. The relevant approaches which can be used are: wirebonding, TAB & flip-TAB, flip-chip, patterned overlay and with conductive adhesives. The first ones were already presented in the previous lessons. We shall briefly present here only the last ones.

The patterned overlay defines interconnects metallurgically joined to component bond pads as part of the intrinsic process used to form interconnects. Thus, both the substrate and the chip attachment approach are defined simultaneously. Chip scale-packaging approaches employ a similar method, namely wafer-level packaging. One difference between wafer-level approaches and more generalized patterned overlay approaches is that the former is applied to entire wafers, as opposed to heterogeneous arrangements of individual components.

The use of conductive adhesives permits rapid attachment of components to substrates at low temperatures. In conductive adhesives, conductive particles are loaded into a polymer matrix, which, upon curing, forms a conductive bridge. The technique is commonly applied in low-cost, low-performance

# Chapter 3

# Typical Approaches

There are several methods we see today for chip interconnects, such as the MCM method which integrates and interconnects multiple standard ASIC components on a package substrate, the 2.5D package method which integrates ASIC components on a Si or interposer layer (organic material doping), including die-to-die connections between two or more die via an interposer layer. stacking and interconnecting in the z-axis dimension. For commercialization, there should be three options from the EDA provider's point of view: hardcore IP, softcore IP, and Chiplet. The third option is a process that allows Fabless to place the bought hardcore IP on the intermediary layer, laminate or stack it and then interconnect it.

Referring to AMD's previous EPYC processor release: the introduction of the MCM approach to EPYC processor design will require 10% more wafer area than a single die for I/O communication/connection function blocks between bare dies (D2D), redundant logic, and other additional features. In the end, however, the overall processor chip cost is still 41% less than a single-die processor, and as individual die sizes and densities are scaled up, future yields could steadily exceed those of single-die.

The so-called multi-chip module MCM is a chip module constructed by directly adhering and interconnecting multiple bare chips on various material substrates

composed of conductor layers and dielectric layers. In another word, it is incorporating a module composed of multiple chips into one package. The chips may be ICs, diodes, transistors, MOSFETs, or other active components. The point is that all of them are enclosed in the same package.

The term *MCM* is currently overused. Here we would like to give a definition of MCM for classification. If we look at the packaging category based on the electronic component evolution cycle, we can find that packaging one component is called *packaging*, and packaging multiple components is called *multi-chip package* (MCP). When a part of the circuit or a module is packaged, it is called a multi-chip module package (MCM). The main difference between MCP and MCM is whether it is a complete circuit. MCP has only active components, while MCM includes active components and passive components.

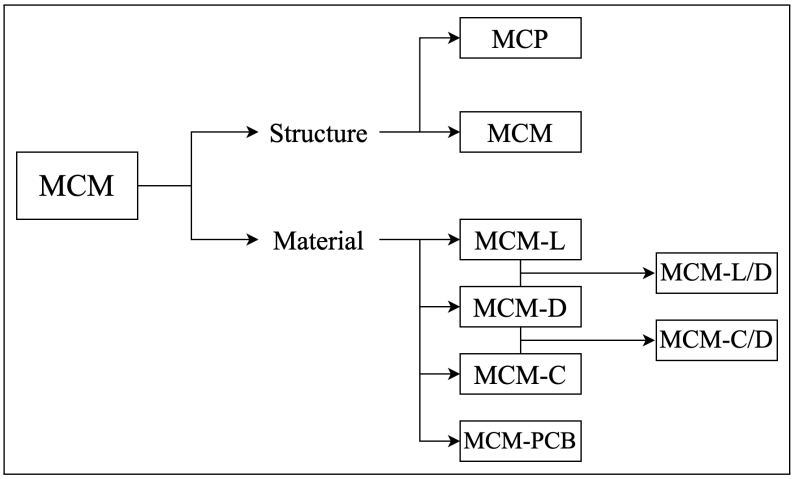


**Figure 3.1: Illustration of MCM categories.**

According to different materials and processes, we can divide MCM into four main categories Figure 3.1.

## 3.1 MCM-L (Laminated) and MCM-L/D

The circuit wires and contacts are formed by deposition or etching on the low temperature co-fired ceramic sheet or metal sheet. Then chips, transistors, and other active components and passive components such as resistors and capacitors are bonded. In order to improve the buried density, it can be combined with MCM-D (so-called MCM-L/D) to achieve higher density by deposition.

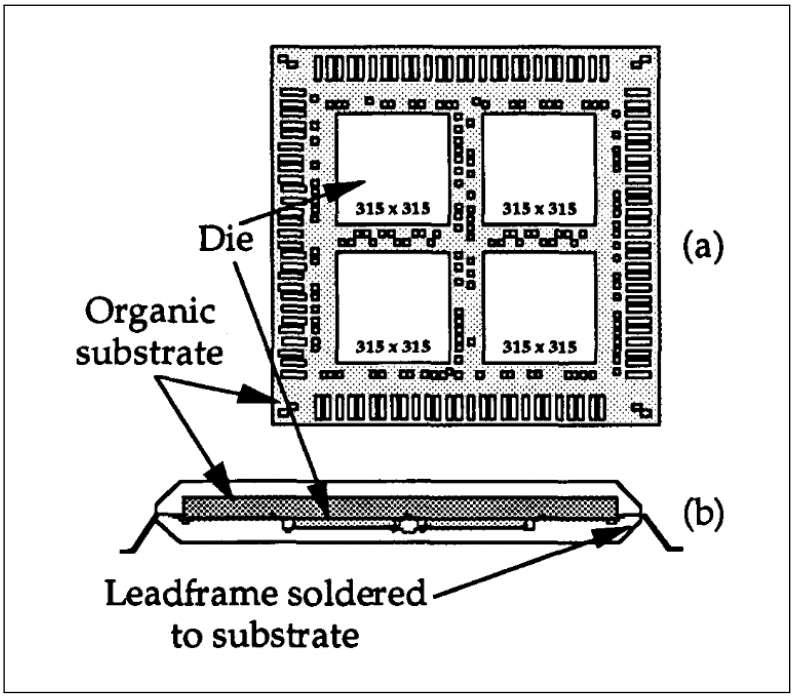


**Figure 3.2: Schematic of MCM-L packaging of four chips.(Ref. [11], Fig. 4 )**

The development of MCM-L involves evolutionary technological advances to reduce interconnects and vias. From the perspective of cost, it is best to use traditional PWB technology for MCM-L manufacturing. However, this becomes more and more difficult because they need a higher interconnect density of multichip modules continues. Since MCM technology is being considered for the application of mass consumer products, it is very important to focus on controlling the cost of high-density MCM-L. The most important characteristic of evaluating

MCM-L technology is the packaging efficiency which is given below.

$$Packaging\ \ efficiency(\%) = \frac{Silicon\ \ chip\ \ area}{Package\ \ area} \tag{3.1}$$

## 3.2 MCM-C (Ceramic), MCM-C/D

It is based on a multilayer ceramic substrate. This method forms wires and contacts in different layers, then, bonds IC, transistors, and other active components, and resistors, resistors, and passive components such as capacitors. In order to increase the buried density, it can be combined with MCM-D (so-called MCM-C/D) to achieve higher density by deposition. MCM-C mainly uses thick film technology (such as combustible metal) to form conductive patterns. It is completely composed of ceramic or glass-ceramic materials, or other materials with a dielectric constant higher than 5. In short, MCM-C is constructed on ceramic or glass-ceramic substrates. The advantages of MCM-C are more wiring layers, wiring density, packaging efficiency, and performance are higher, mainly used for high-reliability products with operating frequency (30-50) MHz.

These ceramics, along with alumina, are fired at high temperatures and require refractory metallization systems, such as tungsten and molybdenum metals. Ceramics fired at temperatures below 1000 ° C can also be used. Low-temperature co-fired ceramics (LTCC) are mainly composed of borosilicate glass systems with gold or silver metallization. MTCC is a new ceramic packaging material system, which uses copper metallization to realize low resistance wiring. These glass-ceramic MCM-C materials show excellent conductivity and good dielectric properties for high-speed transmission lines, which can greatly reduce the propagation delay.

Traditional substrate materials (Al2O3, SiC, etc.) and high temperature sintered ceramics (HTCC) not only have high sintering temperatures (> 1500 ° C) but also can only be co-fired with metals with high melting point and high resistance (Mo, W, etc.), which is not conducive to reducing production costs. Therefore, a new low-temperature co-fired ceramic (LTCC) technology has been developed. Low sintering temperature can make good metal conductors (Cu, Ag, etc.) burn together with a ceramic casting sheet, improve the conductivity of a thick film circuit and reduce the cost.

Due to the development of large-scale integrated circuits and the improvement of IC chip integration, speed and power, it is required to improve the heat dissipation conditions, increase the number of I / O, reduce the interconnect size, reduce the signal loss, reduce the volume of devices and reduce the cost. Therefore, the substrate material must have high thermal conductivity, low dielectric constant, and loss; Multilayer ceramic low-temperature co-fired substrate is widely used because of its simple equipment, low cost, and good matching of thermal expansion coefficient between ceramic components and chip materials, easy metal wiring and so on.

## 3.3 MCM-D (Deposited)

It forms circuit wires and contacts on the substrate by vapor deposition and other methods. Since it can be made into extremely fine line widths, the wiring density is high.

MCM-D uses thin-film deposition technology to deposit metal materials onto ceramic or silicon or aluminum substrates, lithographing signal lines, power lines, and ground lines, and making multi-layer substrates (up to several dozen layers) in turn. It is mainly used in high-performance products above 500MHz, with a

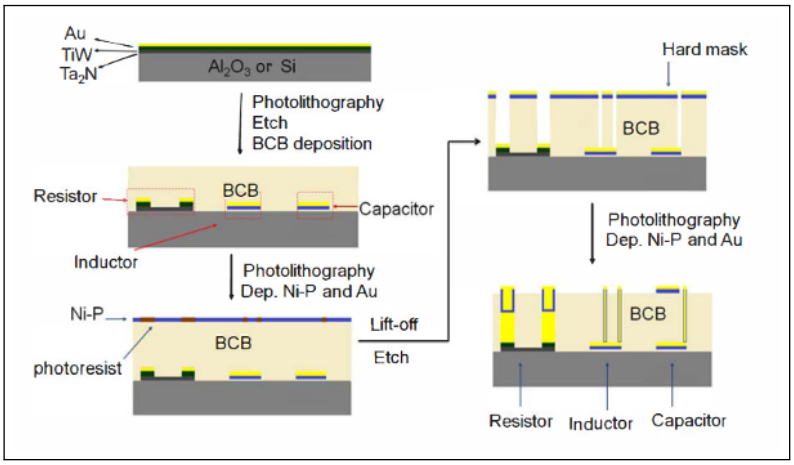


**Figure 3.3: Schematic of MCM-D packaging.**

line width and spacing of 10-25mm μm and an aperture of 1050μm, thus having the advantages of high assembly density, short signal channels, small parasitic effects, and low noise, which can significantly improve the high-frequency performance of the system.

MCM-D is the most expensive of several substrates, mainly because the wiring uses a process similar to that used in chip manufacturing. MCM-D forms the interconnected signal lines of the substrate by depositing a thin metal film. Its substrate multilayer wiring process can be planned as a thin film process. If Si is used as the substrate, i.e. MCM-Si, also using Al as the wiring material, the fabrication process is identical to that of the IC chip, with the main difference being the number of layers of wiring. Generally, the metal wiring of a chip does not exceed two layers, whereas the wiring of MCM-D is usually no less than two layers. The ceramic-based MCM-D wiring process is similar to the conventional thin-film circuit manufacturing process. A typical MCM-d substrate fabrication process is shown below.

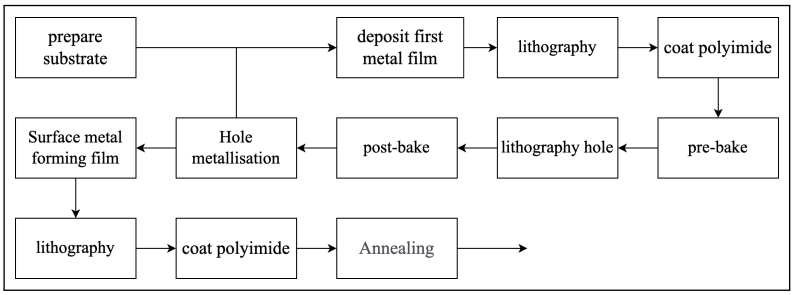


**Figure 3.4: Work flow of MCM-D packaging.**

## 3.4 MCM-PCB

Because ceramic materials are not easy to sinter and produced, and the functions of ceramic substrates many are very similar to PCB multilayer circuit boards, there are also manufacturers who use PCB multilayer circuit boards as the substrate of MCM. However, the moisture absorption of PCB multilayer circuit boards has always been an obstacle to its use in harsh conditions. Furthermore, coupled with the poor heat resistance of PCB multilayer circuit boards, although new materials and processes, and high-density interconnect (HDI) wiring technology, the cost of the plate is low, the processing is convenient, and it has economies of scale, which can already meet the requirements of environmental standards, it is still difficult to break through the traditional application fields dominated by ceramic substrates for a while.

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