EE6610- IC packaging

Assoc. Prof. Poenar Daniel Puiu

APPENDIX 3 after L3b

3- Multichip & 3D packaging (continued)

3.5- Complex assembly structures and 3D systems (continued)

3.5.3- 3D systems (continued)

3.5.3.1- Large-scale join configurations

3.5.3.2- Input/Output location

3.5.4- Die & package stacks

A.1- Large-scale join configurations

Electronic assemblies that are densely packaged can be joined in one of ***three basic orientation styles***, as shown in Fig.A.1:

a) The edge-plane connection (Fig.A.1-a): ***the edges of a stacked electronic assembly engage a planar surface orthogonally at regular pitch spacings****. This results in contacts formed on the edge of the spaced assemblies on two contacts/pads that exist on a planar surface area*. Edge-plane connections are commonly found in motherboard-to-daughtercard assemblies.

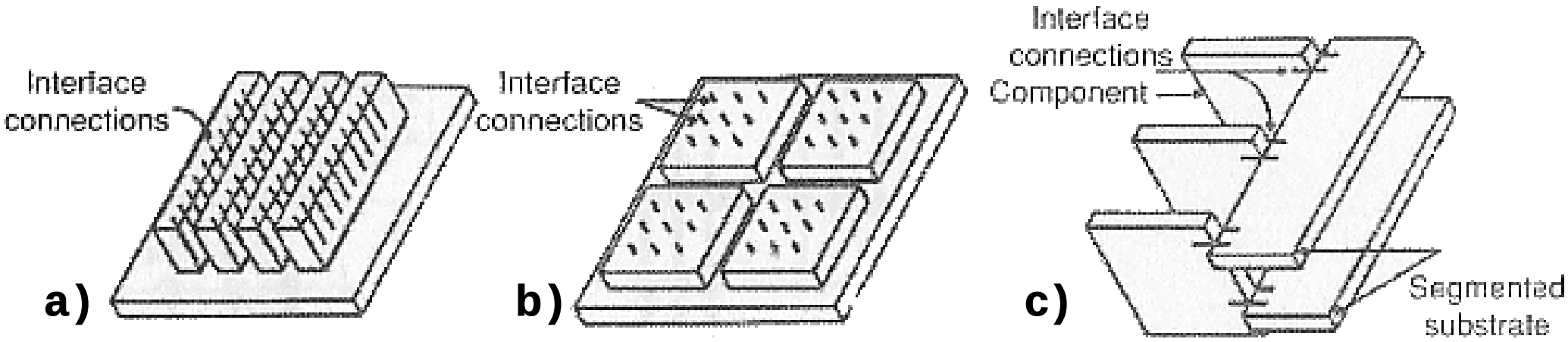


Fig.A.1: Joining configurations for 3D assemblies: a) Edge-plane; b) Plane-plane; c) Edge-edge.

b) **The plane-plane connection** (Fig.A.1-b) *takes advantage of the planar surface area of two different assemblies that are mounted so that at least part of the overlapping surfaces can be dedicated to contact distribution*. It has the advantage of ***greater surface area for contacts***. In mezzanine assemblies, which can be viewed as a stack sequence of plane-plane connections, 3D arrangements are also possible.

c) ***Edge-edge contacts*** (Fig.A.1-c): ***two sets of regular assemblies consisting of a sequence of stacked circuit layers can be abutted so that their edge surfaces come into contact***. *The engagement angles can be varied, which produces an arrangement such that signals from a layer of one set can be broadcast to any or all layers of the second set*. Such arrangements can be useful in communication routing applications.

A.2- Input/Output location

There are two basic possibilities to arrange input/output (I/O) terminals on each of the constituent stacked elements (boards, MCMs, packages, die):

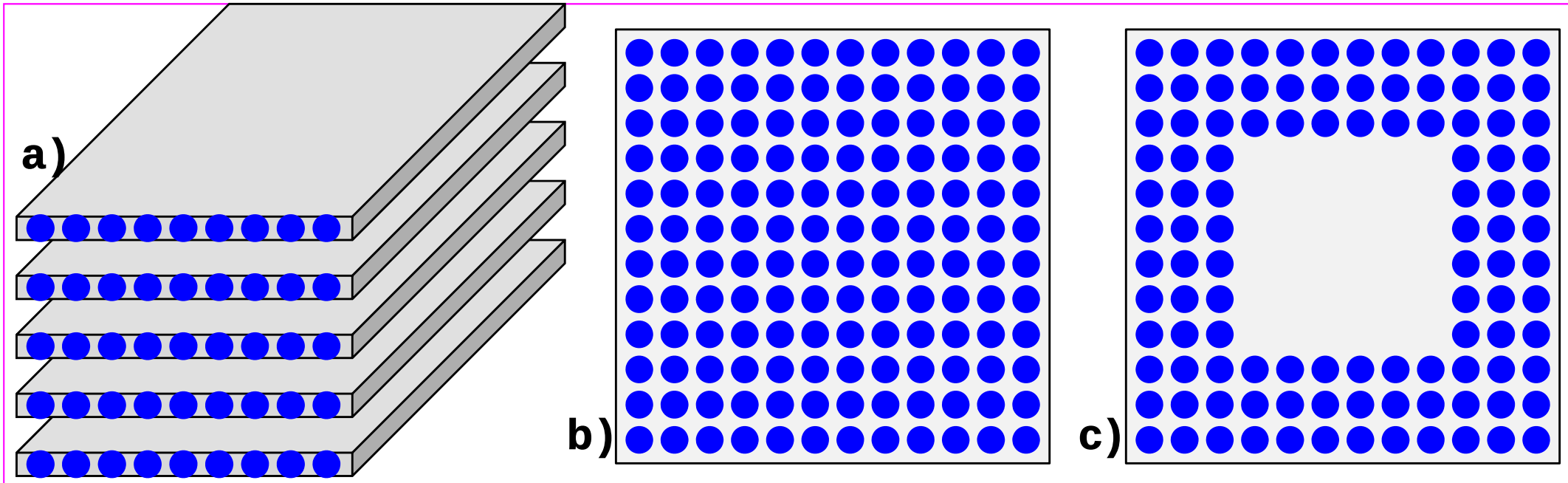


Fig.A.2: I/O configurations for 3D assemblies: a) Perimeter; b) Areal, and c) Border.

perimeter and *areal*, with a third one (*border*) being a variation of the 2nd one. Fig.A.2 shows these possible I/O configurations.

a) The perimeter I/O configuration: ***applies to edge-plane connections and involves the arrangement of conducting terminals on the edge surfaces of stacked elements***.

Advantage: *very compact, since no additional vertical headroom is taken up by interconnect structures*.

Disadvantage: since this approach is limited to only perimeter contact schemes, it is difficult to build structures with very many I/O. This disadvantage can be mitigated by adding multiple rows of conductors on each edge surface, although this technique results in increased complexity of the elemental assemblies.

b) The areal I/O configuration: ***applies to*** **plane-plane** ***connections, and distributes the I/O contacts across the top and bottom surface area of an assembly***. This scheme ***permits the formation of 3D stacks with very high theoretical I/O densities*** when a mezzanine-style construction is involved.

c) The border I/O configuration is a slight variation of the areal scheme: ***I/O pads are restricted to the border region of a planar surface***. Usually, the placing of components is confined to the resulting space within the annular frame. This scheme is ***simpler to implement since it avoids some of the obvious practical problems in combining the placement of I/O pins and components***.

The previously mentioned **plane-plane (face-to-face)** ***contact geometry provides the greatest amount of overlap geometry between two elements of a 3D assembly***, and this overlapping region *can be densely populated with contacts* between the two elements.

Disadvantage: *Difficulties occur in cases where* ***pass-through connections*** *are required. These are routing requirements for signals that pass through to nonadjacent layers, and as such they are not strictly useful to the element containing the contacts for these connections.*

These complications can be minimized by rearranging the various layers by placing in neighbouring positions the elements that need to contact one another. As an example, Fig.A.3-a shows the case of a five-layer stack of plane-plane connected elements, in which contacts unique between element 2 and element 4 must traverse through element 3, for example. In this case reordering is used to reduce the number of pass-throughs, as shown in Fig.A.3-b. *In some cases, it may be advantageous to use instead the edge-plane connection scheme or even combine both these methods*.

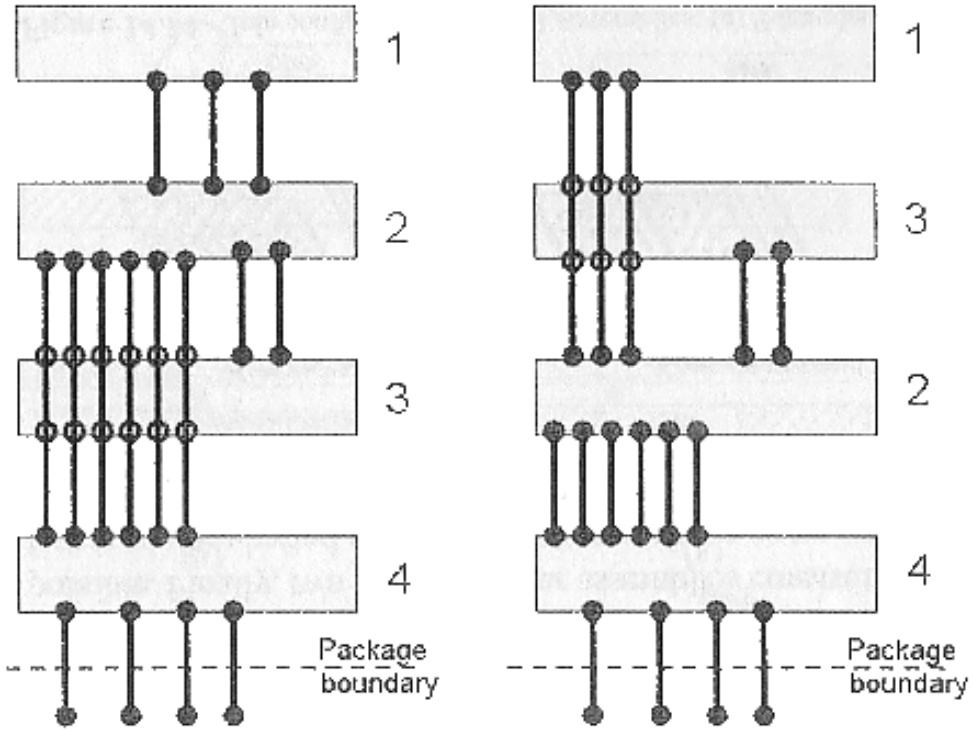


Fig.A.3: Reducing pass-through connections in a vertical stack of elements interconnected using the plane-plane approach:
a) Initial configuration; b) Reordered configuration that minimizes the number of pass-throughs.

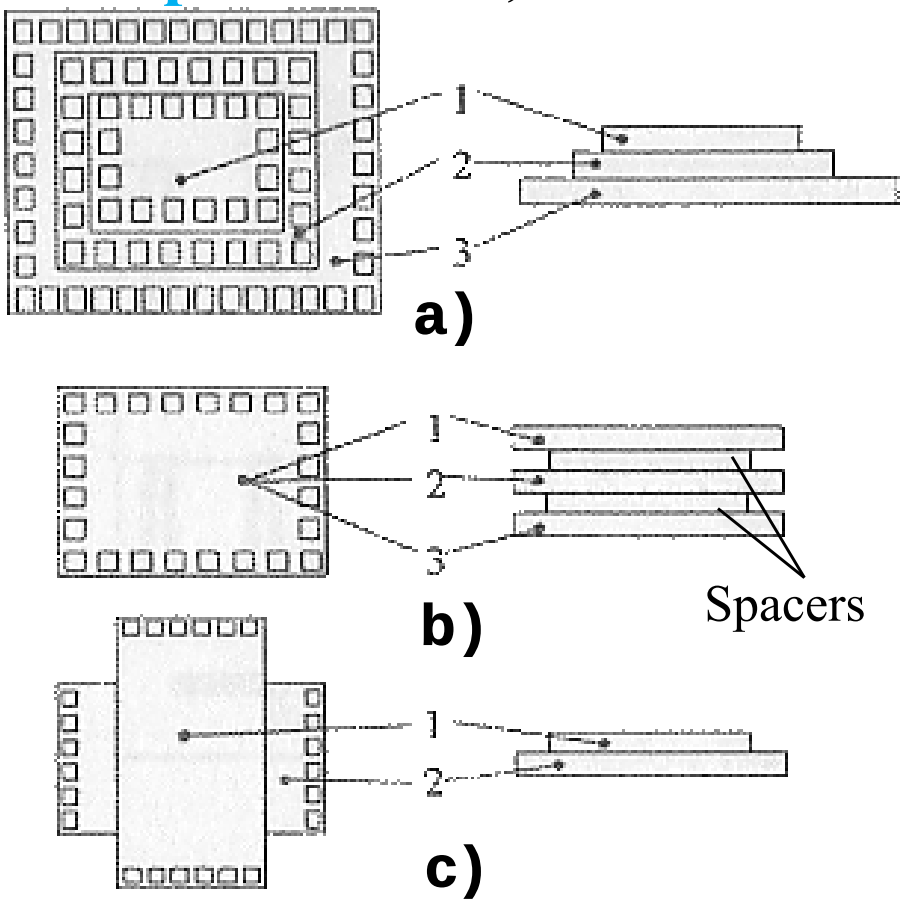
A.3- Die & package stacks

Die/package stacks seek to exploit the floorplan of a substrate in the most effective way. These approaches typically do not feature a special substrate but rely on relatively simple connection schemes, such as multiple tiers of wirebonds.

The classification of various types of die-stacking can be done as a function of the four basic elements or dimensions in its composition:

a) Layer configuration,
b) Connective relationship,
c) Type of attaching element used *and* ***d) Role of substrate,*** .

(A) The layer configuration *identifies the relationship of the shapes of individual elements making up a stacked IC or package.* There are **3 basic possibilities**, as shown in Fig.A.4. In all of these approaches, the



A.4 3D die layer configurations: a) Telescopic, b) Homogeneous, c) Staggered.

GOAL remains the same: *Expose all necessary bond pad surfaces of each stacked element and do so in the minimal amount of volume*.

A.1- In the **telescopic approach** increasingly smaller dies are arranged above larger dies.

A.2- The **homogenous arrangement** (Fig.A.4-b) is useful in assemblies based on regular components. Shown in illustration is the introduction of spacers, which provide headroom

for wirebonding. When wirebonding is not employed, the spacers may not be necessary.

A.3- In the **staggered approach** the dies are arranged so as to expose different parts of a die at different levels for easy wirebond access.

(B) The connective relationship between the elements of a stacked die or package are, in many cases, a very sophisticated system of point-to-point connections. For this case, without a more elaborate interconnecting substrate, there are **two basic possibilities**, as shown in A.5, using wirebonding maps for illustrative purposes:

B.1- Bond pads at one vertical level of a stack are completed by connection to a vertical **nearest** neighbor (Fig.A.5-a). This scheme amounts to an **intrastack or relative bonding**. *In the illustration, all of the connections are* ***shared****, meaning that each bond*

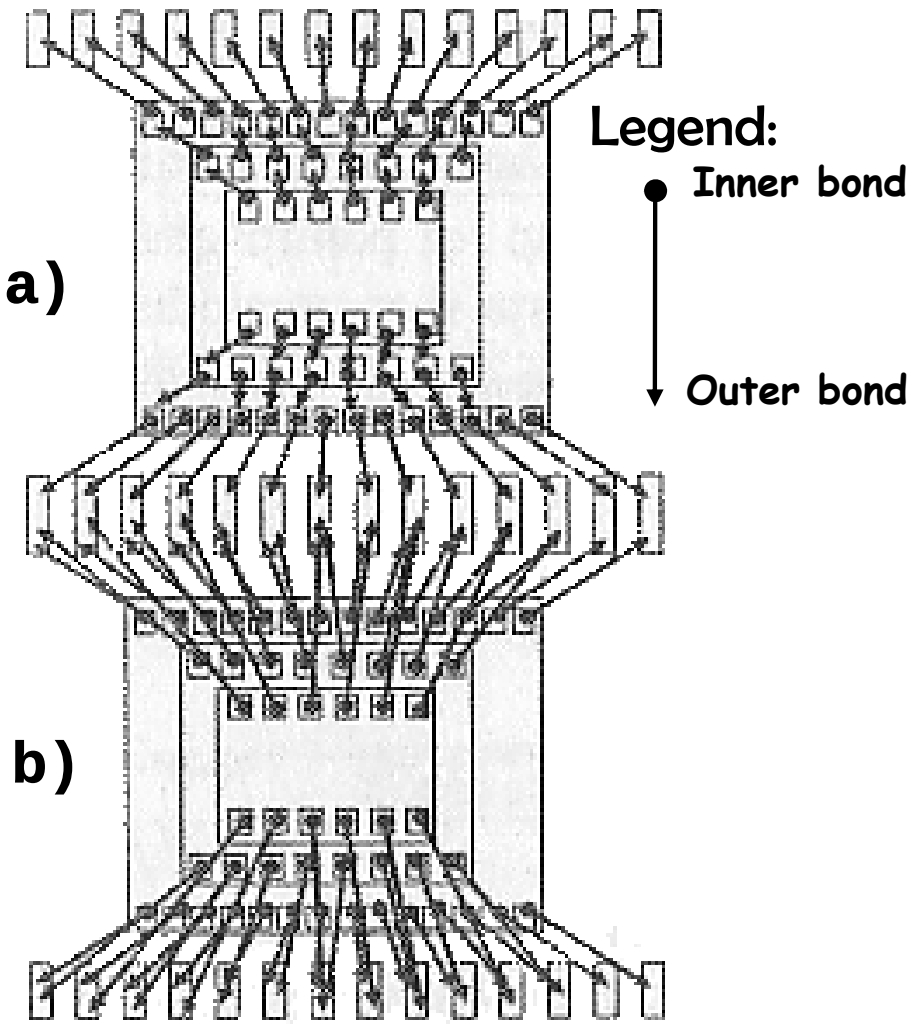


Fig.A.5: 3D die bond-out schemes:
a) Relative, or intrastack;
b) Absolute, or direct substrate.

pad from a different level connects to a bond pad that connects to yet another level. This is not a strict limitation, as individual bond pads can be dedicated to separate connections between each layer. Dedicated pads are minimized due to the obvious reduction of die surface area available for overlap and for placement of active circuitry. Another application of relative connections occurs when a vertical stack is placed very close to another die or vertical stack sharing a common mechanical substrate. In this case, wirebonds can bridge across and connect, similar to the approaches used in multicomponent packages.

B.2- The absolute or direct substrate connection (Fig.A.5-b)

does not employ intermediate connections but directs that all outer bond connections be made to a common substrate. This approach is ultimately **limited in the number of layers** that can be accommodated. **Each additional layer ↑ the average wirebond length and substrate footprint while ↓ yield**.

A few practical examples of wirebonded die stacks based on combinations of layer arrangements and bond-out schemes are shown in Fig.A.6, demonstrating the aforementioned absolute and relative bonding approaches. The most dominant form of 3D packaging is a two-die chip stack using a telescoping or staggered arrangement and direct substrate bonding. Notice that in Fig.A.6-b the long edges of the chips should not contain any bond pads in order to simplify the bonding by eliminating the possibility of entangling wirebonds of components on 2 different levels. On the other hand, the approach shown in Fig.A.6-c requires bond-over-bond

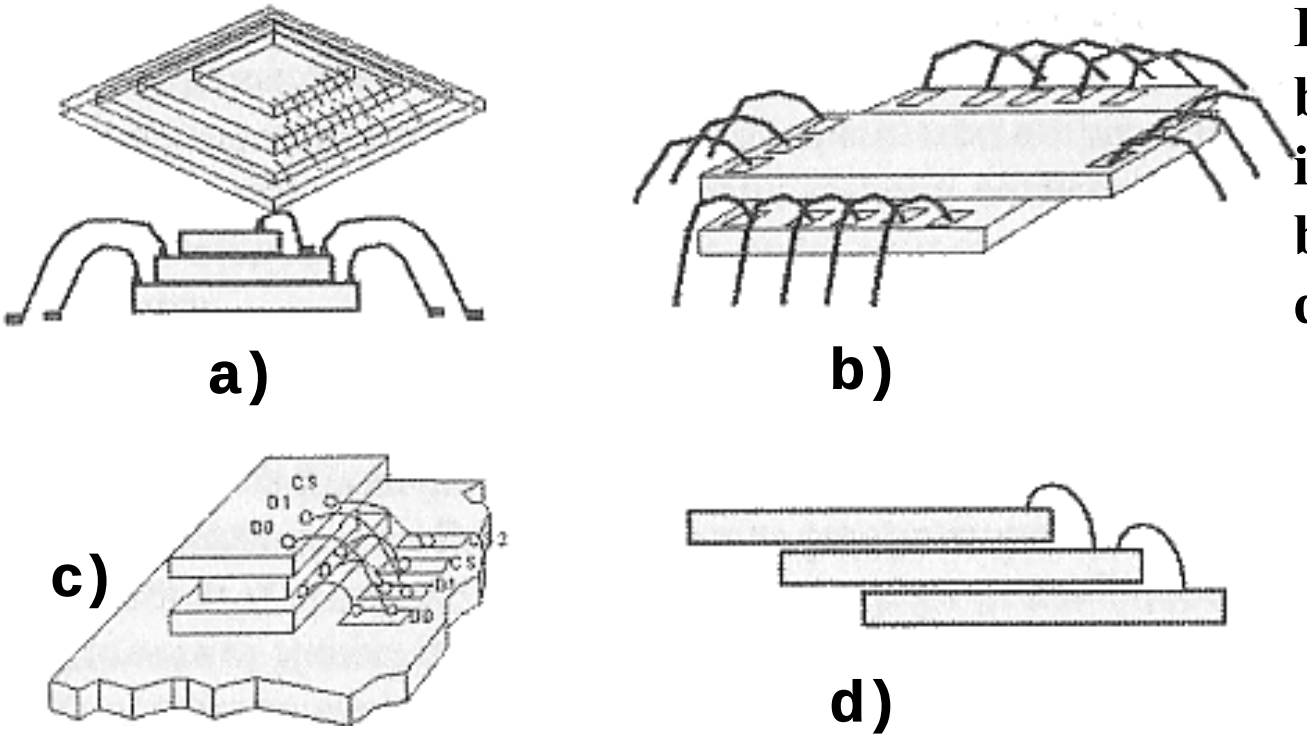


Fig.A.6: 3D IC stacking methods based on wirebonding interconnection: a) Telescoping, b) Staggered bond-out, c) Spacer, d) Staggered staircase.

connections which can be considerably complex, requiring different types/thicknesses of bond wires based on the length and/or orientation of individual bond wires. Fig.A.6-c also demonstrates the role of spacers in a homogeneous stack. Finally, Fig.A.6-d demonstrates an unusual stair-step arrangement of die using a combination of die staggering and relative die bonding.

(C) The approach used for attaching & interconnecting the elements in stacked/3D configurations. The possible methods are:

C.1- Wirebonding: has been considered in all previous examples.

C.2- TAB approaches, e.g. the **3D Plus method**: *TAB frames are stacked, potted, and then cut and polished to form flat-edge surfaces, which are then patterned*.

C.3- Micro-Z ball stack method (Fig.A.7): *individual dies are joined bond-side down onto individual accessory substrates. Interior ports are cut into the substrate and individual die bonds are formed through this portal. The finished layers are then stacked using BGA connections patterned on the border of each substrate. The BGA of the final level becomes the contacts of the primary package*.

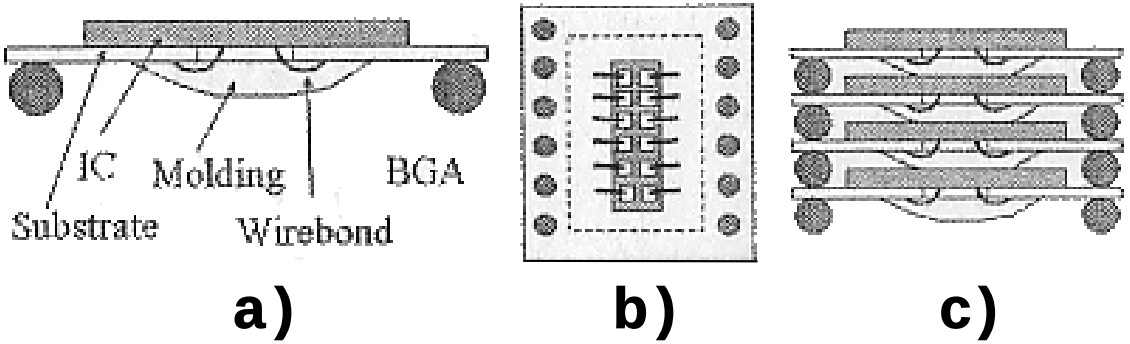


Fig.A.7: The Micro-Z ball-stack technology: a) Cross-section of a single layer; b) Plan view; c) A 4-die stack.

C.4- Flip-chip technology: The most natural method involves a simple chip-on-chip stack in which one or more small dies are face-down bonded onto a larger die, creating a simple two-level stack.
Additionally, flip-chip and wirebonding can be combined in the same stack. In one scheme, a flip-chip die is attached to a substrate. Then a simple die stack, such as a two-die or three-die chip stack, can be simply glued onto the mounting surface created by the backside of the mounted flip-chip component. It is also conceivable that face-to-face flip-chip mounting arrangements can be substituted for the spacers concept shown in Fig.A.6-c. Such a scheme could ↑ the effective density by replacing the otherwise inert spacers with active silicon.

C.5- Overlay patterning approaches (at die or wafer level) enable direct stacking of dies without spacers (if the respective dies are also designed for this purpose!). In this case the

patterned overlay provides **two functions**: ***bond pad repatterning*** (for die of dissimilar size and shape) and ***insulation between stacked levels***. The bond pad repatterning step provides a means to route surface pads to one or more edges. The stacked assembly must be completed by forming an edge overlay to connect layers together.

D) The role of the substrate. *All previous schemes (except the Micro-Z ball approach) use a single substrate*. One way to ↑ **density** is to *use the single mounting substrate as a mirror plane and attach another stack at the bottom of the substrate*. This approach is straightforward in cofired ceramic packages where two cavities are formed. Using this scheme, die stacks containing up to 8 layers have been formed.