

YANJUN YANG

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EDUCATION

The University of Edinburgh

PhD Student in Engineering, Centre for Electronics Frontiers

Sept, 2022 - present

Edinburgh, Scotland

- Supervisors: Dr Alex Serb, Prof Themis Prodromakis
- Research theme: Cognitive processing system implementation based on associative memories

Nanyang Technological University

MSc (Electronics)

Aug, 2021 - Aug, 2022

Singapore

- Core units taken: Digital Integrated Circuit Design, Electromagnetic Compability Design, Genetic Algorithms and Machine Learning, Advanced Wafer Processing, Integrated Circuit Packaging

Tongji University

BEng. in Electronic Science and Technology

Sept, 2017 - July, 2021

Shanghai, China

- Core units taken: Design and Analysis of Digital Integrated Circuits, Computer Architecture, Principles for Design of Integrated Circuit Chips, Embedded Systems

CURRENT PROJECTS

ASOCA3-FPGA

The University of Edinburgh

Jan, 2024 - present

PhD Sub-project

- Developing a high-performance graph database accelerator on FPGA at million-entry level
- Project leader in architecture and system design

ASOCat

The University of Edinburgh

Sept, 2022 - present

PhD Sub-project

- Building a Copycat-based cognitive model compatible with an associative memory chip
- Designing and implementing its software/hardware interface

PUBLICATIONS

A Resource-efficient Dually-addressable Memory Architecture on FPGA

ISCAS 2025

May, 2025

London, United Kingdom

- Presented a resource-efficient BRAM-based DAM architecture on FPGA
- Implemented onto Virtex-7/Virtex UltraScale+ FPGAs with 100% storage efficiency

A Modular Graph Database Accelerator

ECML PKDD 2024

September, 2024

Vilnius, Lithuania

- Presentation in 2nd International Workshop on Deep Learning meets Neuromorphic Hardware

A Single-layer Wideband Microwave Absorber with Reactive Screen, and A Novel Design of Microwave Absorber for Reduction of Radar Cross Section

AP-S/URSI 2020

July, 2020

Montréal, Canada

- Carried out antenna simulation under HFSS and experimental data analyses

RESEARCH EXPERIENCE

Saliency detector

The University of Edinburgh, STMicro

Feb, 2024 - July, 2024

PhD Sub-project

- Developed a hybrid defect detection and classification prototype
- Produced a result analysis and development report

ASOCA2

The University of Edinburgh

Nov, 2022 - Dec, 2023

PhD Sub-project

- Successful tape-out of a memristor-based associative memory SoC
- Core digital hardware developer and verification engineer

ReMap: a Mitchell-based logarithmic conversion circuit

Nanyang Technological University

Aug, 2021 - July, 2022

MSc Dissertation Project

- Optimised a Mitchell-based binary logarithmic approximation method
- Implemented and evaluated corresponding integrated circuits

Design of a hierarchical memory management mechanism

Tongji University

Aug, 2021 - Jan, 2022

Part-time Internship

- Led a hierarchical SRAM-flash interface design with page replacement algorithm
- Applied the design on an automobile-orientated MCU

CoNM: Core of Normal Microarchitecture

Tongji University

Mar, 2021 - Jun, 2021

Graduation Design

- Designed a four-stage RV32I CPU core with static branch prediction in Verilog
- Implemented onto PYNQ-Z1 FPGA board for a successful verification

PROFESSIONAL SKILLS

Familiar with both FPGA and digital ASIC design flows.

Programming Languages

- Proficient in SystemVerilog/Verilog
- Skilled in Bash, Tcl, Python
- Competent in C/C++, VHDL
- Developing skills in CHISEL

Professional Software

- Skilled in Synopsys, Vivado, Cadence
- Good command of MATLAB, ModelSim
- Good knowledge of HFSS, ISE, Keil

Languages

Native in Mandarin and New Xiang, proficient in English

- IELTS 8.0/9.0 (2020), equivalent to CEFR level C1
- Elementary reading proficiency of French

SEMINARS & TALKS

IMNS Seminar

Institute for Integrated Micro and Nano Systems

November, 2024
Edinburgh, Scotland

- Title: Graph Database Acceleration in Digital Hardware

PGR Conference

The University of Edinburgh

April, 2024
Edinburgh, Scotland

- Title: Symbolic Processing Systems Based on Associative Memory

TEACHING

The University of Edinburgh

1st Semester, 2024

- Demonstrator - Digital Systems Design 2 (ELEE08015)
- Marker - Software and Embedded Systems Laboratory 2 (ELEE08022)

The University of Edinburgh

2nd Semester, 2024

- Demonstrator & Marker - Digital Systems Laboratory 3 (ELEE09018)

The University of Edinburgh

1st Semester, 2025

- Tutor & Marker - Digital Systems Design 2 (ELEE08015)
- Marker - Software and Embedded Systems Laboratory 2 (ELEE08022)

HONOURS AND AWARDS

Tongji University

Advanced Summer Internship Individual

1st Semester, 2017

- Awarded for the great performance during summer internship

Tongji University

Outstanding Student Cadre

1st Semester, 2019

- Awarded as the minister of Rights and Welfare Department in Students' Union

INTERESTS

Prefer *Scotches*.

$\frac{1}{2}$ geek, $\frac{1}{2}$ bartender.

Neovim sponsor under WSL2.

Reads Kafka, Hai Zi, and Allan Poe.

Jay Chou, Green Day and Aska Yang fan.

Always plannig to do something in film criticism and lyric writing.