

Recessed Channel Ferroelectric-Gate Field-Effect Transistors with a Dual Ferroelectric Gate Stack for Emerging Memories

Simin Chen, Dae-Hwan Ahn, Seong Ui An, Tae Hyeon Noh, and Younghyun Kim

Abstract— In this study, we propose a novel structure of ferroelectric field-effect transistor (FeFET) that employs gate metal-ferroelectric (FE)-metal-FE-metal-SiO₂ interlayer (IL)-silicon (MFMFMIS) structures, which is called the dual ferroelectric recessed channel FeFET (DF-RFeFET). The proposed device structure is aimed to enhance the memory window (MW) for high-performance memory applications. Through technology computer-aided design (TCAD) simulations with calibrated FE parameters and device models, it has been found that the DF-RFeFET can achieve a larger MW thanks to the enhanced geometric advantage of DF-RFeFET to offer a strong and localized electric field at the inner ferroelectrics near the corner of the gate metal. Moreover, design guidelines for the DF-RFeFET are suggested, including adjusting the inner and outer ferroelectric layers' thickness ratio and the recessed channel depth. The effects of introducing a low-*k* oxide intermediate layer between dual ferroelectric layers and high-*k* gate stacks of IL on the MW have also been investigated. By optimizing the device structures, our proposed DF-RFeFET demonstrated a record MW value of 5.5 V among the previously reported Si FeFETs.

Index Terms— Ferroelectric FETs (FeFET), recessed channel, MFMIS

I. Introduction

DURING recent decades, the demand for memory in servers, data centers, cloud computing, artificial intelligence, and other areas has been increasing. Since the ferroelectricity has been found in the impurity doped HfO₂, such as HfZrO₂ (HZO), HfAlO₂ (HAO), and HfLaO₂ (HLO), the ferroelectric field-effect transistors (FeFETs) are considered as an excellent candidate for fast and high-density emerging nonvolatile memory applications [1, 2]. These applications require

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energy-efficient and fast-speed memory performance. To satisfy these, many studies have been conducted on optimizing the device structure to improve the performance of FeFETs, particularly for memory window (MW) [3-5]. Recently, the recessed channel FeFET (RFeFET) with a metal-ferroelectric (FE)-interlayer (IL)-semiconductor (MFIS) structure has been proposed [6]. In comparison to the planar FeFET, the RFeFET can offer improved memory characteristics by modifying a capacitance ratio between the FE and IL capacitor through the capacitor radius. However, the MFIS-structure RFeFET has the drawback that there is a very narrow window to control the capacitance ratio once the radius of the recessed channel and the thickness of IL/FE are determined [7]. To solve the problem, the RFeFETs with a metal-FE-metal-IL-semiconductor (MFMIS) structure were proposed [7, 8]. The internal metal in MFMIS structure RFeFETs allows a larger window to adjust the IL and FE radius ratio, leading to better voltage division between the IL and FE capacitors.

On the other hand, the thickness of the ferroelectric layer is another important factor that determines the memory performance in FeFETs. While a thicker ferroelectric layer is preferred for the large MW, previous studies revealed that the ferroelectric properties of HZO films begin to degrade when their thickness is above approximately 10 nm due to the formation of a non-ferroelectric phase [9-11]. In addition, the thinner HZO thickness can provide a better endurance characteristic because of their breakdown mechanism [12]. These ferroelectric properties of HZO imply that the capacitance matching between the FE and IL capacitor in the MFMIS gate stack will be restricted by the thickness limitation of the HZO ferroelectric layer. To address these issues, the multi-ferroelectric gate is a promising solution. Recently, the dual ferroelectric gate planar FeFETs with a metal-FE-metal-FE-IL-semiconductor (MFMFMIS) structure were reported, which can increase the MW by changing the area ratio of the MFM and MFIS to adjust their electric fields (*E*-field) across each capacitor [13].

In this study, we propose dual ferroelectric recessed channel FeFET (DF-RFeFET) with metal-FE-metal or IL-FE-metal-IL-semiconductor (MFMFMIS or MFIFMIS) structures. The dual ferroelectric layers are expected to break the limitation caused by thickness-dependent ferroelectric properties in MFMIS structure RFeFETs, resulting in a significant increase in the MW. Using the technology computer-aided design (TCAD) simulation, we quantitatively present our investigation of the enhanced *E*-field distribution in the FE layer and the increase of MW in the MFMFMIS structure DF-RFeFET. The effect of the thickness ratio between

the inner and outer ferroelectric layers on the MW is also examined. We also optimized our device structure by varying the recessed channel depth and introducing low- k insulators as an intermediate layer between dual ferroelectric layers. Finally, we examined the effects of equivalent oxide thickness scaling of interlayer with high- k insulators on our device performance.

II. MODEL CALIBRATION

Synopsys TCAD Sentaurus was used for the simulation with model calibration. First, the simulation parameters were calibrated to the measured polarization (P)-electric field (E) curves of the TiN-Hf_{0.5}Zr_{0.5}O₂-TiN (MFM) capacitor [6], as shown in Fig. 1(a). The Preisach model was used in TCAD simulation to describe the multi-domain features of Hf_{0.5}Zr_{0.5}O₂ (HZO) with the parameters of remanent polarization ($P_r = 20 \mu\text{C}/\text{cm}^2$), saturation polarization ($P_s = 40 \mu\text{C}/\text{cm}^2$), coercive field ($E_c = 0.67 \text{ MV}/\text{cm}$), dielectric constant ($k = 25$) and response time ($T_p = 250 \text{ ns}$). Our simulation results show a good agreement with the polarization characteristics of fabricated ferroelectric capacitors, indicating an accurate calibration of simulation models and parameters.

In addition, the simulated transistor's electrical characteristics were also calibrated using the measured hysteretic Drain current (I_D)-Gate voltage (V_G) curves of the fabricated planar FeFET [6]. The I_D-V_G curves were simulated with a fast V_G sweep from -0.5 to 1.5 V at the drain voltage (V_D) of 0.05 V after applying a gate voltage of $\pm 3\text{V}$ with a duration time of 10 μs for program/erase operation [14]. To obtain an accurate source/drain (S/D) leakage current, including the gate-induced drain leakage (GIDL) component, we used the band-to-band tunneling model [15] and the OldSlotboom model, which takes into account the impact of heavy doping on the band gap narrowing in the S/D region. Fermi statistics was also used. Fig. 1(b) shows that the simulated I_D-V_G curve matches well with the measured data.

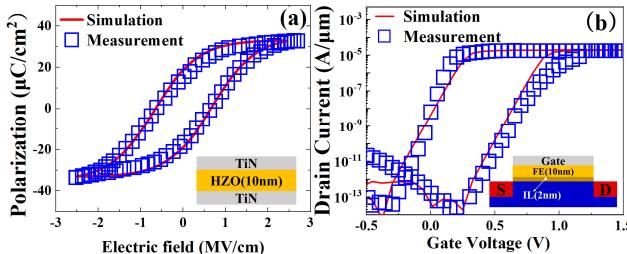


Fig. 1. Measured and simulated (a) P - E curves of MFM capacitor (b) Hysteretic I_D - V_G curves of planar FeFET

III. RESULTS AND DISCUSSION

The schematics of our proposed DF-RFeFET with the metal-FE-metal-FE-metal-IL-semiconductor (MFMFMIS) structure, and single ferroelectric recessed channel FeFET (SF-RFeFET) with a metal-FE-metal-IL-semiconductor (MFMIS) structure are present in Figs. 2(a) and Fig. 2(b), respectively. We adopted an effective channel length of 80 nm (L_{EFF}), an IL thickness (T_{IL}) of 2 nm, and a total FE thickness of 15 nm with the two 1-nm-thick metals. The IL can provide a high interface quality at the oxide/semiconductor interfaces, indispensable for high effective mobility in the field effect

transistor [1]. The internal metal inserted between two FE layers allows for separate control of the inner FE and outer FE thickness ratio. The intensity of E -field distribution in the non-rounded part of the IL leads to a decrease in endurance, thus the equipotential metal is inserted between the outer FE layer and IL to uniform the IL E -field [7]. The detailed device parameters are listed in the table in Fig. 2.

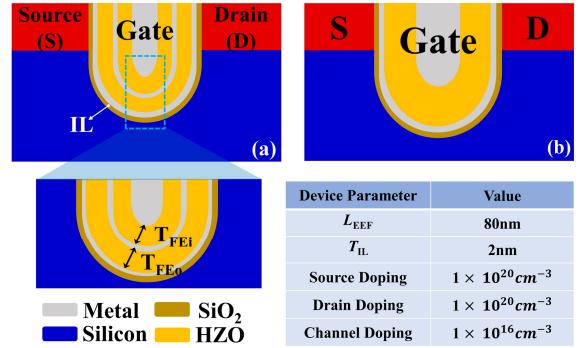


Fig. 2. Structures of (a) our proposed DF-RFeFET, (b) SF-RFeFET, and table with device parameters and values.

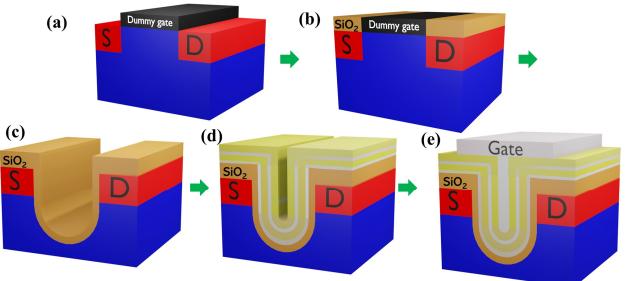


Fig. 3. (a) Dummy gate is formed, and source/drain (S/D) is defined by ion implantation. (b) Interlayer dielectric is deposited and then planarized by chemical mechanical polishing (CMP). (c) The dummy gate is removed, and the round-shaped channel is formed below the S/D by etching the silicon substrate. (d) Sequential deposition of IL/metal/FE/metal/FE by atomic layer deposition (ALD). (e) Metal gate formation.

The fabrication flow of the proposed DF-RFeFET is depicted in Fig. 3. Firstly, a dummy gate is formed by deposited oxide/polysilicon, and source/drain (S/D) is defined by self-alignment ion implantation. Then, the interlayer dielectric is deposited and then planarized by chemical mechanical polishing (CMP). The dummy gate is removed, and the round recessed channel is formed below the S/D by isotropic dry etching of the silicon substrate. Finally, the deposition of metal/FE/metal/FE/gate metal is sequentially filled by atomic layer deposition (ALD). The back-end-of-line (BEOL) process, which is identical to the conventional CMOS process, is skipped here.

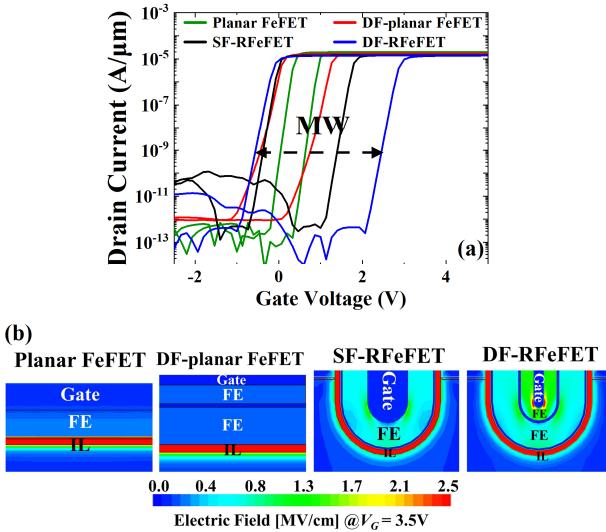


Fig. 4. (a) Hysteretic I_D - V_G curves with V_G sweeping range from -2.5 to 5 V (b) E -field contour extracted at $V_G = 3.5 \text{ V}$.

To investigate the memory characteristics of the proposed DF-RFeFET, we compared the hysteretic I_D - V_G characteristics of planar FeFET, the dual ferroelectric planar FeFET (DF-planar FeFET) with a metal-FE-metal-FE-insulator (MFMFIS) structure, and the SF-RFeFET in Fig. 4(a). The gate voltage was swept from -2.5 V to 5 V at $V_D = 0.05 \text{ V}$. Prior to the gate voltage sweeping, the rectangular pulses with amplitudes of $\pm 5 \text{ V}$ and duration time of $10 \mu\text{s}$ were applied to the gate for program/erase operation. The MW was extracted by analyzing the threshold voltage shift resulting from the program/erase operation. Here, the threshold voltage is defined as a gate voltage at $I_D = 10^{-9} \text{ A}/\mu\text{m}$.

The DF-planar FeFET presents an improved MW in comparison to the single ferroelectric planar FeFET. The MW of the FeFET is determined primarily by the coercive electric field (E_c) and the thickness of the ferroelectric layer (T_{FE}), as expressed as follows.

$$MW = 2E_c \cdot T_{FE} \left[1 - \frac{2E_c \cdot \epsilon_{FE} \cdot \epsilon_0}{P_s \cdot \ln \left(\frac{1 + P_r/P_s}{1 - P_r/P_s} \right)} \right] \quad (1)$$

, where ϵ_{FE} and ϵ_0 are the relative permittivity of the ferroelectric and vacuum permittivity, respectively, and P_r and P_s are the remnant polarization and saturated polarization, respectively. The equation reveals that the thicker FE layer increases the MW.

However, the subthreshold swing (S.S.) of DF-planar FeFETs degrades due to the lowered gate controllability of the dual FE gate. For highly scaled FETs, high gate controllability is required to prevent the short-channel effects (SCEs). Therefore, the utilization of the multi-ferroelectric gate in planar structure FeFETs may be constrained due to the decrease in gate controllability.

On the other hand, the SF-RFeFET with a recessed geometry presents a larger MW than the DF-planar FeFET even though SF-RFeFET has a single ferroelectric gate. In addition, it is

found that our DF-RFeFET not only achieves the largest MW but also maintains the excellent S.S. characteristic at the recessed structure and the dual ferroelectric gate stack ($T_{FEi} = 5 \text{ nm}$, $T_{FEo} = 10 \text{ nm}$). For quantitatively understanding the reason for the improved MWs and excellent S.S. in DF-RFeFETs, the E -field contour profiles of the four device structures at $V_G = 3.5 \text{ V}$ are examined as in Fig. 4(b). While the planar structure FeFETs exhibit a uniform E -field in the gate oxide, the E -field distribution in both RFeFETs is non-uniform, indicating that the recessed channel geometry significantly influences the E -field distribution in the ferroelectric layer. The RFeFETs present a strong and localized E -field region near the corner of the metal gate, which contributes to an improvement in the MW and S.S. characteristics [16, 17]. Importantly, it is found that the geometrical advantage of the recessed channel is further enhanced in the dual ferroelectric gate. Particularly, the localized E -field intensity in the inner FE layer is considerably enhanced and their area increases near the corner of the metal gate with a small radius, resulting in a substantially enhanced MW and excellent S.S. characteristics for the DF-RFeFET.

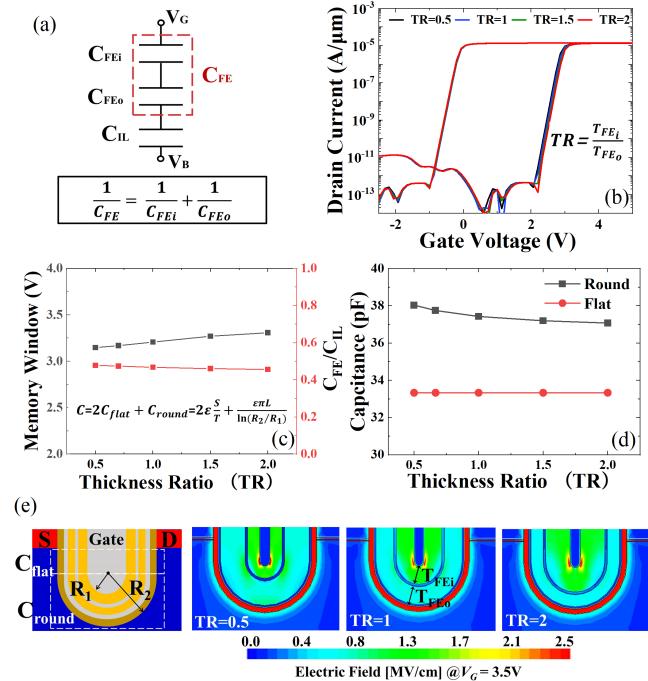


Fig. 5. (a) Equivalent circuit model of MFMFIS. (b) Hysteretic I_D - V_G curves with the different TRs. (c) MW and capacitance ratio with different TRs. (d) Recessed and flat capacitance with different thickness ratios (e) E -field contour with the different TRs extracted at $V_G = 3.5 \text{ V}$.

The recessed channel geometry is a useful structure to modify the FE to IL capacitance ratio (C_{FE}/C_{IL}) shown in Fig. 5(a) by varying the radius of each capacitor. This capacitance ratio plays a crucial role in determining the voltage drops across the respective oxide, thus influencing the MW of RFeFETs. In the case of our DF-RFeFET, the thickness ratio (TR) between the inner ferroelectric and outer ferroelectric layers is an important parameter to control the capacitance ratio [18]. Hence, we conducted a simulation study to further investigate the effect of the TR on MW. The calculated I_D - V_G curves of DF-RFeFETs with different TR values are shown in Fig. 5(b).

The MW very slightly increases as TR increases. The C_{FE}/C_{IL} is calculated using the capacitance calculation formula in Fig. 5(c). The C_{FE}/C_{IL} also slightly decreases as TR increases. It leads to an enhancement of the FE E -field, which results in an increased MW in DF-RFeFETs. The slight increase of MW can be understood in Fig. 5(d), where the change of capacitance mainly comes from the rounded region, and the flat region of capacitance remains constant. As depicted in Fig. 5(e), it can be also observed that the E -field distribution in the FE layers remains nearly constant. Note that the thickness ratio variability due to fabrication process variation will not lead to performance variability for the structure.

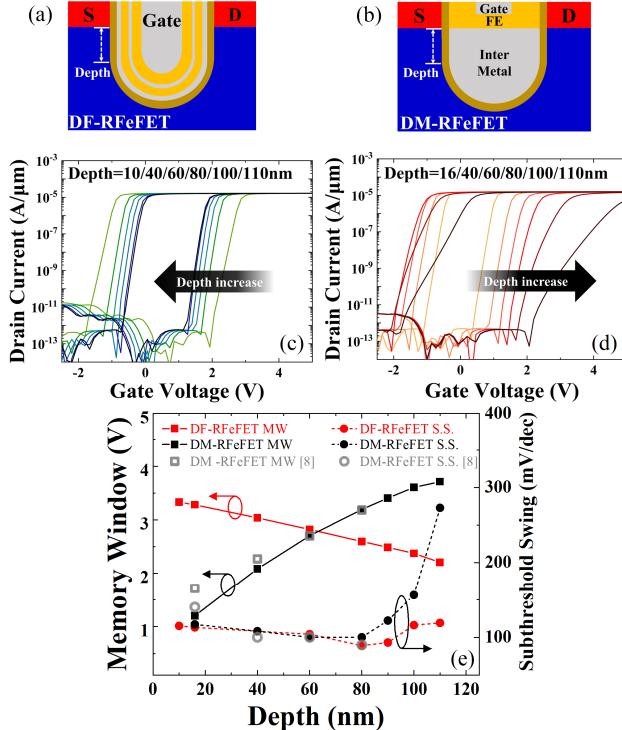


Fig. 6. Schematic images of the depth in (a) DF-RFeFET and (b) DM-RFeFET. Hysteretic I_D - V_G curves with the different depths in (c) DF-RFeFET and (d) DM-RFeFET, the arrow in the diagram indicates the direction of increasing depth. (e) Memory window and S.S. comparisons between DM-RFeFET and DF-RFeFET as a function of depths.

As discussed above, the rounded region in the DF-RFeFET contributes to the determination of the capacitance ratio between the FE and IL capacitors does not significant. Meanwhile, the depth in the flat region of the recessed channel can change the capacitance ratio between the FE and IL capacitors in the RFeFET [8]. We comprehensively studied the effect of depth on both DF-RFeFET and DM-RFeFET, with the depths varying from 10 to 110 nm. The device structures and simulation results of DF-RFeFET and DM-RFeFET are illustrated in Fig. 6(a), 6(c), and Fig. 6(b), 6(d), respectively. Notably, as the depth increases, the MW of DF-RFeFET presents a decreasing trend in Fig. 6(c). In contrast, the MWs of DM-RFeFET exhibit an opposite behavior, implying an enhancement in its performance with increasing depth in Fig. 6(d). However, it is important to highlight that the S.S. of DM-RFeFET experiences significant degradation with an increase in depth, which will be elaborated upon in Fig. 6(e).

Here, a more detailed comparison between the two devices can be observed in Fig. 6(e). In addition, model calibration is carried out to ensure a fair comparison by matching the results with previous studies [8]. Before reaching an 80-nm depth, the S.S. exhibits a steeper slope as the effective channel length increases and the impact of SCEs decreases [19]. After reaching an 80-nm depth, the S.S. of DM-RFeFET significantly increases due to weaker channel controllability resulting from the reduced E -field of the IL [20]. Moreover, previous research has indicated that deeper recessed depths lead to curvature-related issues, which can adversely affect threshold voltage, S.S., and body effects [21]. Correspondingly, our proposed DF-RFeFET exhibits better characteristics, such as larger MW and steeper S.S., particularly at shallower depths. Therefore, it would be better to use DF-RFeFET with less depth.

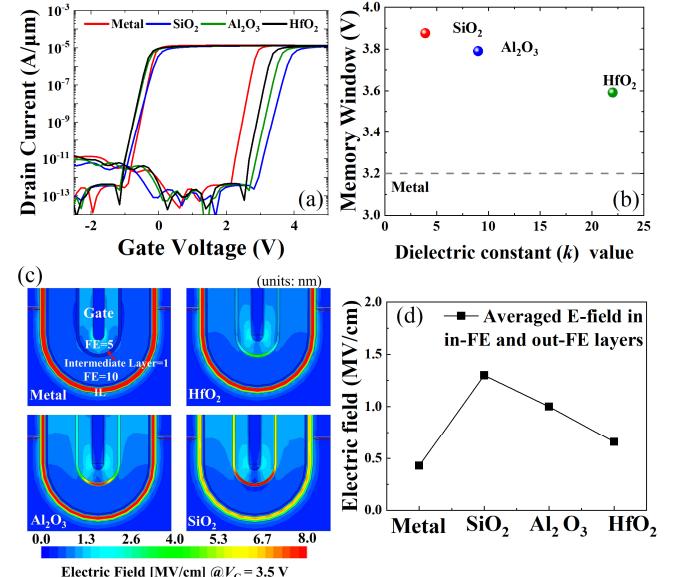


Fig. 7. (a) Hysteresic I_D - V_G curves with the different intermediate layer. (b) MW with the different intermediate layer. (c) E -field contour, and (d) change of averaged E -field across the FE with the dielectric constant of intermediate layer variations.

The key concept of our DF-RFeFETs is to utilize the strong and localized E -field distribution in the inner ferroelectric layer, which arises from the geometrical effects of the recessed channel and improved capacitance matching between the FE and IL capacitors by double ferroelectrics. To optimize our device structure, we additionally simulated DF-RFeFETs with different intermediate layers including metal, SiO₂, Al₂O₃, and HfO₂, which are usually used as intermediate layers [11, 22, 23]. The I_D - V_G curves and MW of DF-RFeFETs with the four intermediate layers are shown in Figs. 7(a) and (b). It is shown that the DF-RFeFETs with oxide intermediate layers achieve a larger MW than those with a metal intermediate layer. Moreover, the MW increases as the dielectric constant (k) decreases. This result can be explained by the E -field distribution, as shown in Fig. 7(c). The inserted low- k intermediate layer leads to a significant voltage drop across the intermediate layer, whereas the voltage drop across the IL decreases. According to Gauss's law, the significantly

increased E -field across the low- k intermediate layer influences the adjacent ferroelectric layers, specifically resulting in an increase in the E -field within the inner ferroelectric layer. Also, a smaller TR will result in an intermediate layer close to the gate making its E -field stronger, thus enhancing the E -field of the inner ferroelectric layer. In addition, it is noticeable that a decrease in the E -field across the IL is advantageous for the superior endurance performance of FeFETs. Fig. 7(d) shows an averaged E -field across the inner and outer ferroelectric layers with various intermediate layers. It is further observed that the low- k intermediate layer increases the average E -field across the inner and outer ferroelectric layers. Therefore, we could conclude that the low- k intermediate layer improves the E -field distribution correlated with the geometrical effects of DF-RFeFETs, leading to a significant improvement in MW for the DF-RFeFETs.

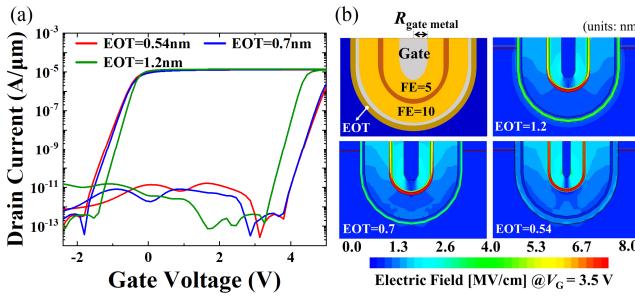


Fig. 8. (a) Hysteric I_d - V_G curves with the various high- k gate stack. (b) Schematics of EOT for the DF-RFeFET and E -field contour extracted at $V_G = 3.5$ V with the different EOTs.

TABLE I
PARAMETER OF VARIOUS HIGH-K GATE STACKS

High- k gate	EOT [nm]	k	T_{IL} [nm]	$R_{\text{gate metal}}$ [nm]	Ref.
SiO_2	1.2	3.9	1.2	2.8	[25]
SiON	0.7	6	1	3	[26]
$\text{SiO}_2/\text{HfO}_2$	0.54	-	2.4	1.6	[27]

Finally, we optimized the IL of DF-RFeFETs based on a SiO_2 intermediate layer. The gate leakage current is considered because it can cause significant standby-power consumption [24]. In addition, the gate leakage current based on direct tunneling via thin IL can lead to metal charging, which can reduce MW and degrade endurance characteristics [7]. The effect of different high- k gate stacks on MW is explored in Table I., which achieves acceptably small gate leakage [25-27]. Varying the thickness of IL while keeping the recess dimension the same. As shown in Fig. 8(a), MW increases as equivalent oxide thickness (EOT) decreases, and the maximum can reach 5.5 V at EOT = 0.54 nm. This can be explained by the enhancement of the FE E -field, especially in the inner ferroelectric layer, as shown in Fig. 8(b). It is also expected that thin EOT can improve the endurance performance of DF-RFeFET because the E -field across the IL decreases.

We compared the MW of our DF-RFeFET with recently reported FeFETs in Table II. The optimized DF-RFeFET achieves an MW of 5.5 V, which is the largest MW among them. Therefore, our proposed structure will be one of the promising solutions for emerging memory applications.

TABLE II
MW COMPARISON WITH DIFFERENT FEFETS STRUCTURES

Ref.	Type	MW [V]
[6]	FeFET	0.6
[6]	RFeFET	1.0
[7]	SF-RFeFET	0.8~2.0
[8]	DM-RFeFET	1.8
This work	DF-RFeFET	5.5

IV. CONCLUSION

In conclusion, we have introduced a novel FeFET structure, DF-RFeFET. Through extensive simulations and analysis using TCAD, we have demonstrated that the DF-RFeFET offers significant enhancements in MW for high-performance memory applications. This is achieved by leveraging the geometric advantage of the DF-RFeFET, which provides a strong and localized E -field within the inner ferroelectrics. The design guidelines have been provided for optimizing the DF-RFeFET, such as adjusting the thickness ratio of the inner and outer ferroelectric layers and the recessed channel depth. Furthermore, we have investigated the impact of introducing a low- k oxide intermediate layer between the dual ferroelectric layers and high- k gate stacks of the interlayer on the MW. By optimizing the device structures, our proposed DF-RFeFET has achieved a remarkable MW value of 5.5 V, surpassing the MW values reported for Si FeFETs in previous studies. These findings highlight the potential of the DF-RFeFET as a promising candidate for future memory applications, providing valuable insights for further advancements in FeFET technology.

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