YANJING LI

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SUMMARY

I am an assistant professor in the Department of Computer Science (Systems Group), University of Chicago. I received my Ph.D. in Electrical Engineering from Stanford University. Prior to joining University of Chicago, I was a senior research scientist at Intel Labs. My research interests lie broadly in the area of computer architecture and systems. I received the DAC Under-40 Innovators Award, Google Research Scholar award, NSF/SRC E2CDA award, European Design and Automation Association (EDAA) Outstanding Dissertation Award, the ACM Great Lakes Symposium on VLSI (GLSVLSI) Best Paper Award, IEEE International Test Conference (ITC) Best Student Paper Award, and IEEE VLSI Test Symposium (VTS) Best Paper Award for novel architecture and system design research. Derivatives of the techniques developed in my PhD thesis have been published by various companies including Mentor, Nvidia, NXP, Renesas, Synopsys, and TI. I also received three Intel divisional recognition awards for mobile processor designs that have been adopted by product groups at Intel.

PROFESSIONAL PREPARATION

Carnegie Mellon University	Pittsburgh, PA	Electrical & Comp. Eng., w/ double major in Computer Sci.	B.S., 2006
Carnegie Mellon University	Pittsburgh, PA	Mathematical Sciences	M.S. w/honors, 2006
Stanford University	Stanford, CA	Electrical Engineering	Ph.D., 2013

APPOINTMENTS

- Department of Computer Science, University of Chicago, Assistant Professor, Sept. 2015-present
- Microarchitecture Research Lab, Intel Labs, Senior Research Scientist, June 2013-August 2015
- Department of Electrical Engineering, Stanford University, Visiting Scholar, June 2013-June 2014
- Department of Electrical Engineering, Stanford University, Research Assistant, Sept. 2006-June 2013
- Future Technology Research Lab, Intel Labs, Graduate Technical Intern, 2010
- Computer Architecture Group, Microsoft Research, Graduate Intern Researcher, 2008
- Test Strategies Group, Intel Corporation, Graduate Technical Intern, 2007
- AIX Quality Group, IBM Corporation, Summer Intern, 2005

RESEARCH INTERESTS

- Computer architecture
- Robust and secure system design
- Emerging technologies

AWARDS AND HONORS

- DAC Under-40 Innovators Award, 2022
- Google Research Scholar Award, 2021
- Best Paper Award, ACM Great Lake Symposium on VLSI, 2019
- Intel Labs Gordy Academy Award, 2015
- Intel Divisional Recognition Award for efficient mobile processor designs, 2012, 2013, 2015
- Outstanding Dissertation Award, European Design and Automation Association, 2013
- Rising Stars in EECS, Massachusetts Institute of Technology, 2013
- Best Student Paper Award, IEEE International Test Conference, 2010
- Best Paper Award, IEEE VLSI Test Symposium, 2010

PUBLICATIONS

1. Takumi Uezono, Yi He, **Yanjing Li,** "Functional In-Field Self-Test for Deep Learning Accelerators in Automotive Applications," *Proc. IEEE International Test Conference (ITC)*, 2022 (to appear).
2. Mehdi Sadi, Yi He, **Yanjing Li**, Mahabubul Alam, Satwik Kundu, Swaroop Ghosh, Javad Bahrami, and Naghmeh Karimi, "On the Reliability of Conventional and Quantum Neural Network Hardware," *Proc. IEEE VLSI Test Symposium (VTS)*, 2022 (invited).
3. Yi He, Takumi Uezono, **Yanjing Li**, "Efficient Functional In-Field Self-Test for Deep Learning Accelerators," *Proc. IEEE International Test Conference (ITC)*, 2021.
4. Mingdai Yang, Mohammad Reza Jokar, Junyi Qiu, Qiuwen Lou, Yuming Liu, Aditi Udupa, Frederic T. Chong, John M. Dallesasse, Milton Feng, Lynford L. Goddard, X. Sharon Hu, and **Yanjing Li**, "A Hybrid Optical-Electrical Analog Deep Learning Accelerator Using Incoherent Optical Signals," *Proc. ACM Great Lakes Symposium on VLSI (GLSVLSI)*, 2021.
5. Yi He, Prasanna Balaprakash, and **Yanjing Li**, "FIdelity: Efficient Resilience Analysis Framework for Deep Learning Accelerators," *Proc. 53rd IEEE/ACM International Symposium on Microarchitecture (MICRO)*, 2020.
6. Reza Jokar, Junyi Qiu, Lynford Goddard, John Dallesasse, Milton Feng, Frederic Chong, **Yanjing Li**, "Baldur: A Power Efficient and Scalable Network Using All-Optical Switches," *Proc. IEEE International Symposium on High-Performance Computer Architecture (HPCA),* 2020.
7. Yi He, **Yanjing Li, "**Time-Slicing Soft Error Resilience in Microprocessors for Reliable and Energy-Efficient Execution," *Proc. IEEE International Test Conference*, 2019.
8. Reza Jokar, Lunkai Zhang, John Dallesasse, Frederic Chong, **Yanjing Li**. "Direct-Modulated Optical Networks for Interposer Systems." *Proc. IEEE/ACM International Symposium on Networks-on-Chip (NOCS)*, 2019.
9. Eric Cheng, Daniel-Mueller-Gritschneder, Jacob Abraham, Pradip Bose, Alper Buyuktosunoglu, Deming Chen, **Yanjing Li**, Uzair Sharif, KevinSkadron, Mircea Stan, Muhammad Shafique, Ulf Schlichtmann, Subhasish Mitra, "Cross-Layer Resilience: Myths, Insights and the Road Ahead," *Proc. ACM/EDAC/IEEE Design Automation Conference (DAC),* 2019 (invited).
10. Yi He, Xi Liang, **Yanjing Li, "**Time-Slicing Soft Error Resilience in Microprocessors for Reliable and Energy-Efficient Execution," *Proc. IEEE International Test Conference*, 2019.
11. **Yanjing Li**, "Skipping Crashes: A Minimal-Cost Framework for Efficient Error Recovery in Approximate Computing Environments," *Proc. ACM Great Lakes Symposium on VLSI (GLSVLSI)*, 2019. **Best Paper Award.**
12. Xinchuan Wu, Timothy Sherwood, Fred Chong, **Yanjing Li**, "Protecting Page Tables from RowHammer Attacks using Monotonic Pointers in DRAM True-Cells," *Proc. ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, 2019.
13. Xi Liang, Yi He, Prasanna Balaprakash, **Yanjing Li**, "Machine Learning Guided Application Error Analysis for Efficient Cross-Layer Resilience," *ACM/EDAC/IEEE Design Automation Conference (DAC)*, Latest Breaking Results, 2018.
14. Xiaoan Ding, Xi Liang, **Yanjing Li**, "Cross-Layer Refresh Mitigation for Efficient and Reliable DRAM Systems: A Comparative Study," *Proc. IEEE International Test Conference*, pp. 1-10, 2017.
15. David Lin, Ted Hong, **Yanjing Li**, S Eswaran, Sharad Kumar, Farzan Fallah, Nagib Hakim, Donald S. Gardner, Subhasish Mitra, "Effective Post Silicon Validation of System-on-Chips using Quick Error Detection," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 33, no. 10, pp. 1573-1590, 2014.
16. Subhasish Mitra, Pradip Bose, Eric Cheng, Chen-Yong Cher, Hyungmin Cho, Rajiv Joshi, Young Moon Kim, Charles R. Lefurgy, **Yanjing Li**, Kenneth P. Rodbell, Kevin Skadron, James Stathis, LLukasz Szafaryn, "The Resilience Wall: Cross-Layer Solution Strategies," *Proc. IEEE International Symposium on VLSI Technology, Systems and Applications and IEEE International Symposium on VLSI Design, Automation and Test*, pp. 1-11, 2014 (Invited).

17. **Yanjing Li**, Eric Cheng, Samy Makar, Subhasish Mitra, "Self-Repair of Uncore Components in Robust System-on-Chips: An OpenSPARC T2 Case Study," *Proc. IEEE International Test Conference*, pp. 1-10, 2013.
18. David Lin, Ted Hong, **Yanjing Li**, Farzan Fallah, Donald S. Gardner, Nagib Hakim, Subhasish Mitra, "Overcoming Post-Silicon Validation Challenges through Quick Error Detection (QED)," *Proc. IEEE/ACM Design Automation and Test in Europe*, pp. 320-325, 2013 (Invited).
19. Subhasish Mitra, Kevin Brelsford, Young Moon Kim, Hsiao-Heng Kelin Lee, **Yanjing Li**, "Robust System Design to Overcome CMOS Reliability Challenges," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems, Special Issue on the IEEE CAS Forum on Emerging and Selected Topics*, vol. 1, no. 1, pp. 30-41, 2011 (Invited).
20. Subhasish Mitra, Hyungmin Cho, Ted Hong, Young Moon Kim, Hsiao-Heng Kelin Lee, Larkhoon Leem, **Yanjing Li**, David Lin, Evelyn Mintarno, Diana Mui, Sung-Boem Park, Nashant Patil, Hai Wei, Jie Zhang, "Robust System Design," *IPSJ Trans. System LSI Design Methodology*, 2011 (Invited).
21. Larkhoon Leem, Hyungmin Cho, Young Moon Kim, Hsiao-Heng Kelin Lee, **Yanjing Li**, Subhasish Mitra, "Cross-Layer Error Resilience for Robust Systems," *Proc. IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, pp. 177-180, 2010 (Invited).
22. Ted Hong, **Yanjing Li**, Sung-Boem Park, Diana Mui, David Lin, Ziyad Abdel Kaleq, Nagib Hakim, Helia Naeimi, Donald S. Gardner, Subhasish Mitra, "QED: Quick Error Detection Tests for Effective Post-Silicon Validation," *Proc. IEEE International Test Conference (ITC)*, pp. 1-10, 2010. **Best Student Paper Award**.
23. **Yanjing Li**, Onur Mutlu, Donald S. Gardner, Subhasish Mitra, "Concurrent Autonomous Self-Test for Uncore Components in System-on-Chips," *Proc. IEEE VLSI Test Symposium (VTS)*, pp. 232- 237, 2010. **Best Paper Award**.
24. **Yanjing Li**, Young Moon Kim, Evelyn Mintarno, Donald S. Gardner, Subhasish Mitra, "Overcoming Early-Life Failure and Aging Challenges for Robust System Design," *IEEE Design and Test of Computers, Special Issue on Design for Reliability and Robustness*, vol. 26, no. 6, pp. 28-39, 2009 (invited).
25. **Yanjing Li**, Onur Mutlu, Subhasish Mitra, "Operating System Scheduling for Efficient Online Self-Test in Robust Systems," *Proc. IEEE International Conference on Computer-Aided Design*, pp. 201-208, 2009.
26. Hiroaki Inoue, **Yanjing Li**, Subhasish Mitra, "VAST: Virtualization Assisted Concurrent Autonomous Self-Test," *Proc. IEEE International Test Conference*, pp. 1-10, 2008.
27. **Yanjing Li**, Samy Makar, Subhasish Mitra, "CASP: Concurrent Autonomous Chip Self-Test Using Stored Test Patterns," *Proc. IEEE/ACM Design Automation and Test in Europe*, pp. 885-890, 2008.
28. **Yanjing Li**, Zhaosong Lu, Jeremy J. Michalek, "Diagonal Quadratic Approximation for Parallelization of Analytical Target Cascading," *ASME Journal of Mechanical Design*, vol. 130, no. 5, pp. 051402-1 - 051402-11, 2008.
29. **Yanjing Li**, Zhaosong Lu, Jeremy J. Michalek, "Diagonal Quadratic Approximation for Parallelization of Analytical Target Cascading," *Proc. ASME International Design Engineering Technical Conferences*, pp. 749-760, 2007.

FUNDING

- IARPA AGILE, 2022-2023
- CERES Research Center, 2021-2024
- Hitachi, unrestricted funding, 2020-2021, $39K
- Google, unrestricted funding, 2020-2021, $60K.

- Hitachi, unrestricted funding, 2020-2021, $60K.
- NSF/SRC E2CDA, "Collaborative Research: Electronic-Photonic Integration Using the Transistor Laser for Energy-Efficient Computing," award #1640192, 2016-2019, $280K.
- UChicago Internal Funding, Strategic Computing Initiative, “Machine Learning Guided Cross-Layer Resilience,” 2016, $65K.

PRESENTATIONS AND INVITED TALKS

- ASPLOS Robust AI Workshop, CERES, GLSVLSI, 2021
- Hitachi, CERES, 2020
- Argonne National Lab, Semiconductor Research Corporation, 2019
- Huawei, Semiconductor Research Corporation, HKUST, CUHK, HKU, CERES, 2018
- ARM, Semiconductor Research Corporation, 2017
- GCASR, Huawei, 2016
- University of Chicago, Intel, 2015
- Princeton University, University of Southern California, University of Illinois at Urbana Champaign, 2014
- Carnegie Mellon University, Intel, 2013

LEADERSHIP, MENTORSHIP, AND DIVERSITY ENGAGEMENTS

- Currently mentoring and have mentored a number of PhD, Master’s, and undergraduate students, including several female graduate and undergraduate students and minority students who produced publications, including a paper that won the best paper award in a major VLSI design conference.
- Volunteer for the University of Chicago FEMMES group, which aims to bridge the gender gap in technology.
- Actively participate in women in EE/CS organizations (University of Chicago, Intel, Stanford University, Carnegie Mellon University, IBM).
- Led a team of several researchers on a major processor design project at Intel Labs.

PROFESSIONAL ACTIVITIES

Associate editor: ACM Transactions on Design Automation of Electronic Systems, 2020-2022, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022-2023

Session organizer/program committee/external program committee: ACM/IEEE International Symposium on Computer Architecture (ISCA) 2020-2022; ACM Architectural Support for Programming Languages and Operating Systems (ASPLOS) 2019-2022; ACM/IEEE Design Automation Conference (DAC) 2020-2022; IEEE/ACM International Symposium on Microarchitecture (MICRO) 2020-2022; IEEE International Test Conference (ITC), 2014-2022; IEEE/ACM International Symposium on Networks-on-Chip (NOCS) 2020; IEEE International Symposium on High-Performance Computer Architecture (HPCA) 2019-2020; ACM Great Lakes Symposium on VLSI (GLSVLSI) 2018-19; IEEE VLSI Test Symposium (VTS) 2016, 2021; International Conference on Supercomputing (ICS) 2016.

NSF panelist: 2016, 2020.