ATHIL SHAJI

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Summary

A dedicated Electronics and Communication Engineer with an M.Tech in VLSI and Microsystems. Skilled in designing, developing, and optimizing electronic systems and components. A detail-oriented professional with a strong foundation in microelectronics and VLSI design, eager to contribute to the growth and success of the organization. For details, click here.

Work Experience

Internship at Vikram Sarabhai Space Centre, Trivandrum May - June 2023

Learned the basics of LabVIEW programming, gaining hands-on experience in its application. Familiarized with the PXI system and its associated protocols, enhancing understanding of modular electronic instrumentation. Additionally, gained exposure to scientific payloads, their design, and operational principles.

Internship at Revolt Aug 2020 - Oct 2021

Worked as a Marketing Intern at Onlive, gaining experience in marketing strategies, campaign management, and customer engagement to drive brand growth and visibility.

Projects

ASIC Design for Double Torsional MEMS Accelerometer by using SGFET

Designed and optimized both single and double torsional MEMS accelerometer structures for improved mechanical performance. Furthermore, architectures a complete readout ASIC for the double torsional accelerometer, implementing a novel Suspended Gate Field-Effect Transistor (SGFET) to achieve high-sensitivity transduction.

Low power Flip Flop design based on True Single Phase Clock

Designed and tested a Low power Flip Flop design based on True Single Phase Clock. The design comprises complementary pass transistor logic and CMOS logic. It offers low power with reduced delay that increases the speed of the flip flop with less circuit complexity.

Bidirectional Dual Micro-Heater Flow Sensor

Designed, modeled, and simulated a Dual Micro-Heater Flow (DMHF) sensor in CoventorWare, featuring poly-Si heaters on a Si_3N_4 membrane. Performed steady-state thermal analysis to validate that the power difference (ΔP) in Constant Temperature mode and Constant Power mode indicates flow direction and magnitude.

Integrated Vehicle Health Management System

Project undertaken under the guidance of Sreelal S (Senior Engineer, VSSC) and funded by IEEE Circuits and Systems, the project focuses on monitoring and managing vehicle health. It leverages the PIC24 Microcontroller for implementation and continued development.

Efficient Hardware Design of Parameterized Posit Adder

Developed parameterized hardware designs for a posit arithmetic adder using Verilog. Analyzed and compared the delay performance of both pipelined and non-pipelined posit adder architectures to optimize efficiency and performance.

Transmission gate based 8T sram

Designed Transmission Gate-based SRAM cell for biomedical applications, reducing power consumption, area, and delay. By eliminating peripheral circuitry during read operations, it improves data stability and efficiency, making it ideal for low-power, compact, high-performance circuits in implantable and wireless devices.

Two-Stage CMOS Operational Amplifier

Designed a two-stage CMOS operational amplifier with a rail-to-rail gain-boosted folded cascode and class AB output stage to enhance speed, DC gain, and signal-to-noise ratio (SNR). The OpAmp offers high DC gain, fast settling time, and low power consumption, making it ideal for high-speed, high-resolution ADCs.

Magneto-plethysmograph and Non-contact ECG for Biomedical Studies

The project focuses on designing an Electrocardiogram (ECG) system for patients using a GMR sensor and INA (Instrumentation Amplifier) for accurate signal acquisition and analysis in biomedical applications.

Density-Based Traffic Control System

The project aims to design a dynamic traffic signal system that adjusts signal timing based on real-time traffic density at each junction. The system utilizes infrared sensors to count vehicles and Arduino UNO to measure the traffic density in each lane, enabling adaptive signal control for optimized traffic flow.

Education

2024 - present	M.tech (VLSI and Microsystems) at **IIST,thiruvanthapuram**	(CGPA: 8.41/10.0)
2020- 2024	B.Tech (ECE) at **TKM College of Engineering**	(CGPA: 8.59/10.0)
2019	Class 12th CBSE	(PERCENTAGE: 91.4%)
2021	Class 10th CBSE	(CGPA: 10.0/10.0)

Publications

"Integrated Vehicle Health Management System: Matlab Simulink" (2019). In: *International Research Journal on Advanced Science Hub* 6.3, pp. 2200–2300. URL: https://doi.org/10.47392/IRJASH.2024.008.

Position and Responsibilities

Finance Head	Indian Society for Technical Education TKMCE (2021 - 2023),TEDx TKMCE(2023-2024)
Content Team	IEEE CASS(Circuit and System) Kerala Section 2023.
Hospitality Head	TKM College of engineering(2024) , HESTA 24
Alumni Wing Coordinato	STEPS TKMCE(2023-2024)
Junior Finance Head	TEDx TKMCE(2022-2023
Logistics Head	Hult Prize Tkmce (2023-2024)

Skills

Skills	Verilog, Comsol, Coventorware, innovus, genus, Cadence, Leadership, Team player, Critical thinking, Problem solving,PIC Microcontroller, Hard working, Basic Coding using C, Matlab simulink, Communication, Organization
Interests	Analog Electronics, Microcontrollers, FPGA, System Verilog, Technology, Football, Travel