

## **Chapter 4 Signal Conditioning And Processing**

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## **Chapter 5 Date Transmission**

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## CHAPTER 4

# SIGNAL CONDITIONING AND PROCESSING



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### **4.1 IMPORTANCE OF SIGNAL CONDITIONING**

Signal conditioning means manipulating an analog signal in such a way that it meets the requirements of the next stage for further processing. The signal conditioning equipment may be required to do process like amplification, attenuation, integrating, differentiation, addition and subtraction and also required to do non linear process like modulation, demodulation, sampling, filtering and wave shaping (clipping and clamping). The signal conditioning in many situation is an excitation and amplification system for passive transducer. For active transducers it may be amplification system. In both the applications, the transducer output is brought up to sufficient level to make it useful for conversion, processing indicating and recording.

### Types of signal conditioning

Depending upon the excitation source, a signal conditioning circuit may have AC or DC voltage source and according to these sources, signal conditioning circuit may be classified as,

- AC signal conditioning system
- DC signal conditioning system
- AC signal conditioning system

It is used for variable reactance transducer and for systems where signals have to be transmitted via long cables to connect the transducer to the signal conditioning equipment. Figure below shows the block diagram of AC signal conditioning system.

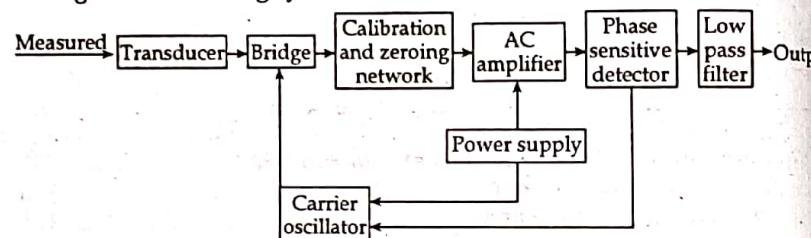


Figure: AC signal conditioning system

The transducers used are the variable resistance or variable inductance transducers. They are employed between the carrier frequency of 50 Hz to 200 kHz. The carrier frequencies are much higher, they are at least 5 to 10 times the signal frequencies. Transducer parameter variations amplitude modulate the carrier frequencies at the bridge output and wave form is phase sensitive so that the polarity of dc output indicates the direction of the parameter change in the bridge output.

In a carrier system amplifier, drift and spurious signals are not of much importance unless they modulate the carrier. However, it is more difficult to achieve a stable carrier oscillator than a comparable dc stabilized source. In carrier systems, it is easy to obtain very high rejection of mains frequency pick up. Active filters can be used to reject these frequency components of the data signal.

### b) DC signal conditioning system

They are generally used for common resistance transducers such as potentiometer and strain gauges.

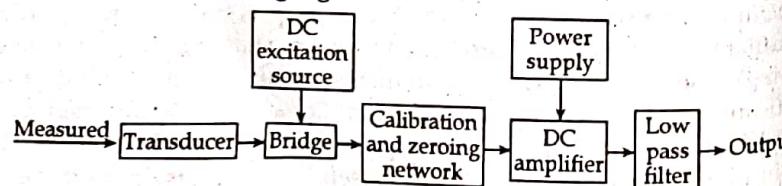


Figure: DC signal conditioning system.

In the calibration and zeroing network unit the calibration of desired or required parameters like voltage, current, resistance is calibrated in terms of measured. For example; Strain gauge is used in the dc bridge whose parameter, found in terms of resistance but is calibrated in terms of force pressure displacement. The zeroing network process for calibration such that only linear portion of the transducer characteristics is generated. Therefore zeroing network fixes the zero point and calibration starts from here. In DC amplifier, we have amplification, integration, addition, subtraction etc units. This unit works only when it is supplied by power supply. The low pass filter is used for filtering high frequency signal.

## 4.2 SIGNAL AMPLIFICATION, FILTERING AND WAVE SHAPING

### a) Signal amplification

It increases voltage level to better match the analog to digital converter (ADC) range, thus increasing the measurement resolution and sensitivity. In addition, using external signal conditioners located closer to the signal source, or transducers, improves the measurement signal to noise ratio by magnifying the voltage level before it is affected by environmental noise.

Commonly used amplifiers used for signal conditioning include sample and hold amplifiers, peak detectors, log amplifiers, antilog amplifiers, instrumentation amplifiers and programmable gain amplifiers.

### b) Attenuation

It is the opposite of amplification. It is necessary when voltages to be digitized are beyond the ADC range. This form of signal conditioning decreases the input signal amplitude so that the conditioned signal is within DC range. Attenuation is typically necessary when measuring voltages that are more than 10 V.

### c) Isolation

It is a device that passes the signal from its source to the measurement device without a physical connection by using transformer, optical or capacitive coupling techniques.

### d) Filtering

It rejects unwanted noise within a certain frequency range. They are used to block out high-frequency noise in electrical measurements.

### e) Excitation

It is required for many types of transducers. For example, strain gauges, accelerometers, thermistors, and resistance temperature detectors (RTDs) requires external voltage or current excitation.

### f) Linearization

It is necessary when sensors produce signals that are not linearly related to the physical measurements. It is the process of interpreting the signal

from the sensor and can be done either with signal conditioning or through software. Thermocouples are the classic example of a sensor that requires linearization.

### g) Clipping and clamping

The diode clamper is a wave shaping circuit that shifts the signal voltage to a desired level. The clipping circuits are diode operated wave shaping circuits that change the V-I characteristics in response to the level of applied signal. A diode can be considered as a voltage controlled switch.

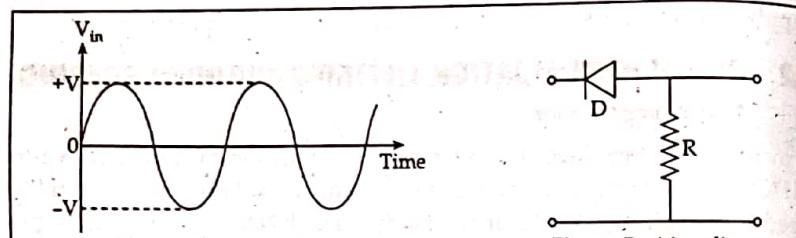


Figure: Input waveform

Figure: Positive clipper

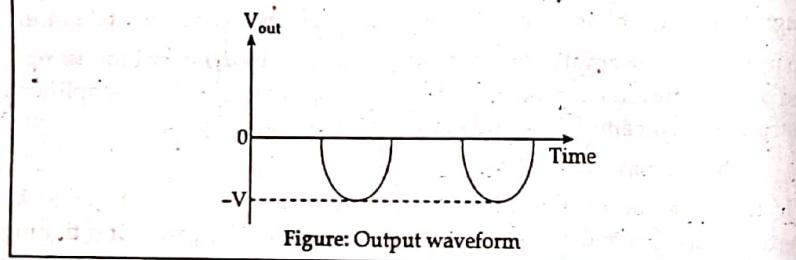


Figure: Output waveform

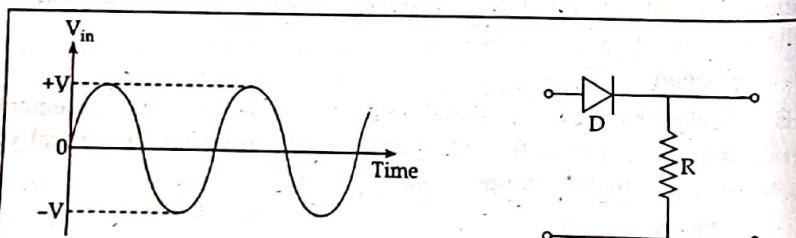


Figure: Input waveform

Figure: Negative clipper

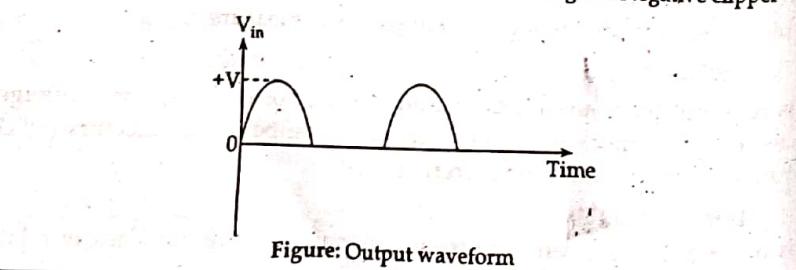


Figure: Output waveform

### Uses of Clippers circuit

- They are frequently used for the separation of synchronizing signals from the composite picture signals.
- They can be used as voltage limiters and amplitude selectors.
- They are used for the protection of transistor from the transients, as freewheeling diode connected in parallel across the inductive load.
- They are used for the generation of new wave forms or shaping the existing wave form.

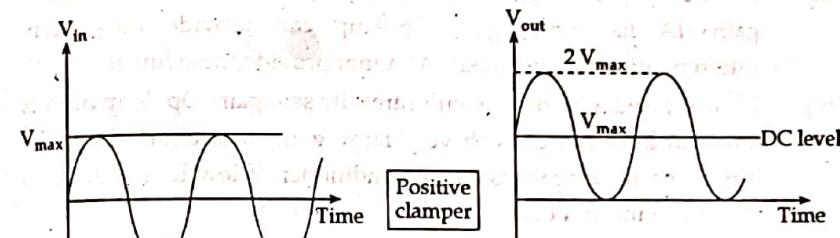


Figure: Input waveform

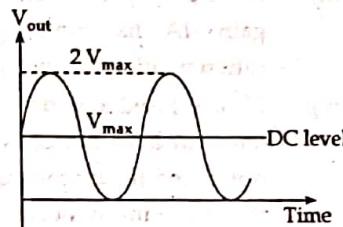


Figure: Output waveform

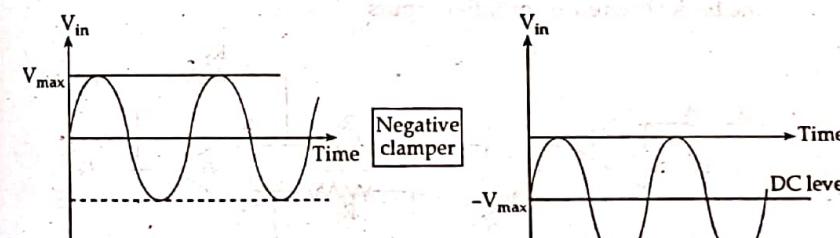


Figure: Input waveform

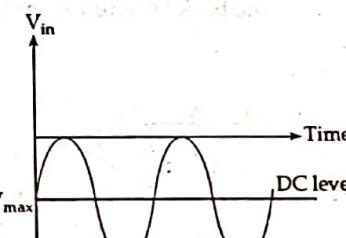


Figure: Input waveform

### Uses of Clamping Circuit

- They are used for removing the distortions.
- They are used as voltage doublers or voltage amplifiers.
- They are used for the protection of the amplifiers from large errant signals.
- For improving the reverse recovery time, clampers are used.
- They are used for identification of polarity of the circuits.

## 4.3 INSTRUMENTATION AMPLIFIER

An instrumentation amplifier is a type of differential amplifier. It is a differential voltage gain device that amplifies the difference between the voltages existing at its two input terminals. The main use of an instrumentation amplifier is for a low level amplification with high CMRR, high input impedance to avoid loading, low power consumption.

There are several characteristics of an instrumentation amplifier that sets it apart from operational amplifier (Op-Amp):

- i) Instrumentation amplifier (IA) has a high impedance differential input whereas Op-Amp has high input impedance.
- ii) IA has high common mode voltage gain and high CMRR. Op-Amp also has high gain and CMRR but IA is superior over Op-Amp.
- iii) An Op-Amp has very large (ideally infinite) amount of voltage gain. IA has finite gain Op-Amp can provide integration, differentiation functions but IA cannot provide these functions.
- iv) IA is a closed loop device with carefully set again. Op-Amp itself is an open loop device with very large gain. This allows IA to be optimized for its role as signal conditioner of low level signals in large amounts of noise.

Instrumentation amplifier using three Op-Amp is shown below. This provides high input resistance for accurate measurement of signals. In this circuit, a non-inverting amplifier is added to each of the basic difference amplifier inputs.

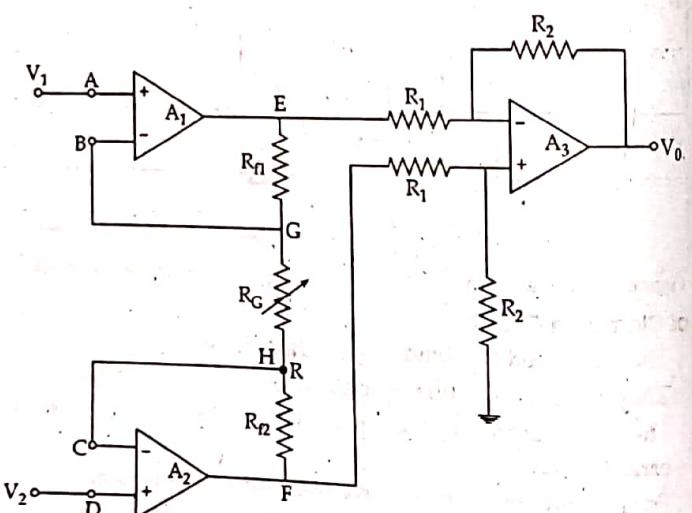
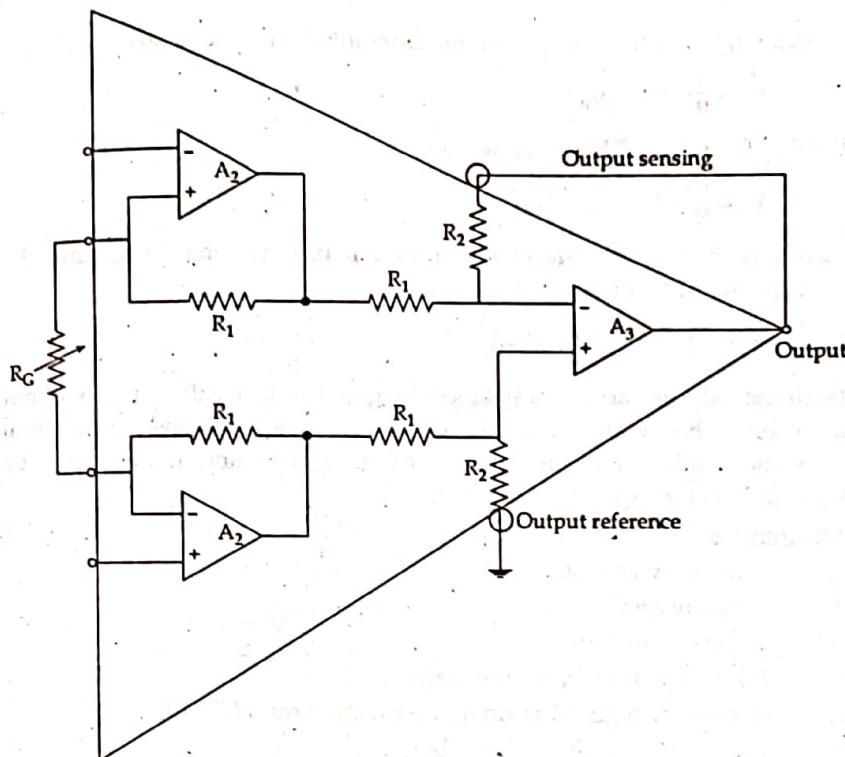


Figure: Instrumentation amplifier

Here Op-Amp  $A_1$  and  $A_2$  are the non-inverting amplifiers forming the input or first stage of the instrumentation amplifier. The Op-Amp is the difference amplifier forming an output stage of the amplifier. The block diagram representation of the three Op-Amp instrumentation amplifier is shown below.



The output of the Op-Amp of the Op-Amp  $A_1$  is  $V_{01}$  and output of the Op-Amp  $A_2$  is  $V_{02}$ . The output stage is a standard difference amplifier,

$$V_0 = \frac{R_2}{R_1} (V_{02} - V_{01})$$

Let the voltage at node A is equal to voltage  $V_1$  and node voltage B is equal to node voltage A. Hence voltage of G is equal to  $V_1$ . Similarly, the voltage of H is  $V_2$ . Applying ohms law between the node E and F, we get;

$$I = \left( \frac{V_{01} - V_{02}}{R_{f1} + R_G + R_{f2}} \right)$$

Let,  $R_{f1} = R_{f2} = R_f$ , then,

$$I = \left( \frac{V_{01} - V_{02}}{2R_f + R_G} \right) \quad (1)$$

In node G and H,

$$I = \frac{V_G - V_H}{R_G} = \frac{V_1 - V_2}{R_G} \quad (2)$$

From equation (1) and (2), we get;

$$\text{or, } \frac{V_{01} - V_{02}}{2R_f + R_G} = \frac{V_1 - V_2}{R_G}$$

$$\text{or, } V_{01} - V_{02} = \frac{(2R_f + R_G)}{R_G} (V_1 - V_2)$$

We know, the output voltage of the differential amplifier is given by,

$$V_o = \frac{R_2}{R_1} (V_{o2} - V_{o1})$$

Putting the value of  $V_{o2} - V_{o1}$ , we get,

$$V_o = \frac{R_2}{R_1} \left(1 + 2 \frac{R_f}{R_C}\right) (V_{o2} - V_{o1})$$

Above is the overall gain of the amplifier. If  $R_1$  is equal to  $R_2$ , then the overall gain of amplifier is given by,

$$V_o = \left(1 + \frac{2R_f}{R_C}\right) (V_{o2} - V_{o1})$$

With the help of variable resistance the gain can be easily varied without disturbing the symmetry of the circuit. The gain depends in external resistance and hence can be adjusted accurately and made stable by selecting the high quality resistance.

#### Advantages

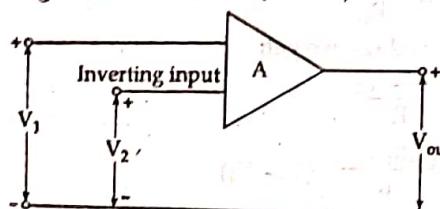
- i) It has very low DC offset
- ii) It has low noise
- iii) There is low drift
- iv) It has very high open loop gain
- v) It has very high common mode rejection ratio (CMRR)
- vi) It has very high input impedances
- vii) It has very high slew rate

## 4.4 OP-AMP IN INSTRUMENTATION

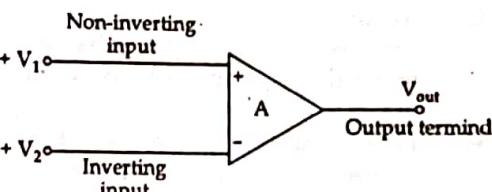
An operational amplifier (Op-Amp) is basically a multistage, very high gain, directly coupled, negative feedback amplifier that provides a stabilized voltage gain. An Op-Amp has high input impedance (exceeding 100 kΩ) and has capability of amplifying signals having frequency ranging from zero Hz to 1 MHZ i.e., Op-Amp can be used to amplify DC as well as AC input signals and it has low output impedance (less than 100 Ω).

The schematic symbol of an Op-Amp is shown below. A is the voltage gain,  $V_1$  is non inverting input and  $V_2$  is inverting input. The differential input is,  $V_{in}$  or  $V_d = V_1 - V_2$

and, Output voltage,  $V_{out} = A \cdot V_{in} = A (V_1 - V_2)$



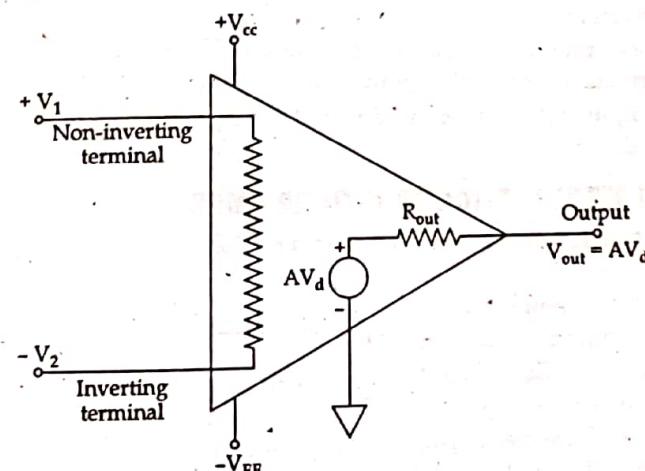
Mostly used circuit symbol for an Op-Amp is shown below. It essentially consists of two input terminals and one output terminal. Here the inputs are marked with plus (+) and minus (-) to indicate non inverting and inverting inputs, respectively.



#### Equivalent circuit of an Op-Amp

The voltage source  $AV_d$  is an equivalent thevenin voltage source and  $R_{out}$  is the thevenin equivalent resistance looking back into the output terminal of the Op-Amp. The output voltage is given as

$$V_{out} = AV_d = A (V_1 - V_2)$$



where,  $A$  = Large signal voltage gain

$V_d$  = Differential input voltage

$V_1$  and  $V_2$  are the input voltages at non-inverting and inverting terminals respectively with respect to ground.

### 4.4.1 Ideal Op-Amp

The Op-Amp is said to be ideal if it has the following characteristics;

- i) Its open loop gain  $A$  is infinite. When an Op-Amp is operated without any connection between the output and any of the inputs (i.e., without feedback), it is said to be in the open-loop condition.
- ii) Its input resistance (i.e., the resistance measured between inverting and non inverting terminals)  $R_{in}$  is infinite. It means that the input current is zero and so it does not load the source. It also means that an ideal Op-Amp is a voltage controlled device.

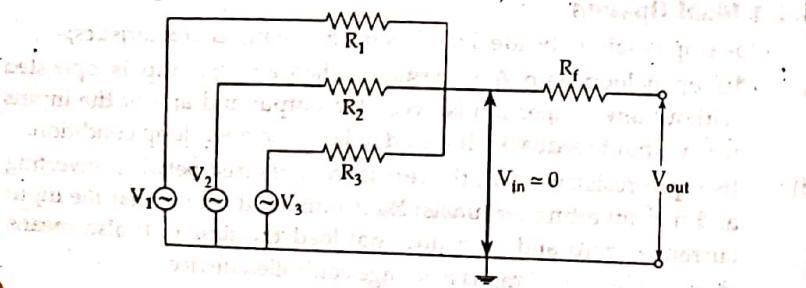
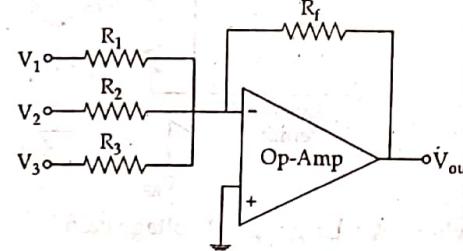
- iii) Its output impedance  $R_{out}$  is zero, i.e., the output voltage  $V_{out}$  does not depend on the load resistance connected between the output terminals i.e., output voltage  $V_{out}$  is independent of the current drawn by the load.
- iv) Perfect balance because of infinite voltage gain, the voltage between the inverting and non inverting terminals of input i.e., differential input voltage  $V = V_2 - V_1$  essentially zero (i.e.,  $V_1 = V_2$ ). For finite output voltage  $V_{out}$ . This implies that  $V_1$  and  $V_2$  track each other.
- v) Infinite frequency bandwidth i.e., it has flat frequency response from dc to infinity so that any frequency signal from zero to infinity Hz can be amplified without attenuation.
- vi) Drift characteristics with temperature is nil.
- vii) Common-mode rejection ratio (CMRR) is infinite so that amplifier is free from undesired common mode signals such as pickups, thermal noise etc.
- viii) Slew rate is infinite so that output voltage changes occurs simultaneously with input voltage changes.
- ix) Output voltage is zero when input voltage is zero i.e., offset voltage is zero.

## 4.5 GENERAL APPLICATIONS OF OP-AMPS

### A. Summing, scaling and averaging amplifiers

The most useful of the Op-Amp circuits employed in analog computers is the summing amplifier circuit. This circuit can be used to add ac or dc signals. This circuit provides an output voltage proportional to or equal to the algebraic sum of two or more input voltages each multiplied by a constant gain factor. Three input summing circuit is shown in figure.

The virtual equivalent circuit is shown below,



Using virtual equivalent circuit, the output voltage can be given in terms of inputs as,

$$V_{out} = -R_f \left[ \frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} \right]$$

If  $R_1 = R_2 = R_3 = R_f$

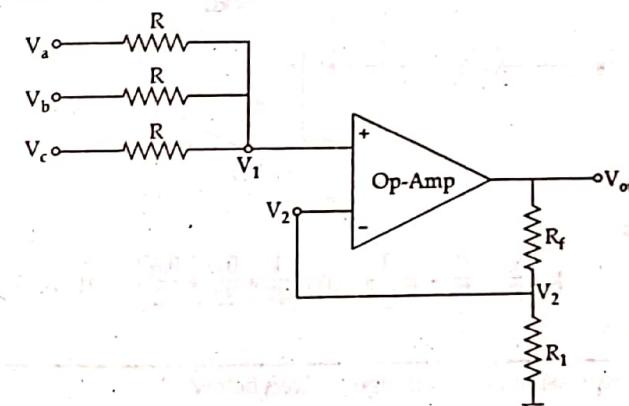
Then,

$$V_{out} = -(V_1 + V_2 + V_3) \quad (1)$$

Op-Amp summing amplifiers are also called mixers. Equation (1) reveals that the output voltage is equal to the negative sum of all input voltages, hence the circuit acts as a summing amplifier.

If each input voltage is amplified by a different factor i.e., weighted differently at the output, the circuit becomes a scaling or weighted amplifiers.

Summing or averaging amplifier circuit can be designed in non inverting configuration by selecting appropriate values of resistors i.e.,  $R_f$  and  $R_1$ .



Using the superposition theorem, the voltage  $V_1$  at the non-inverting terminals is,

$$V_1 = \left( \frac{\frac{R}{2}}{R + \frac{R}{2}} \right) V_a + \left( \frac{\frac{R}{2}}{R + \frac{R}{2}} \right) V_b + \left( \frac{\frac{R}{2}}{R + \frac{R}{2}} \right) V_c = \frac{V_a + V_b + V_c}{3}$$

Hence the output voltage is,

$$V_{out} = \left( 1 + \frac{R_f}{R_1} \right) \left( \frac{V_a + V_b + V_c}{3} \right) \quad (2)$$

Equation (2) reveals that the output voltage is equal to product of average of all input voltages and the gain of the circuit  $\left( 1 + \frac{R_f}{R_1} \right)$ . Hence it is referred to as an averaging amplifier. The gain  $\left( 1 + \frac{R_f}{R_1} \right)$  can be set to any value as per application need.

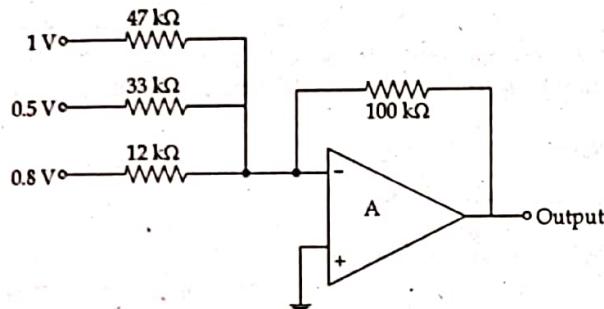
For unity gain, i.e., when  $\left(1 + \frac{R_f}{R_1}\right) = 1$ , the circuit will give average of all the inputs.

In case the gain of the circuit (i.e.,  $1 + \frac{R_f}{R_1}$ ) is made equal to the number of inputs, the output voltage will become equal to the sum of all the input voltages, i.e.,  $V_{out} = V_a + V_b + V_c$ .

Hence the circuit is called a non-inverting summing amplifier.

#### Example 1

Determine the output voltage for the given figure.

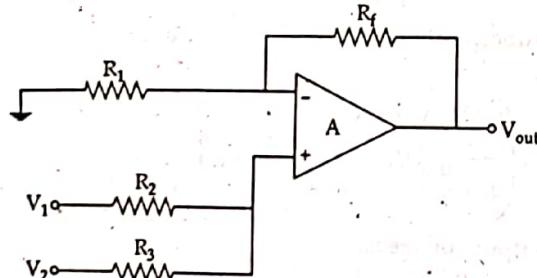


**Solution:**

$$V_{out} = -R_f \left[ \frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} \right] = -100 \left[ \frac{1}{47} + \frac{0.5}{33} + \frac{0.8}{12} \right] = -10.31 \text{ V.}$$

#### Example 2

Find the expression for  $V_{out}$  in figure given below.



**Solution:**

Input at non-inverting input terminal, when  $V_2$  is made zero,

$$V_{in1} = \left( \frac{R_3}{R_2 + R_3} \right) V_1$$

Input at non-inverting input terminal, when  $V_1$  is made zero,

$$V_{in2} = \left( \frac{R_2}{R_2 + R_3} \right) V_2$$

According to superposition theorem,

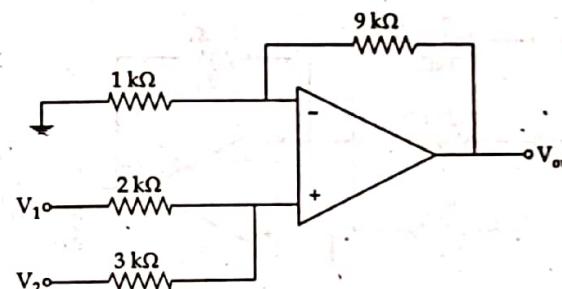
$$V_{out} = V_{out1} + V_{out2}$$

$$= \left(1 + \frac{R_f}{R_1}\right) (V_{in1} + V_{in2}) = 1 + \frac{R_f}{R_1} \left( \frac{R_3}{R_2 + R_3} V_1 + \frac{R_2}{R_2 + R_3} V_2 \right)$$

$$\therefore V_{out} = 1 + \frac{R_f}{R_1 (R_2 + R_3)} (R_3 V_1 + R_2 V_2)$$

#### Example 3

Find the value of  $V_{out}$



**Solution:**

Input at non inverting input terminal,

$$V_{in1} = \left( \frac{3}{2+3} \right) V_1$$

Input at non inverting input terminal, when  $V_1$  is made zero,

$$V_{in2} = \left( \frac{2}{2+3} \right) V_2$$

Input voltage at non inverting terminal,

$$V_{in} = V_{in1} + V_{in2} = \frac{3}{5} V_1 + \frac{2}{5} V_2$$

Thus, Output voltage,

$$V_{out} = \left(1 + \frac{R_f}{R_1}\right) (0.6V_1 + 0.4V_2) = \left(1 + \frac{9}{1}\right) (0.6V_1 + 0.4V_2) \\ = 6V_1 + 4V_2$$

#### Example 4

Realize a circuit to obtain  $V_{out} = -2V_1 + 3V_2 + 4V_3$  using an Op-Amp. Use minimum value of resistance as 10 kΩ.

**Solution:**

For an Op-Amp,

$$V_{out} = - \left[ \frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \frac{R_f}{R_3} V_3 \right]$$

Comparing the above expression with the given expression for the output, i.e.,  $V_0 = -2V_1 + 3V_2 + 4V_3 = - [2V_1 - 3V_2 - 4V_3]$

We have,

$$\frac{R_f}{R_1} = 2,$$

$$\frac{R_f}{R_2} = 3,$$

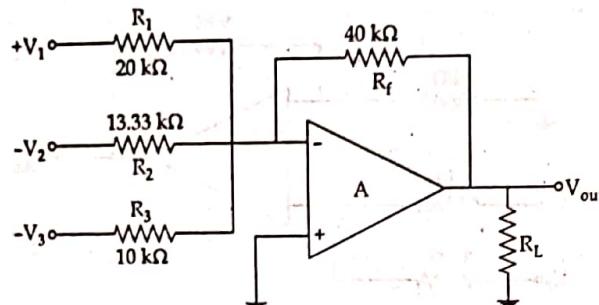
$$\frac{R_f}{R_3} = 4$$

Resistance  $R_3$  will be of minimum value of  $10\text{ k}\Omega$ ,

$$R_f = 4R_3 = 4 \times 10 = 40\text{ k}\Omega$$

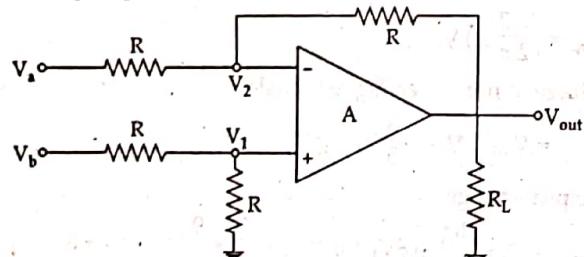
$$R_2 = \frac{R_f}{3} = \frac{40}{3} = 13.33\text{ k}\Omega$$

$$R_1 = \frac{R_f}{2} = \frac{40}{2} = 20\text{ k}\Omega$$



#### B. Subtractor or difference amplifier

This amplifier provides an output equal to the difference of input signals. By selecting appropriate values for the external resistors, the input signals can be scaled or attenuated to the desired value. The circuit so obtained is called the scaling amplifier.



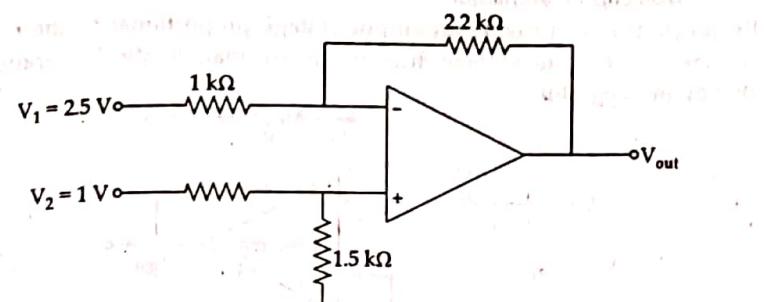
In circuit shown above, all external resistors are of equal value, therefore, gain of the amplifier is unity. So, output voltage,

$$V_{out} = \frac{-R}{R} [V_a - V_b] = V_b - V_a$$

Thus the output voltage  $V_{out}$  is equal to the voltage applied to the non-inverting input terminal less the voltage applied to the inverting input terminal. Hence the circuit is called a subtractor.

#### Example 5

Calculate the output voltage  $V_{out}$  of the circuit shown below. The input voltages are  $V_1 = 2.5\text{ V}$  and  $V_2 = 1\text{ V}$ .



**Solution:**

$$\text{Output voltage, } V_{out1} = -V_1 \times \frac{2.2}{1} = -2.5 \times \frac{2.2}{1} = -5.5\text{ V}$$

$$\text{Output voltage, } V_{out2} = V_2 \times \frac{1.5}{1.5 + 33} \left(1 + \frac{2.2}{1}\right) = 1\text{ V}$$

Applying super position theorem, we have,

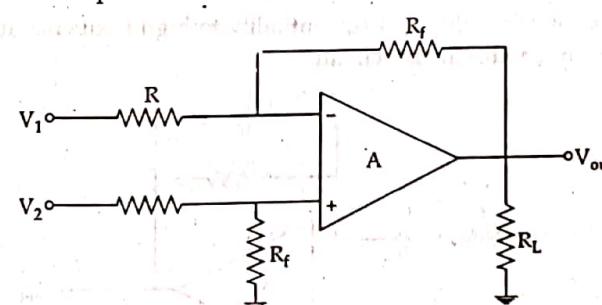
$$V_{out} = V_{out1} + V_{out2} = -5.5 + 1 = -4.5\text{ V}$$

#### Example 6

Design a difference amplifier using an Op-Amp to get the output voltage  $V_{out} = 10(V_2 - V_1)$ . Use minimum value of resistance as  $10\text{ k}\Omega$ .

**Solution:**

A differential amplifier circuit is shown below,



Output voltage is given as,

$$V_{out} = \frac{R_f}{R} (V_2 - V_1)$$

Comparing the above expression with the given expression for output, i.e.,  $V_{out} = 10(V_2 - V_1)$ , we have,

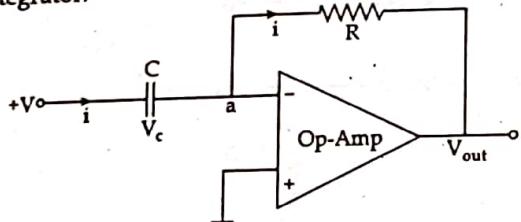
$$\frac{R_f}{R} = 10$$

Selecting  $R = 10\text{ k}\Omega$  (minimum value of resistance to be used)

$$R_f = 10R = 10 \times 10 = 100\text{ k}\Omega$$

**C. Op-Amp differentiator**

Its function is to provide an output voltage proportional to the rate of change of the input voltage. It is an inverse mathematical operation to that of an integrator.



Let  $i$  be the rate of change of charge,

$$\text{i.e., } i = \frac{dq}{dt}$$

Now, charge,  $q = CV_c$

$$\text{so, } i = \frac{dq}{dt} = \frac{d}{dt}(CV_c) = C \frac{dV_c}{dt}$$

Taking inverting input terminals as virtual ground,

$$\text{Output voltage, } V_{\text{out}} = -iR = -\left[C \frac{dV_c}{dt}\right]R$$

$$\therefore V_{\text{out}} = -RC \frac{dV_c}{dt}$$

i.e., output voltage is proportional to the derivation of the input voltage, the constant of proportionality being  $-RC$ .

The problem of instability and susceptibility to high frequency noise can be overcome by modifying the circuit.

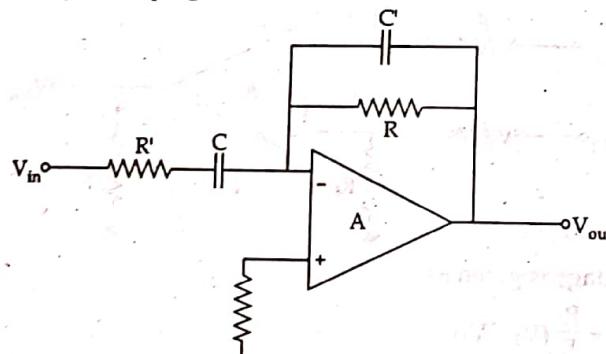
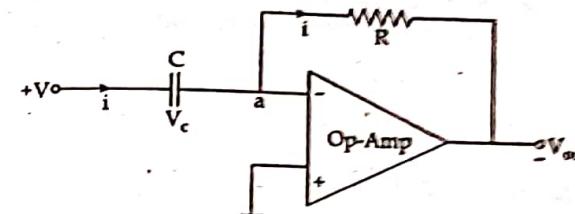


Figure: Practical differentiator

**Example 7**

The input to an Op-Amp differentiator circuit shown below is a sinusoidal voltage of peak value of  $10 \mu\text{V}$  and frequency  $2 \text{ KHz}$ . Determine the output voltage if  $R = 50 \text{ k}\Omega$  and  $C = 2 \mu\text{F}$ .

**Solution:**

$$\begin{aligned} V_{\text{in}} &= V_{\text{max}} \sin(2\pi f t) = 10 \times \sin(2 \times \pi \times 2,000 \times t) \\ &= 10 \sin(4,000 \pi t) \mu\text{V} \end{aligned}$$

$$\text{Scale factor} = RC = 2 \times 10^{-6} \times 50 \times 10^3 = 0.1$$

So, output voltage,

$$\begin{aligned} V_{\text{out}} &= -Rc \frac{dV_c}{dt} \\ &= -0.1 \frac{d}{dt}(10 \sin(4,000 \pi t)) \mu\text{V} \\ &= -0.1 \times 10 \frac{d}{dt}(4,000 \pi t) \mu\text{V} \\ &= 4,000 \pi \cos(4,000 \pi t) \mu\text{V} \end{aligned}$$

$$\therefore V_{\text{out}} = 12.56 \cos(4,000 \pi t) \text{ mV}$$

**D. Op-Amp Integrator**

An integrator is a circuit that performs a mathematical operation called integration. The most popular application of an integrator is to produce a ramp of output voltage, which is a linearly increasing or decreasing voltage.

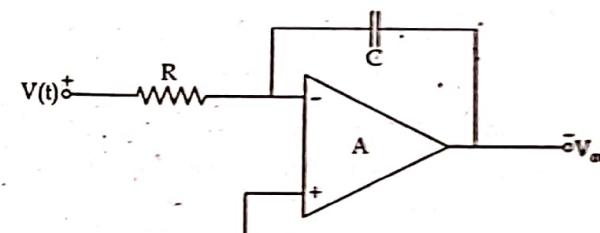


Figure: Op-Amp integrator

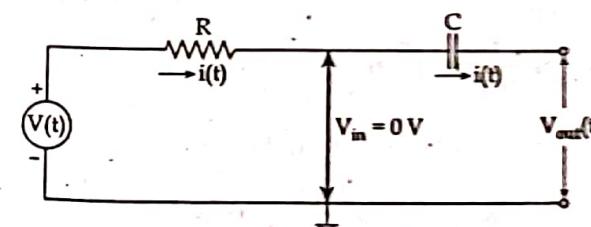


Figure: equivalent circuit of Op-Amp integrator

The input need not be sinusoidal and is therefore, represented by a lower case symbol  $V = V(t)$ . Correspondingly the current as a function of time is designated by  $i = i(t)$ .

$$\text{Hence, } i(t) = \frac{V(t)}{R} \text{ and}$$

$$\text{Output voltage, } V_{\text{out}}(t) = \frac{-1}{C} \int i(t) dt$$

Combining above two equations, we have,

$$V_{\text{out}}(t) = \frac{-1}{C} \int \frac{V(t)}{R} dt = \frac{-1}{RC} \int V(t) dt + A \quad (1)$$

where,  $A$  is an integration constant and is proportional to the value of the output voltage  $V_{\text{out}}$  at time  $t = 0$  second.

Equation (1) shows that the output voltage is the integral of the input voltage, with an inversion and scale factor of  $\frac{1}{RC}$ . If the input voltage is a step voltage, then the output voltage, will be a ramp or linearly changing voltage. If the input voltage is square wave, the output voltage will be a triangular wave and if the input voltage is a sinusoidal one, the output voltage will be cosine wave.

Integrators are widely used in ramp or sweep generators, filters, analog computers etc.

#### Example 8

A sinusoidal signal with a peak value of 6 mV and 2 kHz frequency is applied to the input of the ideal Op-Amp integrator with  $R_{\text{in}} = 100 \text{ k}\Omega$  and  $C_F = 1 \mu\text{F}$ . Find the output voltage.

**Solution:**

Input voltage,

$$\begin{aligned} V_{\text{in}}(t) &= V_{\text{max}} \sin(2\pi ft) \\ &= 6 \sin(2\pi \times 2 \times 10^3 t) \text{ mV} \\ &= 6 \sin(4,000\pi t) \text{ mV} \end{aligned}$$

$$\text{Scale factor, } = \frac{-1}{RC_F} = \frac{-1}{100 \times 10^3 \times 1 \times 10^{-6}} = -10$$

so, Output voltage,

$$\begin{aligned} V_{\text{out}}(t) &= \frac{-1}{RC_F} \int V_{\text{in}}(t) dt \\ &= -10 \int_0^t 6 \sin(4,000\pi t) dt \\ &= -60 \left[ \frac{-\cos(4,000\pi t)}{4,000\pi} \right]_0^t \text{ mV} \\ &= 4.7746 [\cos(4,000\pi t) - 1] \mu\text{V} \end{aligned}$$

#### E. Op-Amp Inverter

$$\text{Here, } i_1 = \frac{V_i}{R_i}$$

$$i_2 = \frac{-V_o}{R_f}$$

Applying KCL at point P,

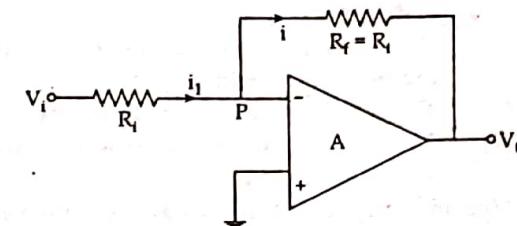
$$i_1 + (-i_2) = 0$$

$$\text{or, } \frac{V_i}{R_i} - \left( \frac{-V_o}{R_f} \right) = 0$$

$$\text{or, } \frac{V_i}{R_i} = \frac{V_o}{R_f}$$

$$\text{or, } \frac{V_i}{V_o} = -\frac{R_f}{R_i}$$

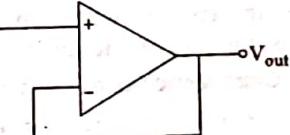
$$\therefore \frac{V_o}{V_i} = -\frac{R_f}{R_i} = A$$



If  $R_f = R_i$  then  $V_o = -V_i$ , i.e., the output voltage is  $180^\circ$  out of phase with the input voltage. Thus Op-Amp act as inverter. (i.e.,  $V_o = -V_i$ ).

#### 4.6 ISOLATION AMPLIFIERS

Isolation amplifiers are a form of differential amplifier that allows measurement of small signals in the presence of a high common mode voltage by providing electrical isolation and an electrical safety barrier. They protect data acquisition components from common mode voltages, which are potential difference between instrument ground and medical instruments to ensure isolation of a patient from power supply leakage current.



An isolation amplifier also called an unity-gain amplifier is an Op-Amp circuit which provides isolation of one part of a circuit from another so that power is not used, drawn or wasted in a part of the circuit. The purpose of an isolation amplifier is to isolate the circuit which appears before the amplifier from the circuit that appears after. It serve as a buffers. They do not amplify signals but serve to isolate parts of circuits or different circuits from each other.

##### Types of Isolation amplifier

- Transformer isolation amplifier
- Optical isolation amplifier
- Capacitive isolation amplifier

##### Application of Isolation amplifiers

- Isolation amplifiers provide electrical isolation and an electrical safety barrier.
- They protect the patients from leakage currents.

- iii) They break the ohmic continuity of electrical signals between input and output.
- iv) These amplifiers are also used for amplifying low level signals in multi-channel applications.
- v) They can eliminate measurement errors caused by ground loops.
- vi) They are usually used as analog interfaces between systems with separated grounds.

Most important characteristics of an isolation amplifier are;

- i) Low leakage current
- ii) Low isolation impedance
- iii) Low isolation voltage (or mode) rejection
- iv) Maximum safe isolation voltage

#### 4.7 INTERFERENCE SIGNALS AND THEIR ELIMINATION

Many systems require electrical measurements which involve detection and measurement of very low level signals. The amplitudes of low level signals are generally less than 1,000 mV. These signals are amplified and then displayed or used. Now in practice, the instruments used for such measurements are in an environment which contains many sources of electrical and magnetic energy. These sources can produce undesired signals called interferences. Such signals also get amplified along with the low level signals and causes serious errors in measurements. The interference signals can be from transmitter, power cables, machineries, switching circuits, human sources and many more.

##### Classification of external Interference signals

The external interference signals are generated due to some physical phenomena. According to the physical phenomena, the external interference signals are classified as;

- a) Capacitive interference
- b) Inductive interference
- c) Ground loop interference
- d) Electromagnetic interference
- e) Conductively interference

##### Minimizing techniques of Interference effects are

- a) Use separate power supply when possible.
- b) Use only one point to ground the circuit.
- c) Use separate grounds for digital and analog signals.
- d) Use shielding to avoid RF coupling when necessary.
- e) Avoid magnetic coupling avoiding loops (use of twisted pair)
- f) Avoid direct capacitive coupling between singles tracks using ground plates and guard rings.
- g) Protecting power supply inputs with feed through to avoid interference signal paths through supply voltages.

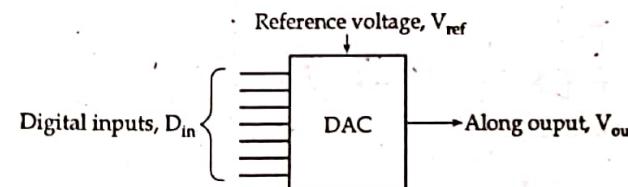
#### 4.8 SIGNAL CONVERSION (ANALOG TO DIGITAL, DIGITAL TO ANALOG)

The Most naturally occurring phenomena are analog in nature. Analog quantities are continuous functions with time and most transducers give an analog output. The data fed to digital devices normally appears in analog form. For example, a temperature difference would be represented by the voltage output of a thermocouple, the strain of a mechanical member would be represented by the voltage resulting from an unbalanced strain gauge resistance bridge. Therefore the need arises for a device that converts analog information into digital forms. Thus, analog to digital conversion devices are used in measurement and instrumentation systems.

Digital to analog conversion involves translation of digital information into equivalent analog information and this is accomplished by the use of digital to analog converter (DAC). DACs are used whenever the output of a digital circuit has to provide an analog voltage or current to drive an analog device. As an example, the output from a digital system might be converted into an analog control signal for adjusting the motor speed or the furnace temperature or for controlling almost any physical variable.

##### 4.8.1 Digital to Analog (D/A) Conversion

Basically, (D/A) conversion is the process of taking a value represented in digital code (such as simple binary or BCD) and converting it into a voltage or current which is proportional to the digital value.



Digital input  $D_{in}$  is defined as an n-bit digital word such that

$$D_{in} = D_0 \times 2^{-n} + D_1 \times 2^{-(n-1)} + D_2 \times 2^{-(n-2)} + \dots + D_{n-1} 2^{-1}$$

where,

$D_0$  = binary digit and equals a 1 or a 0. It is defined as the least significant bit (LSB) and  $D_{n-1}$  the most significant bit (MSB). The analog output signal  $V_{out}$  is related to the digital input signal,  $D_{in}$  through an analog voltage reference,  $V_{ref}$ . The relationship between these three signals is given by,

$$\begin{aligned} V_{out} &= V_{ref} (D_0 \times 2^{-n} + D_1 \times 2^{-(n-1)} + D_2 \times 2^{-(n-2)} + \dots + D_{n-1} 2^{-1}) \\ &= V_{ref} \times D_{in} \end{aligned}$$

$V_{LSB}$  may be defined as to be the voltage change when one LSB changes or mathematically,

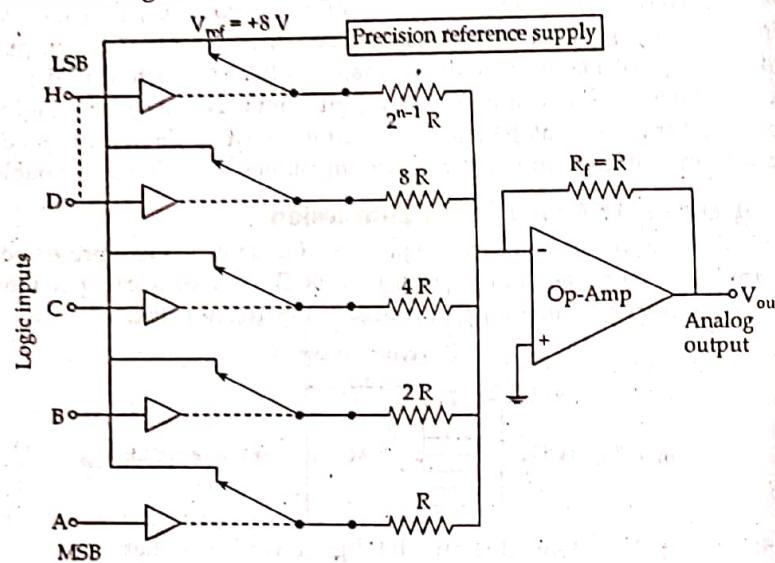
$$V_{LSB} = \frac{V_{ref}}{2^n}$$

There are various techniques which can be used to realize a DAC. The most commonly used techniques are discussed below.

#### A. Weighted resistor DAC

It consists of a precision resistor ladder network, a reference precision voltage supply, logic inputs, semiconductor switches and an operational amplifier (Op-Amp). The inputs A, B, C, D.....H are binary inputs which are assumed to have values of either 0 (low) or 8V (high), when the input is high, the switch closes and connects a precision reference supply to the input resistor and when the input is low, the switch is open. The reference supply produces a very stable, precise voltage required for generating an accurate analog input. The Op-Amp is used as a summing amplifier, which produces the weight sum of the binary inputs.

The basic configuration of a simple DAC is shown below,



In an 8-bit code input, the switch A is actuated by most significant bit (MSB) and the switch H is actuated by least significant bit (LSB). The A input has  $R_{in} = R$  and so the Op-Amp possesses the voltage at A with no attenuation i.e., the output voltage  $V_{out}$  is equal to the reference voltage,  $V_{ref}$ . The B input has  $R_{in} = 2R$ . So, it will be attenuated by half. Similarly the input C, input D and input H will be attenuated by  $\frac{1}{4}$ ,  $\frac{1}{8}$  and  $\frac{1}{2^{n-1}}$  respectively. The amplifier output can thus be expressed as,

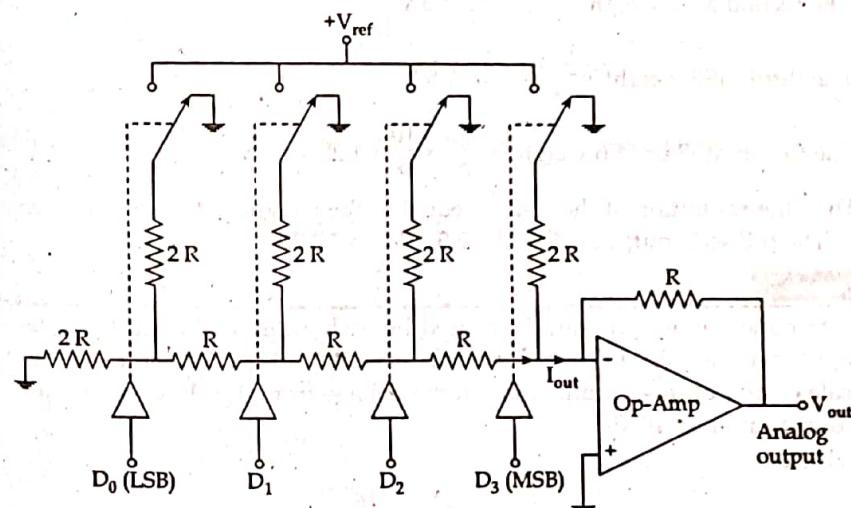
$$V_{out} = - \left( V_A + \frac{1}{2} V_B + \frac{1}{4} V_C + \frac{1}{8} V_D + \dots + \frac{1}{2^{n-1}} V_H \right)$$

The - Ve sign is present in the above equation because the summing amplifier is an inverting amplifier, but it will not concern us here.

There are two serious drawbacks of the above  $\frac{D}{A}$  conversion system. The biggest problem is the large difference in resistor values between the LSB and MSB, especially in high resolution (or many bit) DAC. With the current IC fabrication technology, it is very difficult to produce resistors of values over a wide resistance range that maintain an accurate ratio especially with variations in temperature moreover, the MSB resistor is required to handle a much greater current than that used for LSB resistor. For these reasons it is preferable to employ a circuit that uses resistances of fairly close values.

#### B. Binary ladder or R-2R ladder DAC

One of the most widely used DAC circuit is R-2R ladder network (binary ladder) where the resistors used have only two values and that in the ratio of only 2 to 1. A DAC using R-2R ladder network with four input voltages, representing 4-bits of digital data and DC voltage output is illustrated below.



The output current  $I_{out}$  depends on the positions of the four switches and the digital inputs  $D_0$ ,  $D_1$ ,  $D_2$  and  $D_3$  control the state of the switches. The current is allowed to flow through an Op-Amp current to voltage converter to give  $V_{out}$ . The output voltage (analog),  $V_{out}$  is proportional to the digital input and is given by the equation,

$$V_{out} = \left( \frac{D_0 \times 2^0 + D_1 \times 2^1 + D_2 \times 2^2 + D_3 \times 2^3}{2^4} \right) \times V_{ref}$$

The function of the ladder network is to convert the 16 possible binary values (from 0000 to 1111) into one of 16 voltage levels in steps of  $\frac{V_{ref}}{16}$ .

In general,

$$V_{out} = \left( \frac{D_0 \times 2^0 + D_1 \times 2^1 + D_2 \times 2^2 + D_3 \times 2^3 + \dots + D_{n-1} \times 2^{n-1}}{2^n} \right) V_{ref}$$

Thus we can have more digital or binary inputs and greater quantization for each step by using more sections of ladder network. In general, the voltage resolution for an n-stage ladder network is given as  $\frac{V_{ref}}{2^n}$ .

#### Example 9

Determine the resolution and full scale output and weight of each input bit for the weighted resistor DAC. Assume  $V_{ref} = 10$  V.

**Solution:**

The MSB passes with unity gain, so its weight in the output is equal to  $V_{ref}$  i.e., 10 V.

$$\text{The second MSB weight} = \frac{V_{ref}}{2} = \frac{10}{2} = 5 \text{ V}$$

$$\text{The third MSB weight} = \frac{V_{ref}}{4} = \frac{10}{4} = 2.5 \text{ V}$$

$$\text{The fourth MSB or LSB weight} = \frac{V_{ref}}{8} = \frac{10}{8} = 1.25 \text{ V}$$

Thus the resolution of the DAC is equal to the weight of the LSB i.e., 1.25 V. The full scale output is  $10 + 5 + 2.5 + 1.25 = 18.75$  V.

#### Example 10

Determine the output voltages caused by each bit in a 6-bit ladder if the input levels are 0 = OV and 1 = +6 V. Determine the resolution and full scale output of this circuit. Find out the voltage from the above ladder for a digital input of 101011.

**Solution:**

$$\text{First MSB output} = \frac{D_{n-1} \times 2^{n-1}}{2^n} = \frac{D_{n-1}}{2} = \frac{16}{2} = 8 \text{ V}$$

$$\text{Second MSB output} = \frac{D_{n-2} \times 2^{n-2}}{2^n} = \frac{D_{n-2}}{2^2} = \frac{16}{4} = 4 \text{ V}$$

$$\text{Third MSB output} = \frac{D_{n-3}}{2^3} = \frac{16}{8} = 2 \text{ V}$$

$$\text{Fourth MSB output} = \frac{16}{16} = 1 \text{ V}$$

$$\text{Fifth MSB output} = \frac{16}{32} = 0.5 \text{ V}$$

$$\text{Sixth MSB (LSB) output} = \frac{16}{64} = 0.25 \text{ V}$$

The resolution is equal to the weight of the LSB i.e., 0.25 V.

The full scale output occurs for digital input of 111111.

$$\text{i.e., } 8 + 4 + 2 + 1 + 0.5 + 0.25 = 15.75 \text{ V}$$

Thus, the voltage output for a digital input of 101011,

$$\begin{aligned} V_{out} &= \frac{D_0 \times 2^0 + D_1 \times 2^1 + D_2 \times 2^2 + D_3 \times 2^3 + D_4 \times 2^4 + D_5 \times 2^5}{2^6} \\ &= \frac{16 \times 1 + 16 \times 2 + 0 \times 4 + 16 \times 8 + 0 \times 16 + 16 \times 32}{64} = 10.75 \text{ V} \end{aligned}$$

#### 4.8.2 Analog to Digital (A/D) Conversion

The basic function of an ADC is shown below.

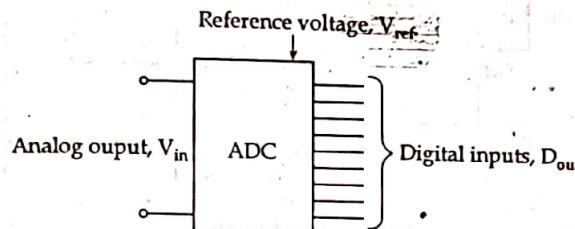


Figure: Basic function of an ADC

The digital output,  $D_{out}$  is the n-bit digital output word while  $V_{in}$  and  $V_{ref}$  are the analog input and reference signals respectively.

For an ADC, these signals are related by equation,

$$V_{ref} (D_0 2^n + D_1 \times 2^{n-1} + D_2 \times 2^{n-2} + \dots + D_{n-1} 2^1) = V_{in} \pm V_x$$

where,  $D_0$  is a binary digit and equals a 1 or a 0.  $D_0$  is also defined as the least significant bit (LSB) and  $D_{n-1}$  is the most significant bit (MSB).  $V_x$  is given by the following expression.

$$-\left(\frac{1}{2}\right) V_{LSB} \leq V_x < \left(\frac{1}{2}\right) V_{LSB}$$

The analog to digital conversion process is known as quantization. The analog to digital (A/D) conversion is the process of converting an analog input voltage into an equivalent digital signal. The operation is somewhat more complex and time consuming than the (D/A) conversion. A number of different methods have been developed and used for (A/D) conversion. Some methods are:

##### A) Ramp (A/D) conversion

This is simplest and popular method of (A/D) conversion and employs a digital counter as the register and allows the clock to increment the counter one step at a time until the reference ramp voltage,  $V_{ref}$  becomes equal to or exceeds the analog input voltage,  $V_A$ .

It is called a digital ramp ADC because the wave form of DAC's output,  $V_{ref}$  is a step-by-step ramp. It is also referred to as a counter type ADC.

Such an ADC quantizes an analog signal through conversion of the signal to a time duration pulse.

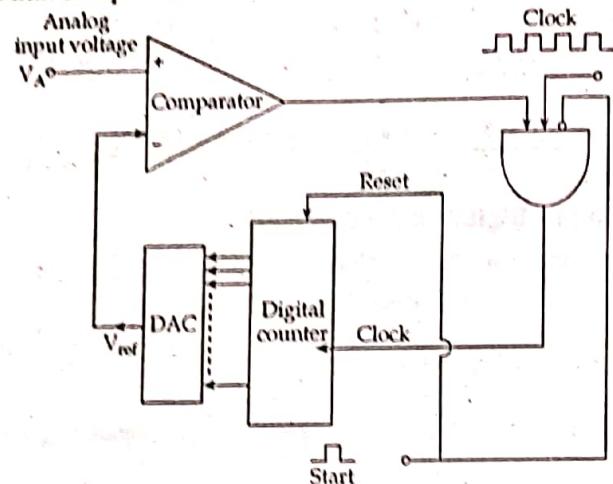


Figure: Logic diagram

Ramp ADC consists of a digital counter, a DAC, an analog comparator and a control AND gate. The digital counter advances from a zero count while the reference voltage increment for each count step. A comparator circuit, receiving both DAC's output (reference ramp voltage  $V_{ref}$ ) and analog input voltage  $V_A$ , provides a signal to stop the count when  $V_A$  rises above  $V_{ref}$ . The counter value at this time is the digital output.

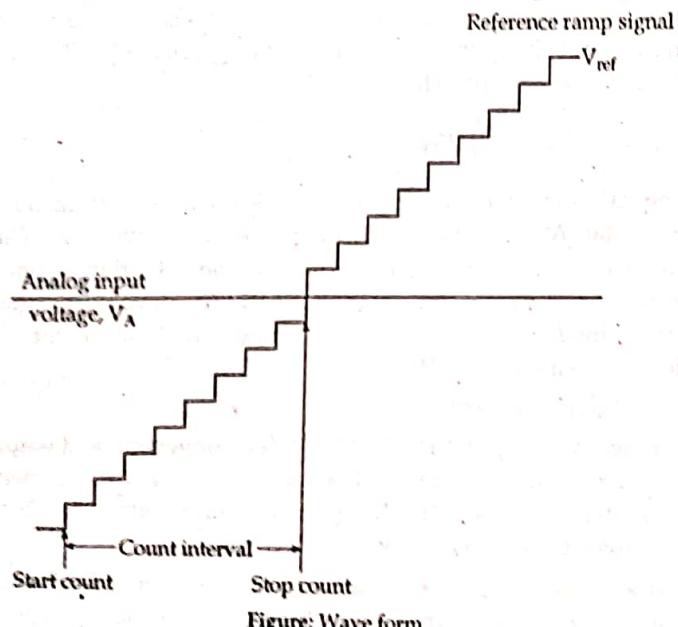


Figure: Wave form

This type of an ADC may be used for conversion of less than 10 or 12 bits at speeds that do not exceed several thousand conversions per second. Higher speeds can be obtained at lower resolution.

#### Advantages

- Very simple circuitry
- Lower cost
- Quite fast, as no need for conversion from digital to analog.

#### Disadvantages

- Poor resolution
- Poor conversion accuracy
- Precise adjustment of ramp (slope) signal and clock frequency required.

#### B) Dual slope (A/D) conversion

This is a popular method of converting an analog voltage into a digital value. The block diagram of the basic dual slope ADC is shown below.

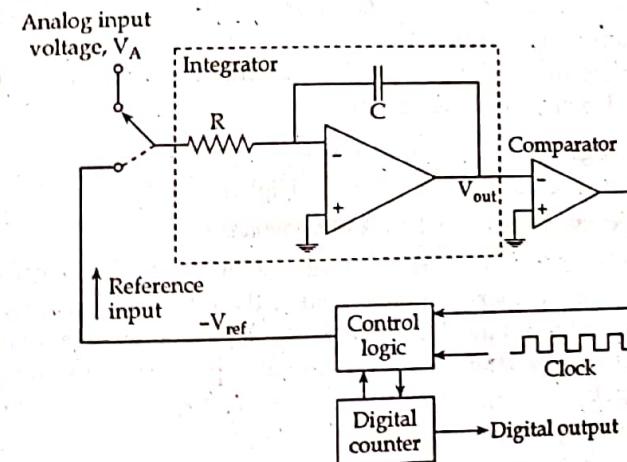


Figure: Logic diagram

The analog voltage to be converted into a digital signal is applied through an electronic switch to an integrator or ramp generator circuit, (essentially a constant current charging a capacitor to give a linear ramp voltage). The counter operated during both positive and negative slope interval of the integrator gives the digital output.

For a fixed time interval, the analog input voltage, connected to the integrator raises the voltage in the comparator to some positive levels. At the end of fixed time intervals the voltage from the integrator is greater for greater input voltages. At the end of the fixed count interval, the count is set zero and the electronic switch connects the integrator to a reference or fixed input. The integrator output or input to capacitor then decreases at a fixed rate until it drops below the comparator reference voltage, at

which the control logic receives a signal (the comparator output) to stop the count. The count shown by the counter at this time represents the digital output of the ADC.

Typically, a dual slope ADC is limited to conversion speeds of from 1,000 to 2,000 samples per second at a resolution of 10 or 12 bits as a result of limitations on the counter counting speed. The conversion rate can be increased to approximate 30,000 samples per second at a 14-bit resolution without markedly increasing the logic requirements by using a two-step integration during the second integration period.

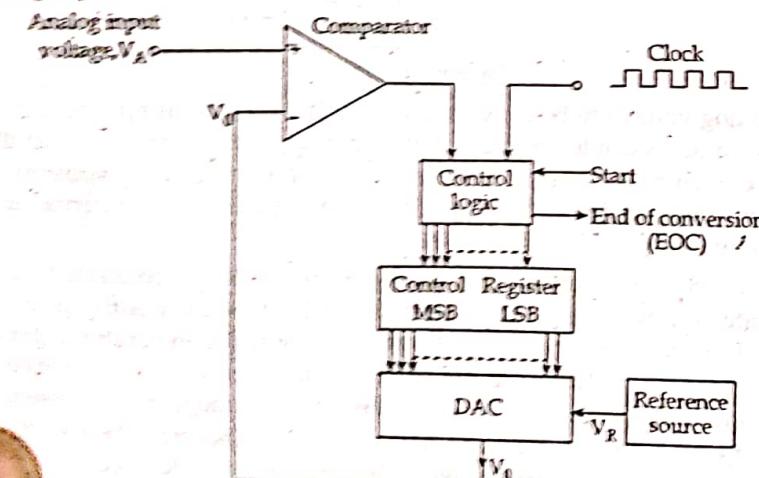
#### Advantage

- i) Clock frequency drift is compensated for, as the same clock and integrator are used to perform conversion during the positive and negative intervals of the count period.
- ii) The above reason also increases accuracy.
- iii) Low conversion time
- iv) The counter can be designed to be in binary, BCD, or any other desired display form.
- v) Setting the clock rate and reference-input value can give desired scaling of the counter output

#### Disadvantage

- i) Complicated circuitry,
- ii) Higher cost
- C) Successive Approximation (A/D) conversion

This is one of the most widely used methods of (A/D) conversion. Though it employs more complex circuitry than that used by ramp (A/D) conversion but it has much shorter conversion time. In addition, it has a fixed value of conversion time that does not depend upon the value of the analog input.



This type of ADC make direct comparison between an unknown input signal and a reference signal. The basic arrangement of a successive approximation ADC as shown in figure above.

This type of ADC however, does not employ a counter to provide the input to the DAC but employs a register instead. The DAC provides a reference variable voltage in steps. The control logic modifies the contents of the register bit by bit until the register data are the digital equivalent of the analog input  $V_A$  within the resolution of the converter. Usually the measurement sequence selects the largest step of the DAC output voltage first. The number of clock pulses represents the digital output of the DAC. Successive approximation ADC can be employed at conversion speeds of up to about 1,00,000 samples per second at resolutions of up to 16 bits. At lower resolutions; speeds of over 2,50,000 samples per second are practical.

When start button is pressed, control register or successive approximation register sets the MSB high i.e., with all other bits to zero so that the trial code becomes 1000 (for 4-bit), DAC converts the trial code into analog equivalent output of DAC given as,

$$V_0 = \frac{V_R}{2^n} [d_{n-1} \times 2^{n-1} + d_{n-2} \times 2^{n-2} + \dots + D_0 2^0] \text{ for } n\text{-bits}$$

$V_0$  is compared with  $V_A$  by comparator.

If  $V_A > V_0$ , then SAR lefts MSB at 1 and makes the next lower significant bit 1 and further compares.

If  $V_A < V_0$ , then SAR resets MSB at 0 and makes the next lower significant bit 1. This procedure is continued for all subsequent bits one at a time until all bit positions have been tested.

If  $V_A = V_0$ , the comparator changes the state and this can be taken as the end of conversion (EOC).

#### D) Parallel or simultaneous or flash type (A/D) conversion

The parallel or simultaneous or flash type ADC is the fastest type of ADC. In this type of conversion, we make use of the parallel comparators, that compares the reference voltages with the analog input voltage. Its main advantage is very high speed of conversion as the speed is restricted only by the switching time of the comparators and the gates. Its main drawback is complexity and cost. An  $n$ -bit converter of this type needs  $2^{n-1}$  comparators,  $2^n$  resistors and a priority encoder.

Figure below depicts a 3-bit flash type ADC which need  $(2^3 - 1) = 7$  comparators. In this method, a reference voltage is connected to a voltage divider that divides it into  $(2^n - 1)$  equal increment levels. Each level is compared to the analog input by a voltage comparator. For any given analog input, one comparator and all those below it will have a high output. All the comparator outputs are connected to a priority encoder,

that generates a binary output corresponding to the input having the highest priority. In this case, the one representing the largest voltage level equal to or less than the analog input. Thus the binary output represents the voltage that is the closest in value to the analog input.

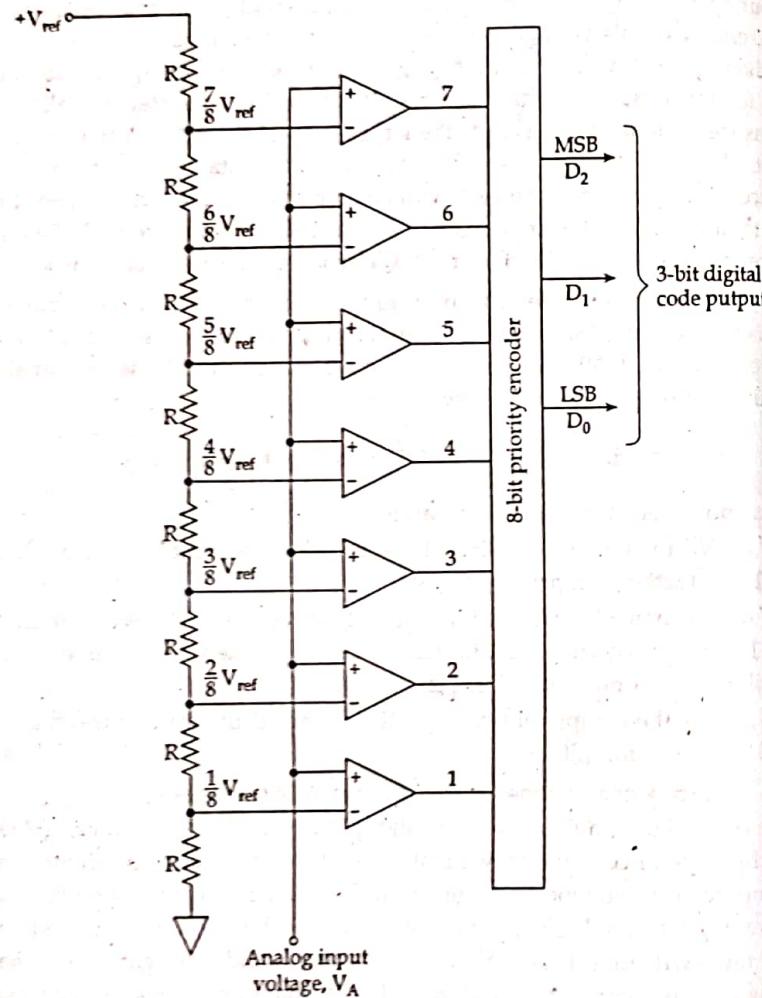


Figure: Parallel type 3-bit ADC

The flash ADC uses no clock signal because there is not timing or sequencing period. The conversion takes place simultaneously. The only delays in the conversion are in the comparators and priority encoders. The voltage applied to the inverting terminal of the upper most

comparator is  $\frac{7R}{7R+R} \times V_{ref} = \frac{7}{8} V_{ref}$  by voltage divider rule.

Similarly, the voltage applied to the inverting terminal of next comparator is  $\frac{6R}{7R+R} \times V_{ref} = \frac{6}{8} V_{ref}$  and so forth. The increment between voltage is  $\frac{1}{8} V_{ref}$ .

#### Advantage

- The fastest conversion process (governed only by propagation delay of the gates)
- Highest accuracy
- Highest resolution possible by increasing the number of comparators.

#### Disadvantages

- Very complicated circuitry
- Cost is proportional to the number of comparators. Which in turn depends on the resolution required.

The comparator and digital outputs for eight different ranges of analog input voltage are given below,

Analog input voltage, $V_A$	Comparator outputs/priority encoder inputs								Digital output		
	C <sub>7</sub>	C <sub>6</sub>	C <sub>5</sub>	C <sub>4</sub>	C <sub>3</sub>	C <sub>2</sub>	C <sub>1</sub>	C <sub>0</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>
$0 < V_A < \frac{V}{8}$	0	0	0	0	0	0	0	1	0	0	0
$\frac{V}{8} < V_A < \frac{2V}{8}$	0	0	0	0	0	0	1	1	0	0	1
$\frac{2V}{8} < V_A < \frac{3V}{8}$	0	0	0	0	0	1	1	1	0	1	0
$\frac{3V}{8} < V_A < \frac{4V}{8}$	0	0	0	0	1	1	1	1	0	1	1
$\frac{4V}{8} < V_A < \frac{5V}{8}$	0	0	0	1	1	1	1	1	1	0	0
$\frac{5V}{8} < V_A < \frac{6V}{8}$	0	0	1	1	1	1	1	1	0	1	
$\frac{6V}{8} < V_A < \frac{7V}{8}$	0	1	1	1	1	1	1	1	1	1	0
$\frac{7V}{8} < V_A < V$	1	1	1	1	1	1	1	1	1	1	1

#### Example 11

Show how 180 V will be converted in 8-bit digital form using successive approximation technique. If the clock frequency is 75 mHz, what will be the conversion time?

Solution:

For an 8-bit converter reference voltage,  $V_{ref}$  be taken as 100 V.  
so, MSB = 100 V

For setting  $D_7 = 1$ ,

$$\text{Output voltage} = V_{ref} \times \frac{2^7}{2^8} = \frac{100}{2^1} = 50 \text{ V}$$

Since  $180 - 100 = 80 > 50$ ; set  $D_7 = 1$

For setting  $D_6 = 1$

$$\text{Output voltage} = V_{ref} \times \frac{2^6}{2^8} = \frac{100}{2^2} = 25 \text{ V}$$

Hence for setting  $D_7 = 1$  and  $D_6 = 1$

$$\text{Output voltage} = 50 + 25 = 75 \text{ V}$$

Since  $80 > 75$ ; set  $D_6 = 1$ ,

For setting  $D_5 = 1$ ,  $D_6 = 1$  and  $D_7 = 1$

$$\text{Output voltage} = V_{ref} \times \frac{2^5}{2^8} + 25 + 50 = \frac{100}{8} + 25 + 50 = 87.5 \text{ V}$$

Since  $80 < 87.5 \text{ V}$ , hence set  $D_5 = 0$

All other digits will be set to zero or 1. Output will be according indicated as a result of successive approximation. The converted 8-bit digital form will be 11001100.

Now conversion time,

$$t_c = \text{Number of bits} \times \text{Time period} = 8 \times \frac{1}{75 \times 10^6} = 10.667 \times 10^{-9} \text{ sec}$$

$$\therefore t_c = 10.667 \text{ nsec.}$$

#### **Example 12**

Find the successive approximation (A/D) output for a 4-bit converter to 3.217 input if the reference is 5 V.

**Solution:**

Set  $d_3 = 1$

$$\therefore \text{Output} = \frac{5}{2^1} = 2.5 \text{ V}$$

Since  $3.217 > 2.5$  and set  $d_3 = 1$

$$\text{Set } d_2 = 1 \quad \therefore \text{output} = 2.5 + \frac{5}{2^2} = 3.75 \text{ V}$$

Since  $3.217 < 3.75$  and set  $d_2 = 0$

$$\text{Set } d_1 = 1 \quad \therefore \text{output} = 2.5 + \frac{5}{2^3} = 3.125 \text{ V}$$

Now  $3.125 < 3.217$  set  $d_1 = 1$

$$\text{Set } d_0 = 1 \quad \therefore \text{output} = 3.125 + \frac{5}{2^4} = 3.4375 \text{ V}$$

Now,  $3.4375 > 3.217$

Thus output of A/D converter is 1010.

#### **4.9 BOARD EXAM QUESTIONS SOLUTION**

1. Describe the block diagram of ac signal conditioning system with a suitable example. [2011/F]

**Solution:** See the definition of 4.1 A

2. Write short notes on interference signal. [2011/F, 2016/S]

**Solution:** See the definition of 4.7.

3. Explain the working principle of instrumentation amplifier with necessary sketch. [2014/F, 2015/F, 2015/S, 2016/F]

**OR**

Write short notes on instrumentation amplifier.

[2012/F]

4. Write short notes on amplifier applications.

[2014/F]

- Solution:** See the definition of 4.5.

5. Write short notes on isolation amplifier.

[2012/S, 2013/S, 2015/F, 2016/F, 2017/S, 2019/F]

- Solution:** See the definition of 4.6.

6. What is an instrumentation amplifier? How does it differ from a single Op-Amp differential amplifier? What are the ideal characteristics of Op-Amp. [2018/S]

- Solution:** See the definition of 4.3 and 4.4.1.

7. Write short notes on signal conditioning.

[2018/S]

- Solution:** See the definition of 4.1.

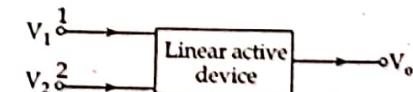
8. Write short on common mode rejection ratio and its significance in instrumentation. [2017/F]

**Solution:**

Common mode rejection ratio (CMRR) is defined as the ratio of differential voltage gain to common mode voltage gain and it is given as

$$\text{CMRR} = \frac{A_d}{A_{cm}}$$

If a differential amplifier is perfect, CMRR would be infinite because in that case common mode voltage gain  $A_{cm}$  would be zero.



In an ideal differential amplifier the output signal  $V_{out}$  is given as,

$$V_{out} = A (V_1 - V_2)$$

where,  $A$  is the gain of the differential amplifier

$$\text{Difference signal, } V_d = V_1 - V_2 \quad (1)$$

and, Common mode signal,  $V_{cm} = \frac{1}{2} (V_1 + V_2)$  (2)

Now let the output voltage  $V_{out}$  be expressed as a linear combination of two input voltages,

$$V_{out} = A_1 V_1 + A_2 V_2$$

where,  $A_1$  = Voltage gain for input  $V_1$  with  $V_2$  grounded.

$A_2$  = Voltage gain for input  $V_2$  with  $V_1$  grounded

$$\text{Also, } V_1 = V_{cm} + \frac{1}{2} V_d$$

$$\text{and, } V_2 = V_{cm} - \frac{1}{2} V_d$$

Thus,

$$\begin{aligned} V_{out} &= A_1 \left( V_{cm} + \frac{1}{2} V_d \right) + A_2 \left( V_{cm} - \frac{1}{2} V_d \right) \\ &= \frac{1}{2} (A_1 - A_2) V_d + (A_1 + A_2) V_{cm} \\ &= A_d V_d + A_{cm} V_{cm} \end{aligned}$$

$$\text{where, } A_d = \frac{A_1 - A_2}{2}$$

$$\text{and, } A_{cm} = A_1 + A_2$$

Here  $A_d$  is the voltage gain for the difference signal while  $A_{cm}$  is the voltage gain for the common mode signal.

$$\text{Thus, CMRR} = \frac{A_d}{A_{cm}}$$

$$\therefore \text{CMRR in dB} = 20 \log_{10} \left( \frac{A_d}{A_{cm}} \right)$$

Hence, higher the value of CMRR, better is the performance of differential amplifier. For improvement of CMRR, it is necessary to reduce common mode gain  $A_{cm}$ . CMRR is the ability of amplifier to reject the common mode signals (unwanted signals) while amplifying the differential signals (desired signals). The higher the CMRR, the better in which the open loop gain is high and common mode gain is low.

For example; when measuring the resistance of a thermocouple in a noisy environment, the noise from the environment appears as an offset on both input leads making it a common mode voltage signal. The CMRR of the measurement instrument determines the attenuation applied to the offset or noise.

#### 9. Write short notes on flash ADC.

[2013/F]

**Solution:** See the definition of 4.8.2 D.

#### 10. What do you understand by signal conditioning? Explain atleast three signal conditioning techniques used in instrumentation.

[2013/F]

**Solution:** See the definition of 4.1 and 4.2.

#### 11. Write short notes on filtering and its types. [2014/S, 2015/S, 2018/S]

**Solution:**

An electric filter is a network designed to attenuate certain frequencies but pass others without attenuation. Electrical filters are used in practically all circuits which require separation of signals according to their frequencies.

Filters may be classified in a number of ways as follows:

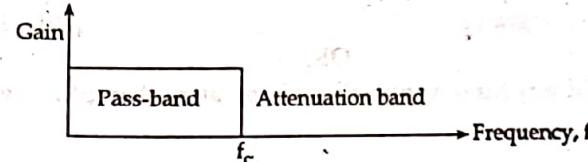
- a) Analog or digital filters
- b) Active or passive filters
- c) Audio frequency or radio frequency filters

Analog filters are designed to process analog signals using analog techniques while digital filter process analog signals using digital techniques. A passive filter is built with passive components such as resistors, capacitor and inductors while active filters make use of transistor or Op-Amp in addition to resistors and capacitors.

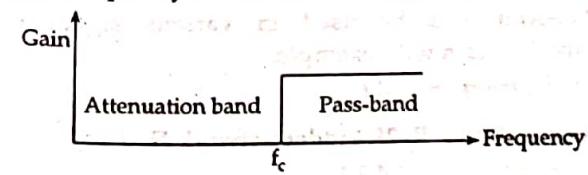
Filters may be classified as,

- a) Low pass filters
- b) High pass filters
- c) Band pass filters
- d) Band stop filters
- e) All pass filters

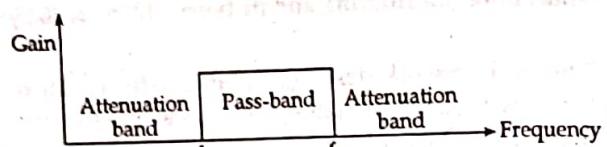
A filter that provides a constant output from dc up to a cutoff frequency  $f_c$  and then passes no signal above that frequency is called an ideal low pass filter.



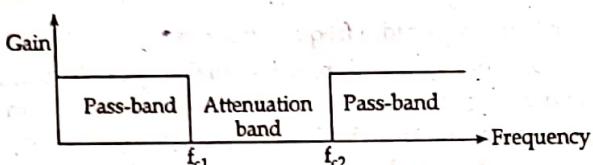
A filter that provides or passes signals above a cutoff frequency  $f_c$  is a high pass filter. It has a zero gain starting from zero to a frequency  $f_c$ , called the cutoff frequency and above this frequency, the gain is constant.



When the filter circuit passes signals that are above one cutoff frequency and below a second cutoff frequency, it is called a band-pass filter. Thus a band pass filter has a pass band between two cutoff frequencies  $f_{c2}$  and  $f_{c1}$  where  $f_{c2} > f_{c1}$  and two stop bands;  $0 < f < f_{c1}$ ; and  $f > f_{c2}$ .



The band stop or band reject filter performs exactly opposite to the band pass i.e., it has a band stop between two cutoff frequencies  $f_{c2}$  and  $f_{c1}$  and two pass bands:  $0 < f < f_{c1}$  and  $f > f_{c2}$ . This is also called a band elimination or notch filter.



12. Write short notes on wave shaping. [2014/S]

Solution: See the definition of 4.2 G.

13. Explain successive approximation type analog to digital converter used in instrumentation system with numerical example. [2011/S, 2012/F, 2013/F, 2017/F, 2017/S, 2019/F]

Solution: See the definition of 4.8.2 C and example 12.

14. Explain with the circuit diagram, how does an Op-Amp act as

- i) an inverter
- ii) a summer
- iii) a sub tractor
- iv) an integrator

[2011/S, 2017/S]

OR

Describe any three application of operational amplifier with neat sketch. [2012/F]

OR

Explain how the Op-Amp can be used as an integrator and differentiator with necessary diagrams and equations. [2016/S]

OR

How Op-Amp can be used in various signal processing operations? Explain with examples. [2018/F]

Solution: See the definition of 4.5.

15. Write short notes on R-2R ladder network DAC. [2018/F]

Solution: See the definition of 4.8.1

16. Describe the working principle of stair case ramp type ADC. List its draw backs. [2018/F]

Solution: See the definition of 4.8.2 A.

Drawbacks of stair case ramp type ADC are,

- i) Speed is less since each time the counter has to begin from zero.
- ii) There may be conflicts if the next input is sampled before completion of one process.

17. Sketch the circuit of summing amplifier using Op-Amp to get  $V_o = 2 V_1 - 3 V_2 - 5 V_3$ . [2014/S]

Solution:

$$V_o = 2 V_1 - 3 V_2 - 5 V_3 = -(-2 V_1 + 3 V_2 + 5 V_3)$$

We know,

$$V_o = -\left[\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \frac{R_f}{R_3} V_3\right]$$

$$\text{Thus, } \frac{R_f}{R_1} = 2$$

$$\frac{R_f}{R_2} = 3$$

$$\frac{R_f}{R_3} = 5$$

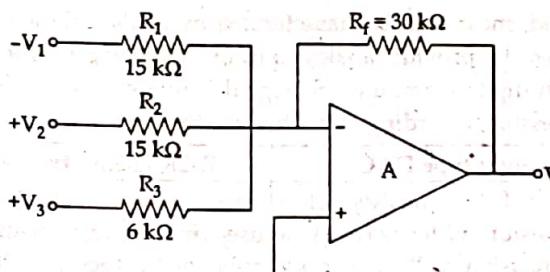
$$\text{Let, } R_f = 30 \text{ k}\Omega$$

$$\therefore R_1 = \frac{30}{2} = 15 \text{ k}\Omega$$

$$\therefore R_2 = \frac{30}{3} = 10 \text{ k}\Omega$$

$$\therefore R_3 = \frac{30}{5} = 6 \text{ k}\Omega$$

Thus, summing amplifier diagram is



18. Sketch the circuit of summing amplifier using Op-Amp to get  $V_o = V_1 - 2 V_2 - V_3$ . [2017/F]

Solution:

$$V_o = V_1 - 2 V_2 - V_3 = -[-V_1 + 2 V_2 + V_3]$$

We know,

$$V_o = -\left[\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \frac{R_f}{R_3} V_3\right]$$

$$\text{Thus, } \frac{R_f}{R_1} = 1$$

$$\frac{R_f}{R_2} = 2$$

$$\frac{R_f}{R_3} = 1$$

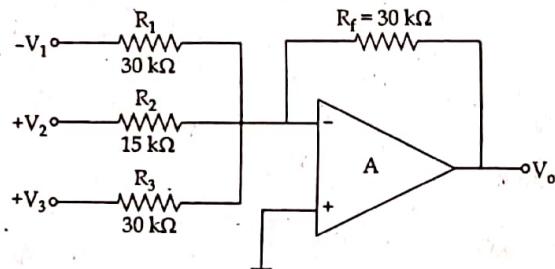
Let,  $R_f = 30 \text{ k}\Omega$

$$\text{so, } R_1 = \frac{30}{1} = 30 \text{ k}\Omega$$

$$R_2 = \frac{30}{2} = 15 \text{ k}\Omega$$

$$R_3 = \frac{30}{1} = 30 \text{ k}\Omega$$

Hence summing Op-Amp circuit is,



19. Why signal conversion is required? Differentiate between binary weighted type and R - 2R ladder type DAC. [2014/S]

**Solution:**

In the real world, most data is characterized by analog signals. Most of the sensors used to provide analog output while data processing is carried out with digital computer. So signal conversion is necessary for analyzing, processing, recording and other works.

Binary weight type DAC	R-2R ladder type DAC
a) This type of DAC consists of a precision resistor ladder network, a reference precision voltage supply logic inputs, semiconductor switches and Op-Amp.	This type of ADC is mostly used and the resistor used have only two values and that is in the ratio of only 2 to 1.
b) It is expensive	It is cheaper
c) It has fast conversion rate	It has slow conversion rate
d) It uses summing type Op-amp circuit.	It uses non-inverting type Op-Amp for non inverting ladder DAC and inverting Op-Amp for inverting type.

e) Op-Amp acts as summer amplifier that produce weighted sum of binary inputs.	Op-Amp acts as a current to voltage converter to provide an output.
f) For n-bit system, $V_o = \frac{V_{ref}}{2^{n-1}} \times R_f$ $(D_{n-1} 2^{n-1} + D_{n-2} 2^{n-2} + \dots + D_0 2^0)$	For n-bit system, $V_o = \frac{V_{ref}}{2^n R}$ $R_f [D_{n-1} 2^{n-1} + D_{n-2} 2^{n-2} + \dots + D_0 2^0]$

20. A 8-bit DAC has reference voltage of 16 V. It uses an R-2R ladder network. Find the minimum value of R such that the output current of the ladder does not exceed 12 mA. Also find the smallest value of quantized current. [2013/S]

**Solution:**

Reference voltage,  $V_r = 16 \text{ V}$

Minimum value of R = ?

Maximum output current = 12 mA

We know,

The output current is maximum when all the bits are 1.

Maximum output current is,

$$I_{out(max)} = \frac{V_r}{R} \times \frac{2^n - 1}{2^{n-1}}$$

$$\text{or, } 0.012 = \frac{16}{R} \times \frac{2^8 - 1}{2^{8-1}}$$

$$\text{or, } R = 16 \times \frac{255}{128} \times 83.88$$

$$\therefore R = 2,656.250 \Omega$$

Hence minimum value of R is 2.656 kΩ  
and, Smallest value of quantized current

$$I_{min} = \frac{V_r}{2^{n-1} \times R} = \frac{16}{2^{8-1} \times 2,656.250} = \frac{16}{128 \times 2,656.250} = 0.00004705 \text{ A}$$

$$\therefore I_{min} = 47 \mu\text{A}$$

21. Find the digital output of 8.217 volt input from a 4-bit successive approximation ADC with reference voltage of 10 volt. [2014/F, 2015/F, 2015/S, 2016/F]

**Solution:**

$$V_{in} = 8.217 \text{ volt}$$

$$V_{ref} = 10 \text{ volt}$$

Number of bit, n = 4

We have,

$$V_o = \frac{V_{ref}}{2^n} [D_{n-1} 2^{n-1} + D_{n-2} 2^{n-2} + \dots + D_0 2^0]$$

Let  $D_3 = 1$ , then

$$V_0 = \frac{10}{2^4} [D_3 2^3 + D_2 2^2 + D_1 2^1 + D_0 2^0] = \frac{10}{2^4} [1 \times 2^3 + 0 + 0 + 0] \\ = 5 \text{ V} < 8.217 \text{ V}, \text{ so set } D_3 = 1$$

Set  $D_2 = 1$ ,

$$V_0 = \frac{10}{2^4} [1 \times 2^3 + 1 \times 2^2 + 0 + 0] = \frac{10}{16} \times 12 \\ = 7.50 \text{ V} < 8.217 \text{ V}, \text{ so set } D_2 = 1$$

Set  $D_1 = 1$

$$V_0 = \frac{10}{2^4} [1 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 0] = \frac{10}{16} \times 14 \\ = 8.74 \text{ V} > 8.217, \text{ so set } D_1 = 0$$

Set  $D_0 = 1$

$$V_0 = \frac{10}{2^4} [1 \times 2^3 + 1 \times 2^2 + 0 \times 2^1 + 1 \times 2^0] = \frac{10}{16} \times 13 \\ = 8.125 \text{ V} < 8.217 \text{ V} \text{ so set } D_0 = 1$$

Hence digital output of 8.217 V analog input is  $(D_3 D_2 D_1 D_0) = (1101)$ .

22. Find the successive approximation (SAR) ADC output for a 4 bit converter to a 3.217 V input, if the reference voltage is 5 V.  
[2012/S, 2016]

Solution:

Input voltage,  $V_{in} = 3.217 \text{ V}$

Reference voltage,  $V_{ref} = 5 \text{ V}$

Number of bits,  $n = 4$

We know,

$$V_0 = \frac{V_{ref}}{2^n} [D_{n-1} 2^{n-1} + D_{n-2} 2^{n-2} + \dots + D_0 2^0]$$

For 4 bit,

$$V_0 = \frac{V_{ref}}{2^n} [D_3 2^3 + D_2 2^2 + D_1 2^1 + D_0 2^0]$$

Set  $D_3 = 1$ ,

$$V_0 = \frac{5}{2^4} [1 \times 2^3 + 0 + 0 + 0] = \frac{5}{16} \times 8 = 2.50 \text{ V} < 3.217 \text{ V} \text{ so set } D_3 = 1$$

Set  $D_2 = 1$

$$V_0 = \frac{5}{16} [1 \times 2^3 + 1 \times 2^2 + 0 + 0] = \frac{5}{16} \times 12 \\ = 3.75 \text{ V} > 3.217 \text{ V} \text{ so set } D_2 = 0$$

Set  $D_1 = 1$

$$V_0 = \frac{5}{16} [1 \times 2^3 + 0 + 1 \times 2^1 + 0] = 3.125 \text{ V} < 3.217 \text{ V} \text{ so set } D_1 = 1$$

Set  $D_0 = 1$

$$V_0 = \frac{5}{16} [1 \times 2^3 + 0 + 1 \times 2^1 + 1 \times 2^0] \\ = \frac{5}{16} \times 11 = 3.4375 \text{ V} > 3.217 \text{ V} \text{ so set } D_0 = 0$$

Thus digital output of 3.217 V is 1010.

23. What will be the successive approximation digital output for a analog input of 3.12 V from a 4 bit converter given that  $E_R = 8 \text{ V}$ . also draw the circuit.  
[2012/F]

Solution:

$$V_{in} = 3.12 \text{ V} \text{ (analog input)}$$

Number of bits,  $n = 4$

$$V_r = 8 \text{ V}$$

Set  $D_3 = 1$

$$V_0 = \frac{8}{16} [1 \times 2^3 + 0 + 0 + 0] = \frac{8}{16} \times 8 = 4 \text{ V} > 3.12 \text{ V}. \text{ So set } D_3 = 0$$

Set  $D_2 = 1$

$$V_0 = \frac{8}{16} [0 + 1 \times 2^2 + 0 + 0] = \frac{8}{16} \times 4 = 2 \text{ V} < 3.12 \text{ V} \text{ so set } D_2 = 1$$

Set  $D_0 = 1$

$$V_0 = \frac{8}{16} [0 + 1 \times 2^2 + 1 \times 2^1 + 1 \times 2^0] = \frac{8}{16} \times 7 \\ = 3.50 > 3.12 \text{ V}, \text{ so set } D_0 = 0$$

Hence output of analog input is 0110

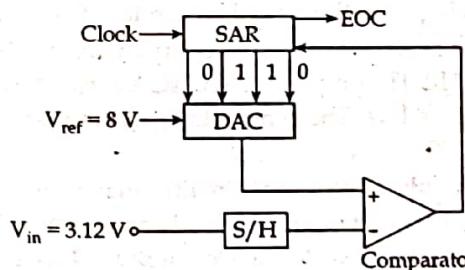


Figure: Circuit for successive approximation ADC

24. Consider a 6 bit DAC with a resistance of  $320 \text{ k}\Omega$  in LSB position. The converter is designed with weighted resistive network. The reference voltage is  $10 \text{ V}$ . The output of the resistive network is connected to an Op-Amp with a feedback resistance of  $5 \text{ k}\Omega$ . What is the output voltage for a binary input of 111010? [2019/F]

Solution:

$$\text{Output current, } I_0 = \frac{E}{R} \left[ d_{n-1} + \frac{d_{n-2}}{2} + \dots + \frac{d_1}{2^{n-2}} + \frac{d_0}{2^{n-1}} \right]$$

Given that;  $n = 6$

Resistance in LSB =  $2^{n-1} R = 2^{6-1} R$

$$\text{or, } 320 = 32 \times R$$

$$\therefore R = 10 \text{ k}\Omega$$

Thus, for binary input of 111010

$$I_0 = \frac{10}{10 \times 10^3} \left[ 1 \times 1 + 1 \times \frac{1}{2} + 1 \times \frac{1}{4} + 0 \times \frac{1}{8} + 1 \times \frac{1}{16} + 0 \times \frac{1}{32} \right]$$

$$= 1.8125 \text{ mA}$$

Therefore output voltage,

$$E_0 = I_0 R_f = -1.8125 \times 5 \times 10^3$$

$$\therefore E_0 = -9.0625 \text{ V.}$$

25. Discuss the different steps involved in successive approximation method to convert analog voltage 13.3 V to its equivalent digital voltage.

[2017/S]

**Solution:**

Draw basic arrangement of a successive approximation ADC from topic 4.8.2 C.

On the first clock pulse, the output register is loaded with 1000 which is converted by the DAC to 8 V. The voltage comparator determines that 8 V is less than the analog input (13.3 V), so the control 1100 logic retain that bit.

On the next clock pulse, the control circuitry makes the output register to be loaded with 1100. The output of the DAC is now 12 V, which is found by the comparator lesser than the analog input. So again the output of the comparator goes high and the control logic retain that bit.

On the next clock pulse, the control circuitry makes the output register to be loaded with 1110. The output of the DAC is now 14, which is found by the comparator goes low. The control logic clears that bit, so the output returns back to 1100.

On the next clock pulse, the control circuitry makes the output register to be loaded with 1101. The output of DAC is now 15 V, which is found by the comparator greater than the analog input. Thus on the next clock pulse, the control logic makes the output register to be loaded with 1101. Thus the output of the ADC is 1101 which is the nearest integer value to the input. At this point, all of the register bits have been processed, the conversion is complete and the control logic activates the EOC output to signal that the digital equivalent of  $V_A$  is now in the output register.

26. Compare and contrast instrumentation amplifier and operational amplifier.

**Solution:** See the definition of 4.3.

[2012/S]