Chapter 4

Signal Conditioning and Processing

Signal Conditioning and its importance

The signal conditioner takes the output from the sensor and converts it into suitable condition so that the rest of the element of the measurement system can perform their particular work satisfactorily. Example: operational Amplifier

It is used for manipulating the signal in such a way that it meets the requirement of the next stage for further processing.

The signal conditioning equipment may be required to do processes like amplification, attenuation, integration, differentiation, addition and subtraction and also required to do non-linear processes like modulation, demodulation, sampling, filtering and wave shaping (clipping and clamping)

Amplification

Amplifiers increase voltage level to better match the analog to digital converter (ADC) range, thus increasing the measurement resolution and sensitivity. In addition, using external signal conditions located loser to the signal source or transducer, improves the measurement signal to noise ratio by magnifying the voltage level before it is affected by environmental noise.

Attenuation

Attenuation, the opposite of amplification, is necessary when voltages to be digitalized are beyond the ADC range. This form of signal conditioning decreases the input signal amplitude so that the conditioned signal is within ADC range. It is typically necessary when measuring voltages are more than 10V.

Filtering

Filter rejects unwanted noise within a certain frequency range. Oftentimes, low pass filters are used to block out high frequency noise in electrical measurements such as 60 Hz power. It is used to prevent aliasing from high frequency signals which is done by using an antialiasing filter to attenuate signals above the Nyquist frequency.

Clipping and clamping

The diode clamper is a wave shaping circuit that shifts the signal voltage to a desired level. The clipping circuits are diode-operated wave shaping circuits that change the V-I characteristics in response to the level of the applied signal. A diode can be considered as a voltage- controlled switch.

Operational Amplifier in Instrumentation

OPAMP is an extremely versatile device that does countless works like isolation, inversion, addition, subtraction, multiplication, division, integration and differentiation. The operational amplifier manufactured with integrated circuit technology contains transistors, diodes, resistors and capacitors.

There are two modes of operation of an operational amplifier

1. Non-inverting mode
   Here, the input voltage is applied to pin 3 and the ouput voltage has the same sign as the input.

2. Inverting mode
   Here, the voltage is applied to inverting input pin 2 and the output voltage has a sign which is opposite to that of the input.
   One of the most popular OPAMP is the 741 type.

Ideal Operational Amplifier

The properties of an ideal operational amplifier are:

a. It should have an infinite input impedance i.e. $Z_i = \infty$.
b. It should have a zero output impedance i.e $Z_o = 0$
c. It should have an infinite open loop gain i.e $A_{v01} = -\infty$.
d. It should have a flat frequency response over a wide range of frequency i.e. its bandwidth BW= ∞.
e. It should have a zero output voltage i.e. $V_o = 0$ (equal voltages are applied to inverting and non-inverting ends of the amplifier)

1. Non-inverting amplifier

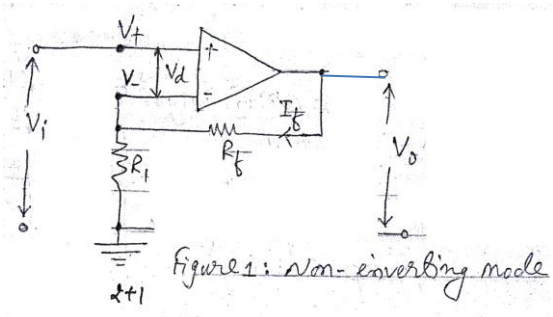


Figure 1: Non-inverting mode

Here, $V_+ = V_i$ ……..(1)

$V_o = I_f (R_f + R_1)$

$\therefore I_f = \frac{V_o}{R_f + R_1}$ ……(2)

$V_- = I_f R_1$

$= \frac{V_o}{R_f + R_1} * R_1$

$= \frac{R_1}{R_f + R_1} * V_o$ ……(3)

As we know that

$V_o = A_{v01}(V_+ - V_-) = A_{v01}\left(Vi - \frac{V_o}{R_f + R_1} * V_o\right)$

$\therefore \frac{V_o}{Av01} = V_i - \left(\frac{R_1}{R_f + R_1}\right) V_o$ ……..(4)

As the output voltage from the OPAMP will be no more than 15 V i.e. a finite quantity and open loop gain A_{v01} is very large, may be taken as infinite, hence the ratio ($\frac{V_o}{Av01}$)tends to zero. So equation (4) becomes

$$V_i - \left(\frac{R_1}{R_f+R_1}\right)V_o = 0$$

or, $V_i = \left(\frac{R_1}{R_f+R_1}\right)V_o$

$$\therefore \frac{V_o}{V_i} = \frac{R_f+R_1}{R_1} = \left(1+\frac{R_f}{R_1}\right) \text{ ……..(5)}$$

Voltage follower mode/ Isolation mode/Buffer mode

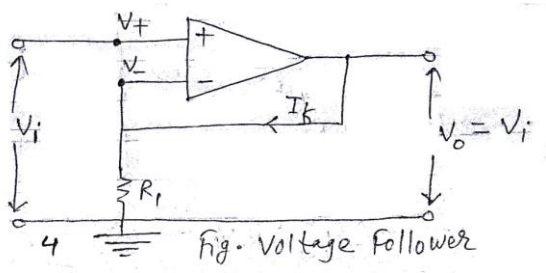


Fig. Voltage Follower

If the feedback resistor R_f =0 as shown in the figure, the circuit is said to be working in isolation mode. Then from equation (5) we get,

$$A = \frac{V_o}{V_i} = 1$$

or, $V_o = V_i$ i.e. the output of the OPAMP exactly tracts/copy/ follows the input voltage in sign and magnitude, so called a voltage follower.

The voltage follower possesses the following characteristics

a. It has large input impedance
b. It has a unity gain
c. It has small value of output impedance

It is used to reduce loading effect as it has high input i
to serve as an ideal Buffer (isolation circuit) and for in

2. Inverting mode

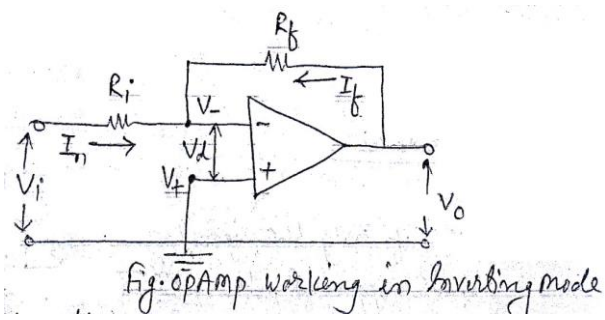


Fig. OPAmp working in Inverting mode

Here, $V_+ = 0$

As we have ,

$V_d = V_+ - V_- = 0$

or, $V_- = V_+ = 0$……..(1)

The V_- is also virtually grounded . Applying KCL at node V_-,

$I_n + I_f = 0$

Or, $\frac{(V_i - V_-)}{R_i} + \frac{V_o - V_-}{R_f} = 0$ (using equation 1)

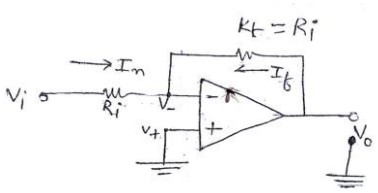
Or, $\frac{V_i}{R_i} + \frac{V_o}{R_f} = 0$

Or, $\frac{V_o}{R_f} = -\frac{V_i}{R_i}$

$$\frac{V_o}{V_i} = A = -\frac{R_f}{R_i} \text{ ……(2)}$$

Applications of the operational Amplifier in instrumentation

1. Inverter

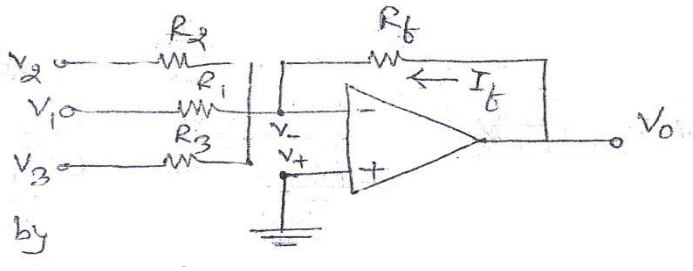


We have,

$$\frac{V_o}{V_i} = A = -\frac{R_f}{R_i}$$

If R_f=R_i, then V_o = -V_i i.e. the output voltage is 180° out of phase with the input voltage.

2. Adder



Here, if only the signal V_1 is applied, then the output is given by

$$V_{01} = -\frac{R_f}{R_1} * V_1 \text{.....(1)}$$

Similarly, $V_{o2} = -\frac{R_f}{R_2} * V_2$.....(2)

$$V_{o3} = -\frac{R_f}{R_3} * V_3 \text{ .....(3)}$$

If all the three signals are applied simultaneously, then the output can be obtained by superposition theorem as

$$V_o = V_{o1}+V_{o2}+V_{o3} = -\left(\frac{R_f}{R_1} * V_1 + \frac{R_f}{R_2} * V_2 + \frac{R_f}{R_3} * V_3\right)$$

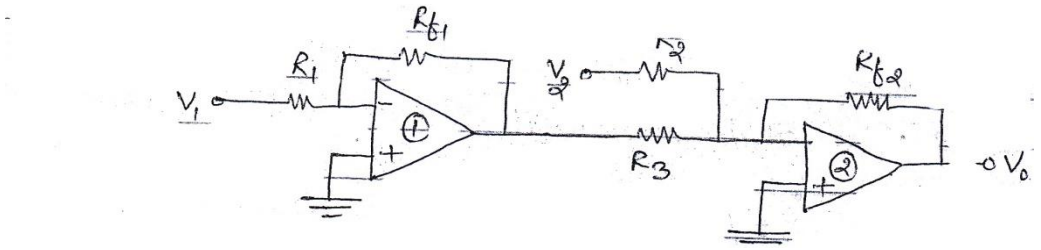
If $R_f = R_1=R_2=R_3$, the circuit acts as a pure adder and the output voltage is

$V_O = -(V_1+V_2+V3)$ i.e. sum of the individual input voltages.

3. Subtractor

The output from OPAMP (1) is given by

$$V_{O1} = -\frac{R_{f1}}{R_1} * V_1 \text{ .....(1)}$$



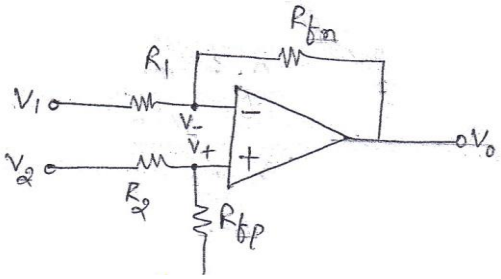
and the final output i.e from OPAMP (2) is given by

$$V_O = -[\frac{R_{f2}}{R_2} * V_2 + \frac{R_{f2}}{R_3} * V_{01}]$$

$$= -[\frac{R_{f2}}{R_2} * V_2 + \frac{R_{f2}}{R3} * (-\frac{R_{f1}}{R_1} * V_1)]$$

If $R_{f1} = R_{f2} = R_1 = R_2 = R_3$, the circuit acts as a pure subtractor and the output voltage is

$V_0 = V_1 - V_2$ Using single OPAMP



Here,

$V_+ = (\frac{R_{fp}}{R_2 + R_{fp}}) * V_2$……(1)

If only V_+ is applied, the output is

$V_{o+} = \left(1 + \frac{R_{fn}}{R_1}\right) * V_+$ as non- inverting amplifier.

As, $V_{O+} = \left(1 + \frac{R_{fn}}{R_1}\right) * \left(\frac{R_{fp}}{R_2 + R_{fp}}\right) * V_2$…….(2)

If only V_1 is applied , the output is given by

$V_{O2} = -\frac{R_{fn}}{R_1} * V_1$ ……..(3) as inverting amplifier

If both signals are applied simultaneously, the output can be obtained by superposition theorem as

$V_O = V_{O+} + V_{O1}$

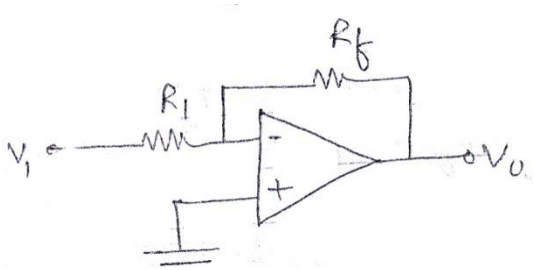
$$= \left(1 + \frac{R_{fn}}{R_1}\right) * \left(\frac{R_{fp}}{R_2 + R_{fp}}\right) * V_2 - \left(\frac{R_{fn}}{R_1} * V_1\right)$$

If $R_{fn} = R_{fp} = R_1 = R_2$,

$V_0 = V_2 - V_1$ i.e the circuit performs subtraction without amplification.

4. Multiplier and Divider

The output voltage of an OPAMP in inverting mode is $V_0 = \frac{-R_f}{R_1} * V_1$



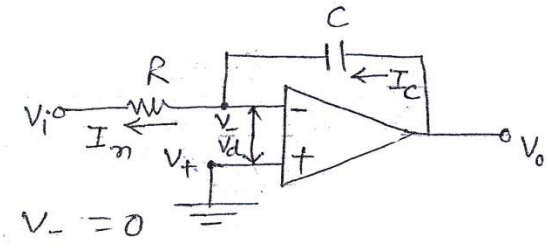
If R_f >R, then the circuit works as multiplier. Suppose, R_f =100 MΩ and R_1=10 MΩ, then

V_O=-10V_1 i.e. the input gets multiplier by a factor 10.

If R_f<R, the circuit acts as divider.

Suppose, R_f=10 MΩ and R_1 = 100 MΩ then $V_O = \frac{V_1}{10}$ i.e the input gets divided by a factor of 10.

5. Integrator



Here, V_+=0

Since for ideal OPAMP, the output voltage V_O is zero, so

V_d =V_+-V_- = 0

or, V_+=V_-=0

Applying KCL at mode V_-,

I_C= I_n

Or, $C\frac{d}{dt}(V_0 - V_-) = -\frac{V_i}{R}$

Or, $C\frac{dV_0}{dt} = -\frac{V_i}{R}$

Or, $\frac{dV_0}{dt} = -\frac{V_i}{CR}$

Integrating both sides w.r.to t, we get

$V_0 = -\frac{1}{Rc}\int V_i dt = -\frac{1}{\tau}\int V_i dt$

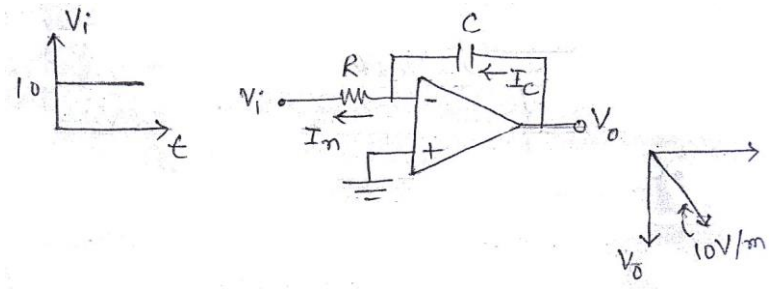
Where,

τ = RC is the time constant of the RC circuit.

Example

Design an integrator which gives a ramp output of -10 V/ms.

Solution:



As the output is a ramp voltage, the input signal V_i should be a dc voltage.

Let V_i=10 V

We know,

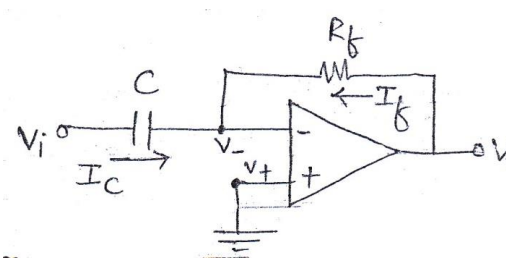
$V_0 = -\frac{1}{RC}\int V_i dt = -\frac{10}{RC} * t$

or, $\frac{V_0}{t} = -\frac{10}{RC} = 10^{-4}$

If R = 1 KΩ then C=10^{-6} F=1 μF.

Therefore, RC=10^{-3}

6. Differentiator



Here, $V_+ = 0$ and

$V_+ - V_- = 0$

or, $V_- = V_+ = 0$

Applying KCL at node V-, we get

$I_C + I_f = 0$

Or, $C\frac{d}{dt}(V_i - V -) + \frac{Vo-V_-}{R} = 0$

or, $C\frac{dV_i}{dt} = -\frac{Vo}{R}$

or, $V_0 = -RC\frac{dV_i}{dt}$

$\therefore V_0 = -\tau\frac{dV_i}{dt}$ where, $\tau = RC$

Example

Sketch the circuit of summing Amplifier using OPAMP to get

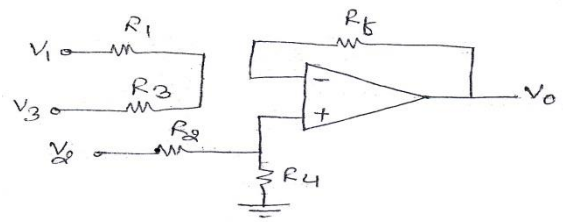
V_0 = -V_1+2V_2-3V_3

Solution,

Here –ve sign of V_0 = -V_1+2V_2-3V_3 indicates inverting terminal input and +ve sign parts of the given output equation indicates non-inverting terminal input.

Now, V_0 = -V_1+2V_2-3V_3 .....(1)

where, -1,+2,-3 indicates the gain.



The resistance between output and inverting terminals i.e R_f and ground and non-inverting terminals i.e R_4 should be identical. Suppose, $R_f = R_4 = 100\ K\Omega$

Using Superposition theorem, for inverting terminals

$V_{O1} = -\frac{R_f}{R_1} * V_1$

or, $\frac{Vo1}{V1} = -\frac{R_f}{R_1} = A\ (Closed\ loop\ gain)$

Comparing with equation (1)

$-\frac{R_f}{R_1} = -1$

$R1 = Rf = 100\ K\Omega$

Similarly,

$V_{03} = -\frac{R_f}{R_3} * V_3$

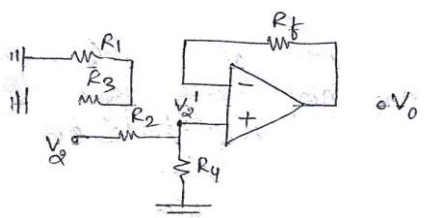
or, $\frac{V_{03}}{V_3} = -\frac{R_f}{R_3} = -3$ using equation (1)

$\therefore R_3 = \frac{R_f}{3} = \frac{100}{3} = 33.33K\Omega$

Again considering only V_2 and applying superposition theorem for nom-inverting terminals,

$V_{02} = \left(1 + \frac{R_f}{R_1||R_3}\right) * V_2'$ .....(2)

where,



$R_1||R_3$= 100 || 100/3

$= \frac{100*\frac{100}{3}}{100+100/3} = \frac{10000}{3} * \frac{3}{400} = 25\ K\Omega$

$V_2' = \left(\frac{R_4}{R_4+R_2}\right) * V_2$ So equation (2) becomes,

$V_{o2} = \left(1 + \frac{R_f}{R_1||R_3}\right) * \left(\frac{R_4}{R_4+R_2}\right) * V_2$

$\frac{V_{o2}}{V_2} = A = 2 = \left(1 + \frac{100}{25}\right)\left(\frac{100}{100+R2}\right)$ using equation (1)

or, $2 = (1+4)\left(\frac{100}{100+R_2}\right)$

or, $\frac{100}{100+R_2} = 0.4 = \frac{2}{5}$

or, $0.4R_2$ +40 = 100

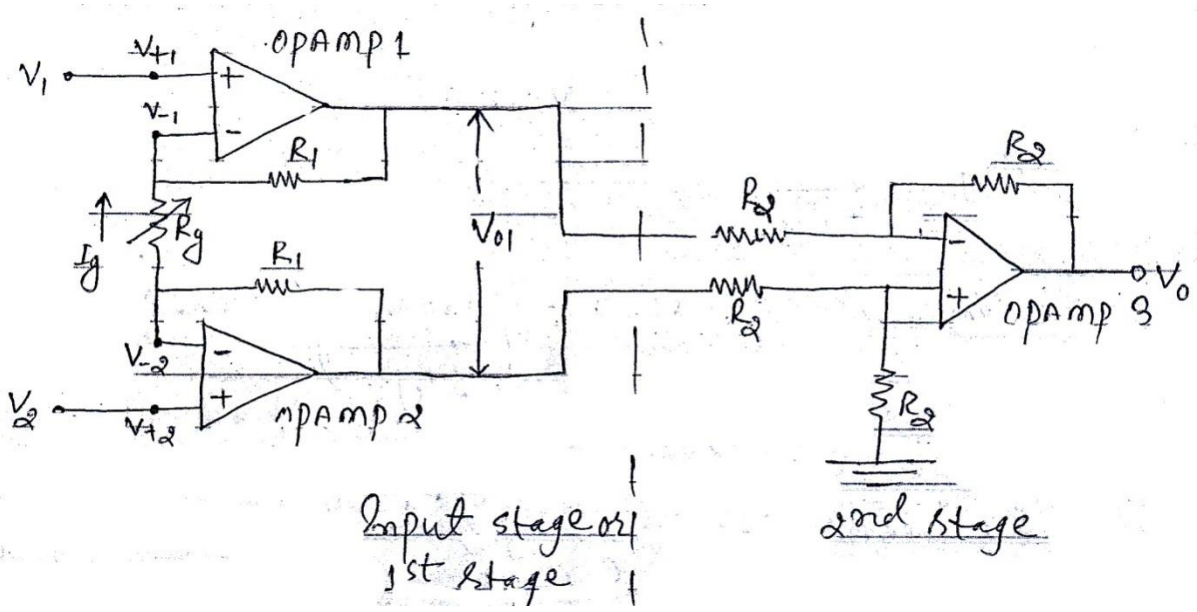
$\therefore R_2 = 150\ K\Omega$

Instrumentation Amplifier (IA)

An instrumentation amplifier is a dedicated differential amplifier optimized for high input impedance and high common mode rejection ratio (CMRR) . It is typically used in applications in which a small differential voltage and a large common-mode voltage are the inputs.

There are several characteristics of an IA that sets it apart from operational amplifier

i. An OPAMP has very large (Ideally infinite) amount of voltage gain. IA has finite gain. OPAMP can provide integration, differentiation functions but IA cannot provide these functions.
ii. IA has a high impedance differential input where as OPAMP has high input impedance
iii. IA has high common mode voltage gain and high CMRR. OPAMP also has high gain and CMRR but IA is superior over OPAMP.
iv. IA is a closed loop device with carefully set again. OPAMP itself is an open loop device with very large gain. This allows IA to be optimized for its role as signal conditioner of low level signals in large amounts of noise.



IA consists of two stages. The first stage offers very high input impedance to both input signals (V_1 and V_2) and allows to set the gain with a single resistor. The second stage is a differential amplifier with the output, negative feedback and ground connections.

The above figure shows that the input stage consists of two carefully matched OPAMPs. Each input V_1 and V_2 is applied to the non-inverting input terminal of its OPAMP. The outputs of OPAMPs are connected together through a string of resistors. The two resistors R_1, are internal to integrated circuit while R_g is the gain setting resistor which may be internal or externally connected.

Now, $V_{+2}= V_2$

As we know

$V_d = V_{+2} - V_{-2}=0$ (For ideal OPAMP, $V_O = 0$ i.e. $V_d =0$)

$V_{-2}=V_{+2}=V_2$

Similarly

$V_{+1}=V_1$ and

$V_{+1}-V_{-1} = 0$

$V_{-1}=V_{+1}=V_1$

$I_g = \frac{V_2-V_1}{R_g}$……(1)

$V_{01} = I_g(R_g + 2R_1) = (\frac{V_2-V_1}{R_g})(R_g + 2R_1)$ using equation (1)

$= (V_2-V_1)\left(1 + \frac{2R_1}{R_g}\right)$

As the second stage is unity gain differential amplifier, the output from second stage is given by

$$V_0 = V_{01} = (V_2 - V_1)\left(1 + \frac{2R_1}{R_g}\right)$$

$$\therefore V_0 = \left(1 + \frac{2R_1}{R_g}\right) * (V_2 - V_1)$$

The differential voltage gain is

$$\frac{V_0}{V_2 - V_1} = \left(1 + \frac{2R_1}{R_g}\right)$$

Thus, by varying the value of R_g, the gain can be varied.

Signal Conversion

General Consideration of A/D and D/A Conversion

A/D and D/A converters relate analog quantities to digital quantities and vice versa through an appropriate code called the binary code in which a number is represented by

$N=d_{n-1}\times 2^{n-1}+d_{n-2}\times 2^{n-2}+\ldots\ldots..+d_2\times 2^2+d_1\times 2^1+d_0\times 2^0$ ……..(1)

where, the coefficient $d_{n-1,}d_{n-2}$……..$d_{2,}d_1,d_0$ assume the values of either 0 or 1

In a four bit system converter, it permits a number from 0-15. Hence, the maximum count for a bit converter is 2^4-1. Therefore, for n-nit system , maximum count =2^n-1.

Resolution = $\frac{Weight\ of\ LSB}{maximum\ count} = \frac{2^0}{2^n-1} = \frac{1}{2^n-1} \simeq \frac{1}{2^n}$

If E_R be the full range of the converter (referenced voltage) then the weight (range) of

MSB = $\frac{1}{2} * range\ of\ converter$

= $\frac{E_R}{2}$ and

The weight (range) of the LSB = $\frac{1}{2^n} * Range\ of\ converter = \frac{E_R}{2^n}$

For a four bit converter having E_R as reference or full range voltage, the analog output for different digital inputs are given as follows:

Digital inputs	Analog Inputs
1000	$E_R/2$
0100	$E_R/2^2$
0010	$E_R/2^3$
0001	$ER/2^4$

If all bits are high i.e. input is 1111, then the analog output can be obtained by superposition theorem i.e

$$E_0 = \frac{E_R}{2} + \frac{E_R}{2^2} + \frac{E_R}{2^3} + \frac{E_R}{2^4}$$

$$= E_R(1 \times 2^{-1} + 1 \times 2^{-2} + 1 \times 2^{-3} + 1 \times 2^{-4})$$

$$= E_R(d_3 2^{-1} + d_2 2^{-2} + d_1 2^{-3} + d_0 2^{-4})$$

$$= \frac{E_R}{2^4}(d_3 2^3 + d_2 2^2 + d_1 2^1 + d_0 2^0)$$

Hence, for n-bit system, output voltage (analog) is given by

$$E_o = \frac{E_R}{2^n}[d_{n-1} 2^{n-1} + d_{n*2} 2^{n-2} + \cdots + d_0 2^0]$$

Example:

Find out the analog output for a digital input of 1010 if the reference voltage is 8 volt.

Solution,

We know

$$E_o = \frac{E_R}{2^4}[D_3 2^3 + d_2 2^2 + d_1 2^1 + d_0 2^0]$$

$$= \frac{8}{16}[1 * 2^3 + 0 * 2^0 + 1 * 2^1 + 0 * 2^0]$$

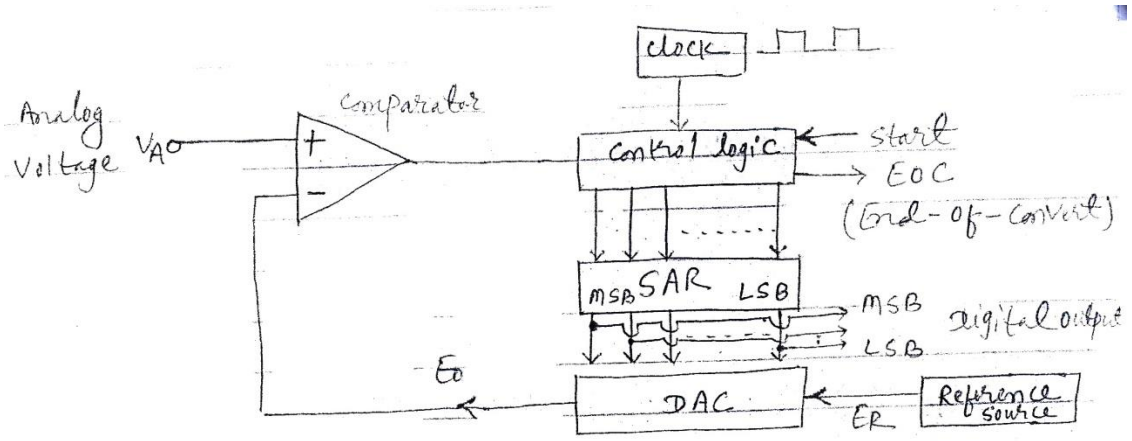
$$= \frac{1}{12}(8 + 2) = \frac{10}{2} = 5\ Volts$$

Analog to Digital Converters (ADC)

Why analog signal is converted to digital form?

1. Most of the real world physical quantities such as voltage, current, temperature, time etc are available in analog form. But it is difficult to process, store or transmit them without introducing considerable error. So , for processing, transmission and storage purposes , it is often convenient to express these variables into digital form.
2. Digital form gives better accuracy and reduces noise.

i. Successive Approximation ADC (Potentiometric Type)



Successive approximation ADC consists of comparator, control logic SAR (Successive Approximation Resistor), DAC and Reference source.

V_A represents the analog input voltage,. When START button is pressed, SAR sets the MSB high i.e. with all other bits to zero so that the trial code becomes 1000 (for 4-bit). DAC converts the trial code into analog equivalent output of DAC given as

$$E_o = \frac{E_R}{2^n}[d_{n-1}2^{n-1} + d_{n*2}2^{n-2} + \cdots + D_0 2^0] \quad for\ n-bits$$

E_o is compared with V_A by comparator.

If $V_A > E_O$, then SAR lefts MSB at 1 and makes the next lower significant bit 1 and further compares.

If $V_A < E_O$, then SAR resets MSB at 0 and makes the next lower significant bit 1. This procedure is continued for all subsequent bits one at a time until all bit positions have been tested.

When $V_A = E_O$, the comparator changes the state and this can be taken as the End-of-conversion (EoC)

For example, for 4-bits signal

1st approximation,

Input to DAC = 1000

Output from DAC = $E_O = \frac{E_R}{2^n}[D_3 2^3 + d_2 2^2 + d_1 2^1 + d_0 2^0]$

$= \frac{E_R}{2^4}[1 * 2^3 + 0 * 2^0 + 1 * 2^1 + 0 * 2^0]$

$= \frac{8}{16}E_R$

Now, $V_A > E_O$, then the bit D_3 remains at 1 and the next bit i.e. d_2 is set to 1.

2nd Approximation

Input to DAC = 1100

Output from DAC = $E_O = \frac{E_R}{2^4}[1 \times 2^3 + 1 \times 2^2] = \frac{12}{16}E_R$

Now, $V_A < E_O$, the the bit d_2 is reset to 0 and the next bit i.e. is set to 1.

3rd approximation

Input to DAC = 1010

Output from DAC = $E_O = \frac{E_R}{16}(1 \times 2^3 + 1 \times 2^1) = \frac{10}{16}E_R$

Now $V_A > E_O$ then the bit d_1 remains at 1 and the next bit d_O is set to 1.

4th approximation

Input to DAC = 1011

Output from DAC= $E_O = \frac{E_R}{16}(1 * 2^3 + 1 * 2^1 + 1 * 2^0) = \frac{11}{16}E_R$

Now, $V_A < E_O$, then the bit d_O is reset to 0 and digital equivalent of the analog input voltage will be $d_3 d_2 d_1 d_0 = 1010$

Example:

Find the successive approximation A/D output for a 4 bit converter to a 3.217 volt input if the reference voltage is 5 Volt.

Solution

i. Set $d_3 = 1$

$$\therefore output = E_O = \frac{E_R}{2^n}[D_3 2^3 + d_2 2^2 + d_1 2^1 + d_0 2^0]$$

$$E_O = \frac{5}{2^4}(1 * 2^3) = 2.5\ V$$

Now, 3.218>2.5 and $\therefore set\ d_3 = 1$

ii. Set $d_2 = 1$

$$\therefore output\ (E_O) = \frac{5}{16}(1 * 2^3 + 1 * 2^2) = \frac{5}{16} * 12 = 3.75V$$

Now, 3.217<3.75 and set $d_2=0$

iii. Set $d_1=1$

$$\therefore output\ (E_O) = \frac{5}{16}(1 \times 2^3 + 1 \times 2^1) = \frac{5}{16} * 10 = 3.125V$$

Now, 3.217>3.125 and set $d_1=1$

iv. Set $d_O=1$

$$\therefore output\ (E_O) = \frac{5}{16}(1 * 2^3 + 1 * 2^1 + 1 * 2^0) = \frac{5}{16} * 11 = 3.4375V$$

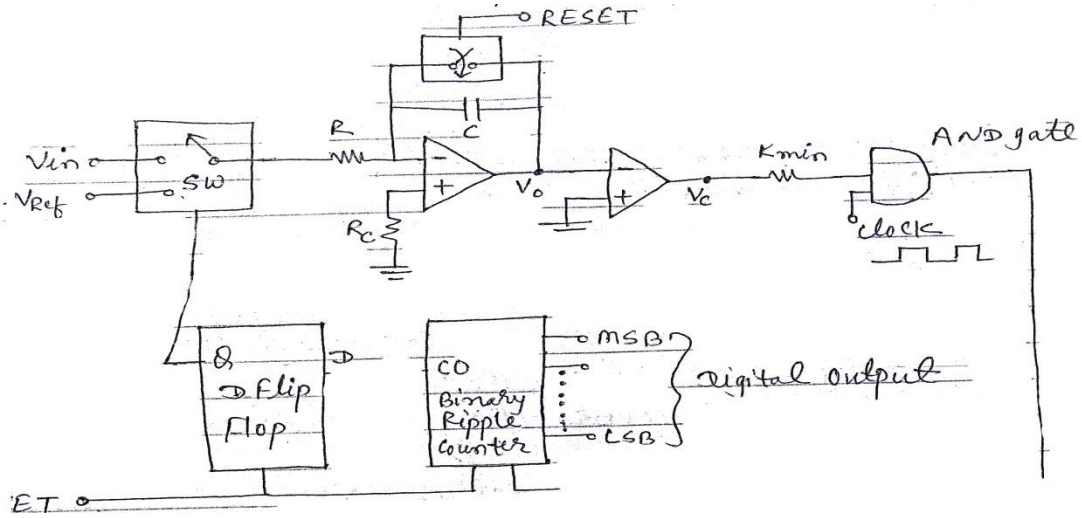
Now, 3.217<3.4375 and set $d_O = 0$

Thus, the output of A/D converter is 1010

Successive Approximation Type ADC are widely applied because of their combination of high resolution and speed. They can perform conversions within 1 to 50 micro seconds rather

than milliseconds required by stair case Ramp, Dual slope and Voltage to frequency converter types. However, they are more expensive than these slower types.

ii. Dual Ramp (Dual Slope) ADC



The circuit diagram shows, the integrating type Dual Ramp(Dual Slope) ADC. It performs conversion in an indirect manner first changing analog input to a linear function of time or frequency and then to a digital code. Dual slope ADC is the most widely used integrating type ADC. Binary counter is RESET and results 0000 digital output (4 bits) switch (SW) moves to 0 position and Vin is fed to an integrator which produces a Ramp output wave from ($V_O = -\frac{V_{in}}{T} * t$) . The capacitor charges. The ramp signal starts at zero and increases for fixed interval of time T_1, equal to the maximum count of the counter multiplied by the clock frequency. The slope of the ramp signal is proportional to V_{in}. It results VC (Comparator output) high. AND gate enables and the counting starts (0000……1111) where 2^n-1 pulses are applied. For pulse 2^n i.e. at the end of the ineterval T_1, counter resets. Carry Bit (C_O) of the ripple counter causes the switch to move to $-V_{Ref}$ position. In this position, a constant current $-V_{Ref/R}$ begins to discharge the capacitor. The count continues until capacitor C being discharged completely i.e. $V_O<0$. As V_O becomes positive , V_C becomes low which disables AND gate and counting stops. The resultant count is proportional to the input voltage V_{in}.

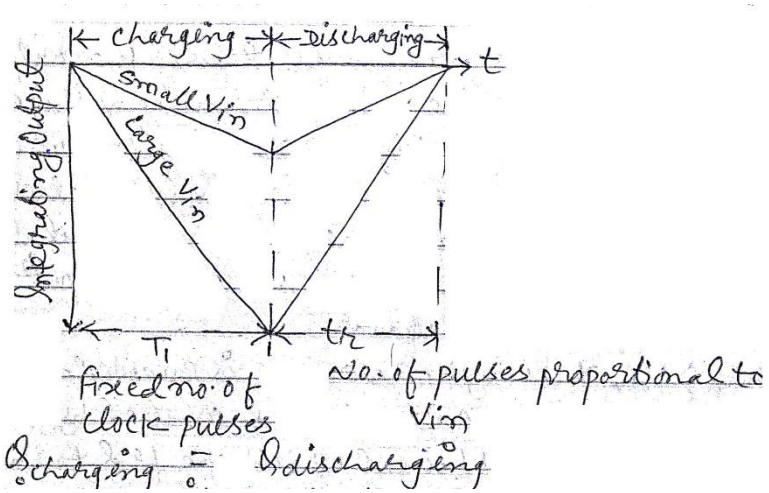
Advantages:

The main advantages are :

- Good accuracy of conversion
- Low cost

Disadvantage:

-slow speed of operation

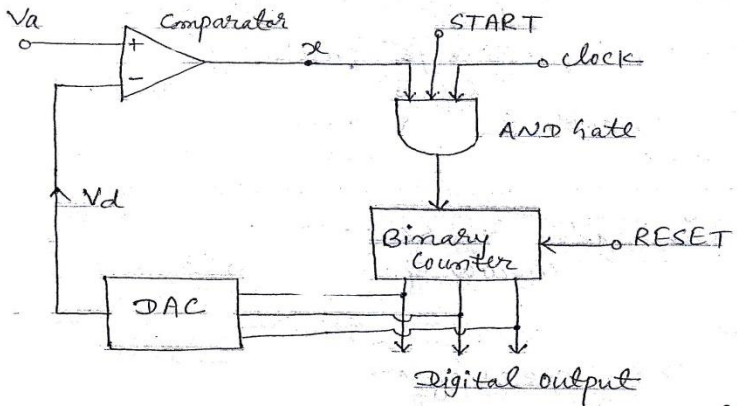


Now, $Q_{charging} = Q_{discharging}$

Q= CV $\frac{iT_1}{C} = \frac{it_r}{C}$ $or, \frac{V_{in}}{R}T_1 = \frac{V_{Ref}}{R}t_r$

Or, $V_{in} = V_{Ref}\left(\frac{t_r}{T_1}\right) \therefore V_{in} \propto t_r$ i.e. The count recorded is proportional to the input voltage.

iii. Stair case Tamp Type (Counting Type) ADC



Binary counter is reset to zero count by the reset pulse. The digital output is zero equivalent. So, the output of DAC is zero i.e. V_d=0. Since V_a(input analog voltage) >V_d, output of the comparator is high i.e. x is high (1). When START button is pressed, AND gate is enabled and the clock pulse is counted by the Binary counter. There is Digital output. But the counting does not stop here. The equivalent DAC output (V_d) is compared with V_a by the comparator.

If V_a>v_d , x is high, AND gate is enabled. The clock pulses are passed through the AND gate and counted by the Binary counter. Digital output is obtained which are fed to the computer or any other signal processing.

If V_a<V_d , x is low i.e. 0 and AND gate is disabled. This stops the counting. At the time V_d≥V_a, the digital output of the counter represents the analog input voltage.

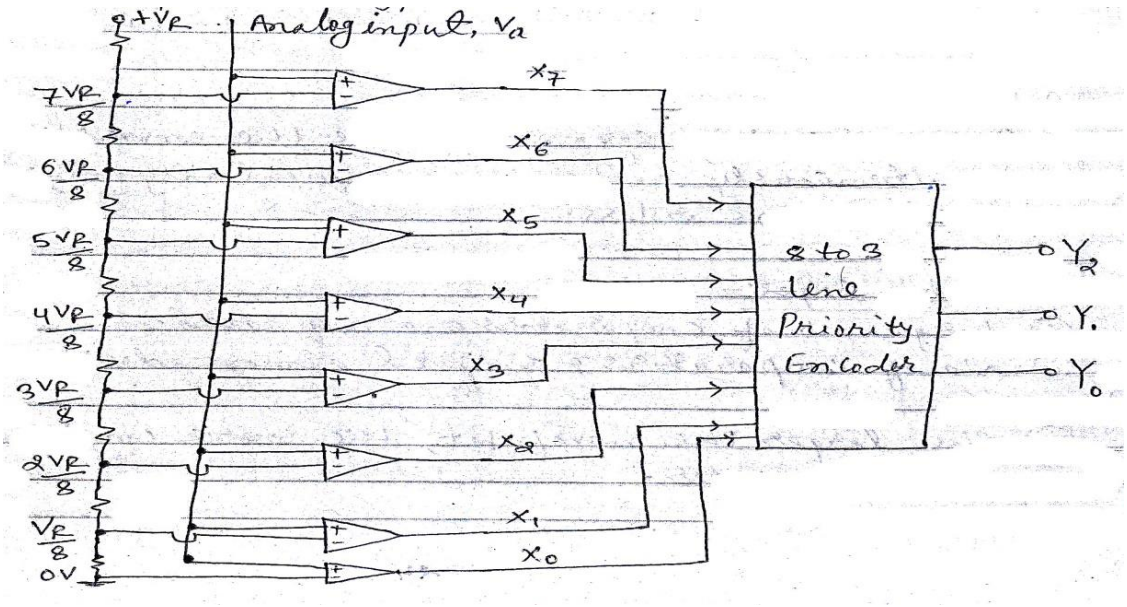
For a new value of analog input V_a , a second RESET pulse is applied to clear the counter. Upon the end of the RESET and with START button ON, the counting begins again.

Serious Drawbacks:

a. The counter frequency must be low enough to give sufficient time for the DAC to settle and for the comparator to respond.

b. When $V_a > V_d$, x is high and AND gate is enabled and counter counts and digital output is one bit more than the exact value. To remove this problem,, we can use UP/DOWN counter. In this process, when DAC output is more than V_a , the counter reverses the direction and count down by one count and it decreases the count by 1 LSB.

iv. Flash or parallel Type ADC



The circuit diagram of the 3 bit parallel type (Flash Type) ADC is shown above. In this technique, the input voltage is fed simultaneously to one input of each comparator. The other input of the comparator is a reference voltage. The circuit consists of a resistive divider network, 8 OPAMP comparators and 8 to 3 line encoder. Its truth table is given below;

Advantages:

It has very high speed because the conversion takes place simultaneously rather than sequentially .Typical conversion time is 100 ns or less.

Disadvantages:

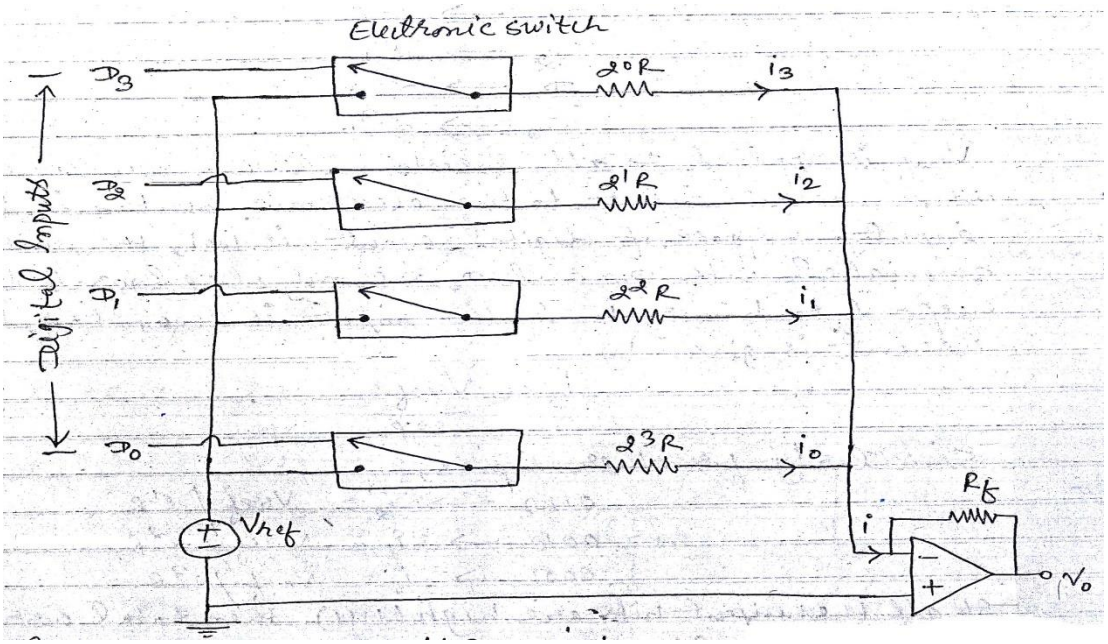
i. Large no. of comparators are required.
ii. No. of comparators required almost doubles for each added bit
iii. The larger the no. of bit, the more complex is the priority encoder.

Input voltage (V_a)	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	Y_2	Y_1	Y_0
0 – $V_R/8$	0	0	0	0	0	0	0	1	0	0	0
$V_R/8$ - 2 $V_R/8$	0	0	0	0	0	0	1	1	0	0	1
2 $V_R/8$- 3 $V_R/8$	0	0	0	0	0	1	1	1	0	1	0
3 $V_R/8$ - 4 $V_R/8$	0	0	0	0	1	1	1	1	0	1	1
4 V_R/ 8- 5 $V_R/8$	0	0	0	1	1	1	1	1	1	0	0
5 $V_R/8$-6 $V_R/8$	0	0	1	1	1	1	1	1	1	0	0
6 $V_R/8$-7 $V_R/8$	0	1	1	1	1	1	1	1	1	1	0
7 $V_R/8$ -8 $V_R/8$	1	1	1	1	1	1	1	1	1	1	1

Digital to Analog Conversion (DAC)

Typical applications of DAC include microcomputer interfacing, CRT graphics generation, programmable power supplies, digitally controlled gain circuits, digital filters etc.

i. Weighted Resistor Network (WRN) DAC



In the WRN DAC, the resistance are weighted reverse eight binary system i.e the resistance associated with the MSB has the least value and as we move from MSB to LSB, the resistance value increases by a factor of 2 as shown.
Let resistance associated with MSB for n-bit is R i.e

$$D_{n-1} \rightarrow 2^0 R$$
$$D_{n-2} \rightarrow 2^1 R$$
$$D_{(n-3)} \rightarrow 2^2 R$$
.
.
.
$$D_0 \rightarrow 2^{n-1} R$$

Hence, for 4 bit system we have

$$D_3 \rightarrow 2^0 R$$
$$D_2 \rightarrow 2^1 R$$
$$D_1 \rightarrow 2^2 R$$
$$D_0 \rightarrow 2^3 R$$

V_{ref} is applied to all resistors through electronic switches and another input to the electronic switch is the digital input. Suppose if digital input is 1001, the switches associated with D_3 and D_O are only closed i.e. these switches respond to binary 1. If the input is 1000, then the current is given by

$$i_3 = V_{ref}/2^0 R$$

Similarly for other inputs,

$0100 \rightarrow i_2 = \frac{V_{ref}}{2\ \ R}$

$0010 \rightarrow i_1 = V_{ref}/2^2 R$

$001 \rightarrow i_0 = \frac{V_{ref}}{2^3 R}$

If all the input bits are high (1111) , then total current i can be obtained by superposition theorem.

$$i = i_3 + i_2 + i_1 + i_0$$

$$= \frac{V_{ref}}{R}(1 + 1 * 2^{-1} + 1 * 2^{-2} + 1 * 2^{-3})$$

$$= \frac{V_{ref}}{2^3 R}(1 * 2^3 + 1 * 2^2 + 1 * 2^1 + 1 * 2^0)$$

$$= \frac{V_{ref}}{2^3 R}(D_3 2^3 + D_2 2^2 + D_1 2^1 + D_0 2^0)$$

Advantages:

- easy principle/construction
- fast conversion

$$\therefore V_O = -iR_f = -\frac{V_{ref}}{2^3 R} * R_f(D_3 2^3 + D_2 2^2 + D_1 2^1 + D_0 2^0)$$

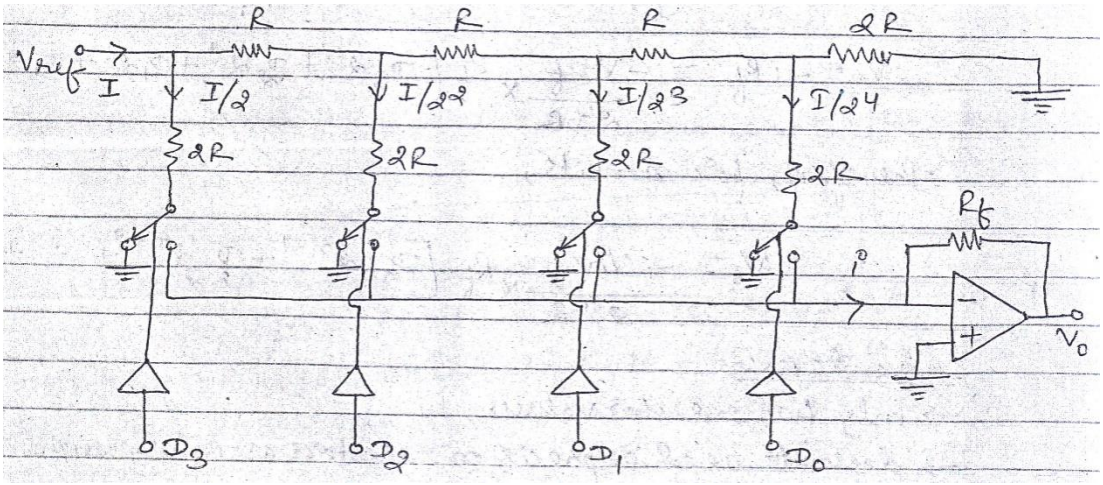
Hence, for n-bits system

$$V_O = -\frac{V_{ref}}{2^{n-1} R} * R_f(D_{n-1} 2^{n-1} + \cdots \ldots \ldots \ldots + D_0 2^0)$$

Disadvantages:

1. As the number of n-bit goes on increasing, the resistance values as well as the complexity of the circuit increases. So, cost will be high.
2. As the number of bit increases, the tolerance of the resistance associated with LSB may exceed the value of resistance in MSB.
3. As the number of bit increases, the variation in the value of the resistance will be large and so the power rating. This is not required in the process of IC manufacturing.

ii. R-2R Ladder Network DAC



In a ladder network right of each node, there are two equal resistors and each having the value 2R and placed across. Hence, the current entering to the node is divided as $I/2^n$ where n is the number of nodes starting from MSB to LSB i.e. it generates a current given by I/2, $I/2^2$, $I/2^3$, ……, $i/2^n$. So, the ladder network generates a binary sequence of current. If all bits of digital inputs are high i.e. for a 4-bit converter, digital input is 1111, then the total current I is obtained by superposition theorem

$$i = \frac{I}{2} + \frac{I}{2^2} + \frac{I}{2^3} + \frac{I}{2^4}$$
$$= I(1 * 2^{-1} + 1 * 2^{-2} + 1 * 2^{-3} + 1 * 2^{-4})$$
$$= \frac{V_{ref}}{R}(D_3 2^{-1} + D_2 2^{-2} + D_1 2^{-3} + D_0 2^{-4})$$
$$= \frac{V_{ref}}{2^4 R}(D_3 2^3 + D_2 2^2 + D_1 2^1 + D_0 2^0)$$

Now, the analog output voltage V_O is given by

$$V_O = -iR_f = -\frac{V_{ref}}{2^4 R} * R_f[D_3 2^3 + D_2 2^2 + D_1 2^1 + D_0 2^0]$$

Therefore, for n-bits

$V_O = -\frac{V_{ref}}{2^n R} * R_f\ [D_{n-1} 2^{n-1} + D_{n-2} 2^{n-2} + \cdots + D_0 2^0]$

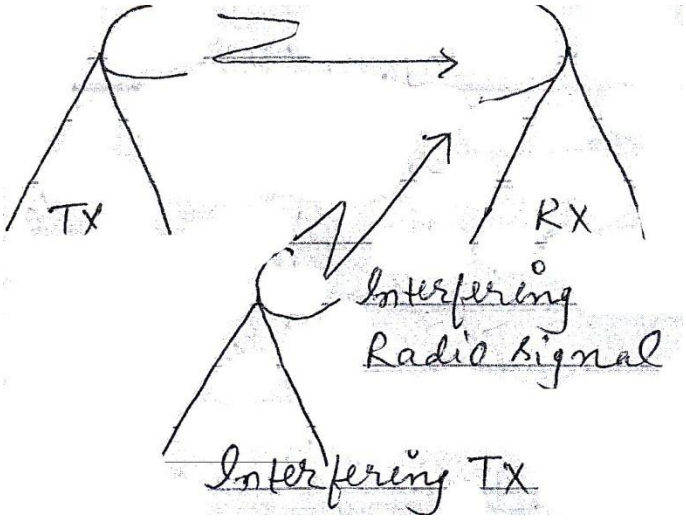
Advantages:

- Only two resistor values
- Does not need as precision resistors as Binary weighted DAC
- Cheap and easy to manufacture.

Disadvantage:

- Slower conversion rate

Interference Signals and their elimination



Interference is contamination by extraneous signals. This may be signals from other transmitter, power cables, machineries, switching, circuits, human sources and many more.

Appropriate filtering can remove interference to the extent that the interfering signals occupy different frequency bands than the desired signal. Interference may be the coherent signals from other systems (and sometimes the circuit itself) that enters into the desired system. Interference is external signals in opposition to noise. For this reason, the best way to minimize its effects is to identify the interference paths to our circuits/systems. Its major limitation is in precision measurements and the detectability (resolution).

The major parts for interference are:

i. Signals coupled in inputs and outputs
ii. Capacitive coupling
iii. Inductive coupling

iv. Magnetic coupling
v. RF coupling

Capacitive coupling

- Conductors in the close proximity interference with each other
- Implements high pass RC filter across the noise source and the signal
- Noise appearing on the signal proportional to the noise source level
- Problem with high frequency and high impedance signals

Inductive coupling

- Magnetic flux generated due to noise circuit will induce current in neighboring circuits
- Roughly proportional to the areas of the two circuits
- Noise generated is an added voltage in parallel, therefore independent of signal level.
- Can be differentiated from capacitance by changing the load impedance (if noise level stays the same, then we have inductive coupling)

Minimizing of interference Effects

- Avoid direct capacitive coupling between signals tracks using ground planes and guard rings.
- Avoid magnetic coupling avoiding loops(use of twisted pair)
- Protecting power supply inputs with feedthroughs to avoid interference signal paths through supply voltages.
- use shielding to avoid RF coupling when necessary.
- Use separate grounds for digital/analog signals
- Use only one point to ground the circuit.
- Use separate power supply when possible