POWER ELECTRONICS

LAB ASSIGNMENT

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Table of content

Switching Losses “Q1”

R load

First At 50 Hz

Circuit implementation Using LTspice

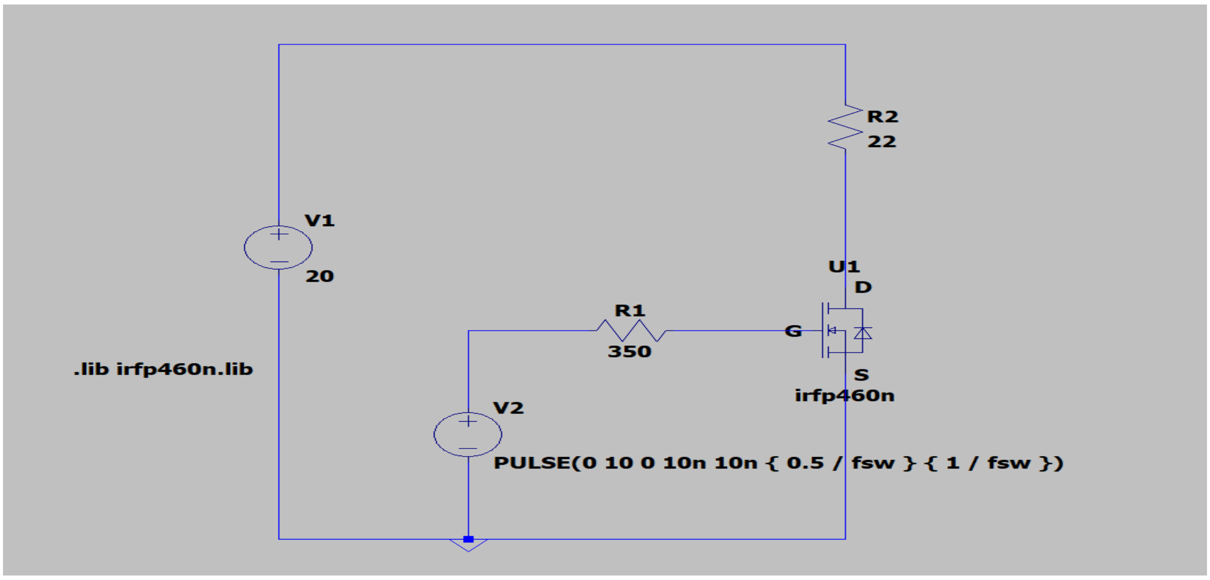


Figure 1 Circuit Implementation at 50Hz

Voltage, current, power waveforms

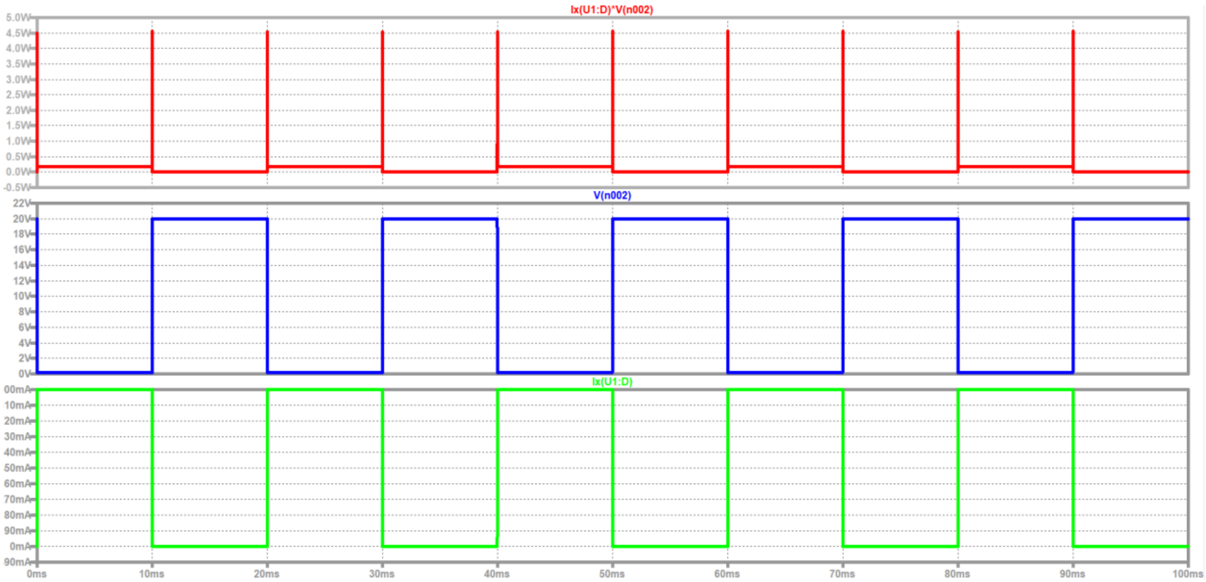


Figure 2 Voltage, Current, Power at 50Hz

Switching losses calculations

- switching on losses

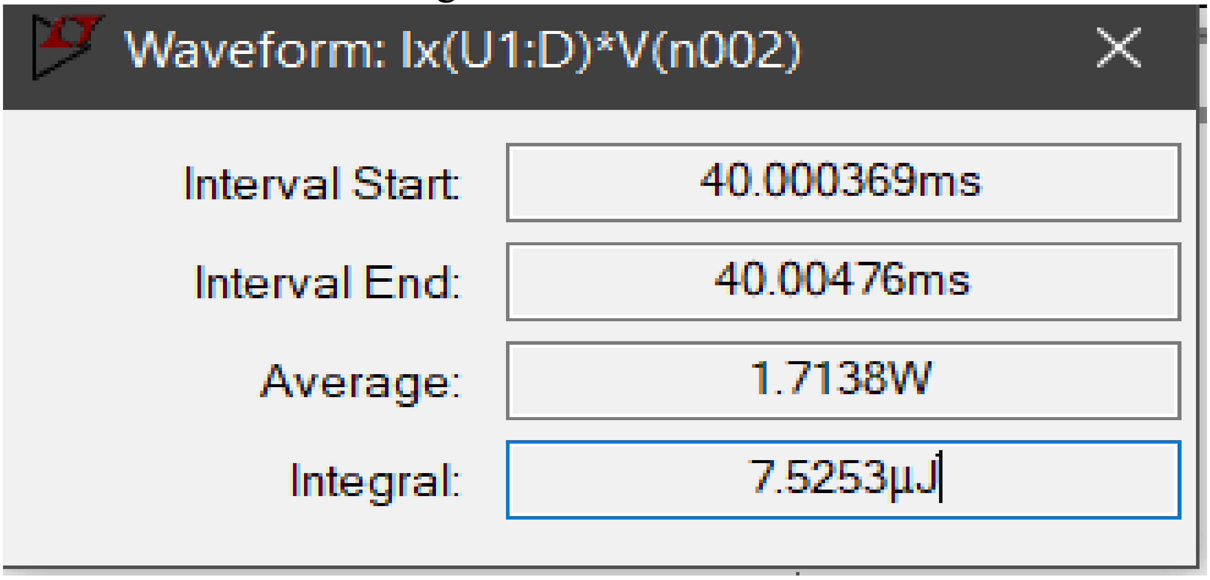


Figure 3 Switching On losses at 50 Hz.

- switching off losses

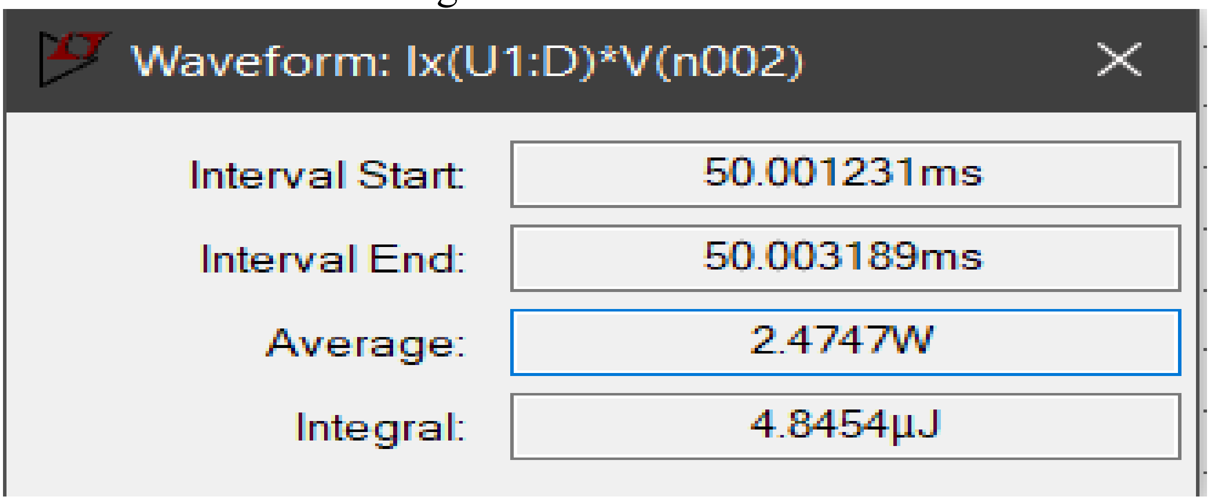


Figure 4 Switching off losses at 50 Hz.

LTspice Calculations

$$\text{Pon} = 7.5253 * * 10^{-6} * 50 = 3.76265 * 10^{-4}\ Watt.$$

$$\text{Poff} = 4.8454 * * 10^{-6} * 50 = 2.4227 * 10^{-4}\ Watt.$$

Actual Reading

Switching On

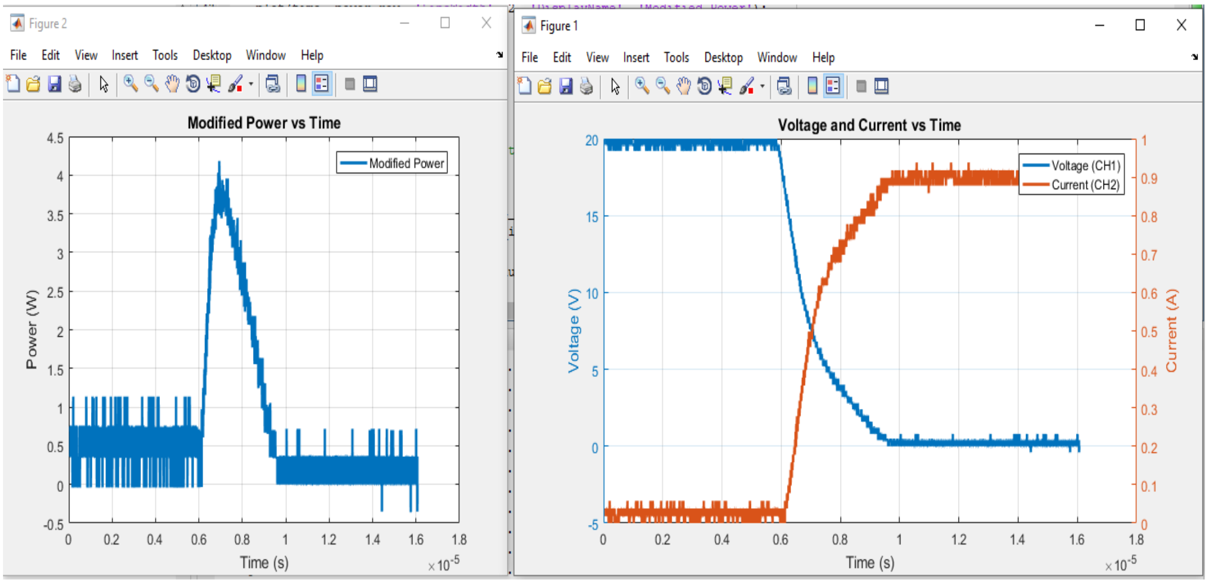


Figure 5 Actual Voltage, Current, Power switching on at 50Hz

Switching On Calculation

P= 8.1373e-6 * Fs

```
Integrated Power between 5.848e-06s and 9.64e-06s: 8.1373e-06 W
```

P = 50*8.1373e-6 = 4.068e-4 w

TON = 3.8e-6 sec

Calculated results

(1/6) ×v×i×fs×ton = (1/6) ×20×0.9×3.8e-6×50 = 5.7e-4

Switching Off

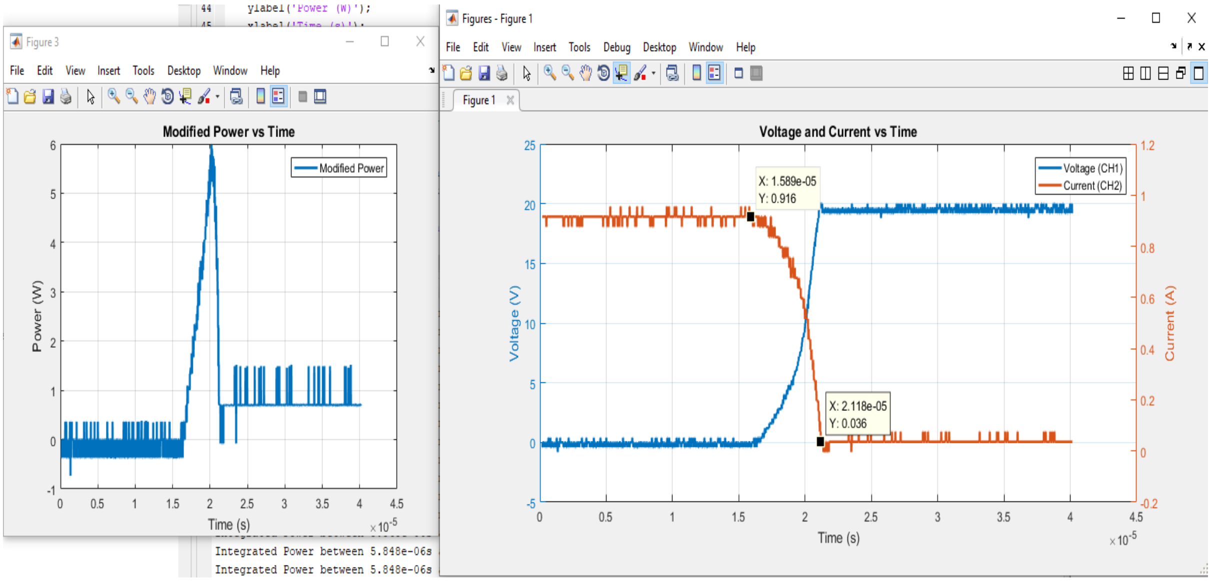


Figure 6 Actual Voltage, Current, Power Switching off at 50 Hz

Switching Off Calculation

P= 1.4445e-5 * Fs

```
Integrated Power between 1.589e-05s and 2.118e-05s: 1.4445e-05 W
```

P = 50 * 1.4445e-5 = 7.222e-4 w

Toff = 5.29e-6 sec

Calculated results

(1/6) ×v×i×fs×toff = (1/6) ×20×0.9×5.29e-6 ×50 = 7.935e-4 w

Second at 1000 Hz

Voltage, Current and power waveforms

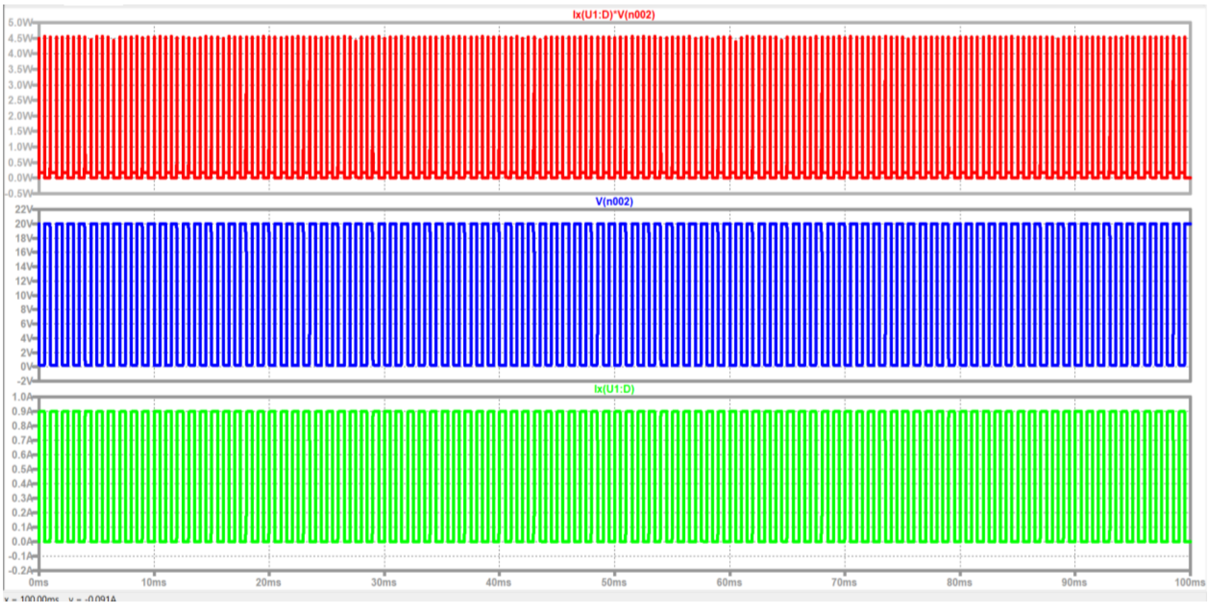


Figure 7 Voltage, Current , Power at 1000 Hz.

Power losses calculations

- Switching on losses

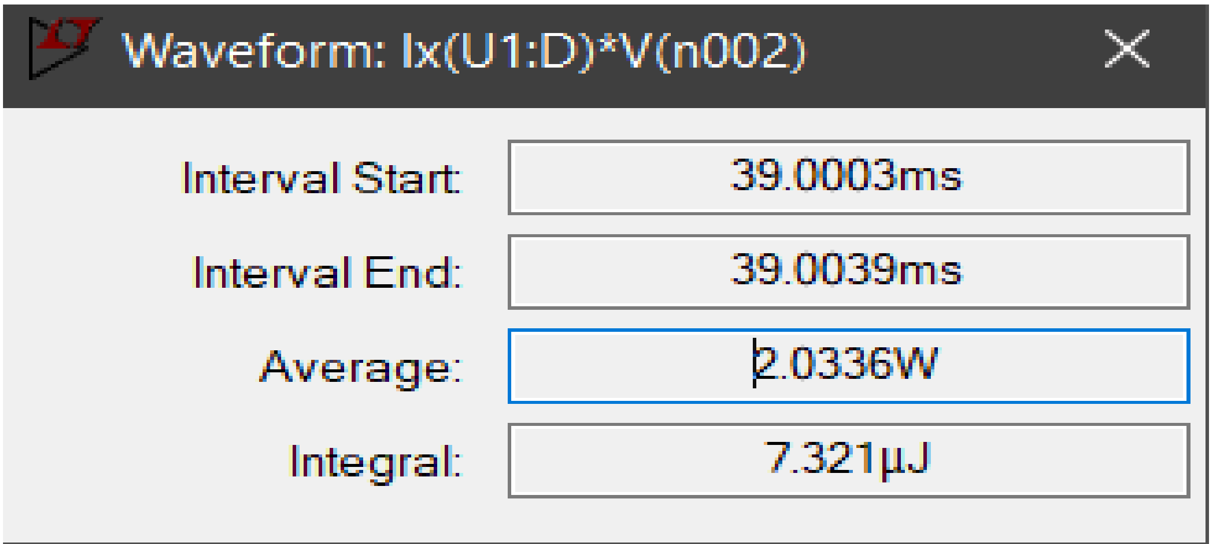


Figure 8 Switching on losses at 1000 Hz.

- Switching off losses

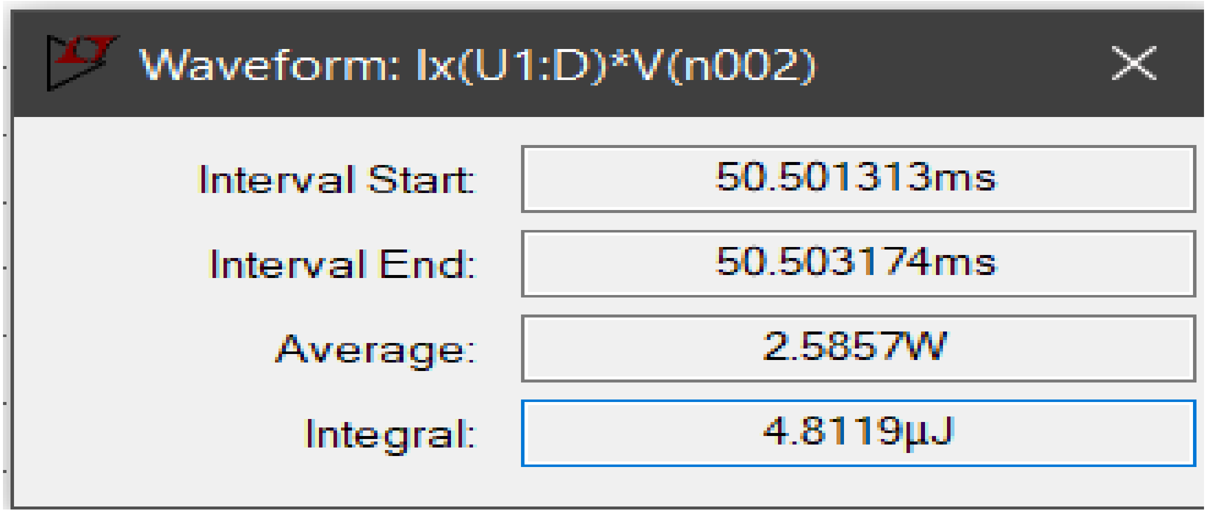


Figure 9 Switching off losses at 1000 Hz.

LTspice calculations

$$Pon = 7.321 * 10^{-6} * 1000 = 0.007321 \text{ Watt.}$$

$$Poff = 4.8119 * 10^{-6} * 1000 = 0.0048119 \text{ Watt.}$$

Actual Reading

Switching On

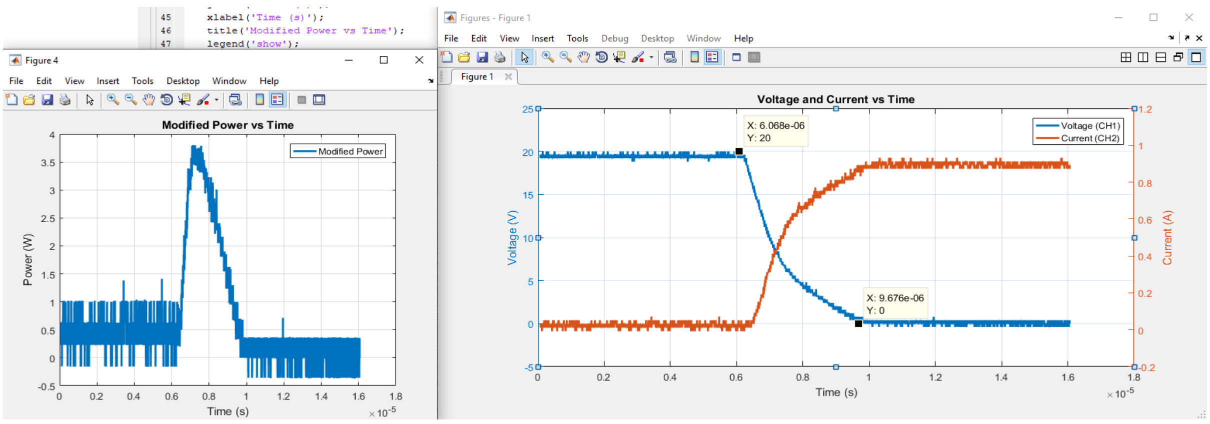


Figure 10 Actual Voltage, Current, Power switching on at 1000Hz.

Switching On Calculation

P= 7.5627e-6 * Fs

```
Integrated Power between 6.068e-06s and 9.676e-06s: 7.5627e-06 W
```

P = 1000 * 7.5627e-6= 7.5627e-3 w

TON = 2.996e-6 sec

Calculated results

(1/6) ×v×i×fs×ton = (1/6)×20×0.9×2.996e-6×1000 = 8.988e-3 w

Switching Off

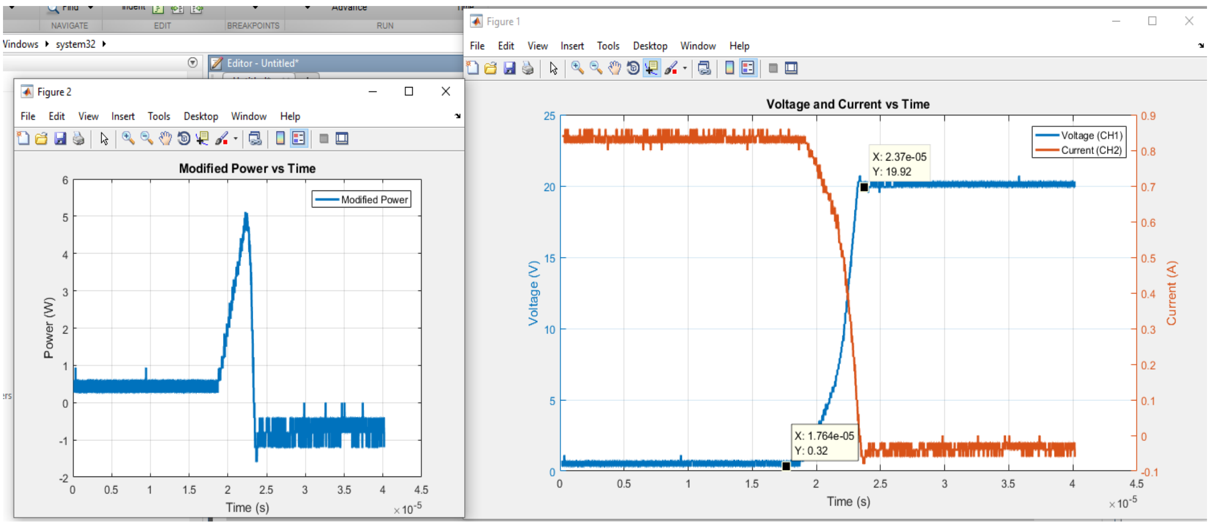


Figure 11 Actual Voltage, Current, Power switching off at 1000Hz.

Switching On Calculation

P= 1.3387e-5 × Fs

```
Integrated Power between 1.784e-05s and 2.37e-05s: 1.3387e-05 W
```

P = 1000 ×1.3387e-5 = 13.387e-3 Watt

Toff = 6.06e-6 sec

Calculated results

(1/6) ×v×i×fs×toff = (1/6) ×20×0.9×6.06e-6×1000 = 18.18e-3 W

At 10K Hz

Volt, Current and power waveforms

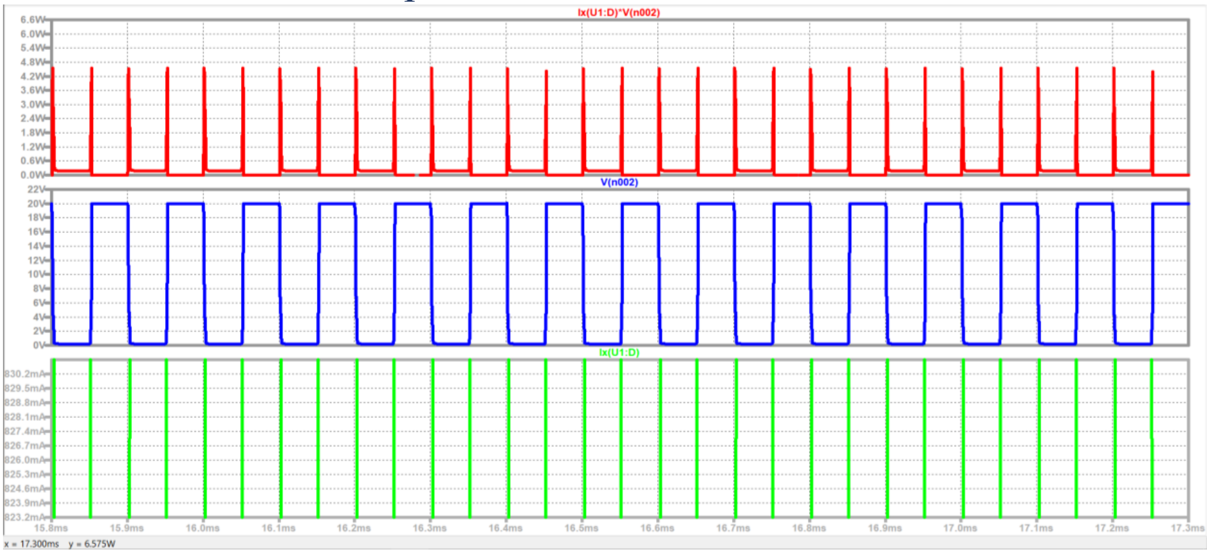


Figure 12 Voltage, Current, Power at 10K Hz

Switching on losses

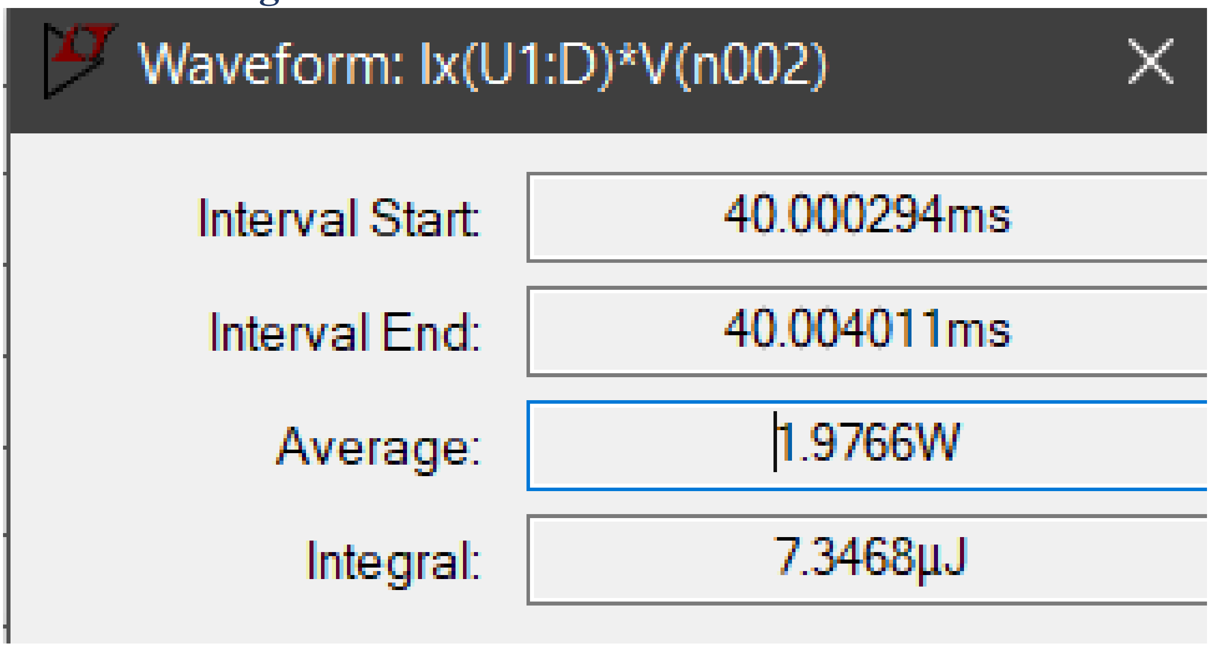


Figure 13 Switching On losses at 10K Hz

Switching on curves

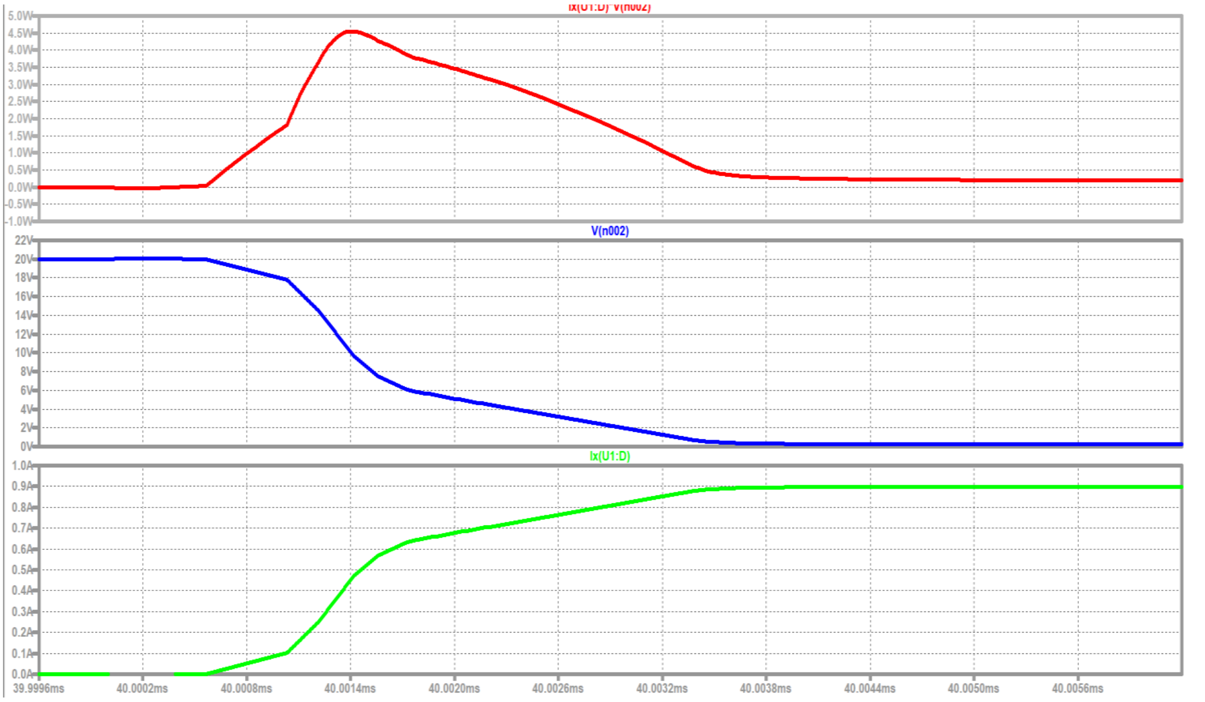


Figure 14 Switching on curve at 10K Hz.

Switching off curves

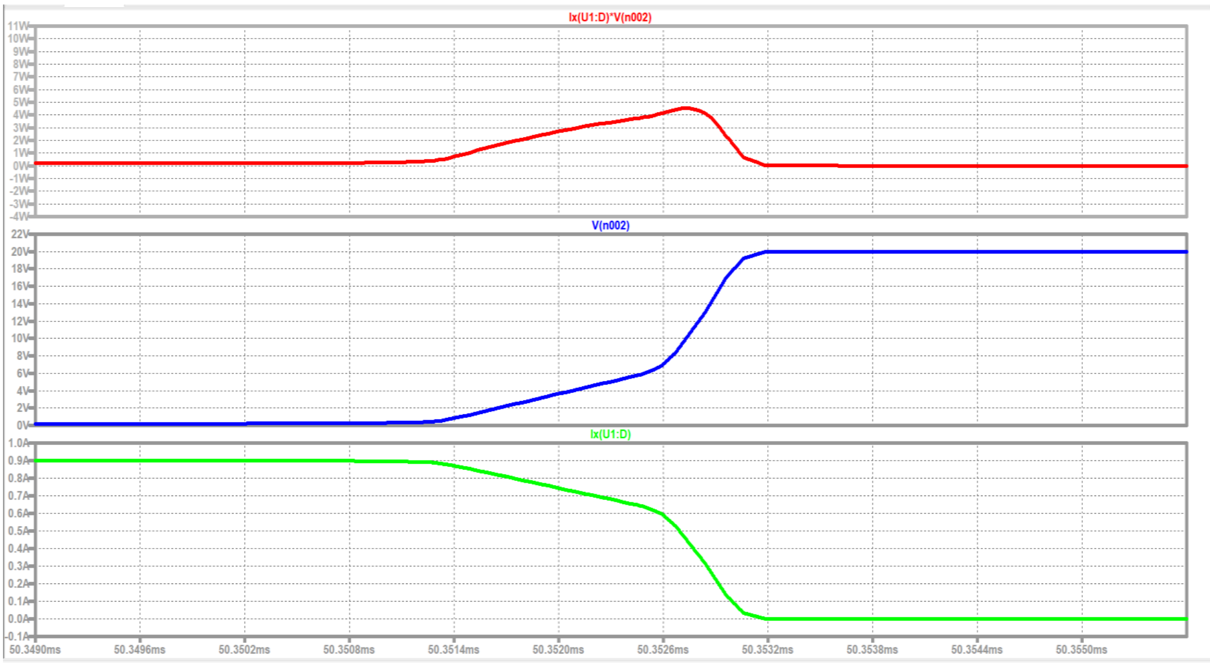


Figure 15 Switching Off losses at 10K Hz.

Actual Reading

Switching On

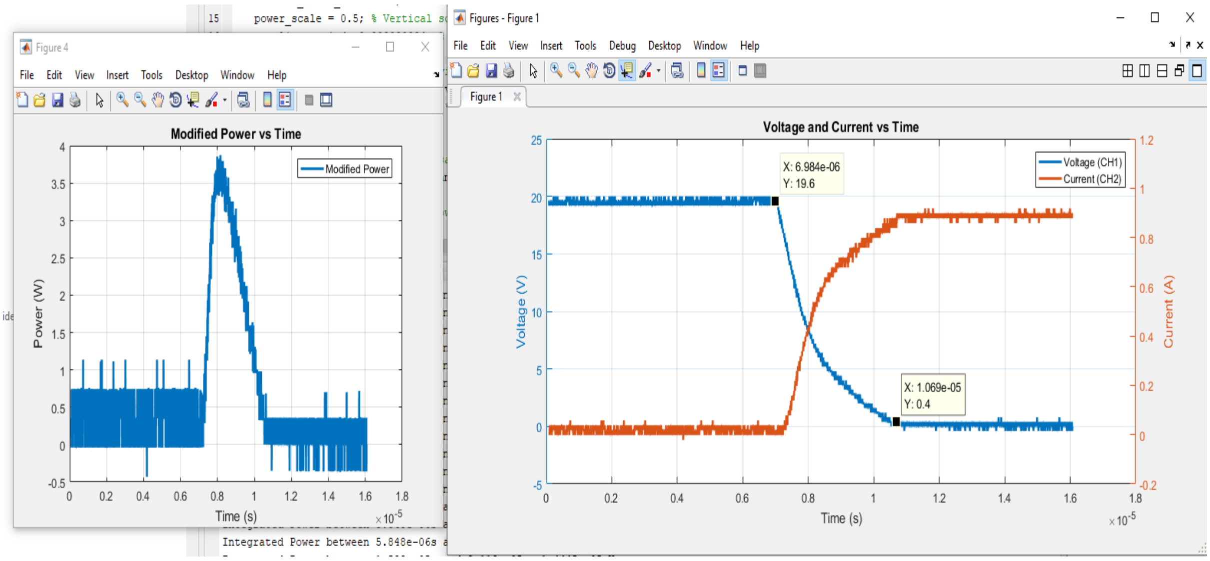


Figure 16 Actual Volta, Current, Powe Switching on at 10K Hz

Switching on Calculation

P= 7.4898e-6 * Fs

```
Integrated Power between 6.984e-06s and 1.069e-05s: 7.4898e-06 W
```

P = 10000*7.4898e-6 = 0.07489 w

TON = 3.706e-4 sec

Calculated results:

(1/6) *v*i*fs*ton = (1/6) *20*0.9*7.4898e-6*10e3 = 11.18e-3

Switching Off

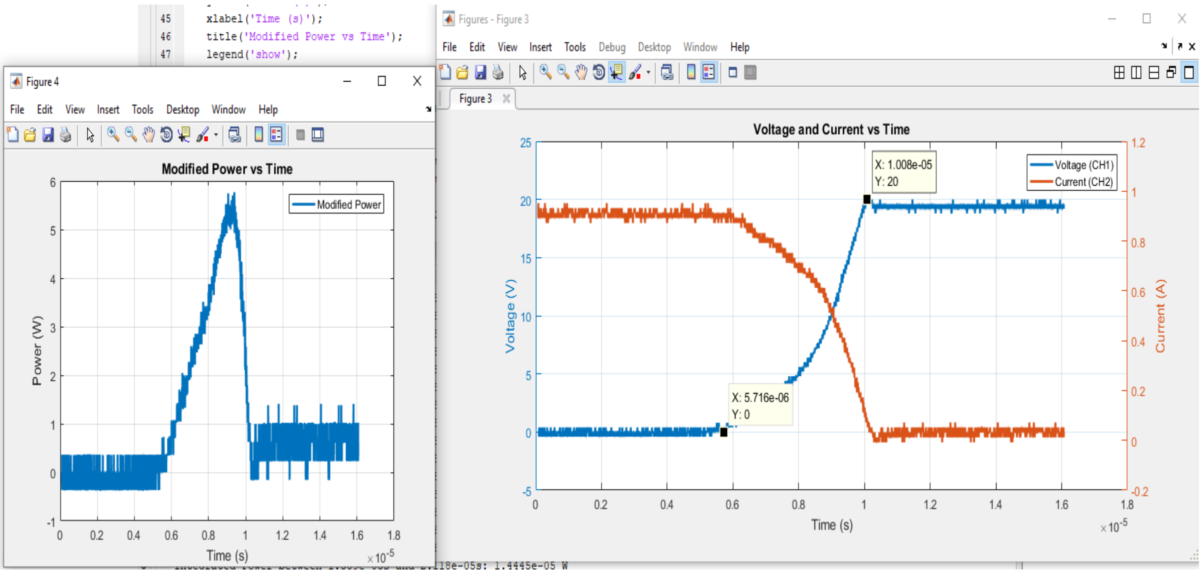


Figure 17 Voltage, Current, Power Switching Off at 10K Hz

Switching Off Calculation

P= 1.3541e-5 * Fs

```
Integrated Power between 5.716e-06s and 1.008e-05s: 1.3541e-05 W
```

P = 10000* 1.3541e-5= 0.13541 w

Toff = 4.364e-6 sec

Calculated results:

(1/6) *v*i*fs*toff = (1/6) *20*0.9*5.29e-6 *10e3= 0.13092 w.

RL- Load

Circuit implementation

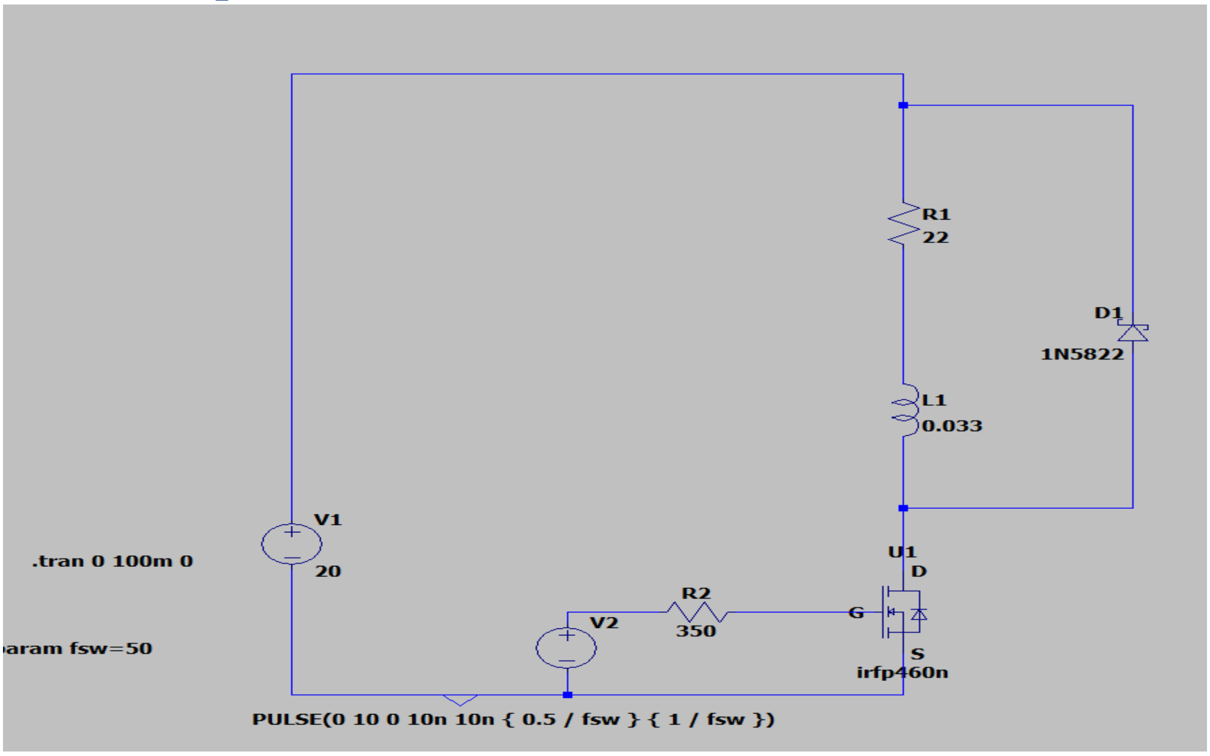


Figure 18 Circuit implementation at R-L load

At 50 Hz

Voltage, current and power waveforms

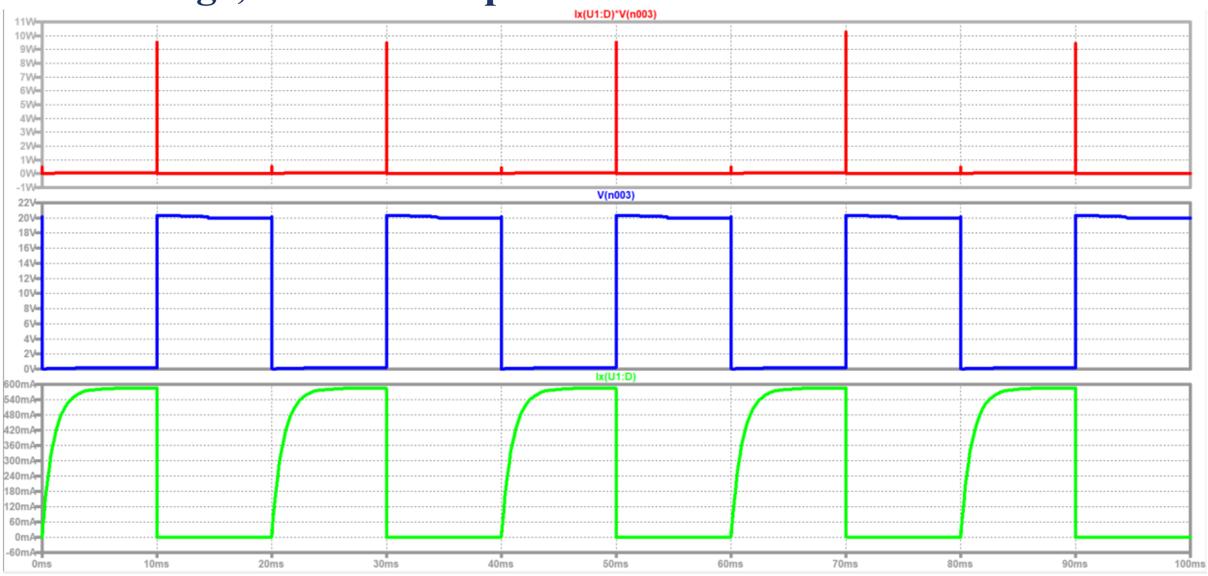


Figure 19 Voltage, Current, Power At 50 Hz RL load

Switching losses

- Switching on power losses

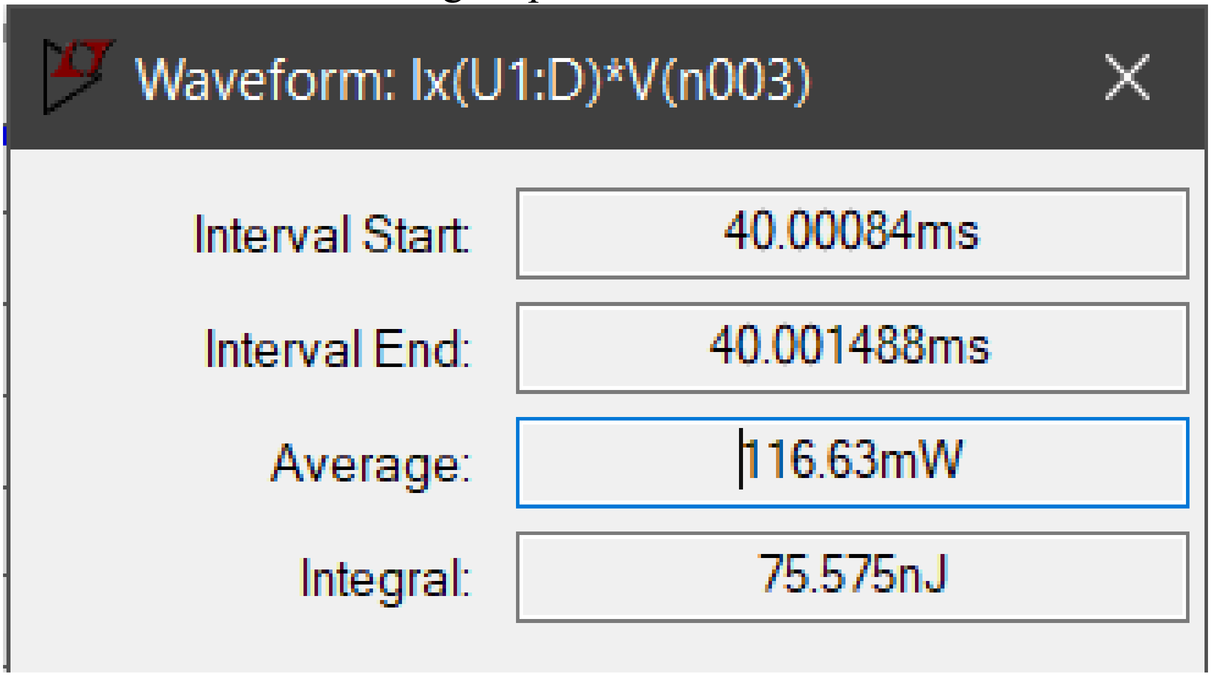


Figure 21 Switching on power losses at 50 Hz R-L loads.

- Switching off power losses

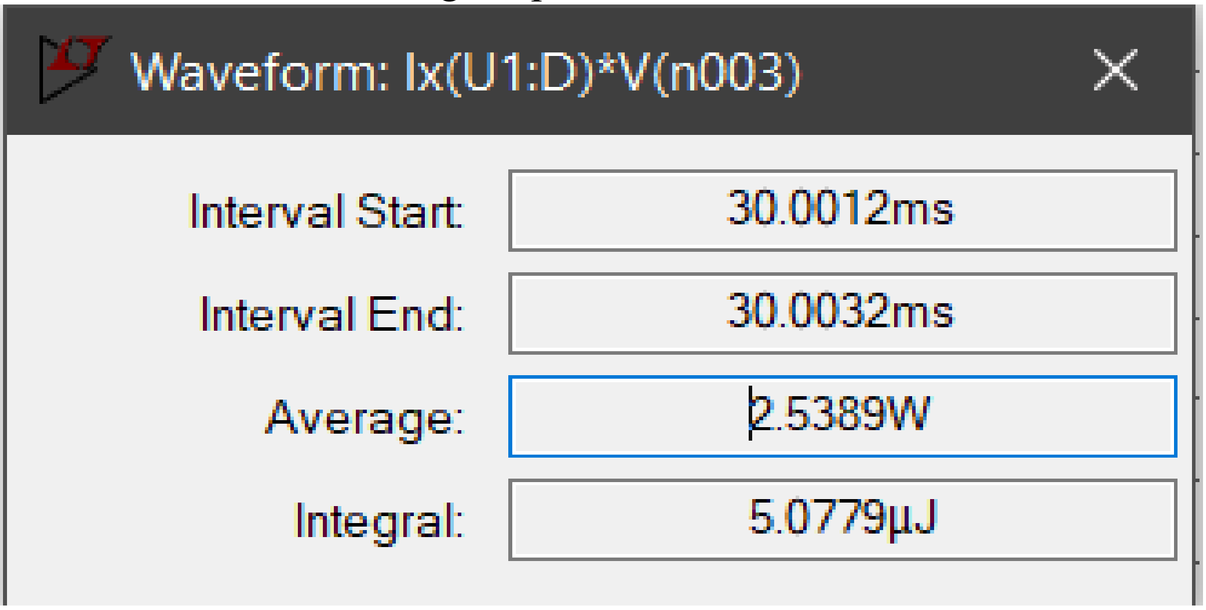


Figure 20 Switching off power losses at 50 Hz R-L load

LTspice calculations

$$\text{Pon} = 75.575 * 10^{-9} * 50 = 3.77875 * 10^{-6}\ Watt$$

$$\text{Poff} = 5.0779 * 10^{-6} * 50 = 2.53895 * 10^{-4}\ Watt$$

Actual Reading

Switching on

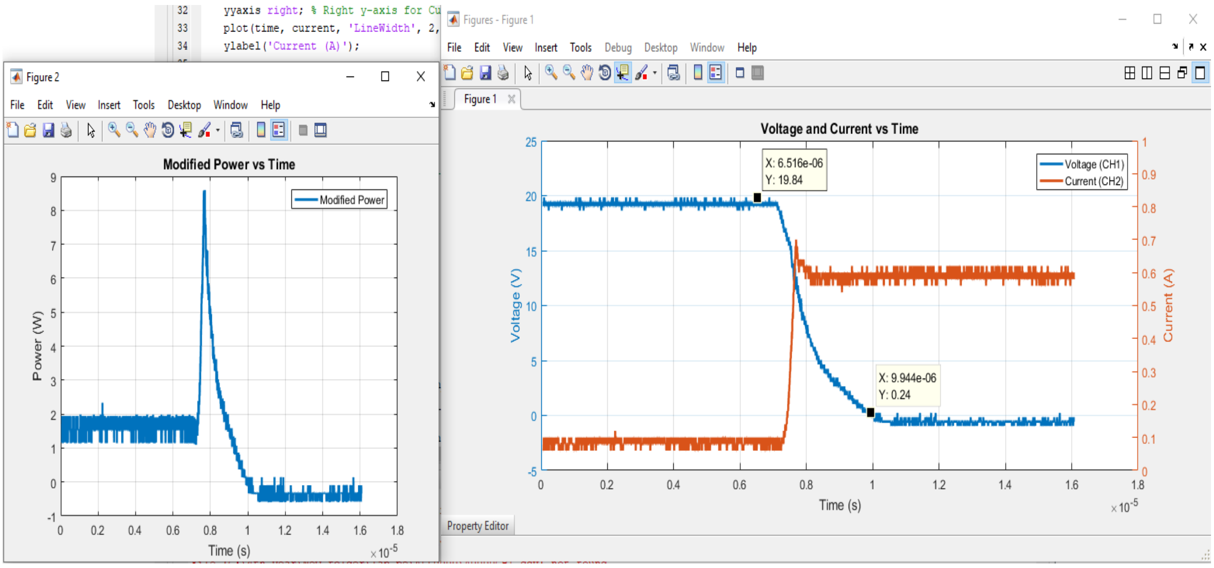


Figure 22 Voltage, Current, Power Switching on at 50 Hz R-L loads.

Switching On Calculation

P= 8.306e-6 * Fs

```
Integrated Power between 6.516e-06s and 9.944e-06s: 8.3806e-06 W
```

P = 8.306 e-9*50 = 0.0008306 == 0

TON =3.428e-6 sec

Switching Off

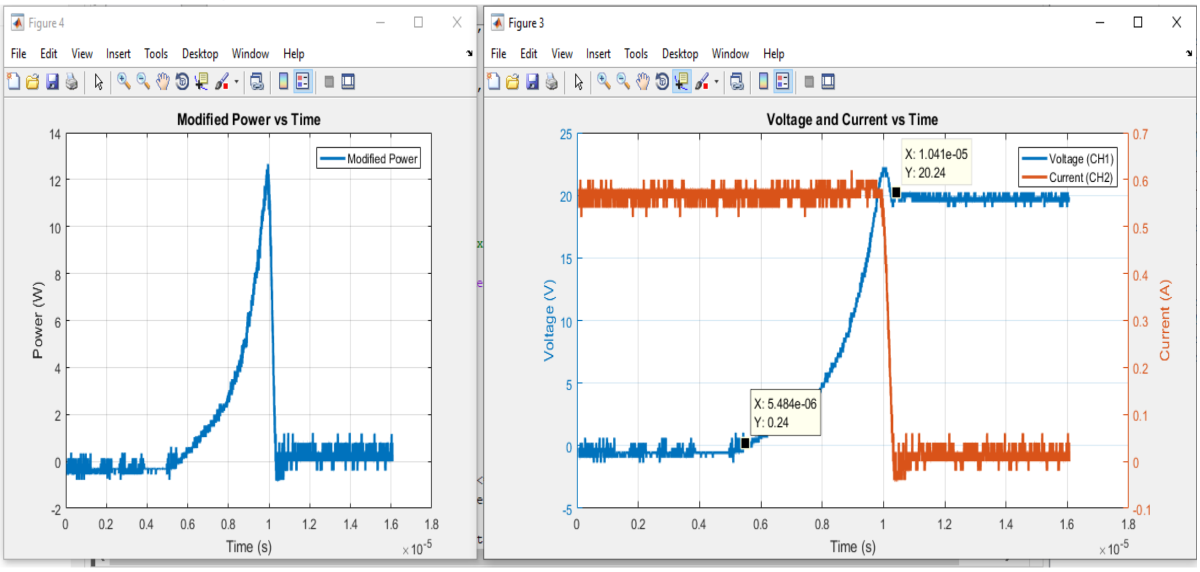


Figure 23 Voltage, Current, Power Switching on at 50 Hz R-L load

Switching Off Calculation

P= 1.8054e-5 * Fs

```
Integrated Power between 5.484e-06s and 1.041e-05s: 1.8054e-05 W
```

P = 50* 1.8054e-5 = 9.274e-4 Watt

Toff = 4.926e-6 sec

Calculated results

(1/2) *v*i*fs*toff = (1/2) *20*0.6*4.926e-6 *50= 14.778e-3 w.

At 1000 Hz

Voltage, Current and power waveforms

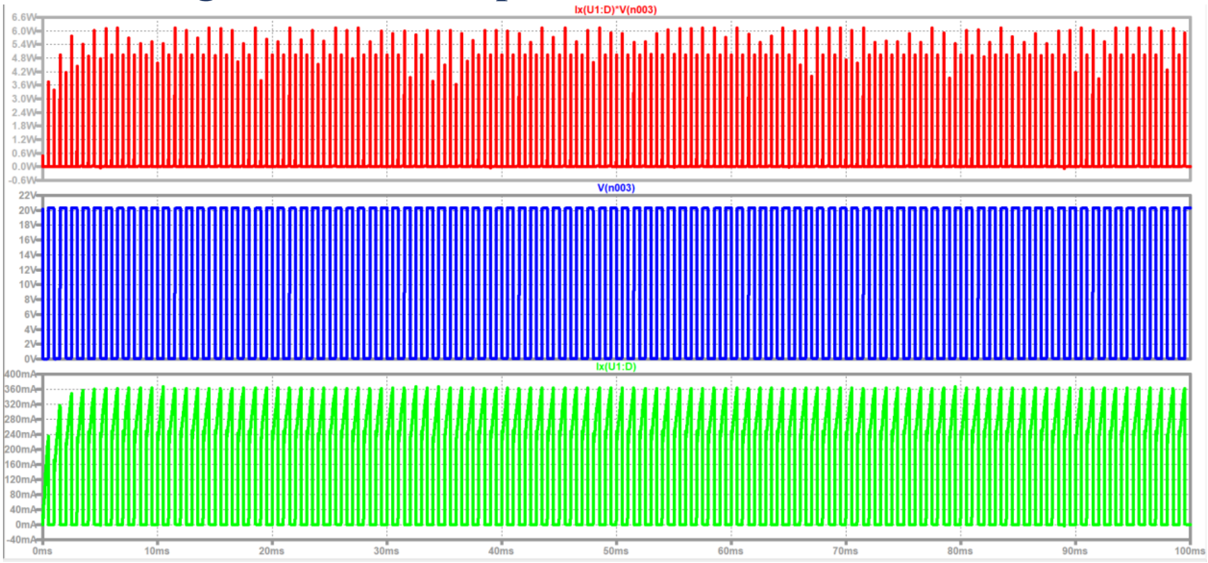


Figure 24 Voltage, Current, Power at 1000 Hz R-L load

Switching losses

- Switching on losses

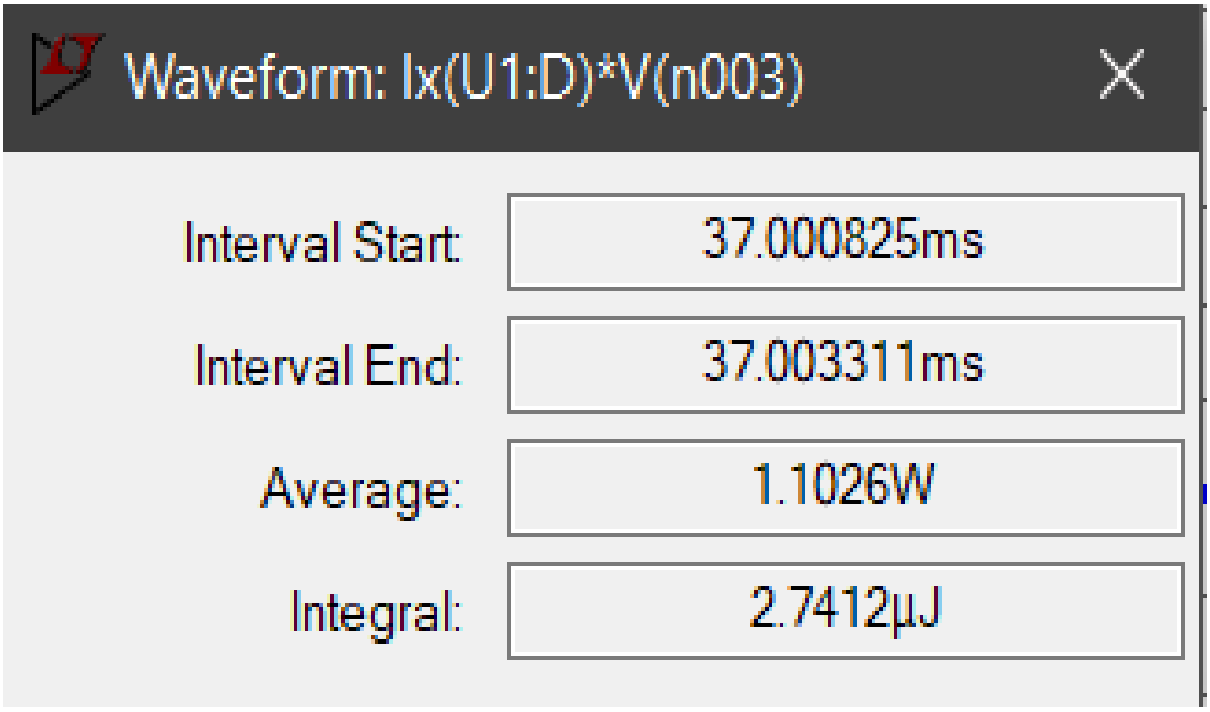


Figure 25 Switching On losses at 1000 Hz R-L load.

- Switching off losses

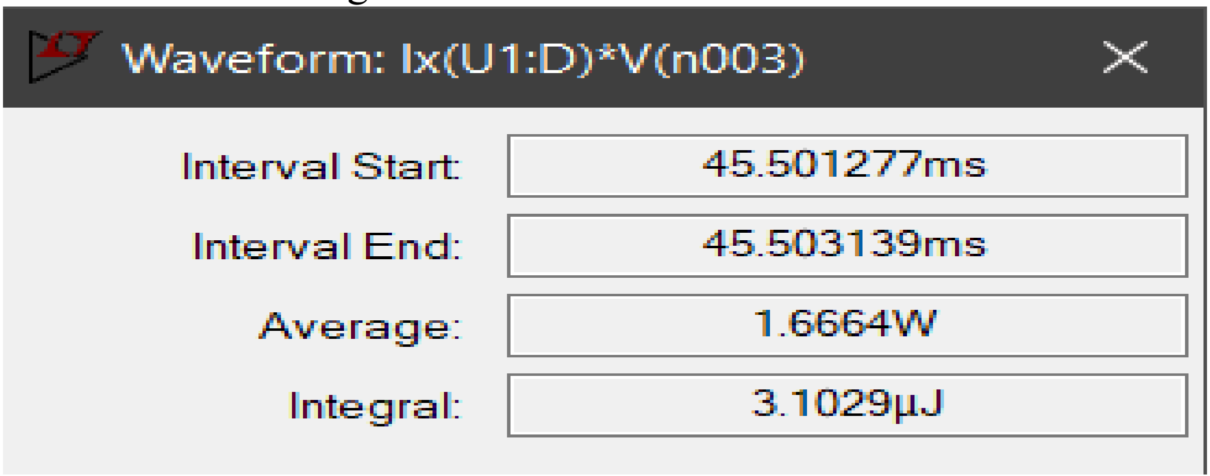


Figure 26 Switching Off losses at 1000 Hz R-L load.

LTspice calculations

Pon = 2.7412 * 10^ (-6)*1000= 2.7412 * 10^(-3) Watt

Poff = 3.1029 * 10^ (-6)*1000=3.1029* 10^(-3) Watt

Actual Reading

Switching On

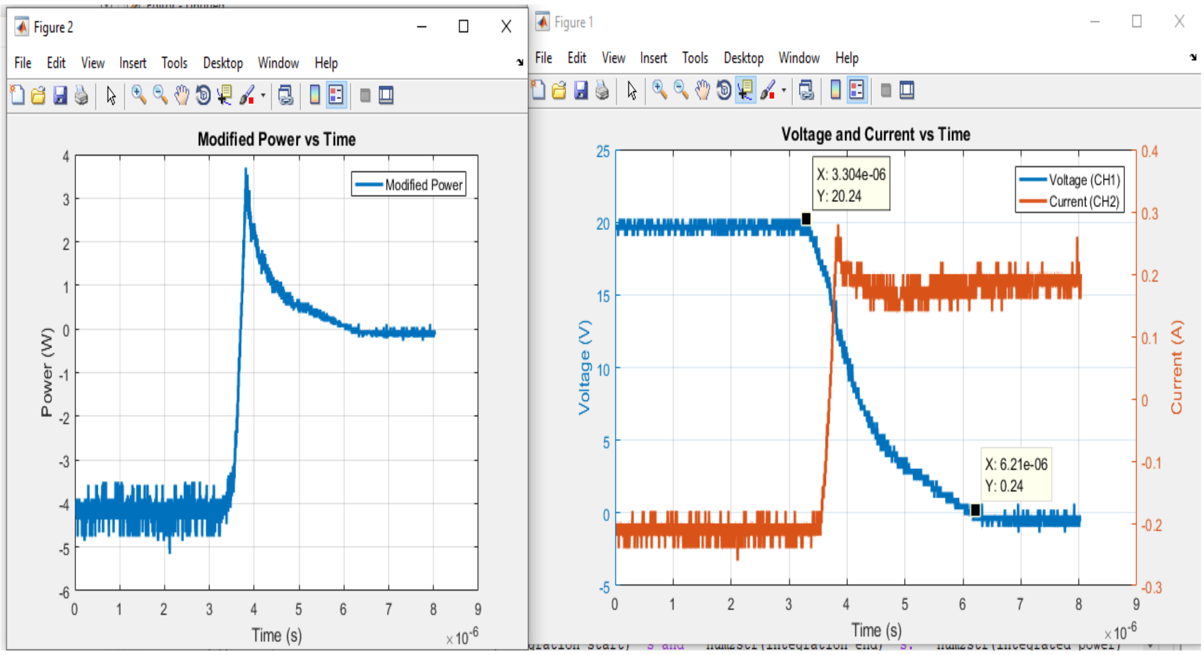


Figure 27 Actual Voltage, Current and power Switching on at 1000 Hz R-L load

Switching On Calculation

P= 8.2816e-7 * Fs

```
Integrated Power between 3.304e-06s and 6.21e-06s: 8.2816e-07 W
```

P = 8.2816 e-7*1000= 8.2816e-4

TON =2.906e-6 sec

Calculated results

(1/2) *v*i*fs*ton = (1/2) *20*0.6*2.906e-6*1000= 17.436e-3 w

Switching Off

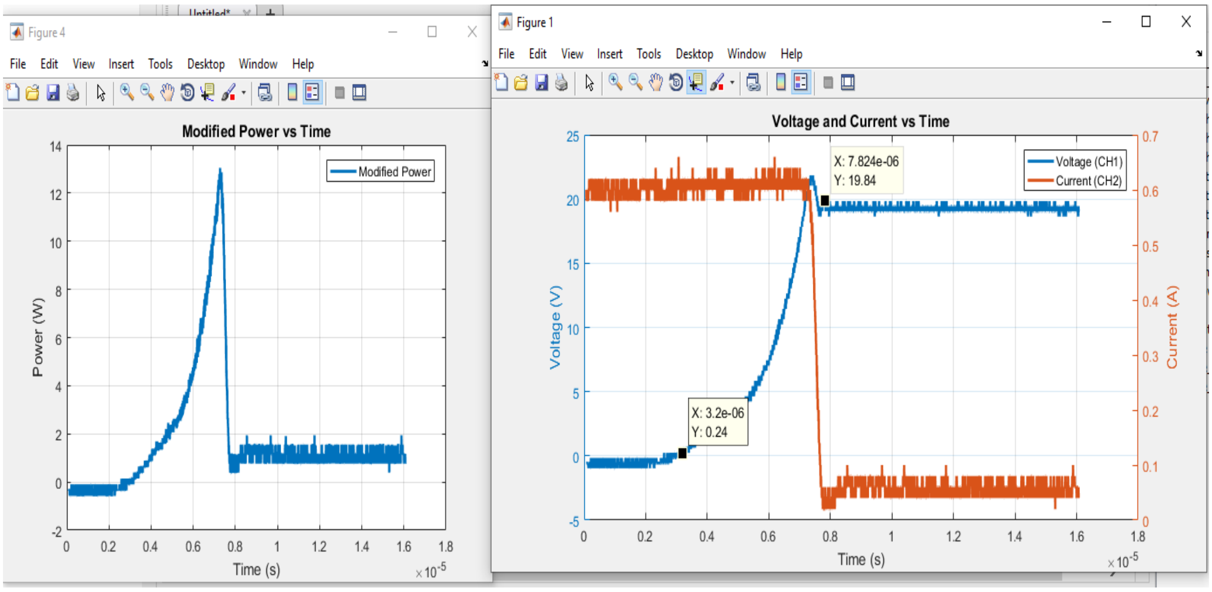


Figure 28 Actual Voltage, Current and power Switching Off at 1000 Hz R-L load

Switching On Calculation

P= 1.8982e-5 * Fs

```
Integrated Power between 3.2e-06s and 7.824e-06s: 1.8982e-05 W
```

P = 1000* 1.8982e-5 = 18.982e-3 watt

Toff = 4.62e-6 sec

Calculated results

(1/2) *v*i*fs*toff = (1/2) *20*0.6*4.62e-6 *1000= 27.72e-3 watt

At 10K Hz

Voltage, Current and power waveforms

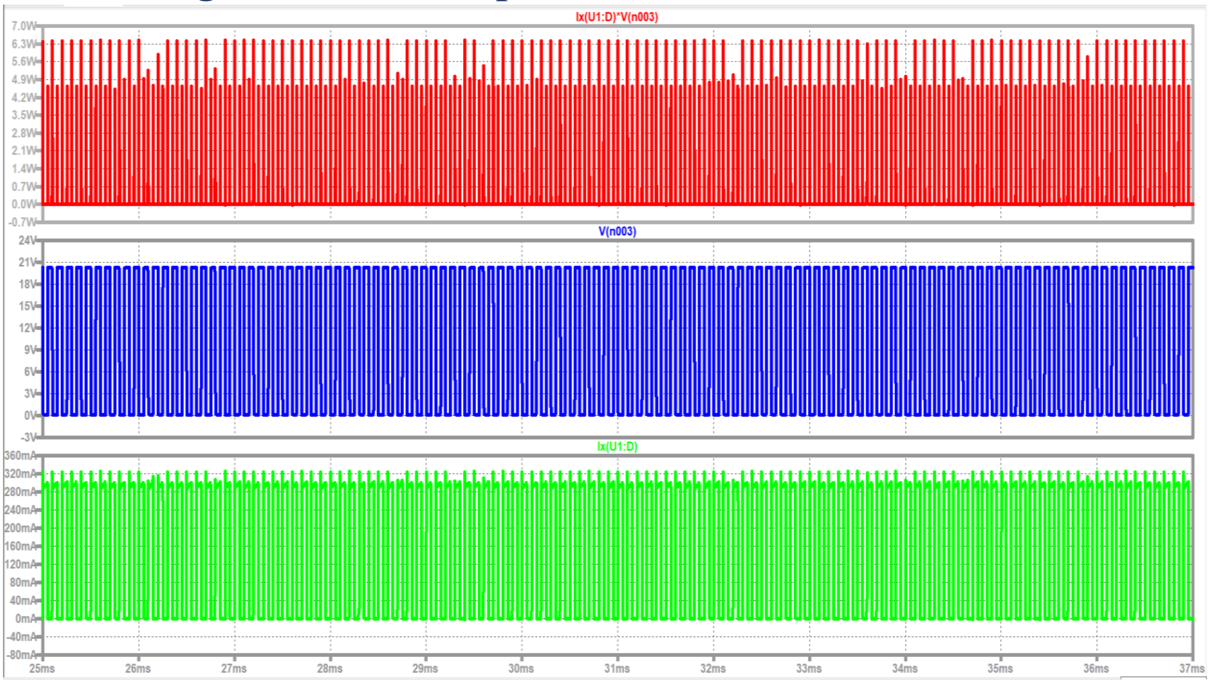


Figure 29 Voltage, Current and power waveforms at 10K Hz R-L load

Switching losses

- Pon switching losses.

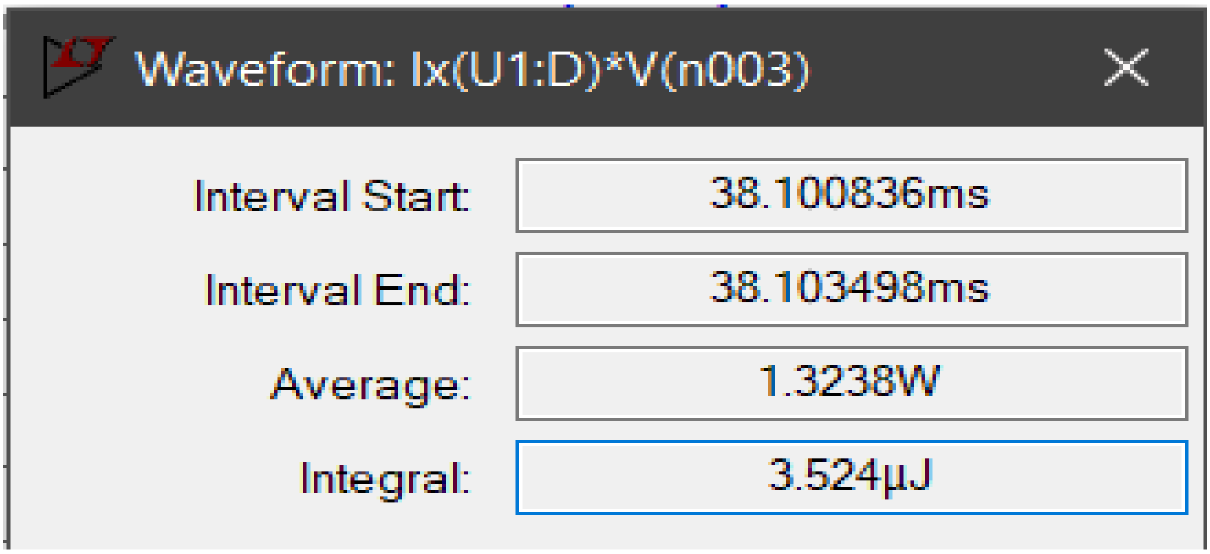


Figure 30 On Switching losses at 10K Hz R-L load.

- Poff switching losses.

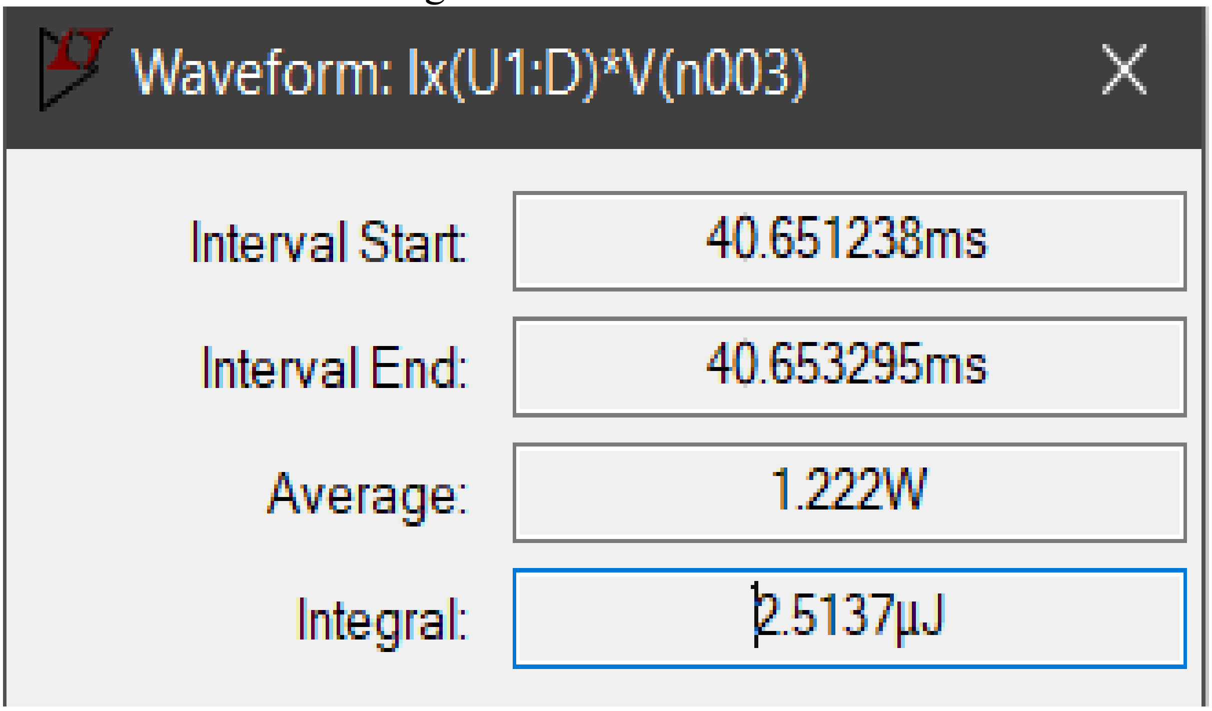


Figure 31 Figure 30 Off Switching losses at 10K Hz R-L load

.LTspice calculations

Pon = $3.524 * 10^{-6} * 10000 = 0.03524$ Watt

Poff = = $2.5137 * 10^{-6} * 10000 = 0.025137$ Watt

Actual Reading

Switching On

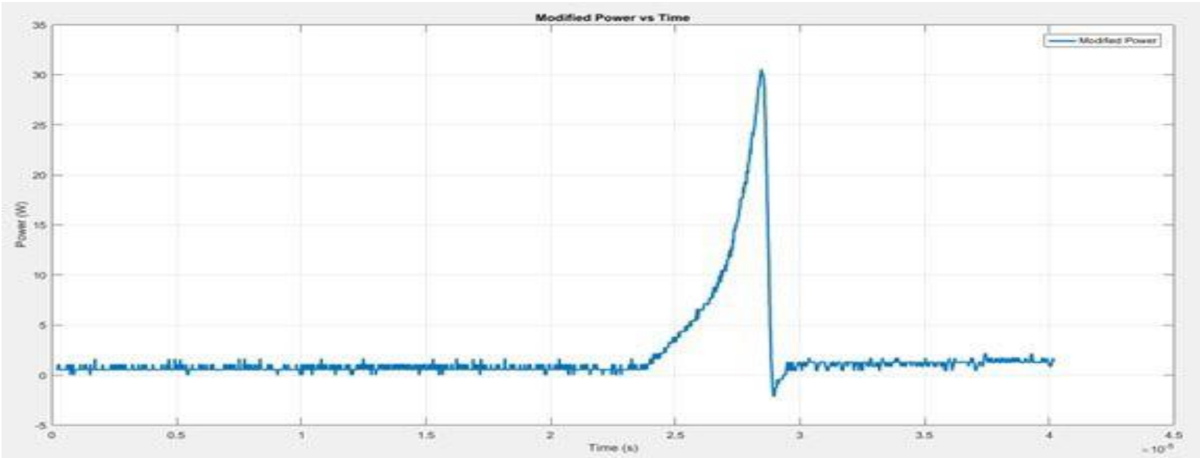


Figure 33 Actual Switching on Power at 10K Hz R-L load

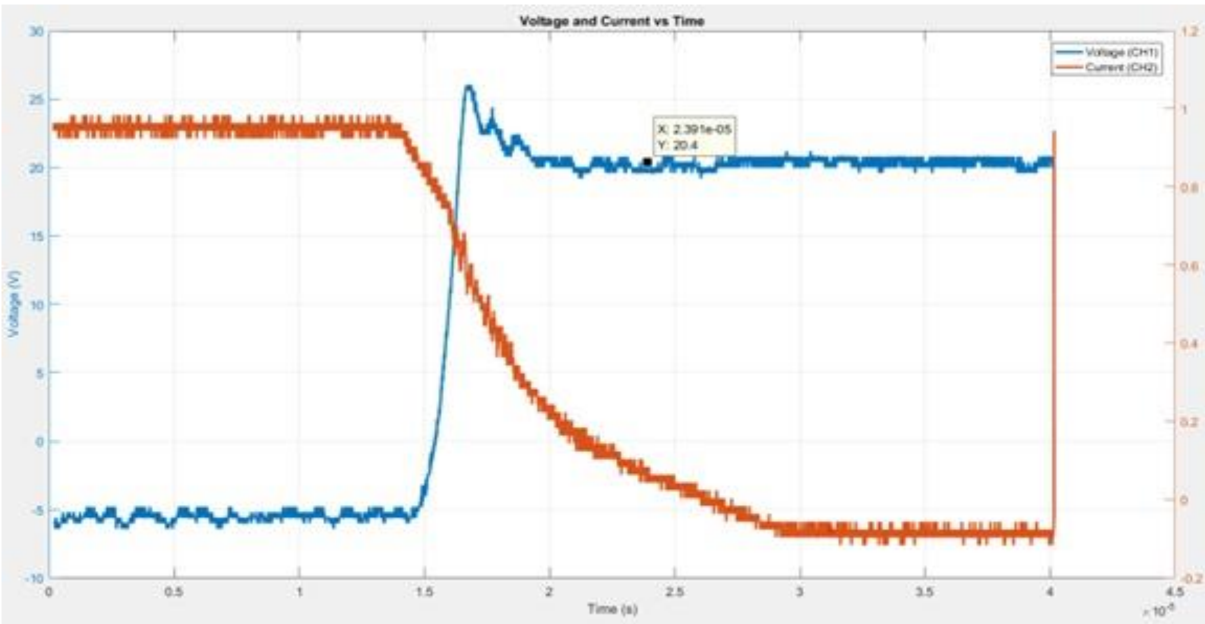


Figure 32 Actual Voltage, Current Switching On at 10K Hz R-L load

Switching On Calculation

P= 2.4026e-6 * Fs , P =2.4026e-6 *10000= 2.4026e-3 w

TON =0.91e-6 sec

Calculated results

(1/2) *v*i*fs*ton = (1/2) *20*0.6*0.91e-6 *10000= 0.0546 w

Switching Off

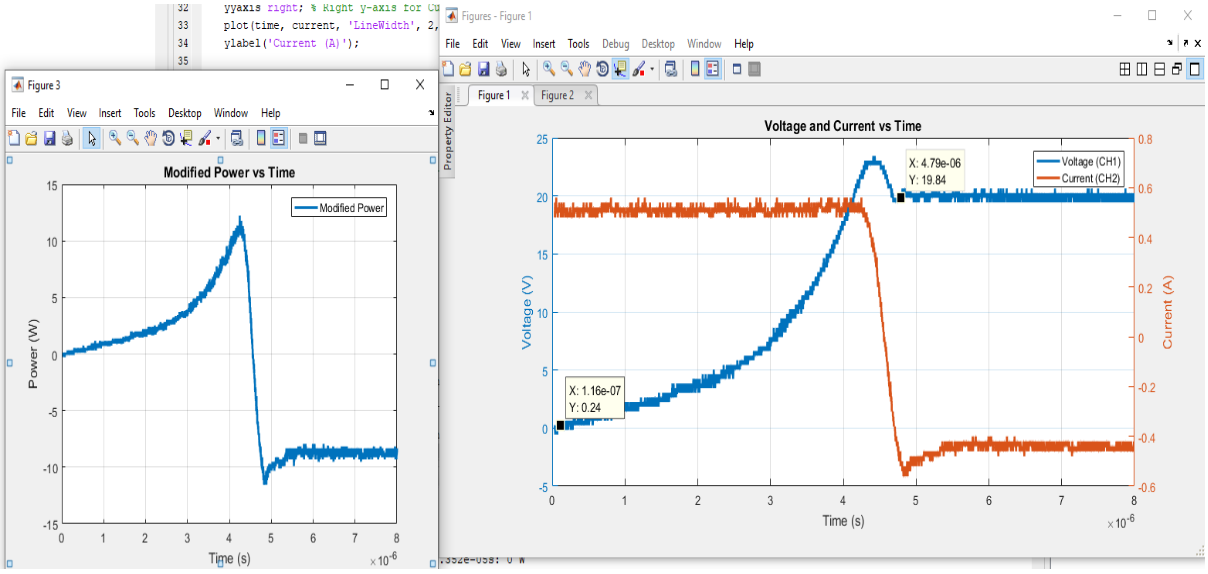


Figure 34 Actual Voltage, Current, Power Switching On at 10K Hz R-L load

Switching Off Calculations

P= 1.4026e-6 * Fs

P =1.4026e-6 *10000= 0.14026w

TON =4.674e-6 sec

Calculated results

(1/2) *v*i*fs*ton = (1/2) *20*0.6*4.674e-6 *10000= 0.28044w

Conclusion

Summary of LTspice readings

R- Load			
Fsw	50 Hz	1000 Hz	10 KHz
Eon	$7.5253 * 10^{-6}$ J	$7.321 * 10^{-6}$ J	$7.3468 * 10^{-6}$ J
Eoff	$4.8454 * 10^{-6}$ J	$4.8119 * 10^{-6}$ J	$4.9669 * 10^{-6}$ J
Pon	$3.76265 * 10^{-4}$ W	0.007321 W	0.073468 W
Poff	$2.4227 * 10^{-4}$ W	0.0048119 W	0.049339 W

R-L Load			
Fsw	50 Hz	1000 Hz	10 KHz
Eon	$75.575 * 10^{-9}$ J	$2.7412 * 10^{-6}$ J	$3.524 * 10^{-6}$ J
Eoff	$5.0779 * 10^{-6}$ J	$3.1029 * 10^{-6}$ J	$2.5137 * 10^{-6}$ J
Pon	$3.77875 * 10^{-6}$ W	$2.7412 * 10^{-3}$W	0.03524 W
Poff	$2.53895 * 10^{-4}$ W	$3.1029 * 10^{-3}$ W	0.025137 W

Comments on LTspice results

1. These readings are not accurate as Ton is greater than Toff which is not valid theoretically. This could happen due to errors in the used models.

2. Power on switching losses at 50Hz have a value in the simulation but it is very small (in nano joules) while theoretically it should have no value (Pon = zero)

Comments on Actual results "MATLAB"

1. The losses between actual and simulation answer is due to the faults in hardware components as we see losses in hardware results is bigger than the simulation one.

2. The parasitic inductance will lead to voltage spikes and overshoots during switching transitions, these spikes contribute to increased power losses due to higher voltage across the MOSFET during switching

Switching losses “Q2”

LTSPICE model

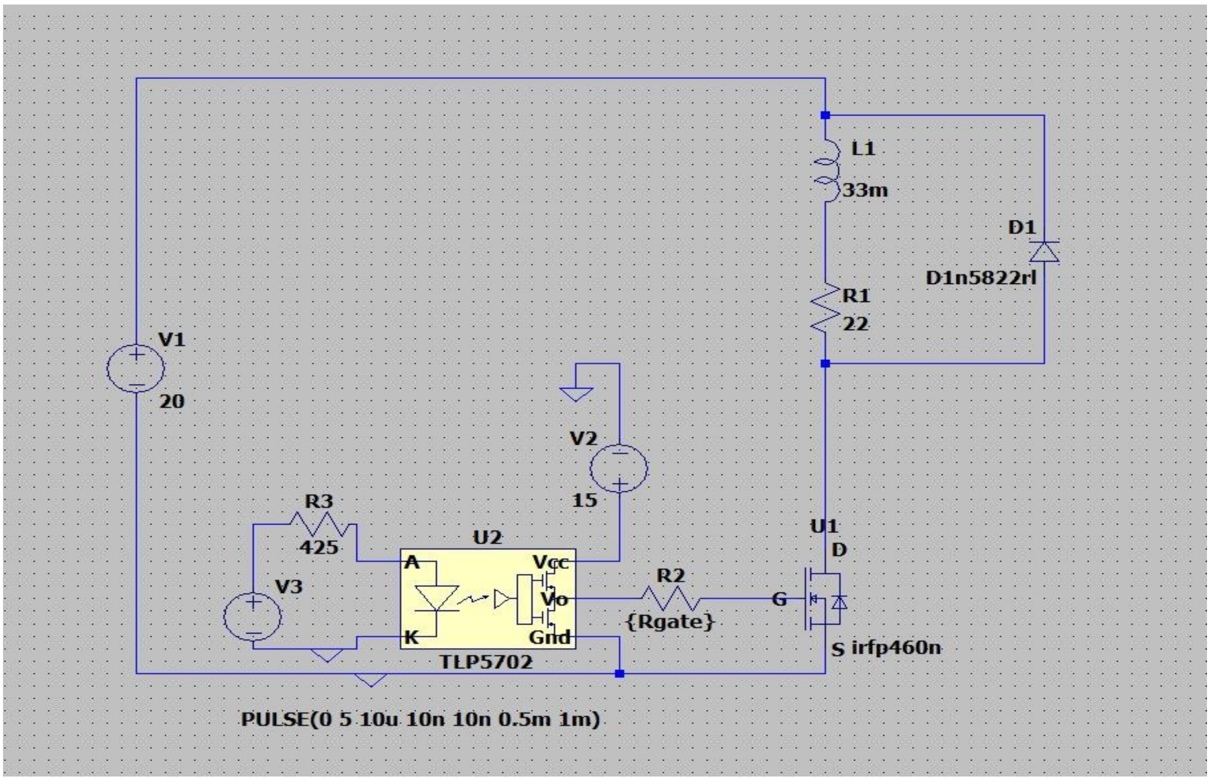
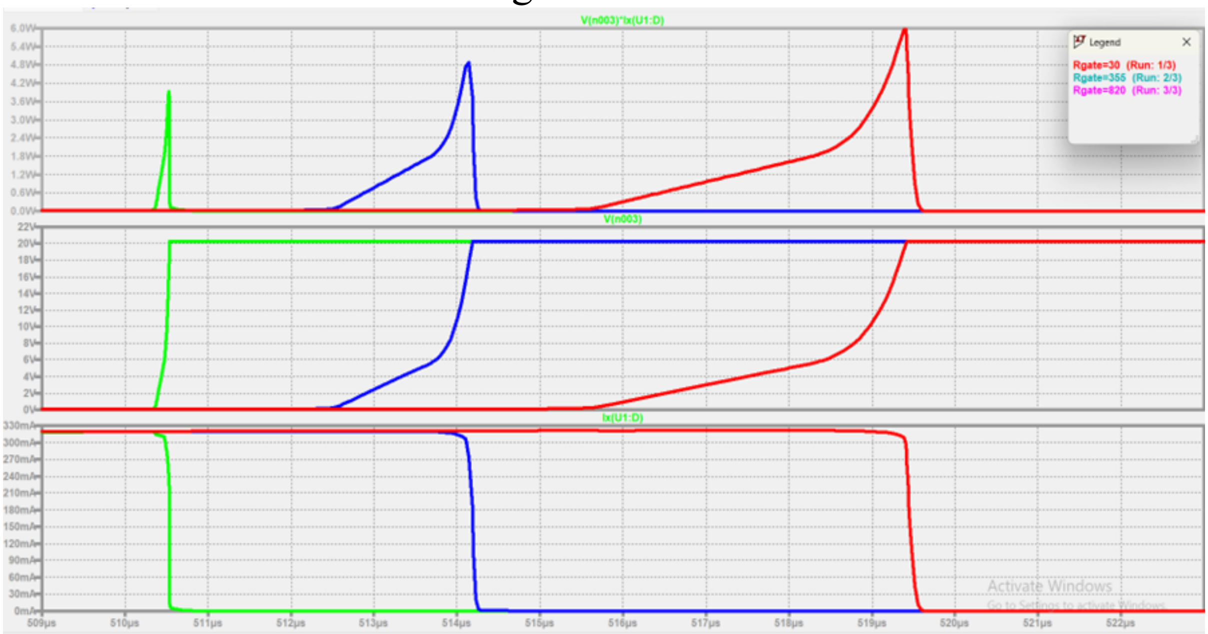
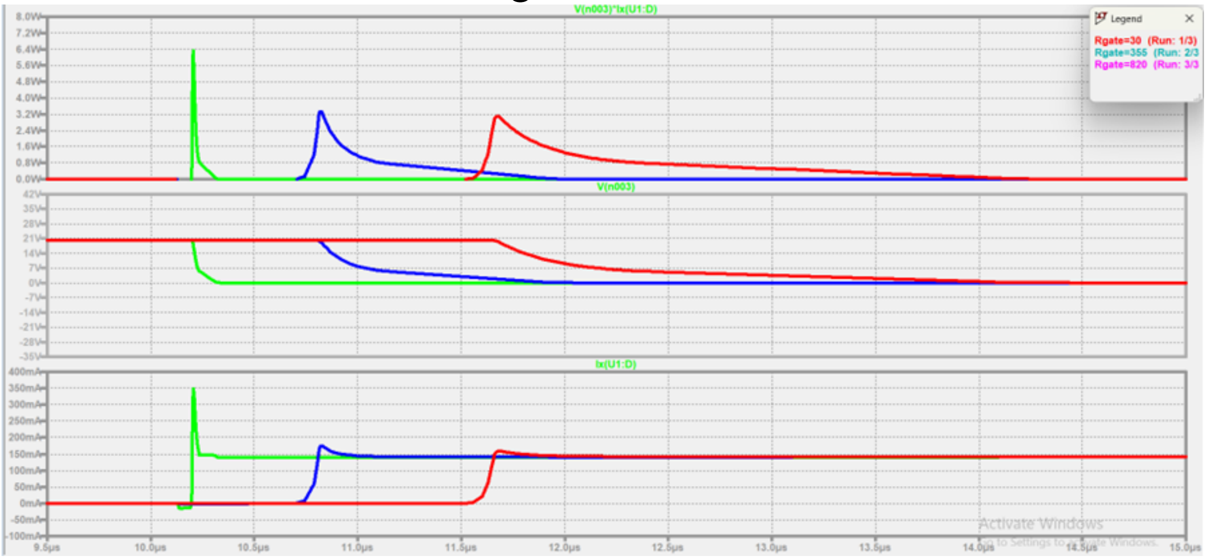


Figure 35 LTSPICE model

- At the moment of turning off the MOSFET



- At the moment of turning on the MOSFET



Analytical solution

At R_3 = 30 ohm

$P_{off} = 0.5*t_{off}*I*V*F_{sw}$

$= 0.5*0.5*10^{-6}*320*10^{-3}*20*1000 = 0.0016$ W

$P_{on} = 0.5*t_{on}*I*V*F_{sw}$

$= 0.5*0.25*10^{-6}*350*10^{-3}*20*1000 = 0.000875$ W

P total = 0.002475 W

At R_2 = 355 ohm

$P_{off} = 0.5*t_{off}*I*V*F_{sw}$

$= 0.5*2*10^{-6}*320*10^{-3}*20*1000 = 0.0064$ W

$P_{on} = 0.5*t_{on}*I*V*F_{sw}$

$= 0.5*1.25*10^{-6}*175*10^{-3}*20*1000 = 0.0022$ W

P total = 0.008588 W

At R_1 = 820ohm

$P_{off} = 0.5*t_{off}*I*V*F_{sw}$

$= 0.5*5*10^{-6}*320*10^{-3}*20*1000 = 0.016$ W

$P_{on} = 0.5*t_{on}*I*V*F_{sw}$

$= 0.5*2.5*10^{-6}*170*10^{-3}*20*1000 = 0.00425$ W

P total = 0.02025 W

Comments

- As R_{gate} increases, the time taken for the MOSFET to turn off or on will increase so the total power switching losses will increase But it will affect the voltage (will decrease the Ringing voltage due to parasitic inductance that will appear in the hardware readings)
- As gate resistance decreases, it allows the MOSFET to reach the on state more rapidly, leading to higher current flow during the on state.

Lab result in MATLAB software

- **At R_3 = 30 ohm**

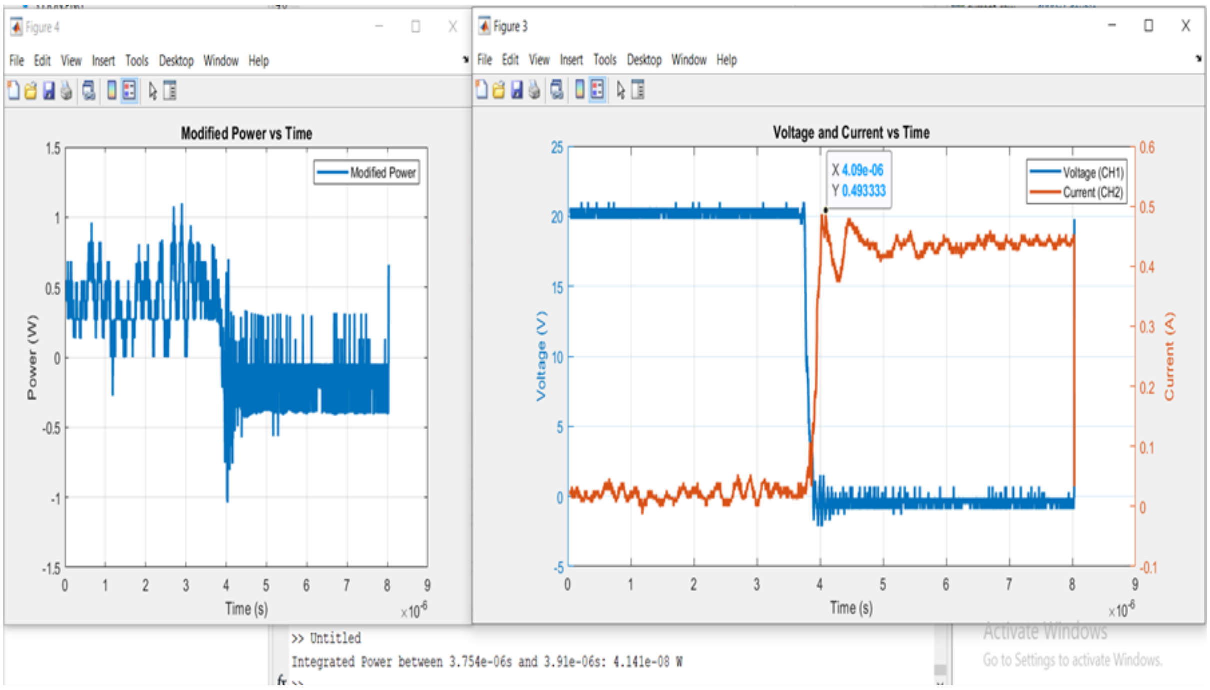


Figure 36 on state for 30-ohm gate resistance

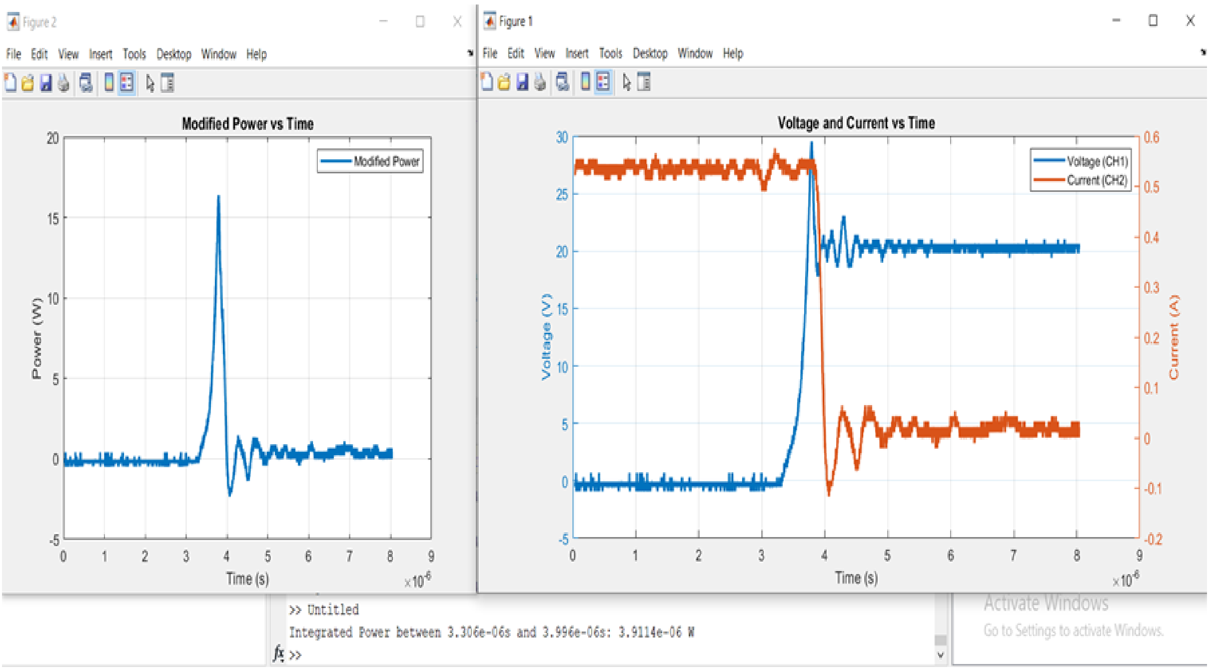


Figure 37 off state 30-ohm gate resistance

- **At R_2 = 355 ohm**

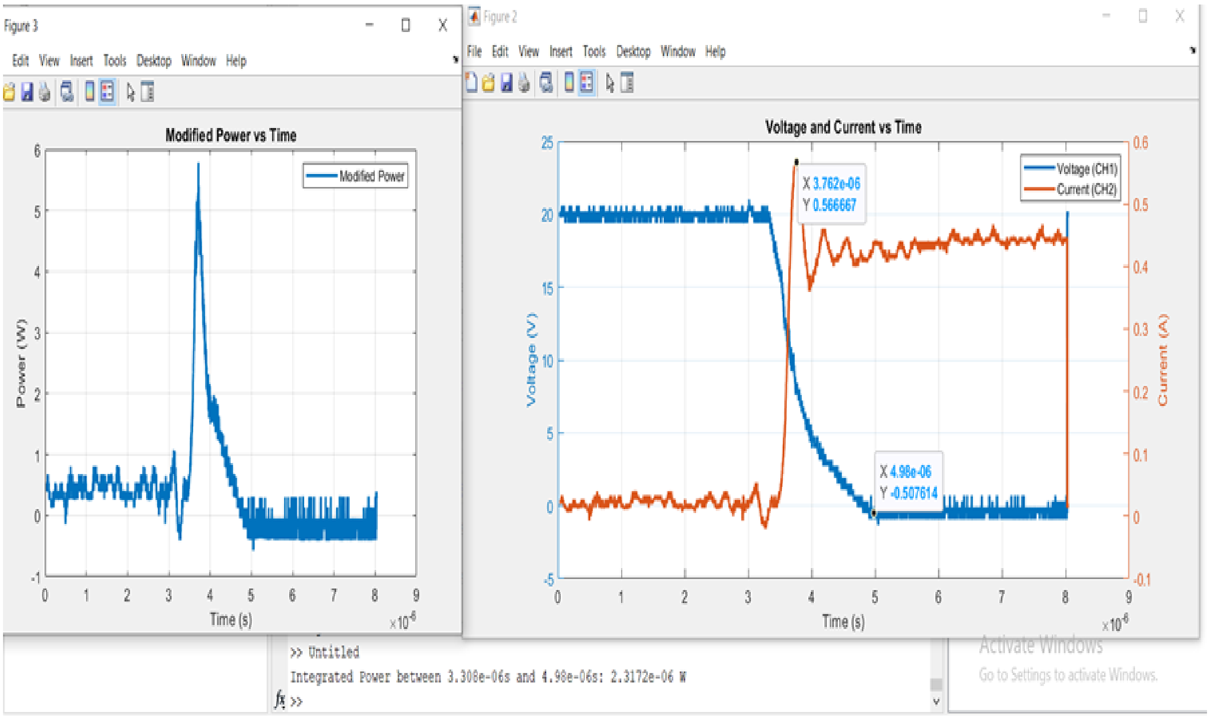


Figure 38 on state 355-ohm gate resistance

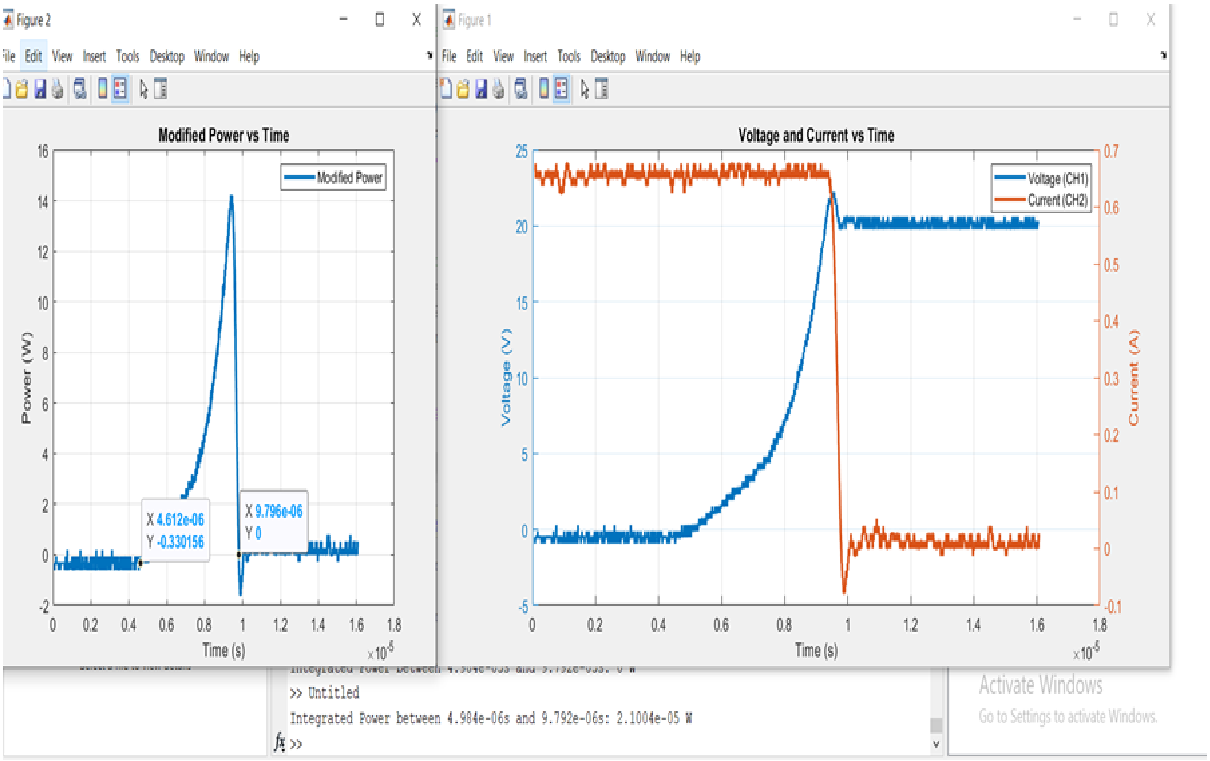


Figure 40 off state 355-ohm gate resistance

- **At R_1 = 820ohm**

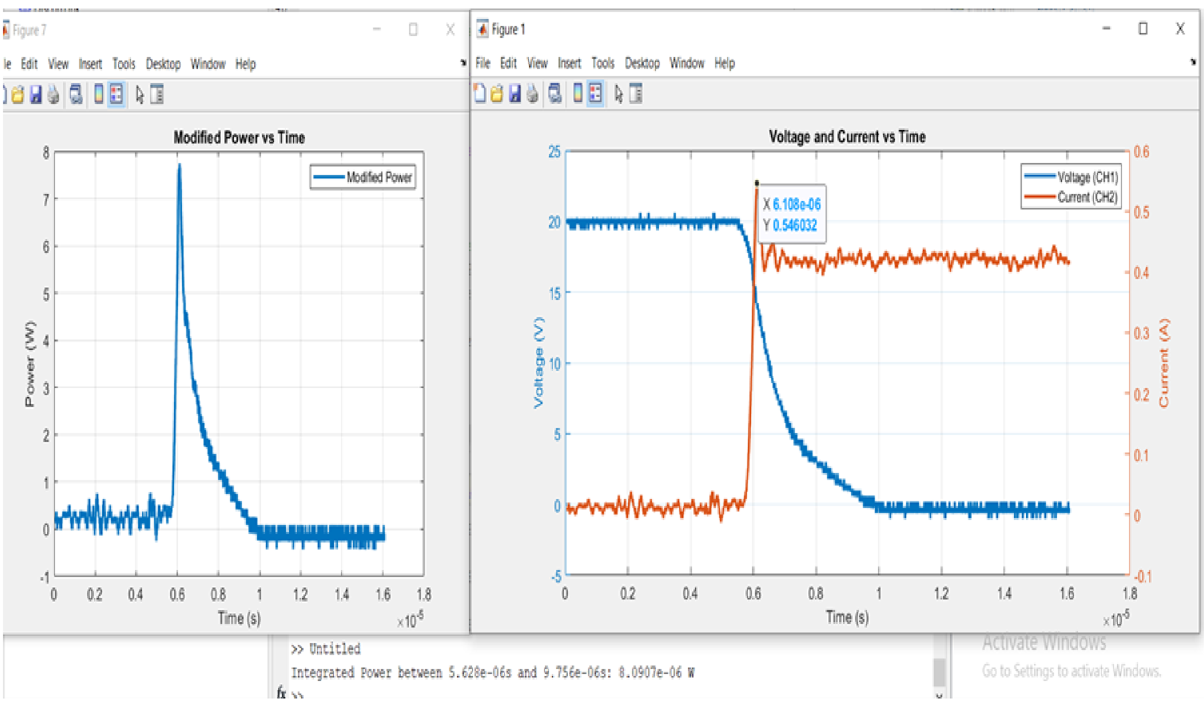
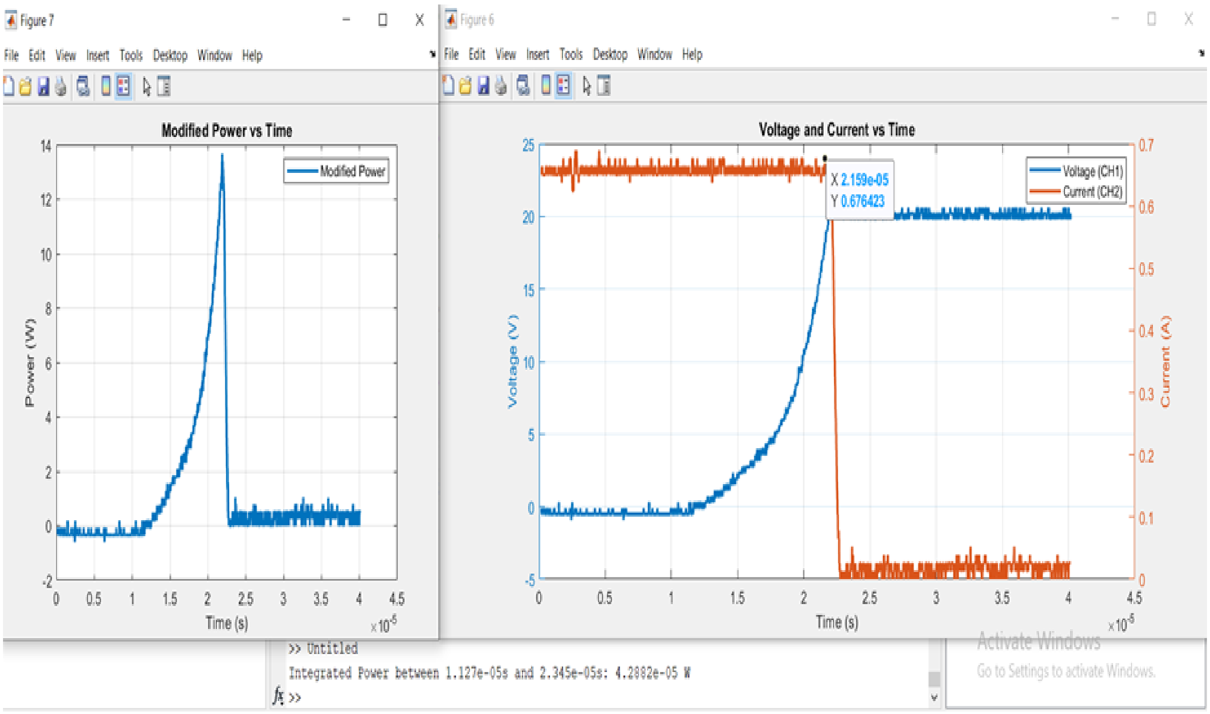


Figure 39 on state 820-ohm gate resistance



COMPARSION

At R_3 = 30 ohm

SIMULATION

$P_{off} = 0.5*t_{off}*I*V*F_{sw}$

$= 0.5*0.5*10^{-6}*320*10^{-3}*20*1000 = 0.0016$ W

$P_{on} = 0.5*t_{on}*I*V*F_{sw}$

$= 0.5*0.25*10^{-6}*350*10^{-3}*20*1000 = 0.000875$ W

P total = 0.002475 W

HARDWARE

P_{off} = 0.0039114W

P_{on} = 0.00004141W

P total = 0.00395281W

At R_2 = 355 ohm

SIMULATION

$P_{off} = 0.5*t_{off}*I*V*F_{sw}$

$= 0.5*2*10^{-6}*320*10^{-3}*20*1000 = 0.0064$ W

$P_{on} = 0.5*t_{on}*I*V*F_{sw}$

$= 0.5*1.25*10^{-6}*175*10^{-3}*20*1000 = 0.0022$ W

P total = 0.008588 W

HARDWARE

$P_{off} = 0.009792$W

$P_{on} = 0.0023172$W

P total = 0.0121092W

At R_1 = 820ohm

SIMULATION

$P_{off} = 0.5*t_{off}*I*V*F_{sw}$

$= 0.5*5*10^{-6}*320*10^{-3}*20*1000 = 0.016$ W

$P_{on} = 0.5*t_{on}*I*V*F_{sw}$

$= 0.5*2.5*10^{-6}*170*10^{-3}*20*1000 = 0.00425$ W

P total = 0.02025 W

HARDWARE

$P_{off} = 0.042882$W

$P_{on} = 0.0080907$W

P total = 0.0509727W

Figure 41 off state 820-ohm gate resistance

COMMENT

The power losses in the hardware model is more than in the simulation model due to

- The difference between the t_{on} and t_{off} in the hardware model because of the Simulation assumes perfect switching transitions, ignoring the finite rise and fall times.
- The presence of parasitic inductance that will lead to voltage spikes and overshoots during switching transitions, these spikes contribute to increased power losses due to higher voltage across the MOSFET during switching

Single Phase Inverter

A single-phase inverter is an electronic device that converts direct current (DC) power into alternating current (AC) power in electrical systems.

The Requirement is to simulate the operation of single-phase inverter with the following specifications:

$$Vdc = 20\,v\,, R_{\emptyset} = 20\,\Omega\,, L_{\emptyset} = 33\,mH\,, F = 50\,HZ$$

Here are some techniques to solve this example:

180° Conduction

SIMULATION BY MATLAB SOFTWARE

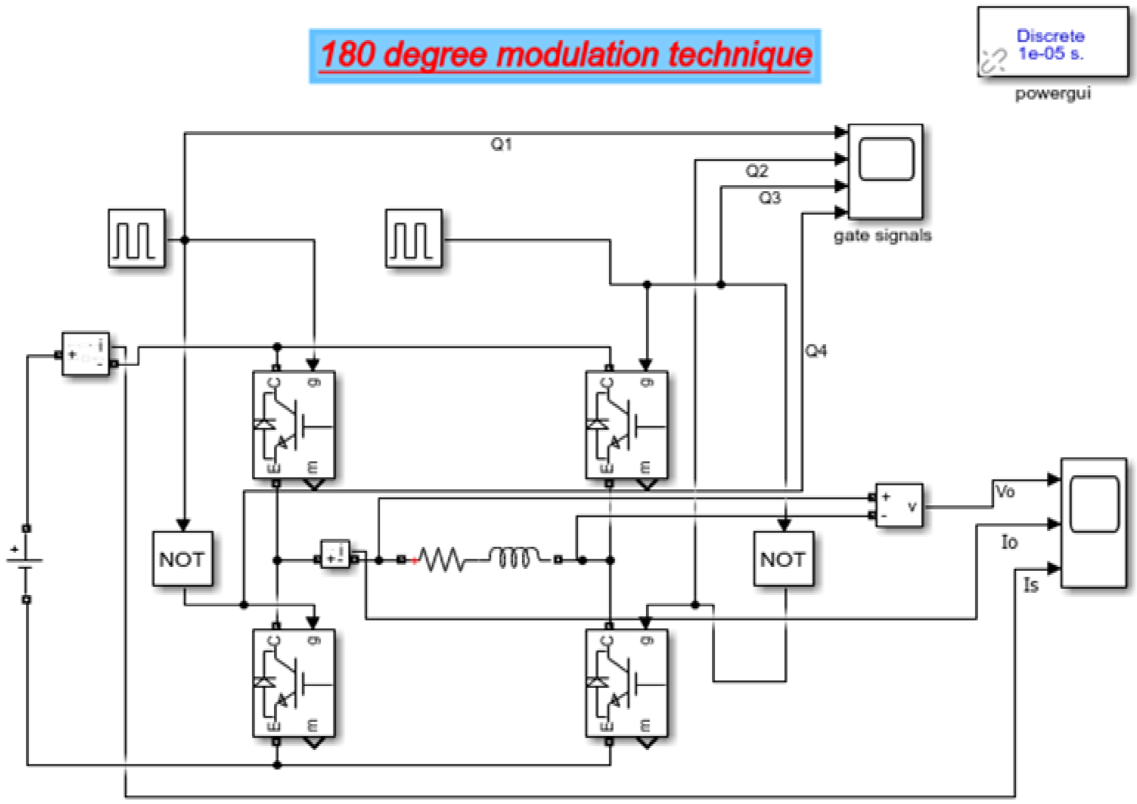


Figure 42 180 degree model

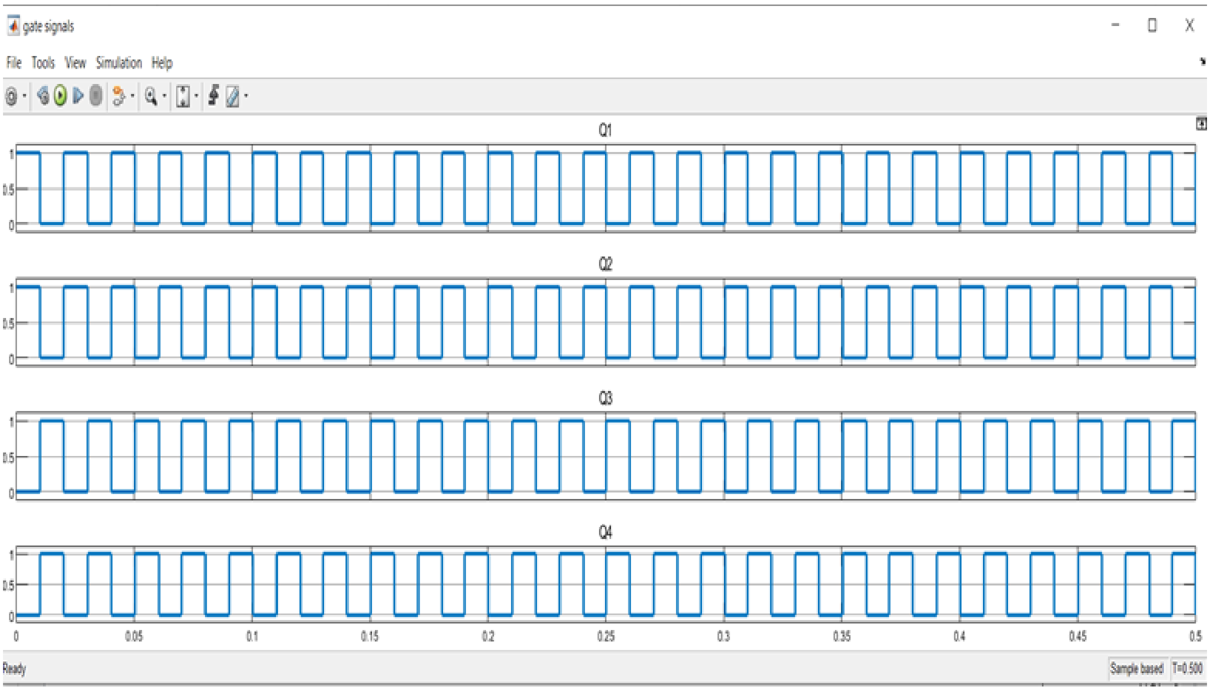
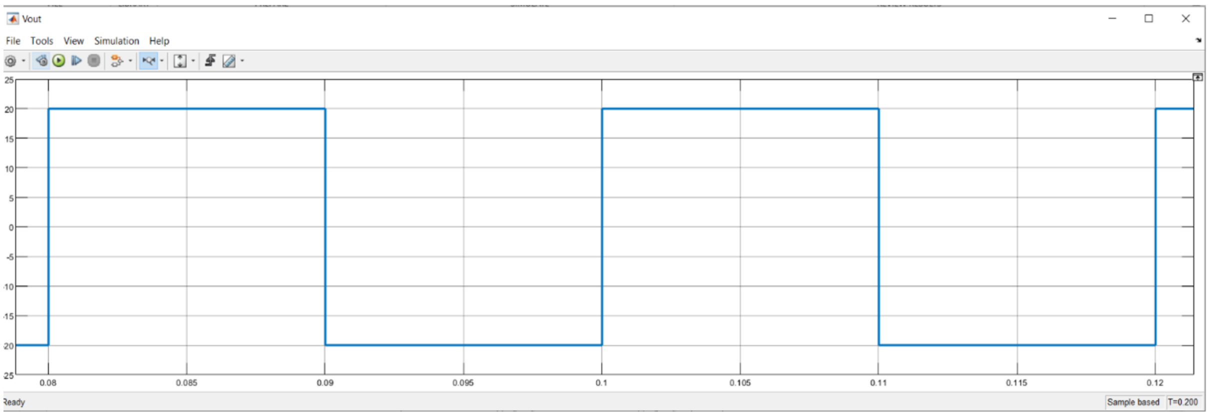
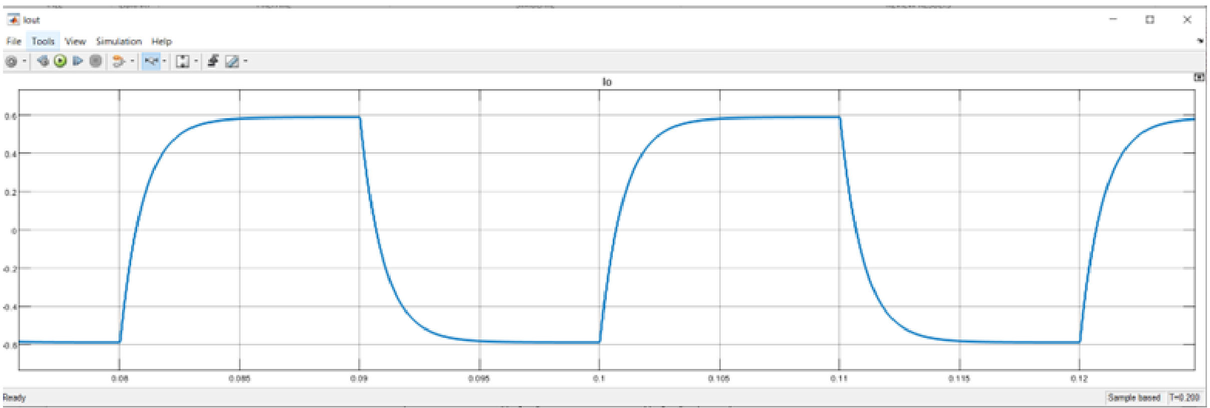


Figure 43 switches signals

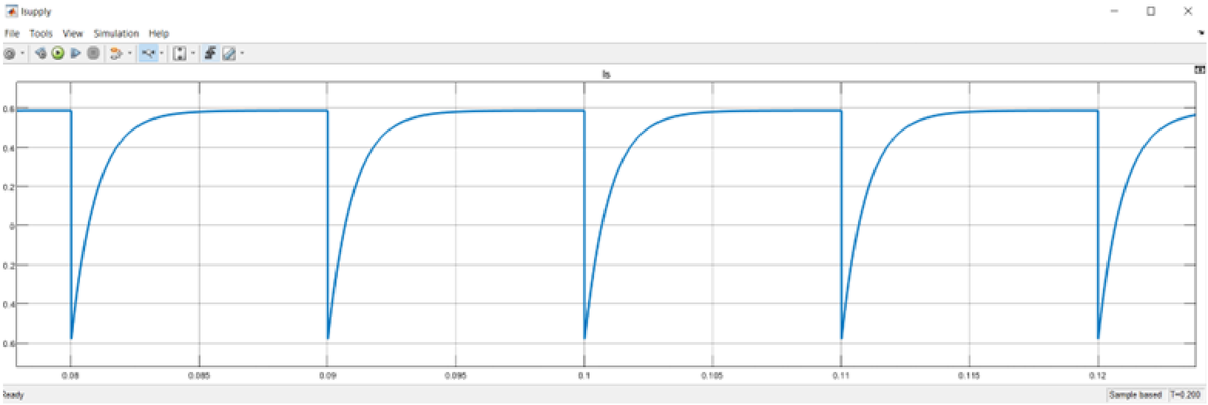
- OUTPUT VOLTAGE WAVE



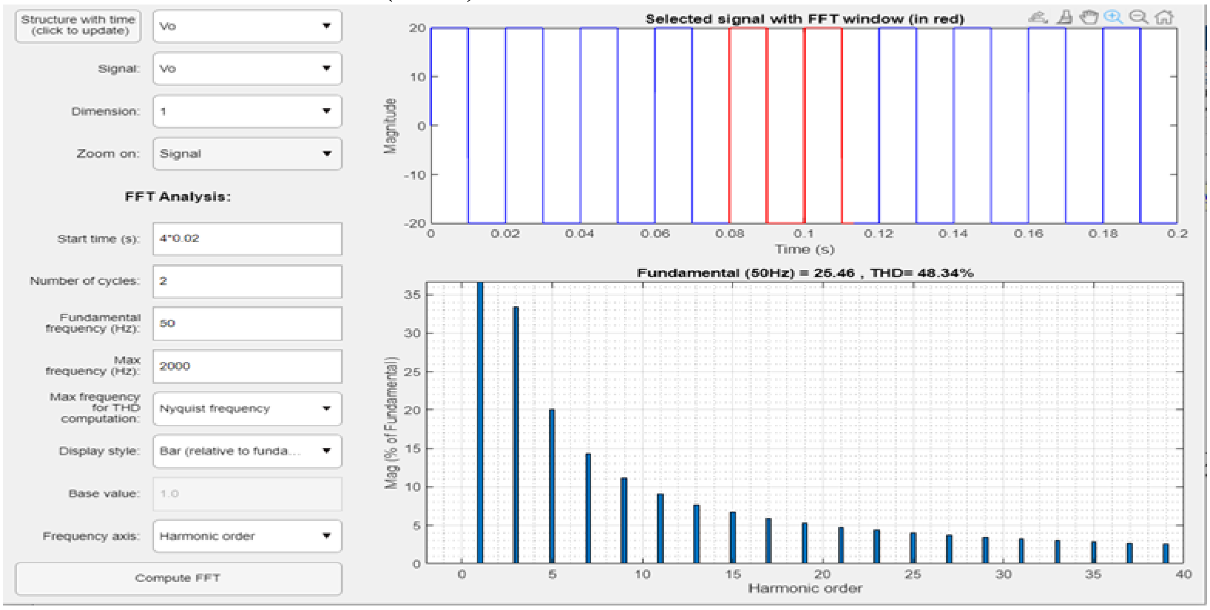
- OUTPUT CUURENT WAVE

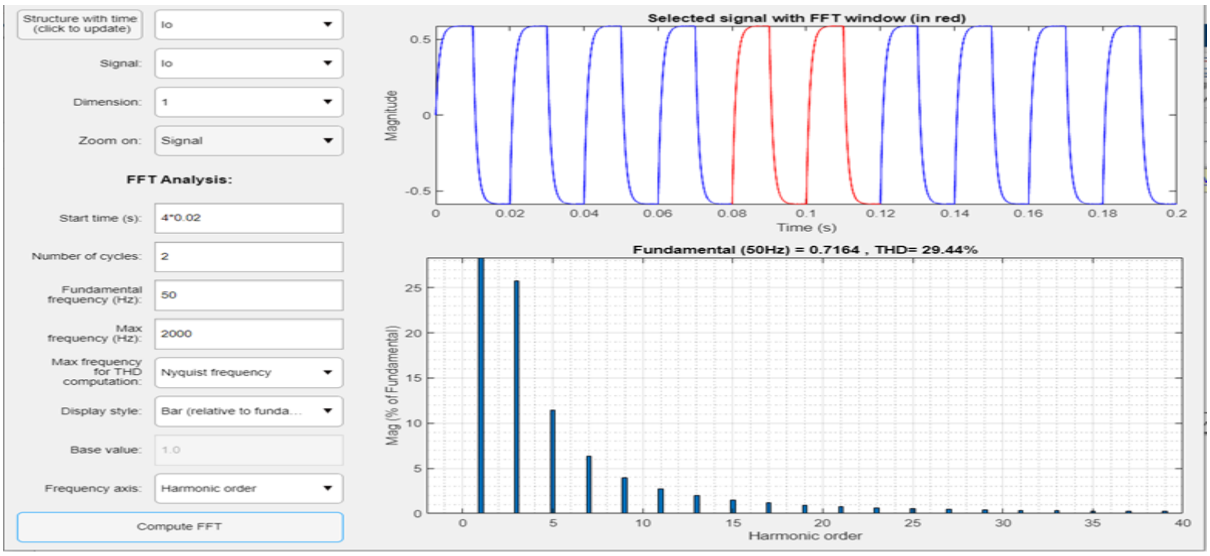


- SUPPLY CUURENT WAVE

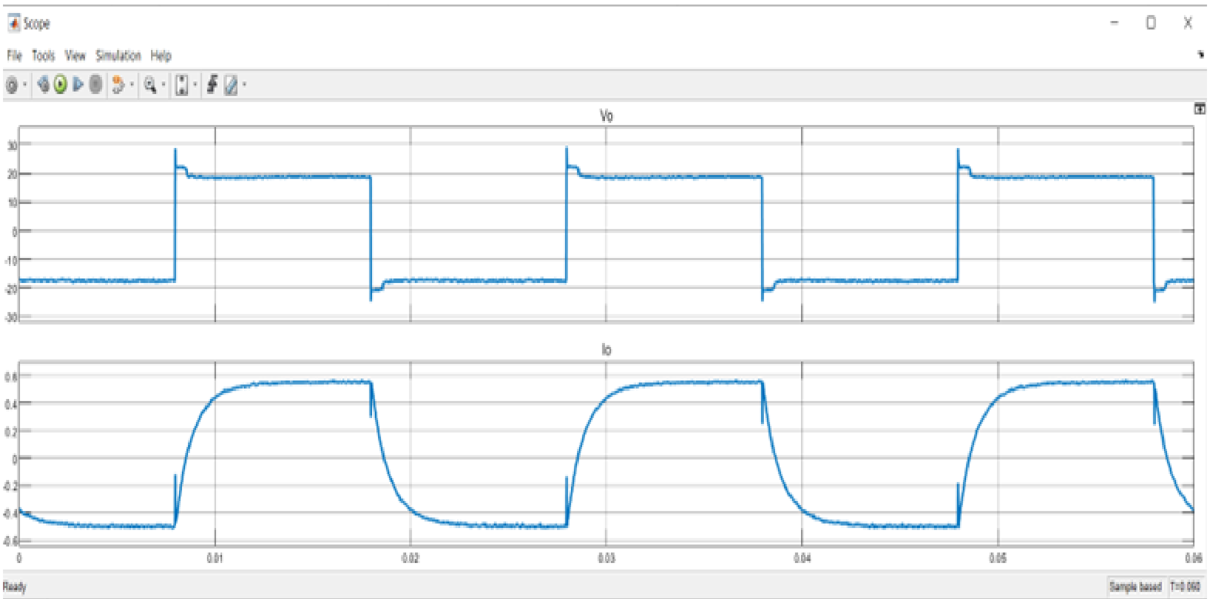


- FAST FOURIR (FFT)

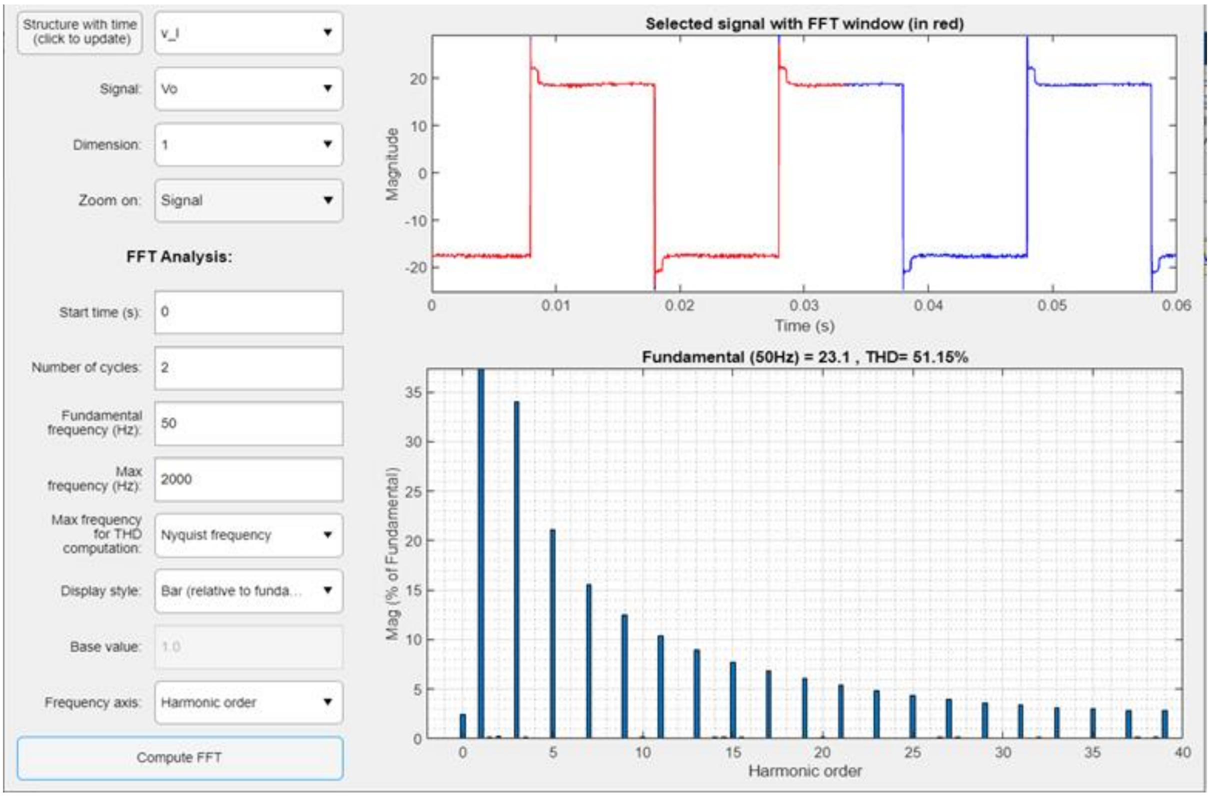


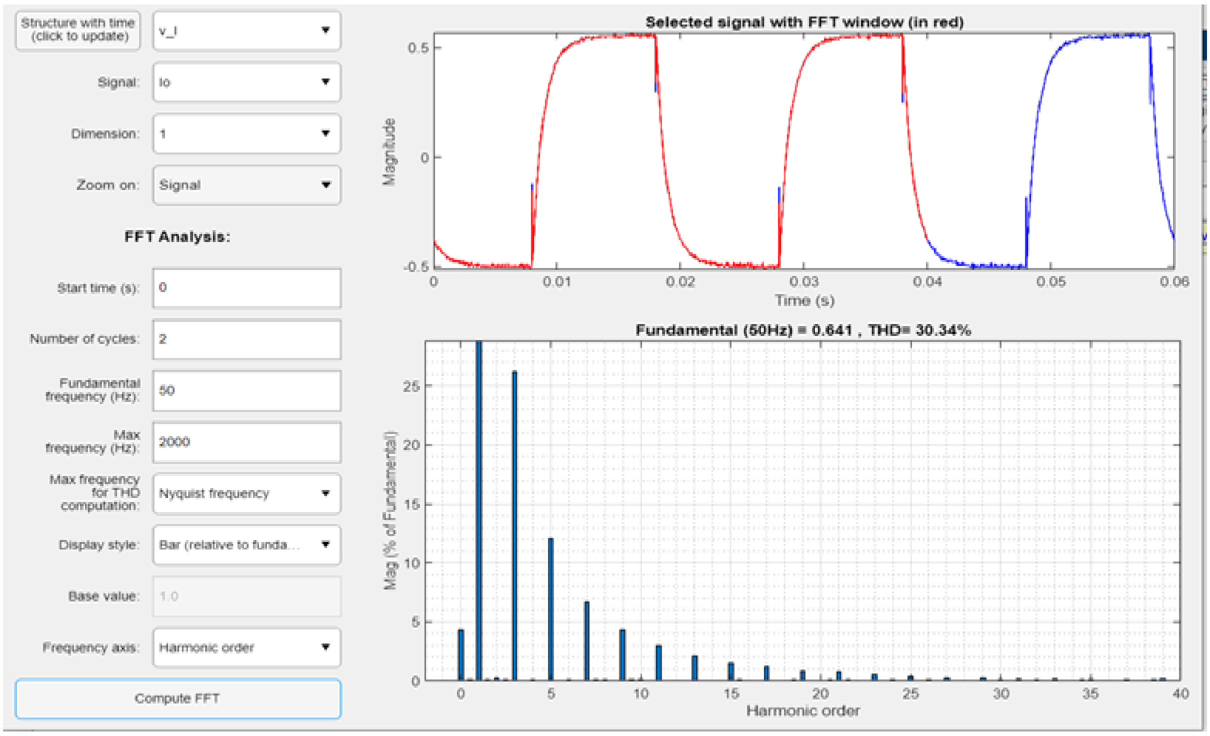


HARDWARE IN THE LAB BY USING MATLAB



FAST FOURIR (FFT)





NOTES

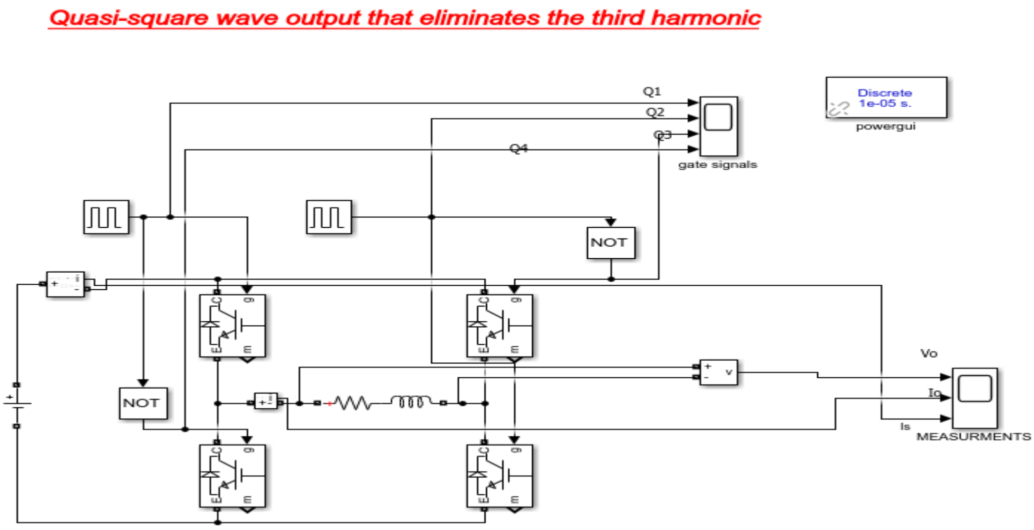
- We found some spikes in the transition between (0 +Vdc -Vdc) in the hardware, this is due to the parasitic inductance caused by wires. The parasitic inductance is an unwanted inductance effect that is unavoidably present in all real electronic devices. Parasitic inductance is caused by the magnetic field generated by the current flowing through the device, which stores and releases energy as the current changes. The parasitic inductance affects the performance of the device, especially at high frequencies, by introducing additional impedance, phase shift, and resonance
- We found that the value of the voltage just after the spikes and for a very few times is greater than the normal value at the rest of the wave, due to the voltage drop made by diode has the same polarity so it added to Vdc cause over voltage and rapidly disappear when diode become off

Quazi

Quasi-square wave output that eliminates the third harmonic

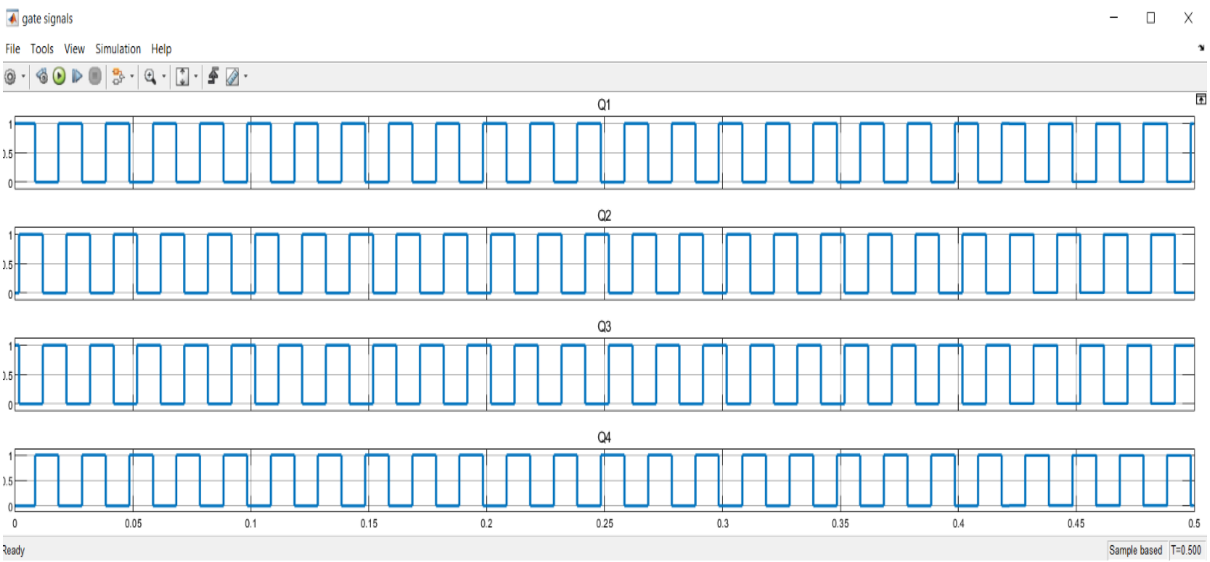
- To eliminate the third harmonic cos(3*alpha) =0

Therefore select an Alpha = 30 degreesSIMULINK model

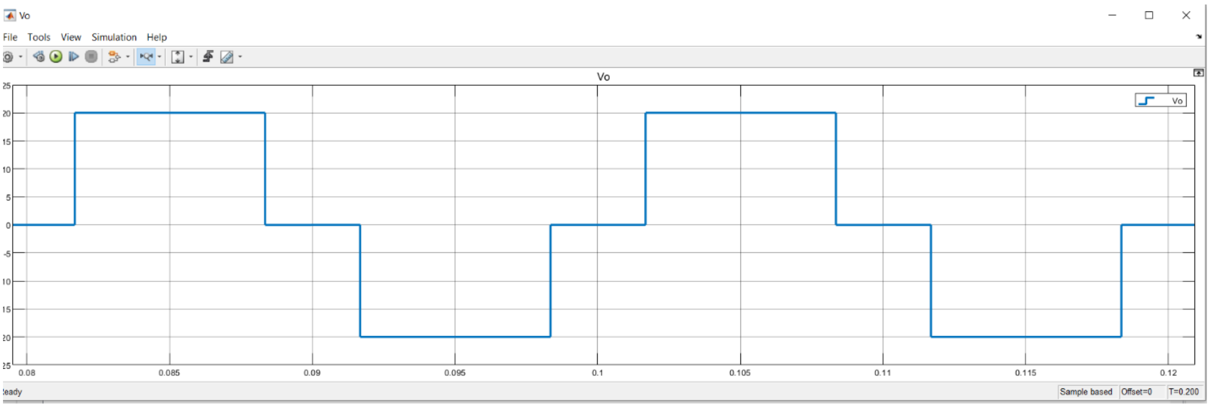


Simulation Waveforms

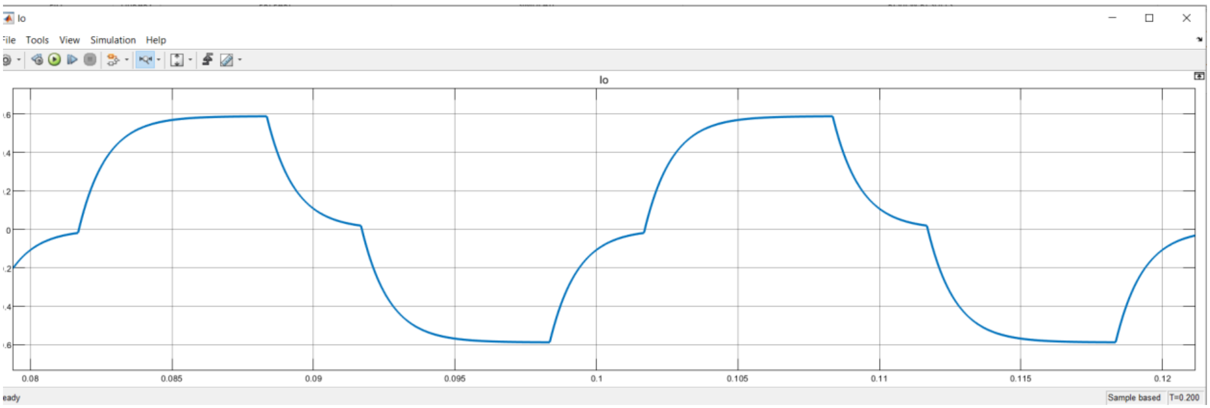
- Gate signals



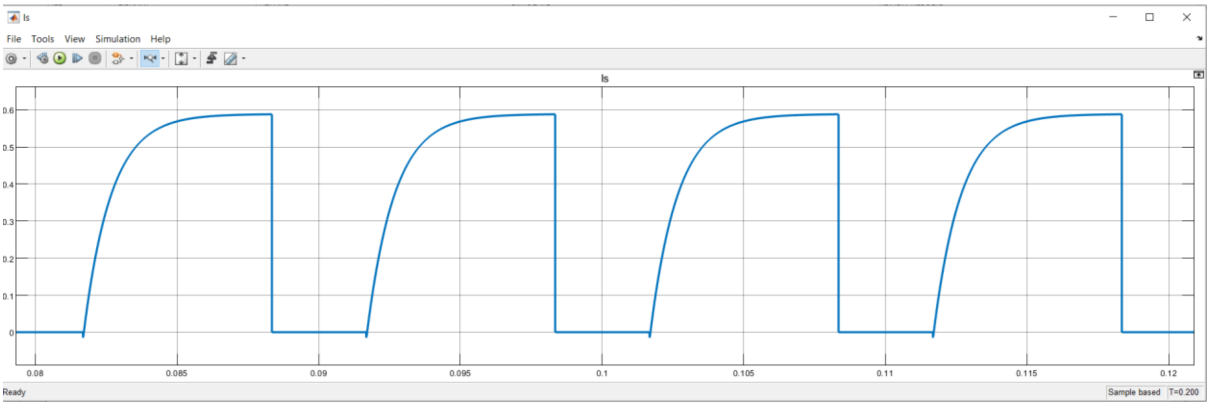
- Output Voltage



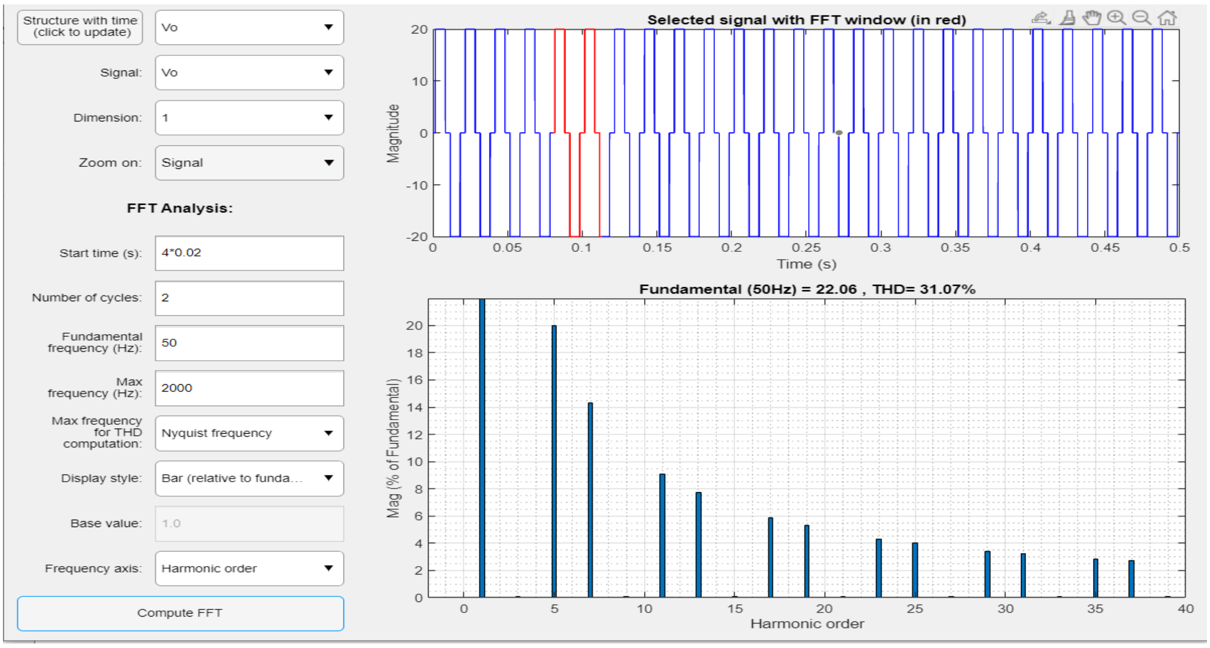
- Output current



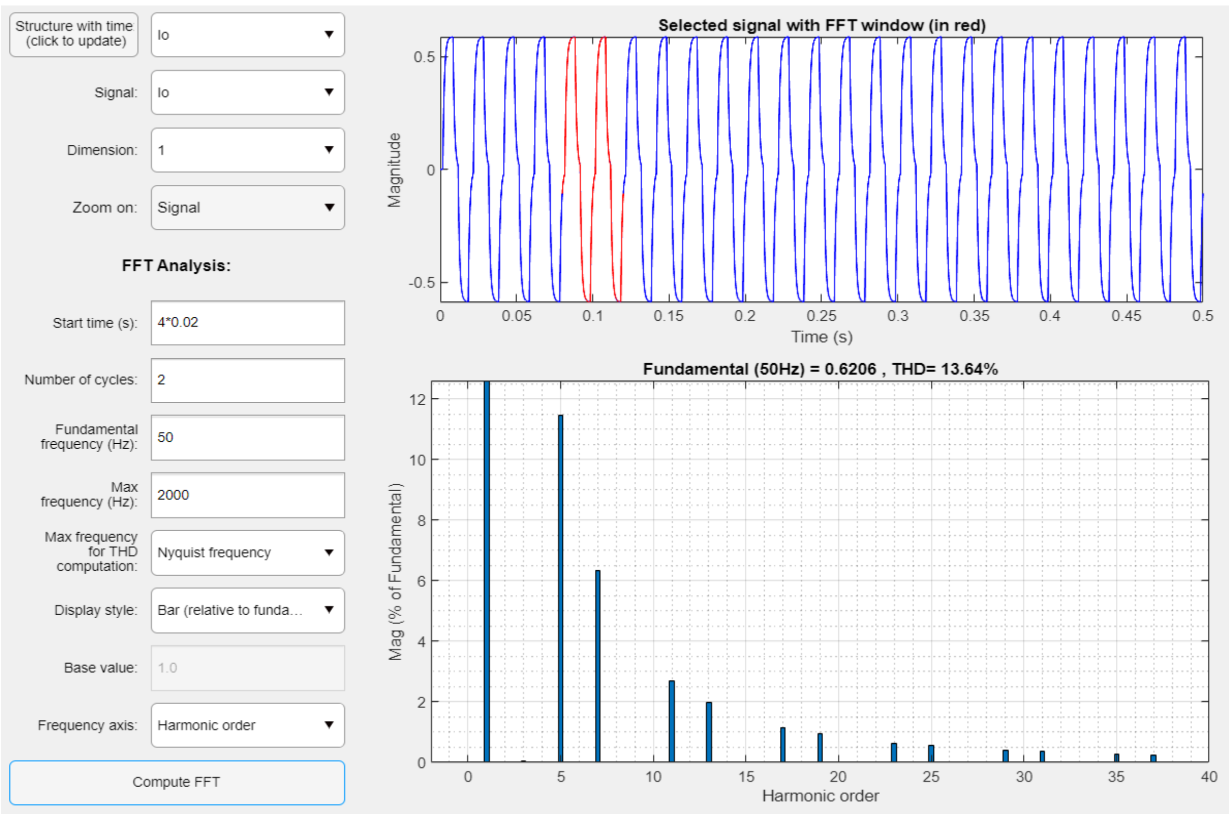
- Supply current



- # Voltage THD

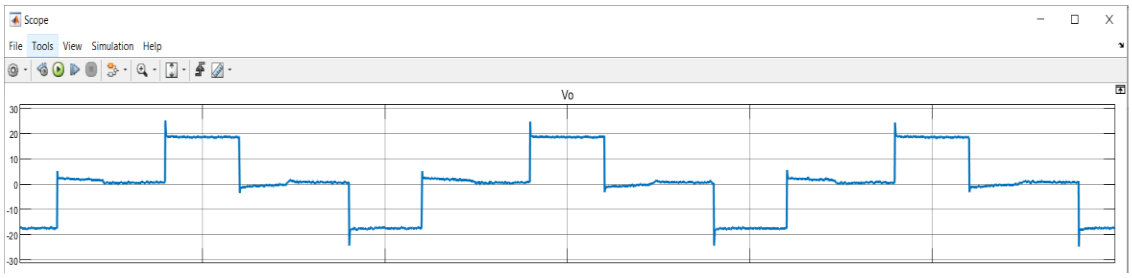


- # Current THD

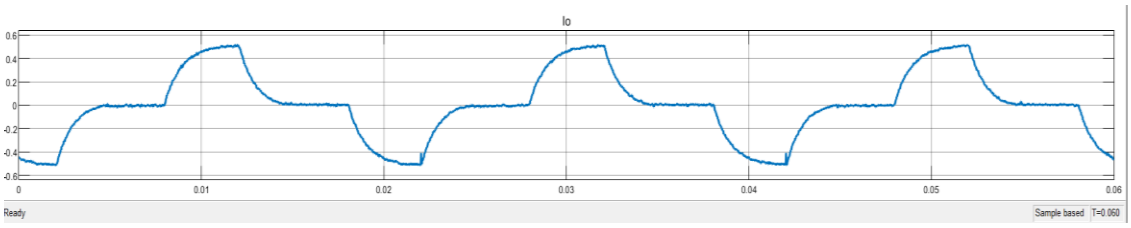


Actual Lab readings

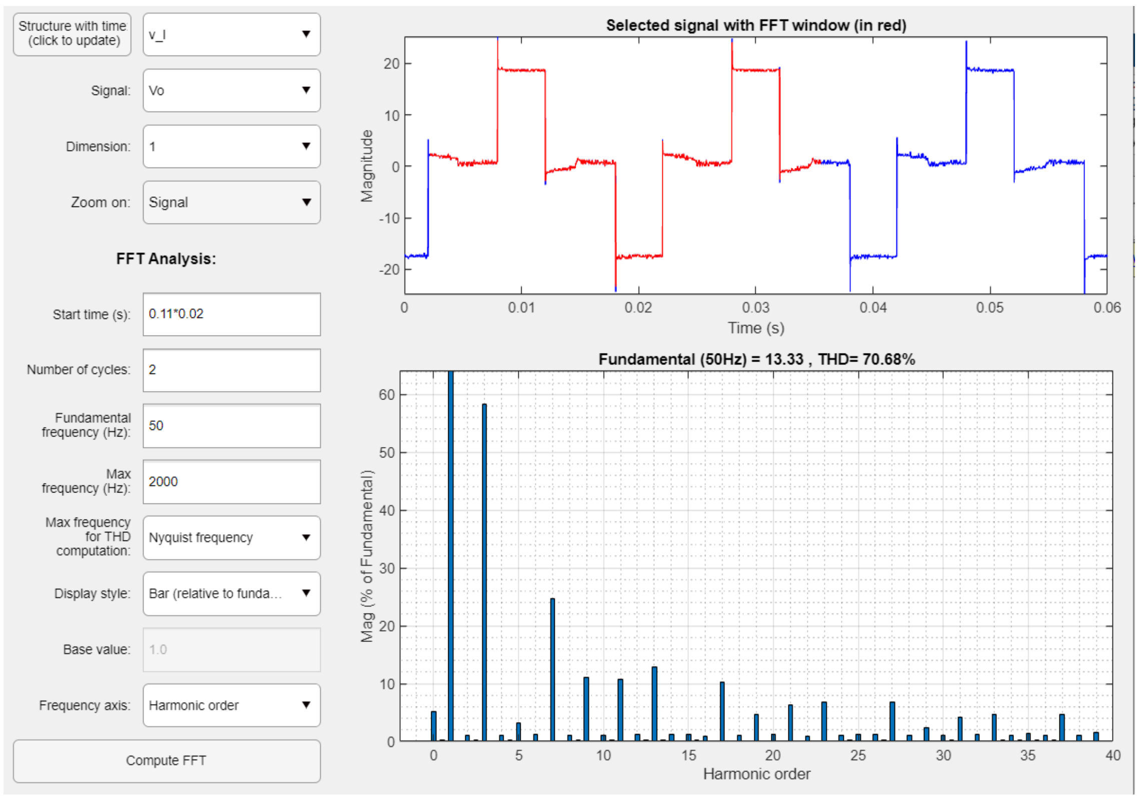
- output voltage



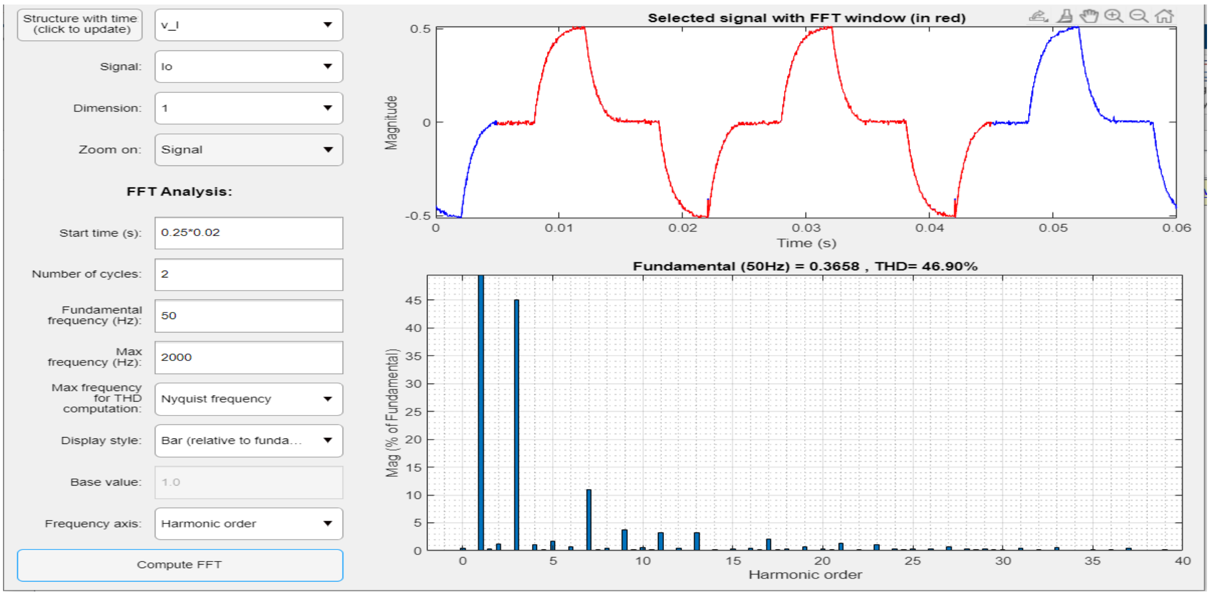
- Output current



- Voltage THD



- Current THD



Comments

- We found some spikes in the transition between (0 +Vdc -Vdc) in the hardware, this is due to the parasitic inductance caused by wires. The parasitic inductance is an unwanted inductance effect that is unavoidably present in all real electronic devices. Parasitic inductance is caused by the magnetic field generated by the current flowing through the device, which stores and releases energy as the current changes. The parasitic inductance affects the performance of the device, especially at high frequencies, by introducing additional impedance, phase shift, and resonance.

- In the model_given in the lab, we see that the inverter operate as Quazi eliminates the fifth harmonic, this is happened by cos(5*alpha) =0, this mean that (alpha=18 or 54 degree), in our case alpha = 54 degree (we know that from fundamental value) this is case a low value of fund. Component cause a very high THD_v.

Optimized PWM

First, we want to cut the signal with specific angels like :

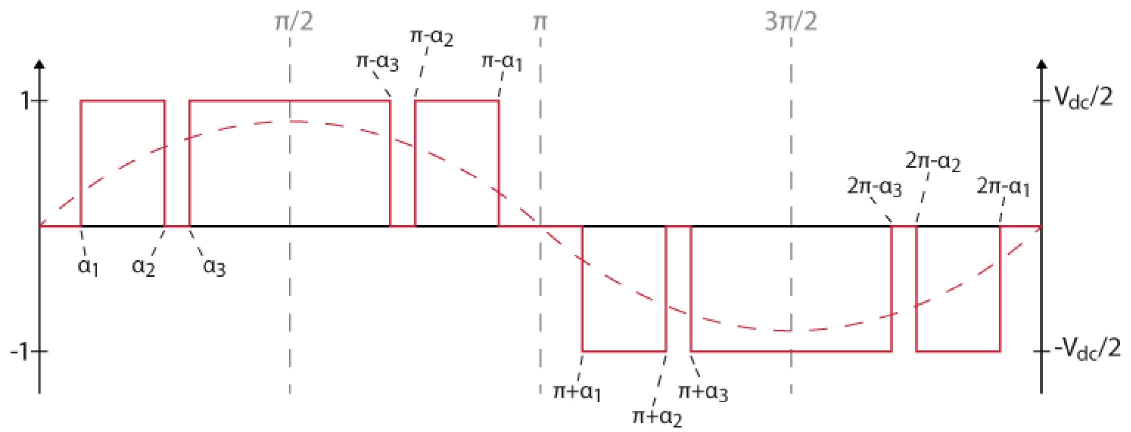


Figure 44 SHE

Matlab Code to get (alpha1 , alpha2 , alpha3)

```
F = @(x) [cosd(x(1)) - cosd(x(2)) + cosd(x(3)) - (11*sqrt(2) / ((4 * (20) ) /  pi));
         cosd(3*x(1)) - cosd(3*x(2)) + cosd(3*x(3));
         cosd(5*x(1)) - cosd(5*x(2)) + cosd(5*x(3))];

      options = optimset('Algorithm', 'trust-region-reflective');
z = fsolve(F, [10, 20, 30], options);
Alpha1 = z(1);
Alpha2 = z(2);
Alpha3=z(3);
```

Figure 46 MATLAB alphas calculating.

Alpha2	54.5868
Alpha3	70.0738
F	@(x)[cosd(x(1))-cosd...
options	1x1 struct
z	[31.8366,54.5868,70.0...

Figure 45 MATLAB workspace

- **Results**

(alpha1, alpha2, alpha3) = (31.8366 , 54.5868 , 70.073)

SIMULINK model

- we designed single phase model to eliminate the 3^{rd} and 5^{th} harmonics.

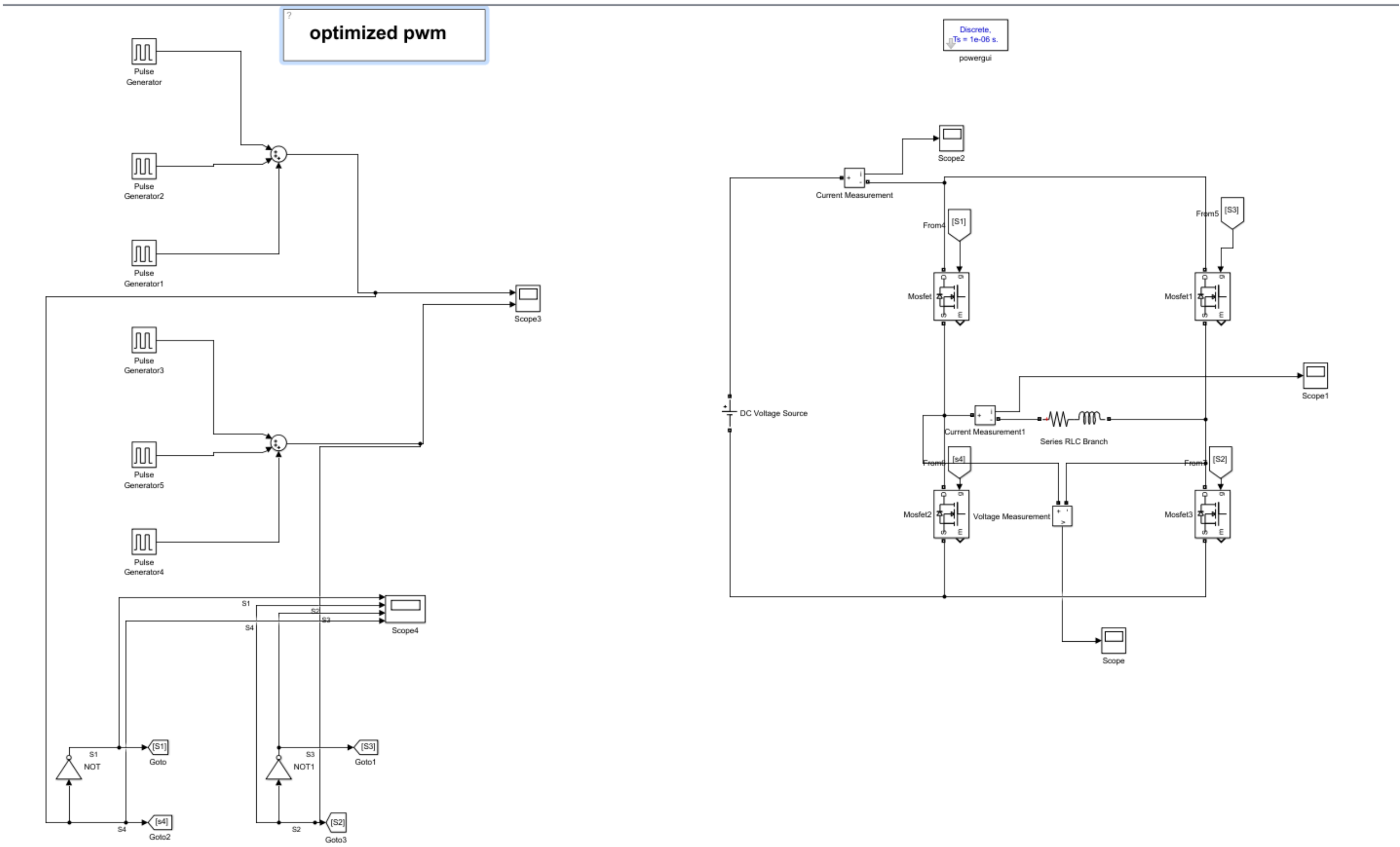


Figure 47 Model of Optimized PWM

Simulation waveforms

- The output voltage

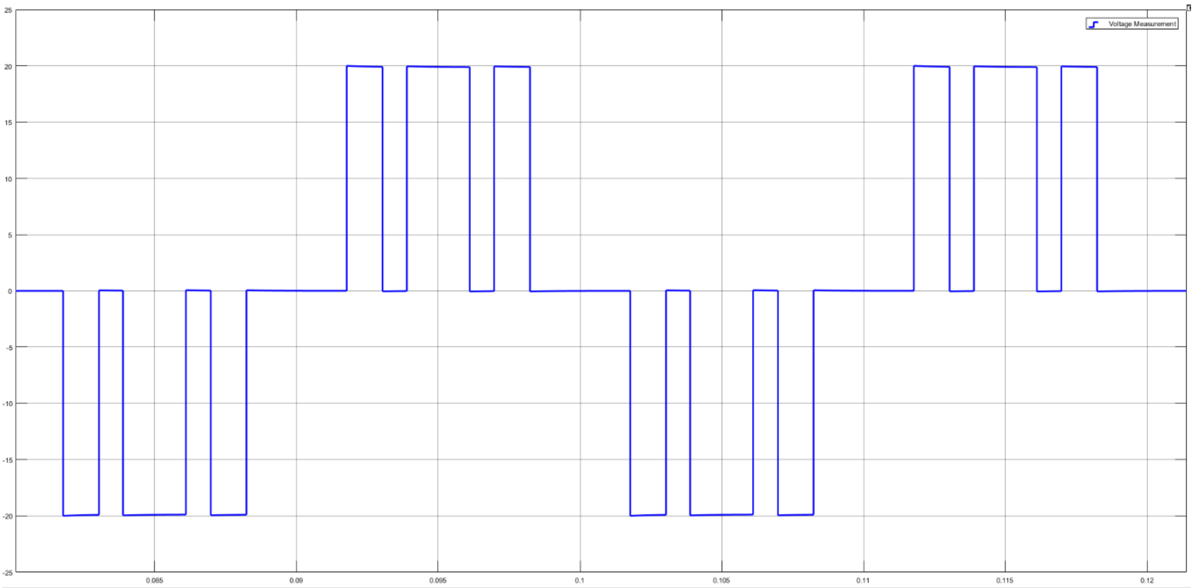


Figure 48 output voltage

- The output current:

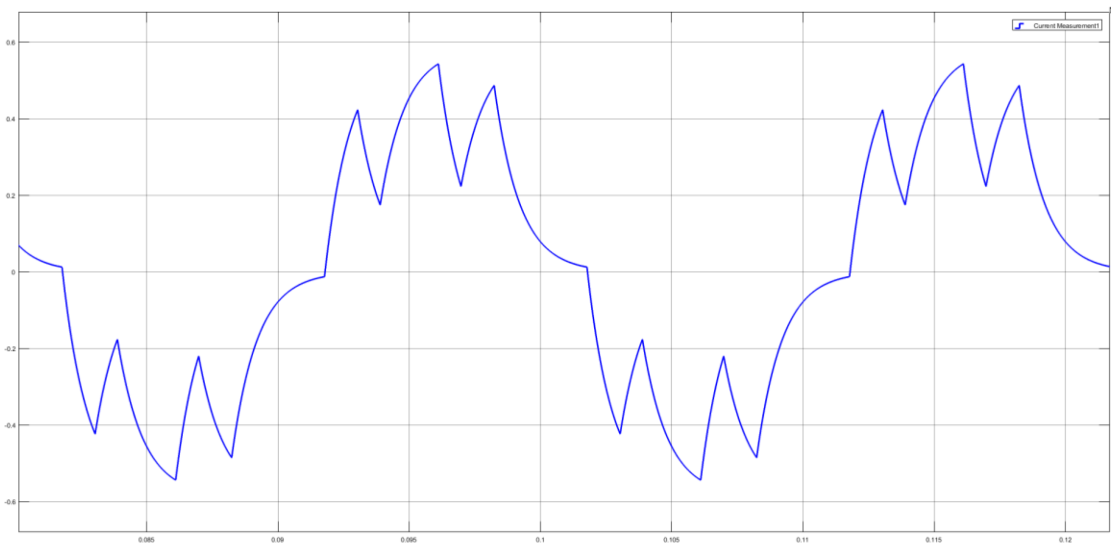


Figure 49 output Current

- Voltage THD

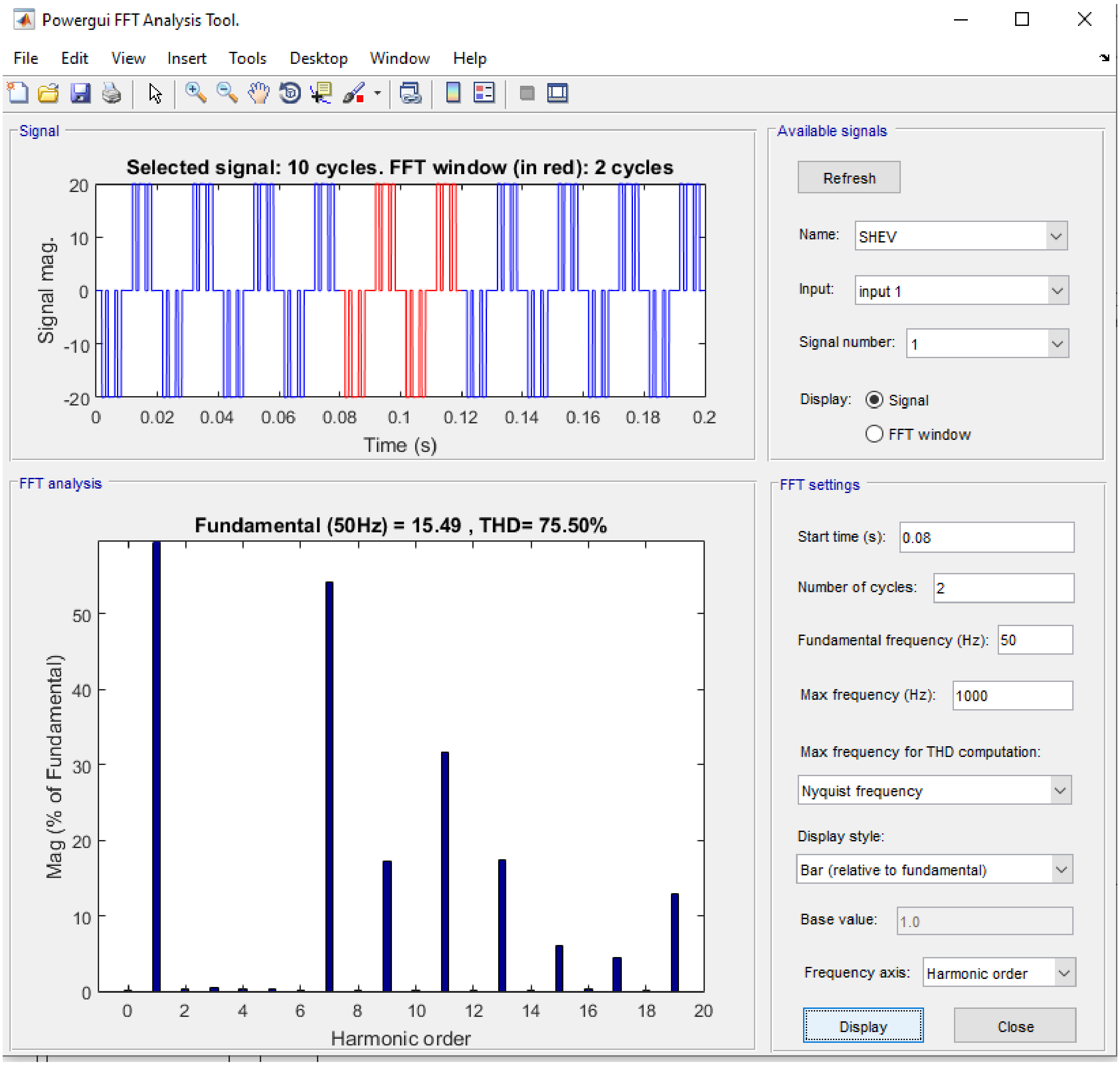


Figure 50 Voltage THD

THD for voltage = 75.50%

- Current THD

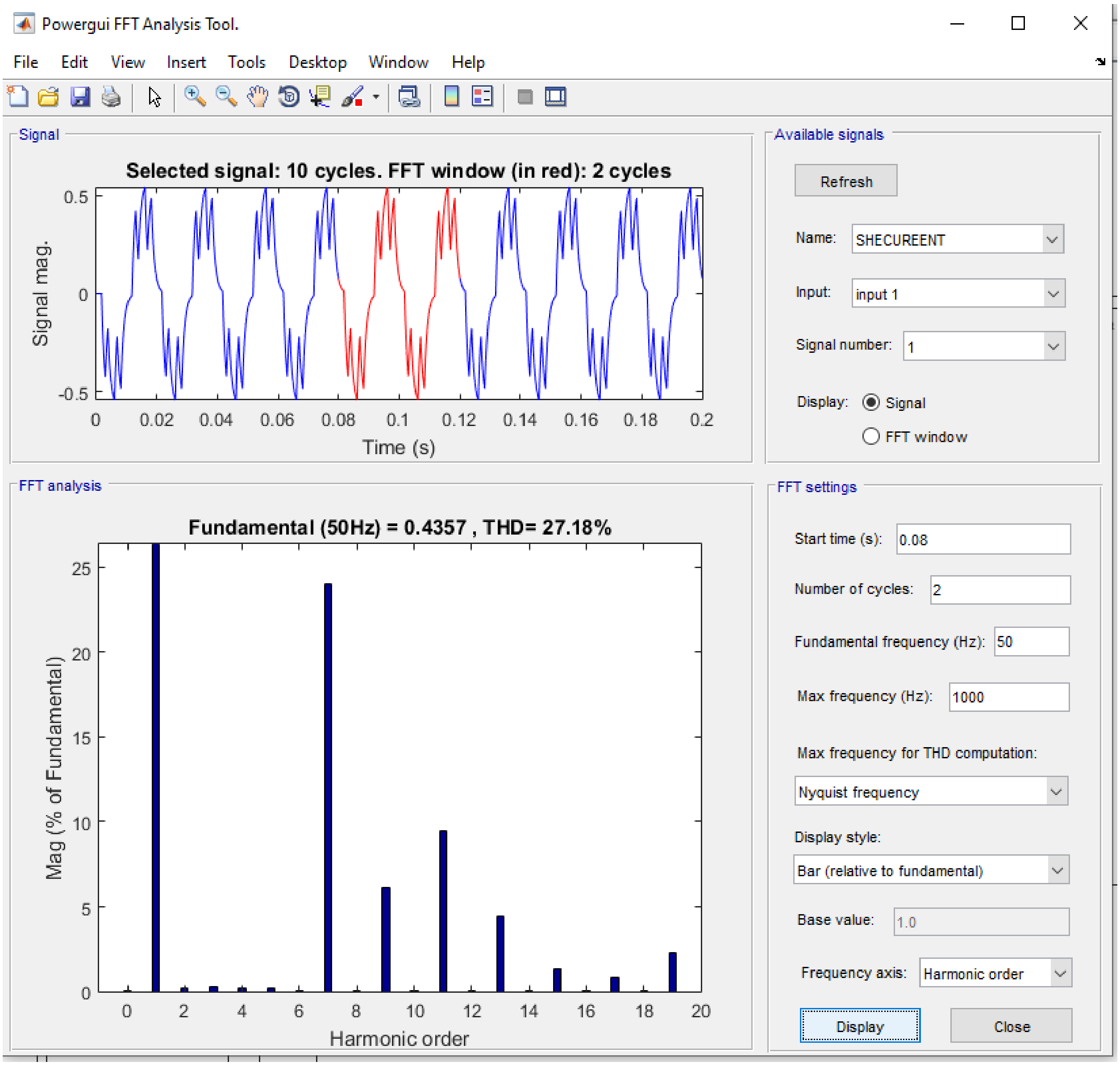


Figure 51 Current THD

THD for current = 27.18%

Actual Readings

As we see we could remove the 3rd and 5th harmonic using our design

We compared MATLAB results with hardware results , so we used signal builder on MATLAB to draw the excel sheet data as a signal.

- Lab Voltage THD

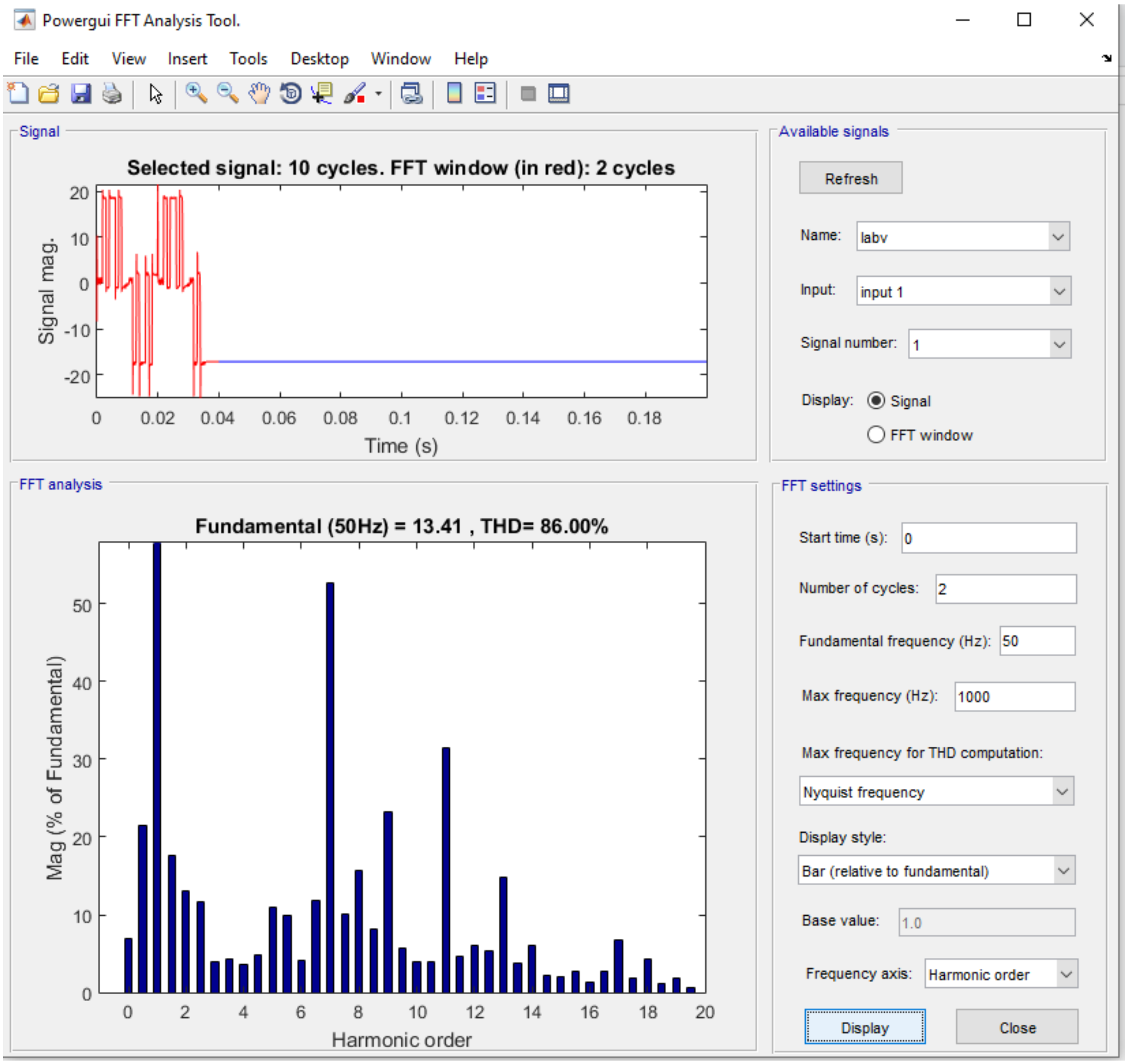
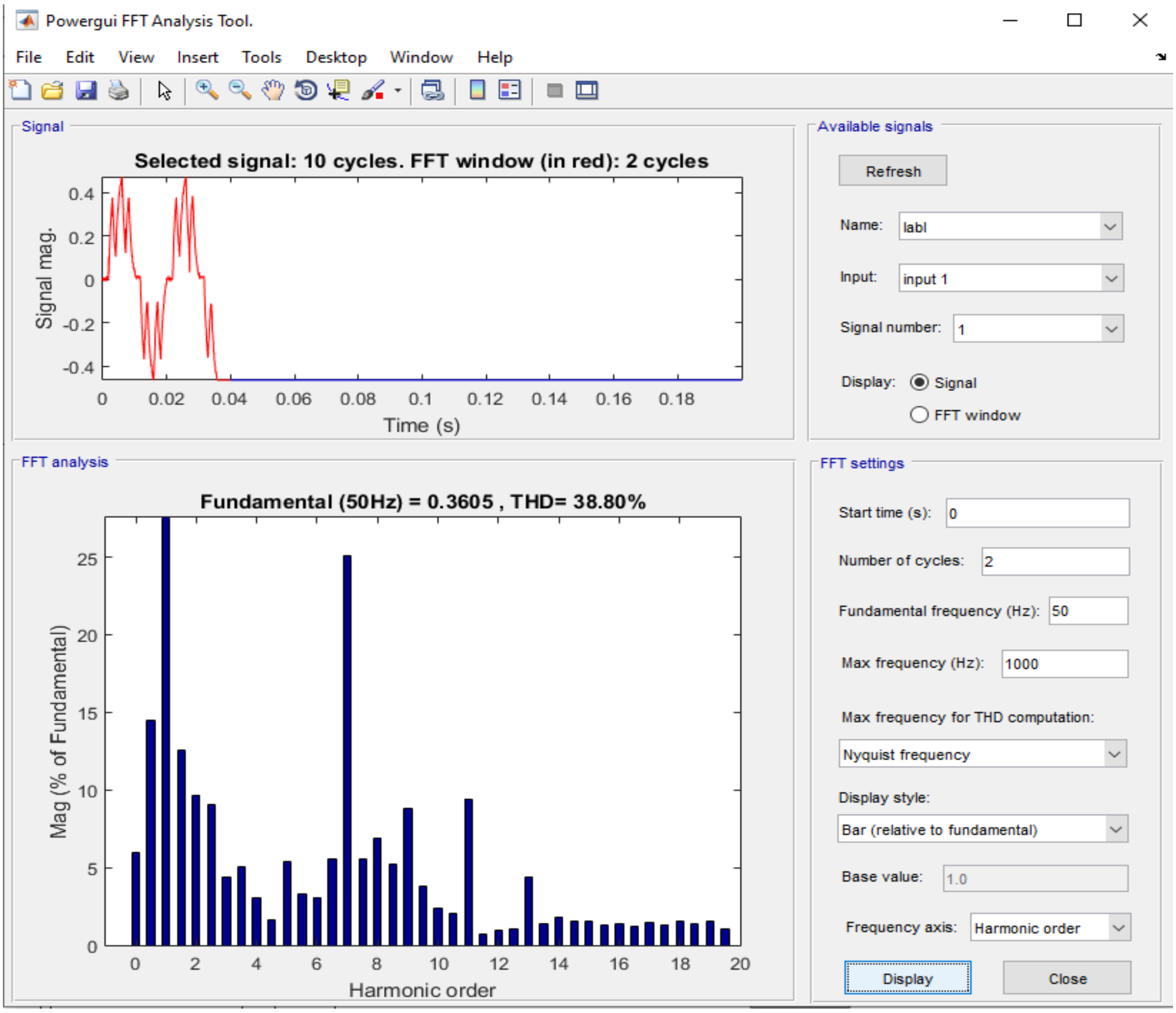


Figure 52 Voltage THD

THD for lab voltage = 86%

- Lab current THD



THD for current = 38.80%

Figure 53 Current THD

<u>**Comments**</u>:

1. We could remove 3rd and 5th harmonics using the MATLAB model.
2. THD for lab readings > THD for the model due to the hardware losses, voltage spikes due to parasitic and voltage drop
3. In the hardware we couldn't remove harmonics, but we minimized it.

Multilevel

SIMULINK model

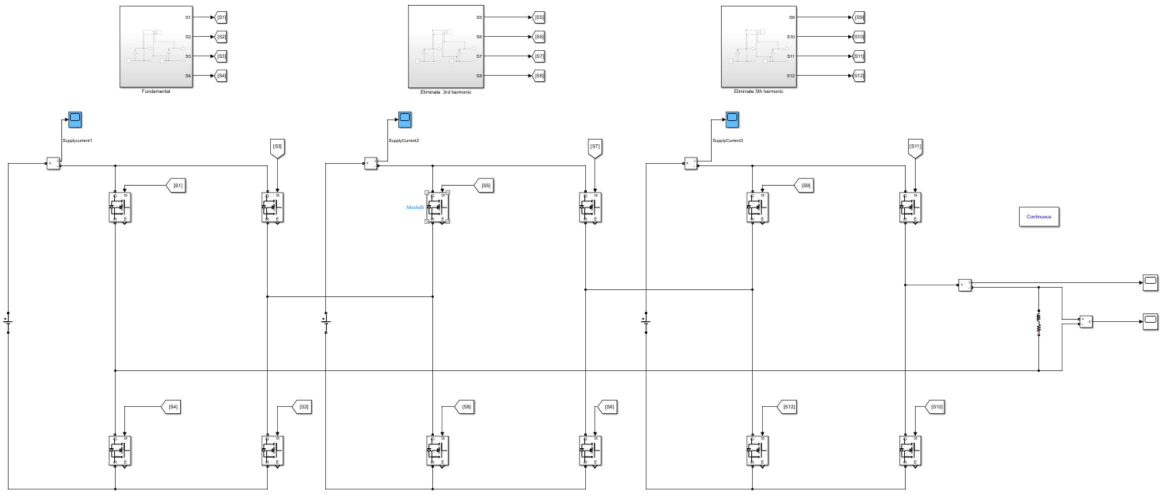


Figure 54 multilevel model

Simulation waveforms

- **Gate signal 1**

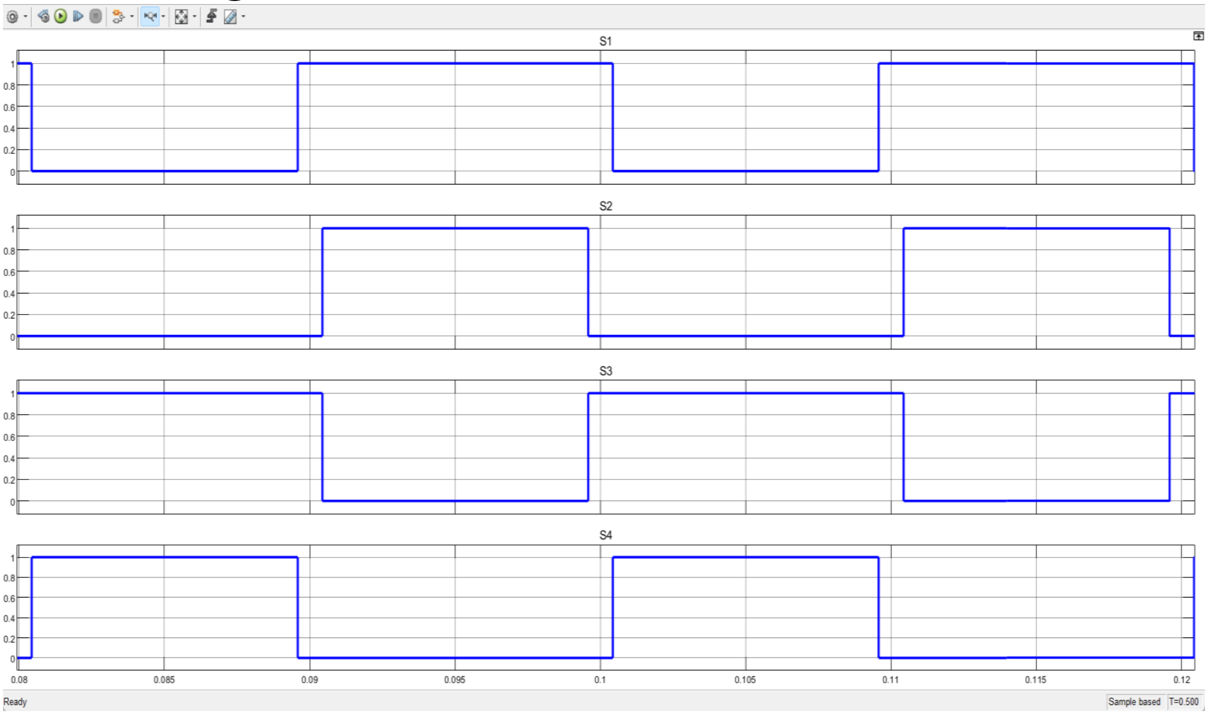


Figure 55 gate signal 1

- **Gate signal 2**

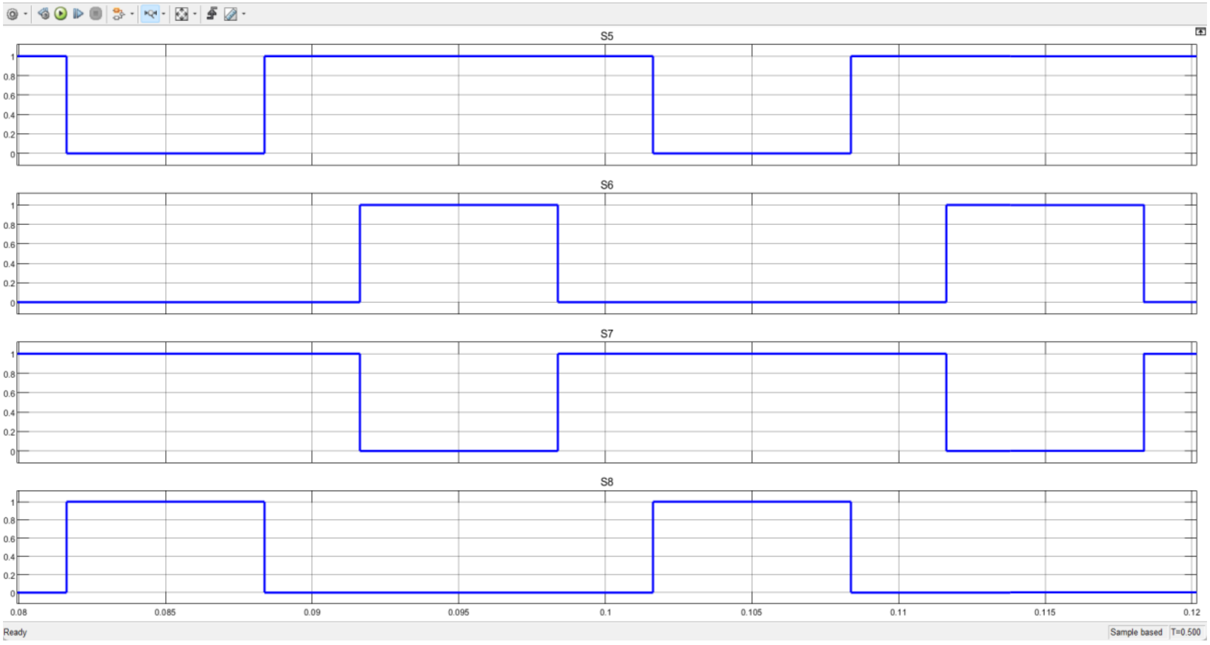


Figure 56 gate signal 2

- **Gate signal 3**

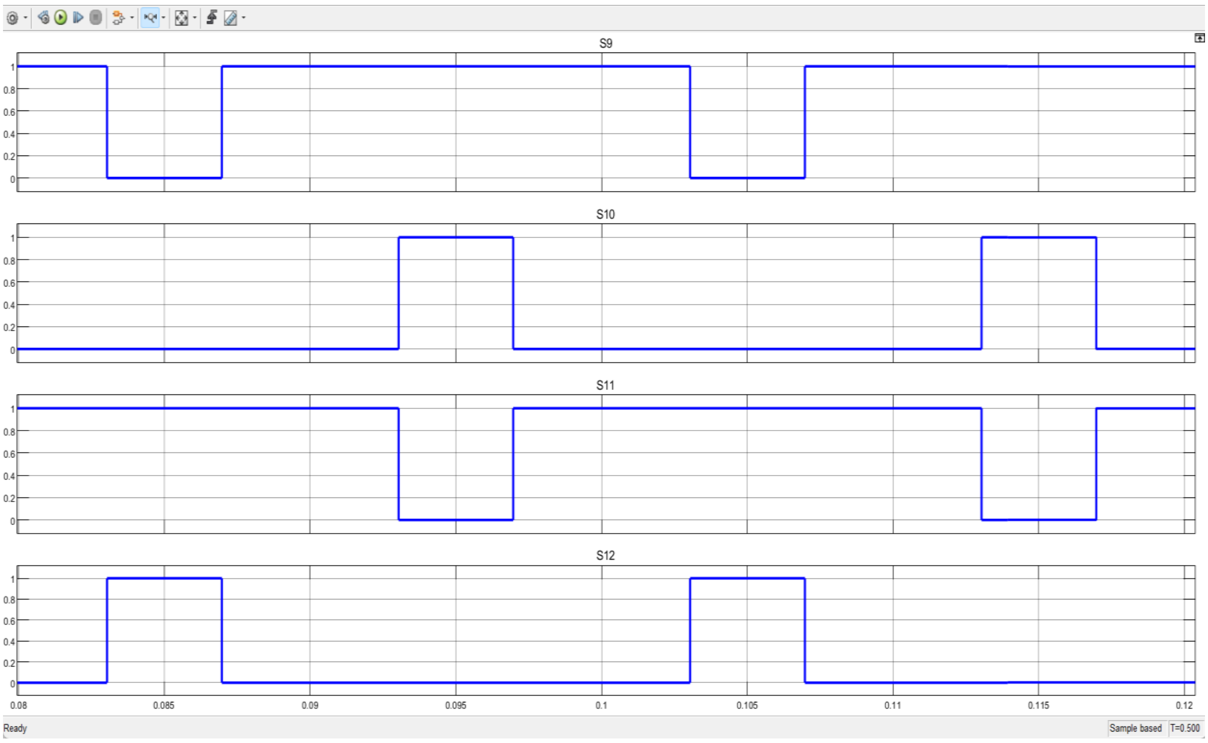


Figure 57 gate signal 3

- **Load voltage**

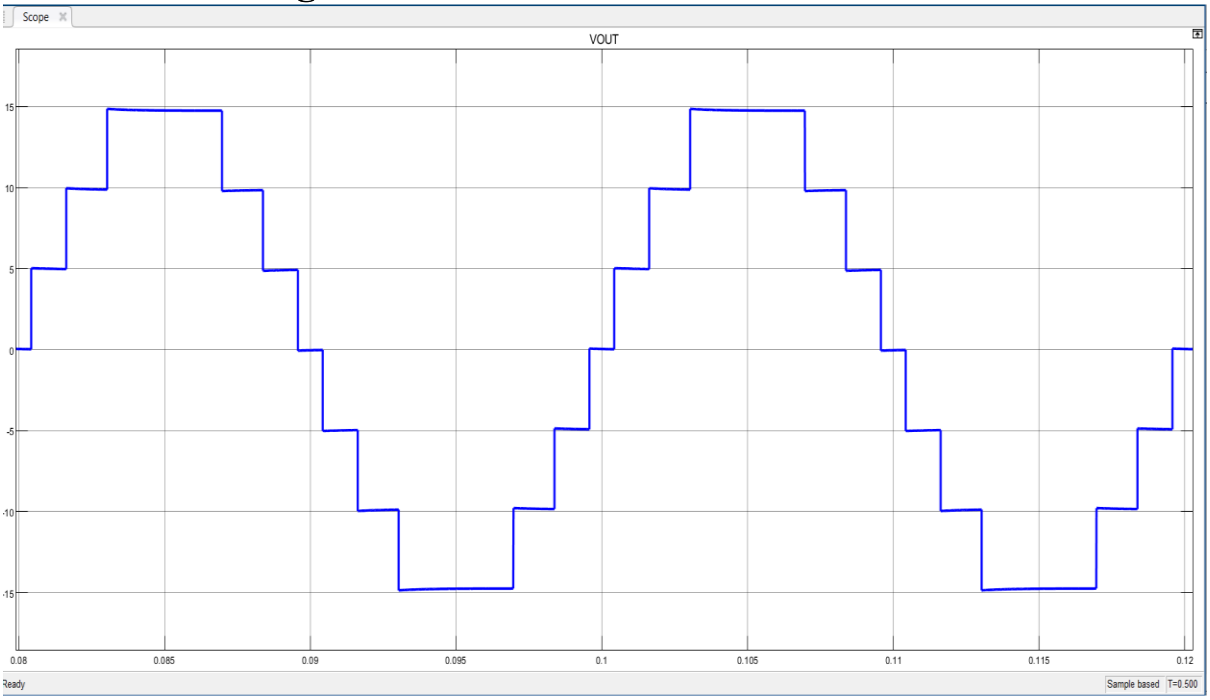


Figure 58 output voltage

- **Load current**

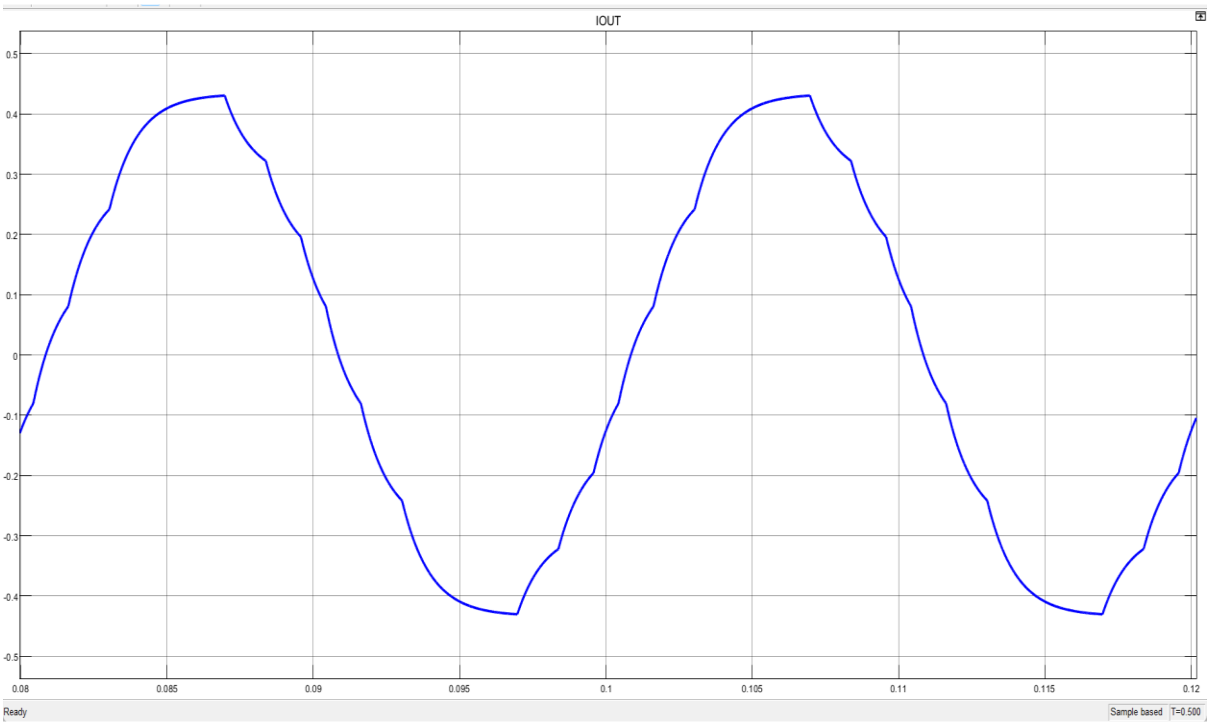


Figure 59 output current

- **Supply current 1**

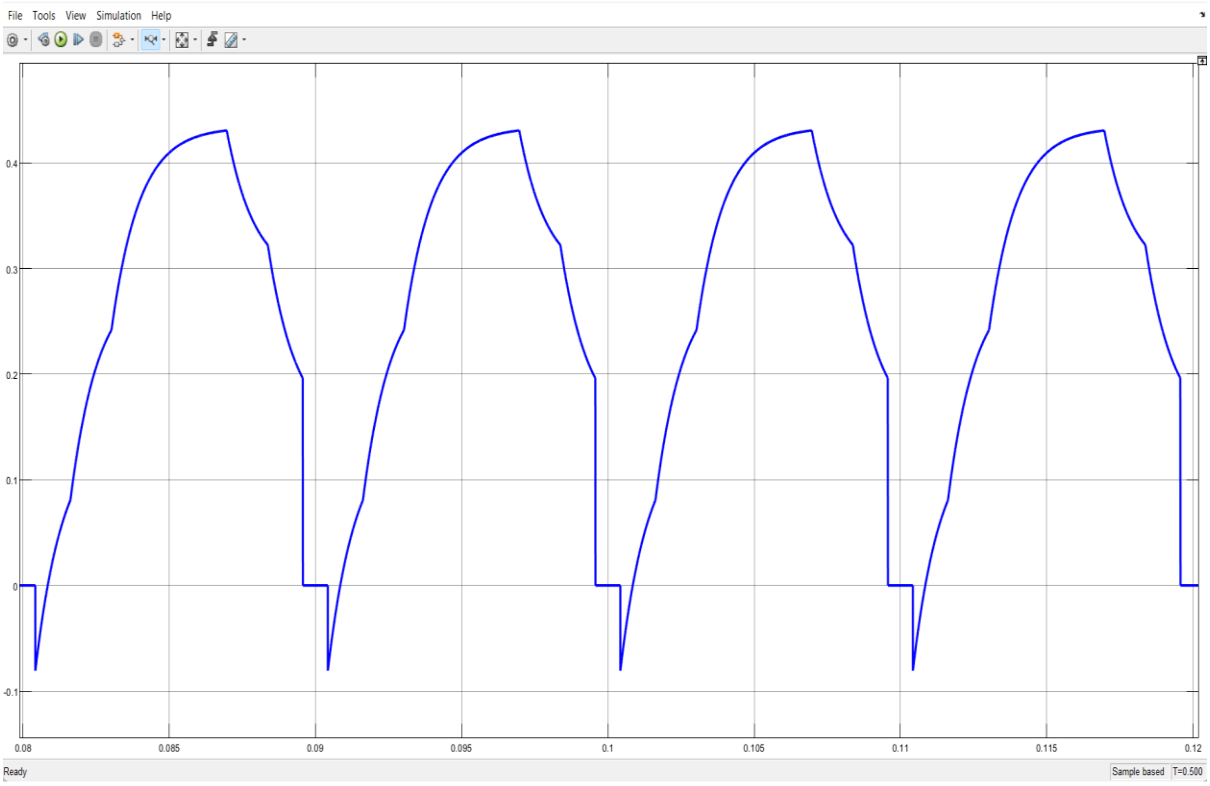


Figure 60 supply current 1

- **Supply current 2**

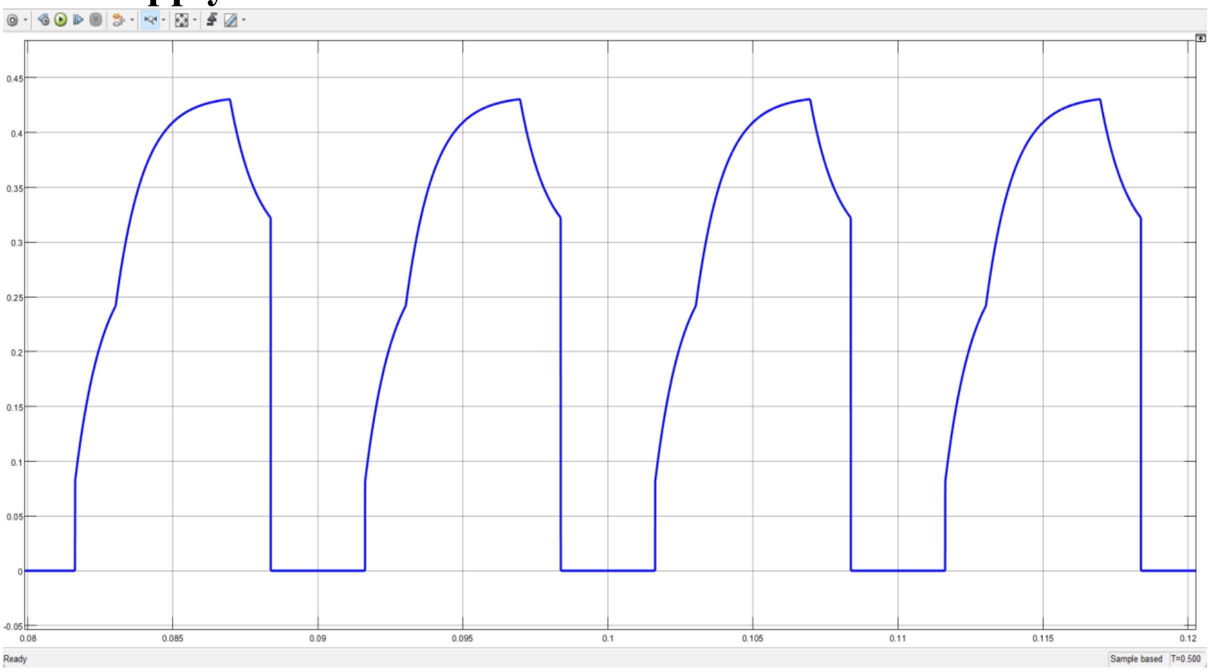


Figure 61 supply current 2

- **Supply current 3**

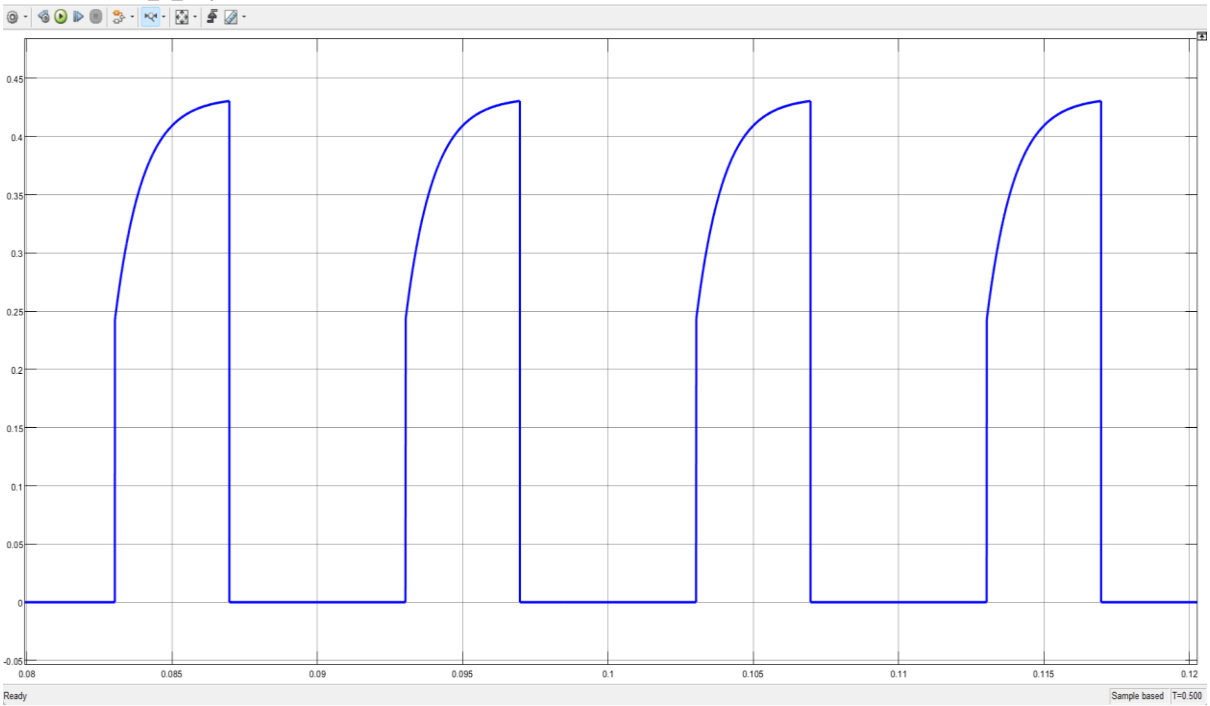


Figure 62 supply current 3

- **THD of the voltage**

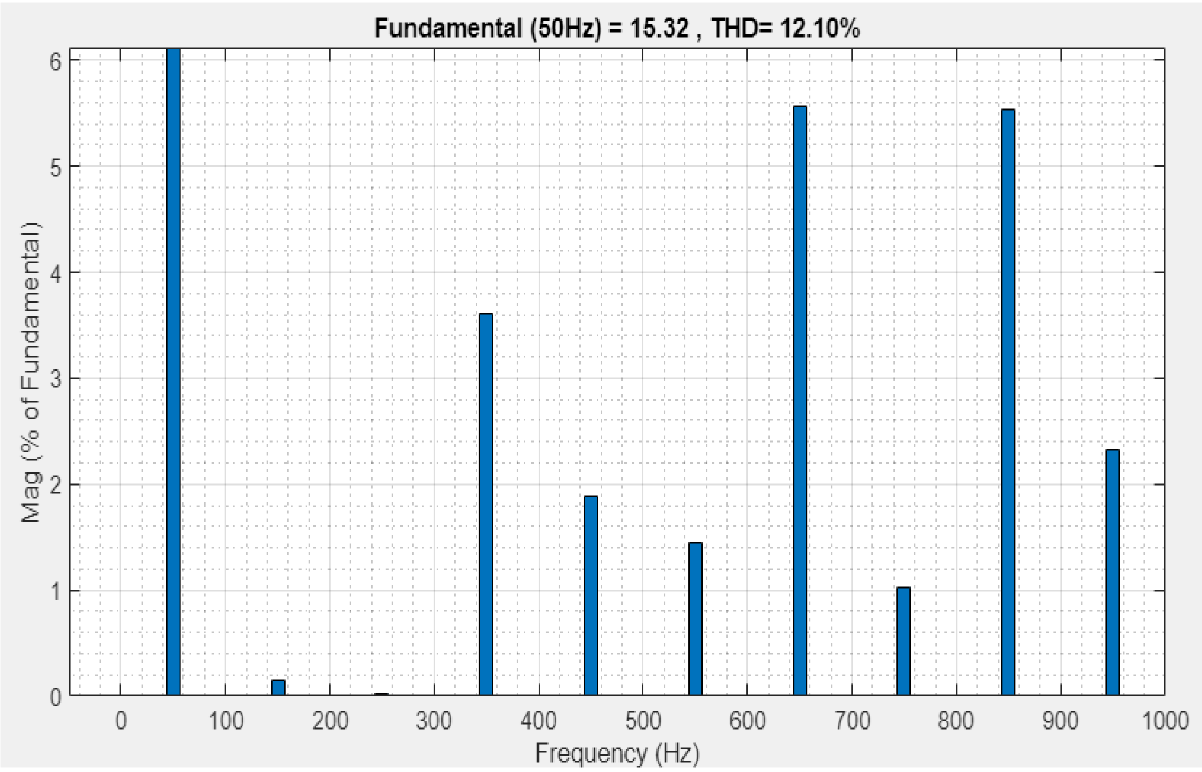


Figure 63 THD of voltage

- **THD of the current**

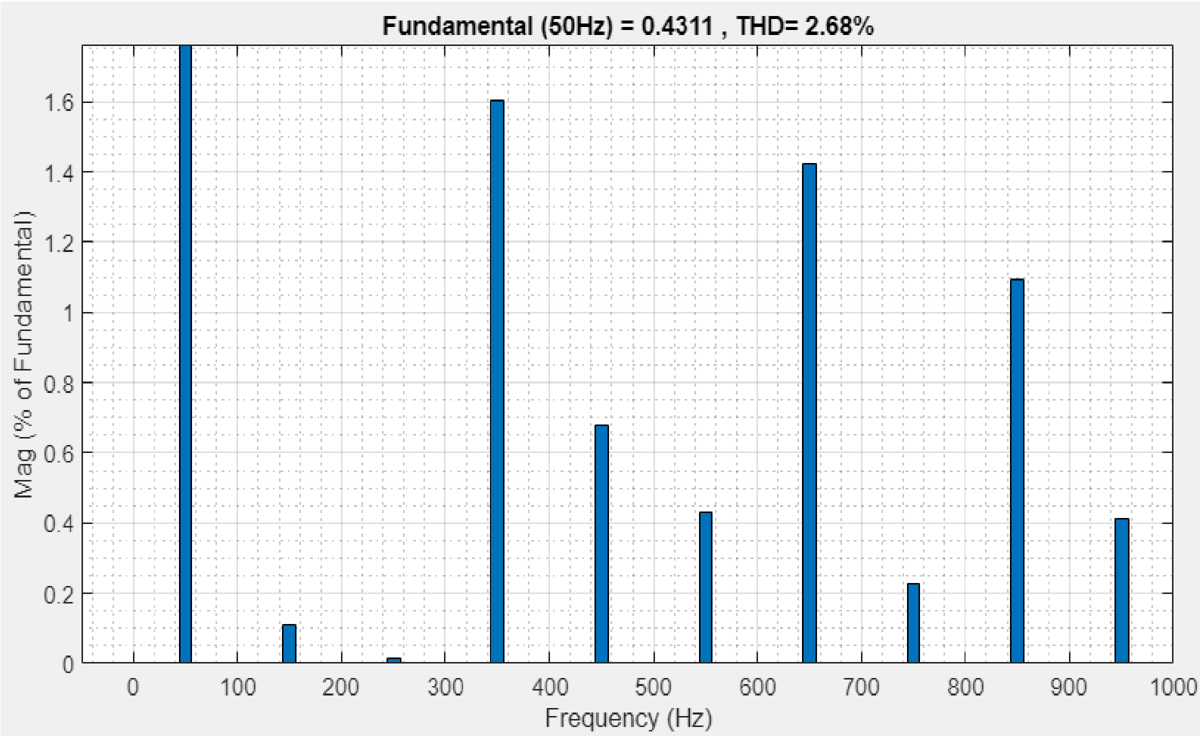


Figure 64 THD of current

- **Matlab code of Alpha calculations**

```
clear
clc
syms a b c
A1 = (4*5/pi)*(cos(a)+cos(b)+cos(c)) == 11*sqrt(2);
A2 = (4*5/(3*pi))*(cos(3*a)+cos(3*b)+cos(3*c)) == 0;
A3 = (4*5/(5*pi))*(cos(5*a)+cos(5*b)+cos(5*c)) == 0;
S = solve([A1,A2,A3],[a,b,c], 'Real' , true);
alpha1 = (S.a)*(180/pi)
alpha2 = (S.b)*(180/pi)
alpha3 = (S.c)*(180/pi)
%............%Results%................%
% alpha1 = 7.67
% alpha2 = 29.25
% alpha3 = 55.5
```

Figure 65 matlab code of alpha

Bipolar Technique

the bipolar PWM technique in a single-phase inverter leading to a more accurate representation of the desired sinusoidal waveform and minimizing harmonic content. In this method we use only one sine wave reference comparing it with sawtooth carrier to make gate signals

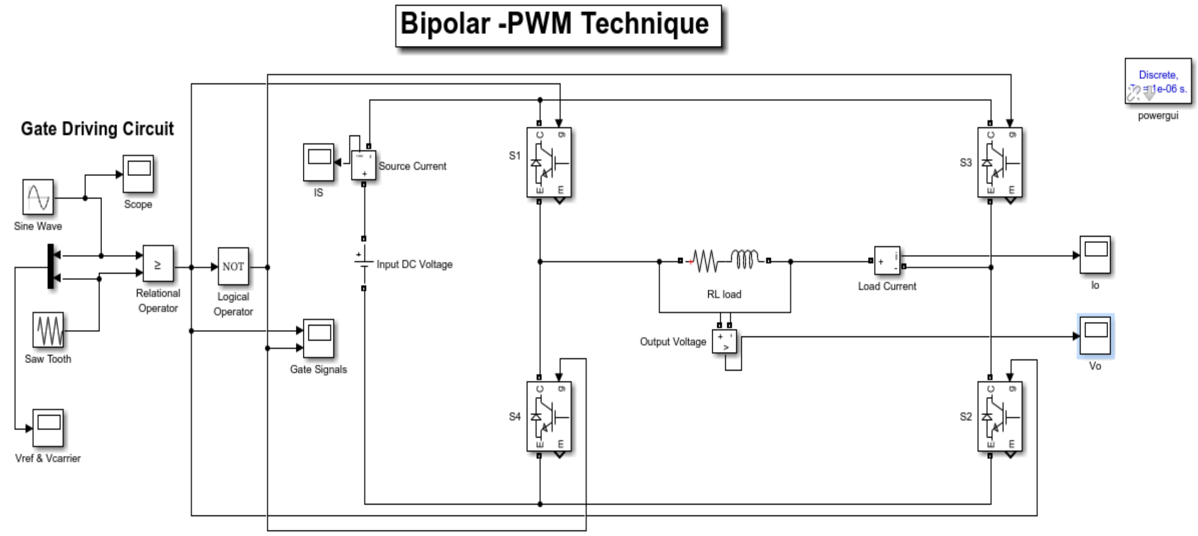


Figure 66 Model of Bipolar Technique

setting inputs

Take $f_{ref} = 50\ HZ$, and it's better to take m_f as odd number.

So, Take $m_f = 201$, $\therefore f_{sw} = 10050\ HZ$

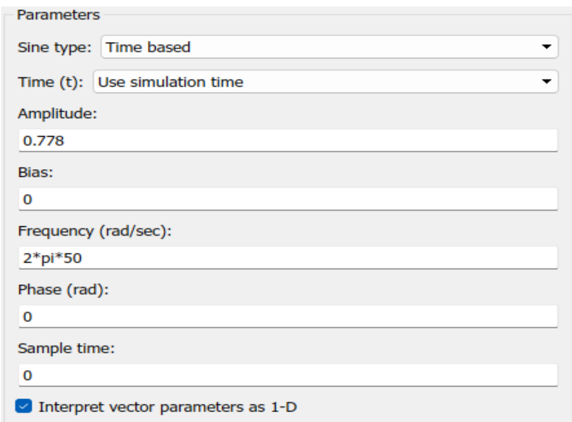


Figure 67 Parameter of reference in "Bipolar"

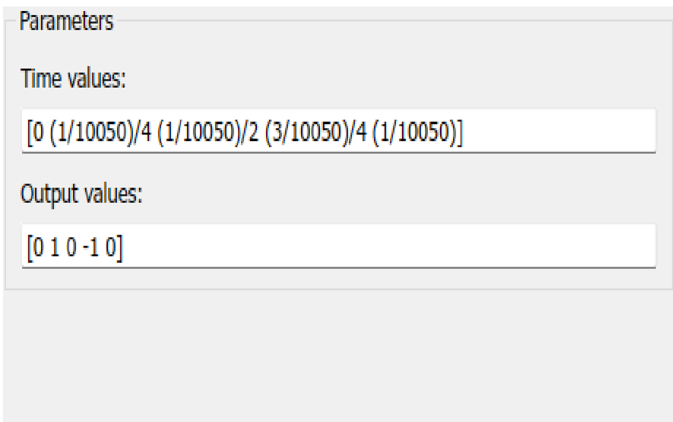


Figure 68 parameter of Saw tooth in "Bipolar".

Simulation Waveforms

- **Gate Signals**

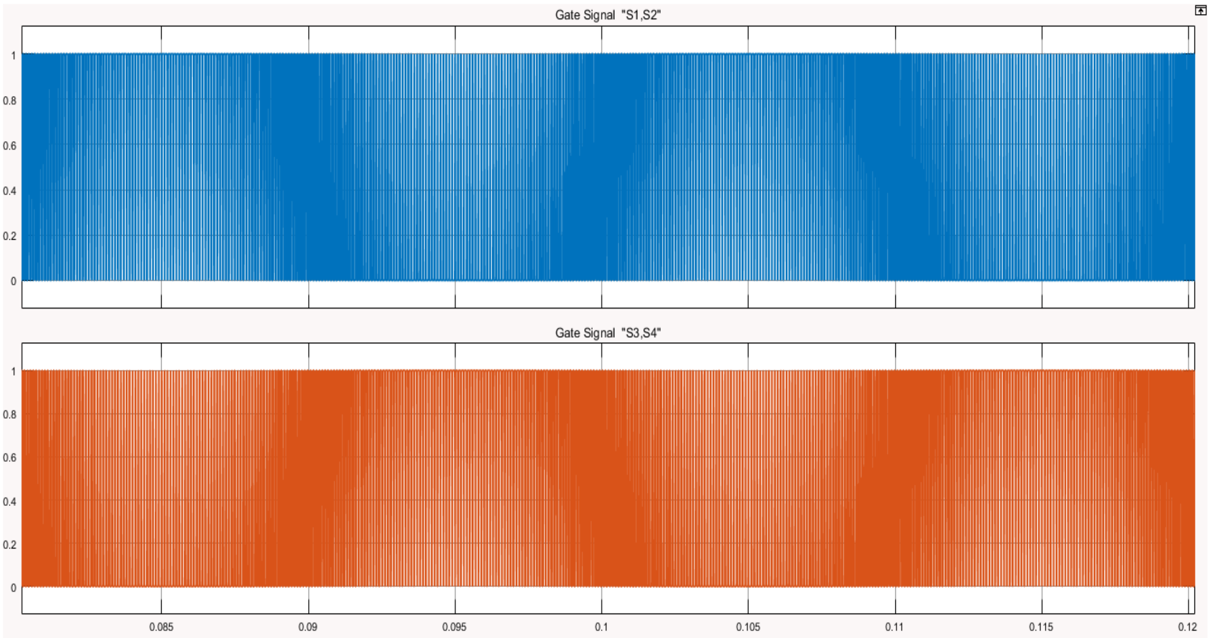


Figure 69 Gate Signal in "Bipolar"

- **Reference vs Carrier**

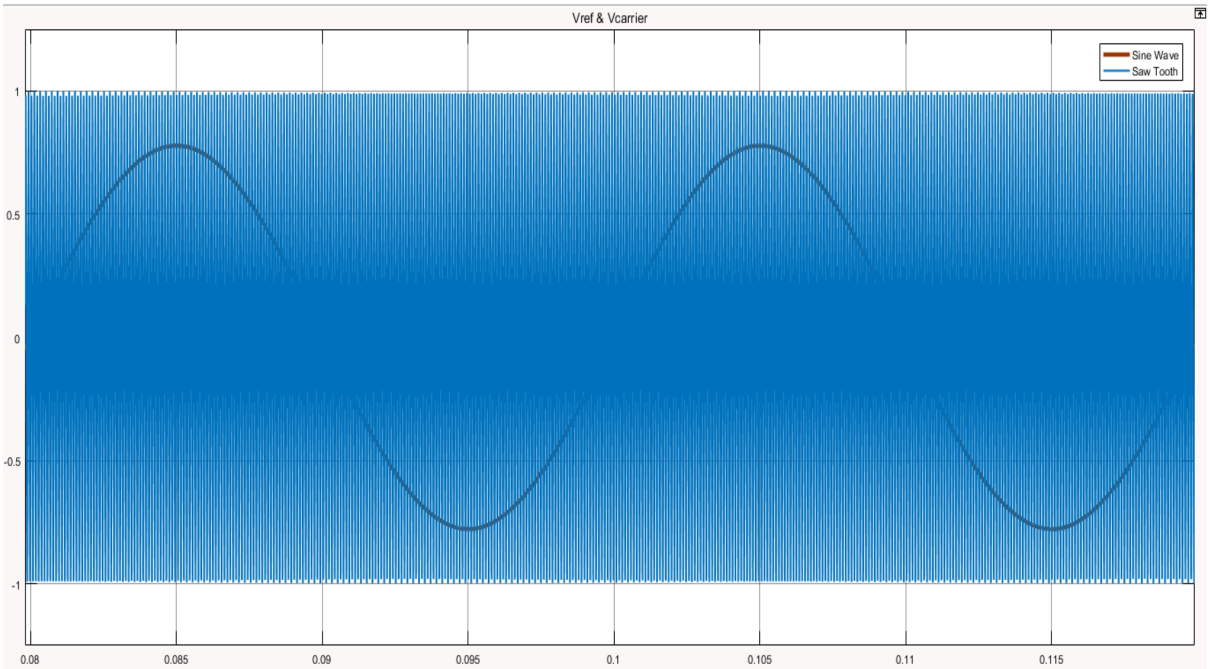


Figure 70 Reference vs Carrier in "Bipolar"

- **Source Current**

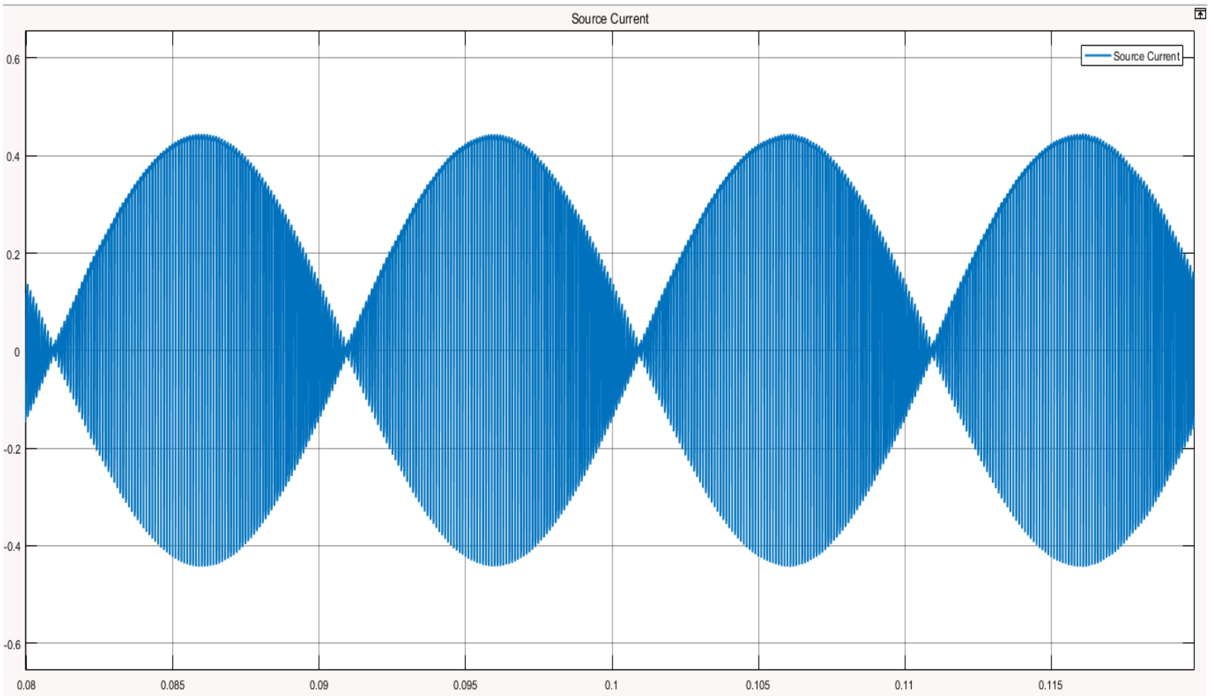


Figure 71 Source current in "Bipolar"

- **Load Current**

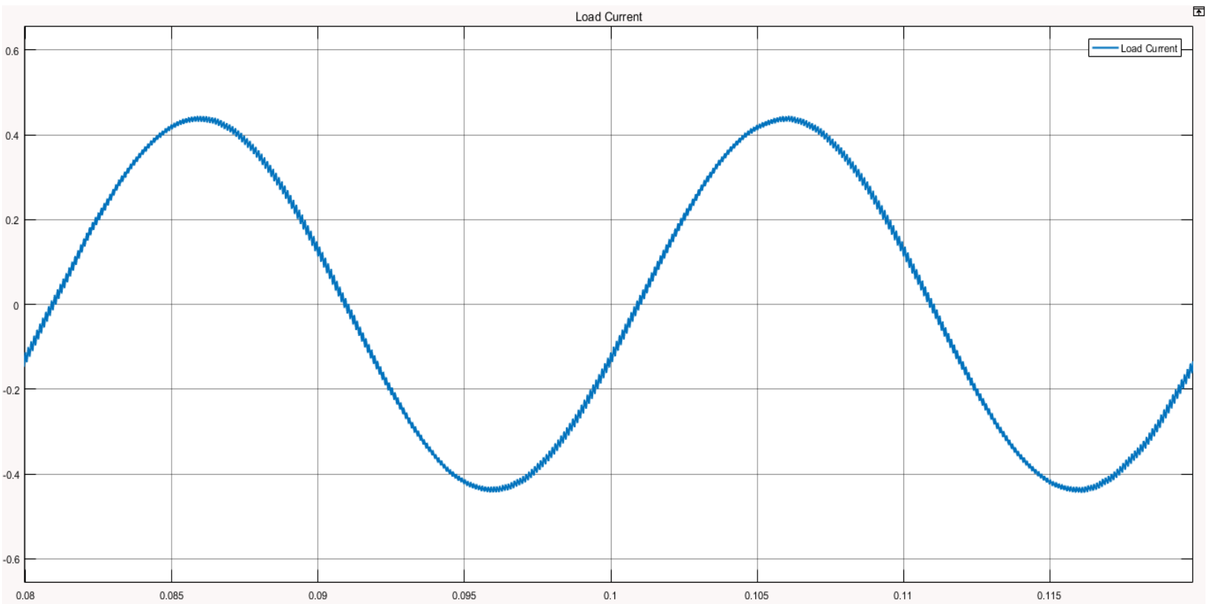


Figure 72 Load Current in "Bipolar"

- **Load Voltage**

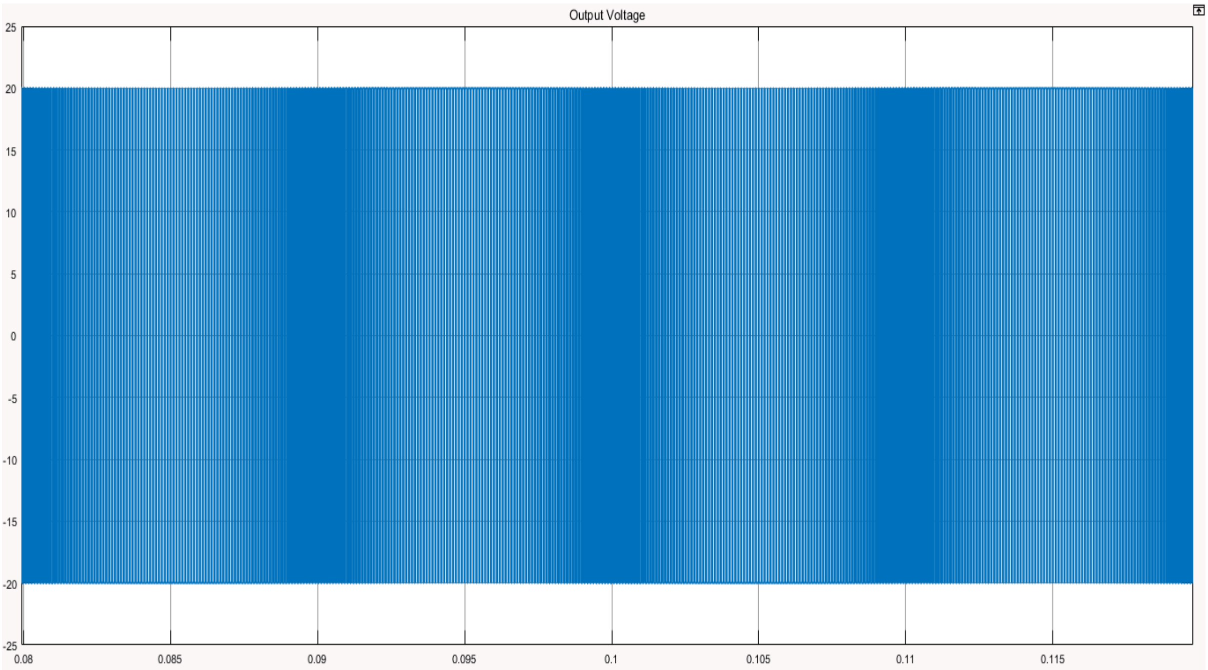


Figure 73 Load Voltage in "Bipolar"

Actual Reading

- **Output Current**

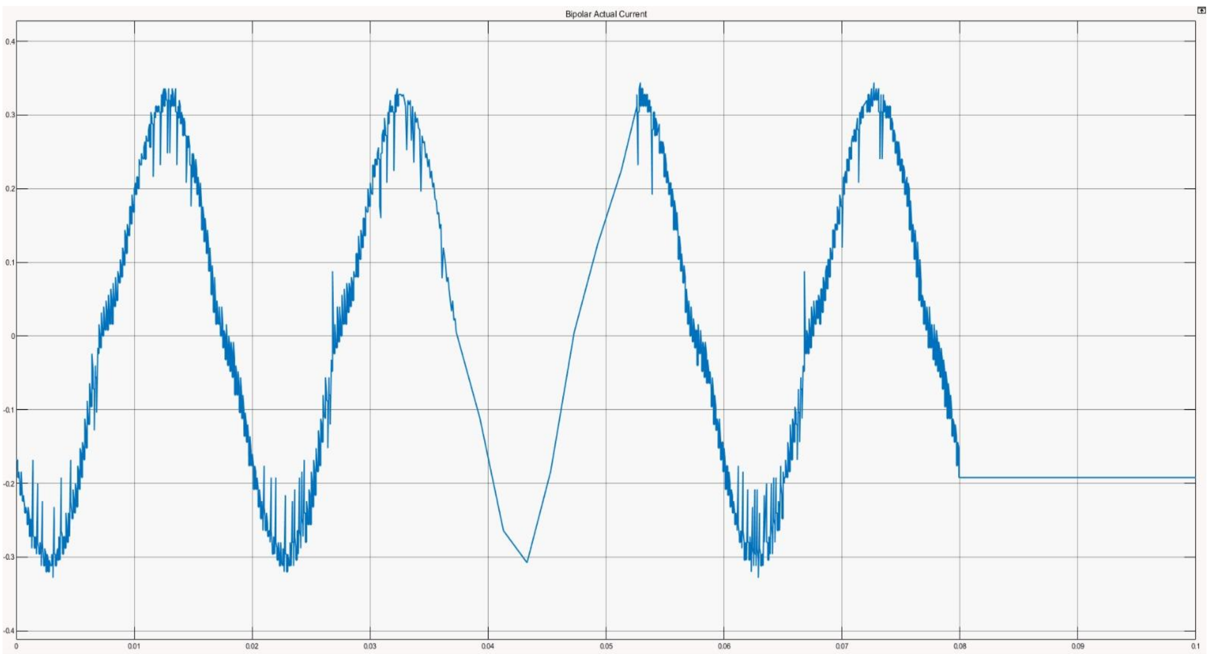


Figure 74 Actual Current "Bipolar"

- **Output Voltage**

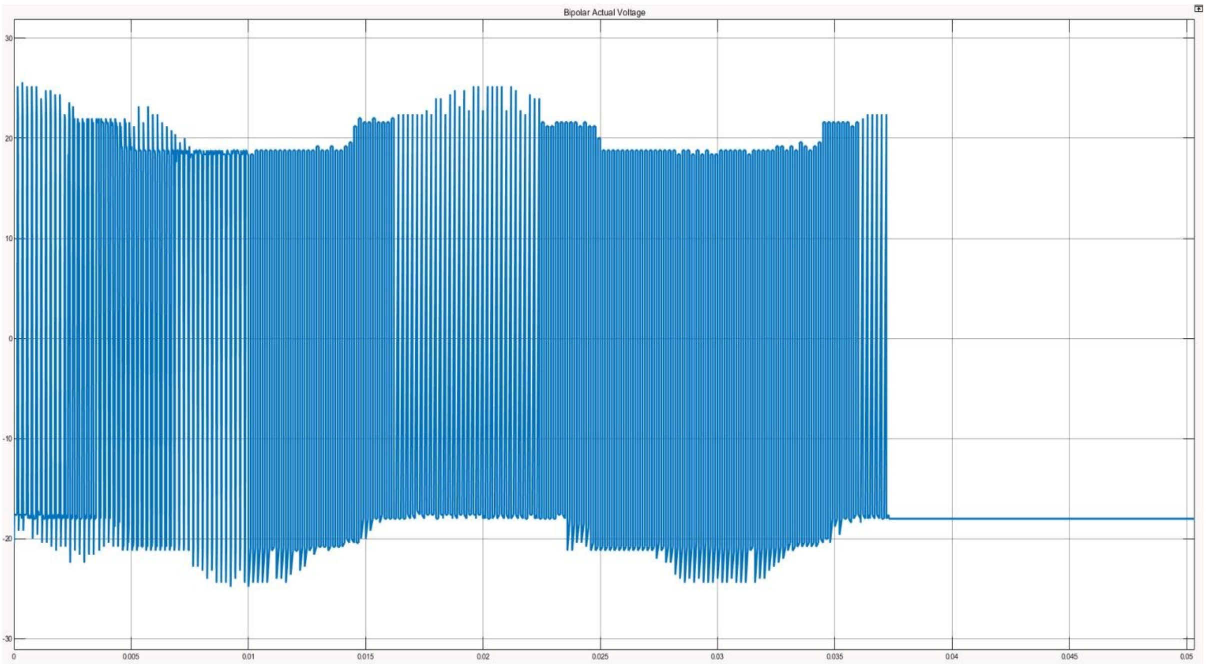


Figure 75 Actual Voltage "Bipolar"

Simulink THD

- $\boldsymbol{THD_i}$

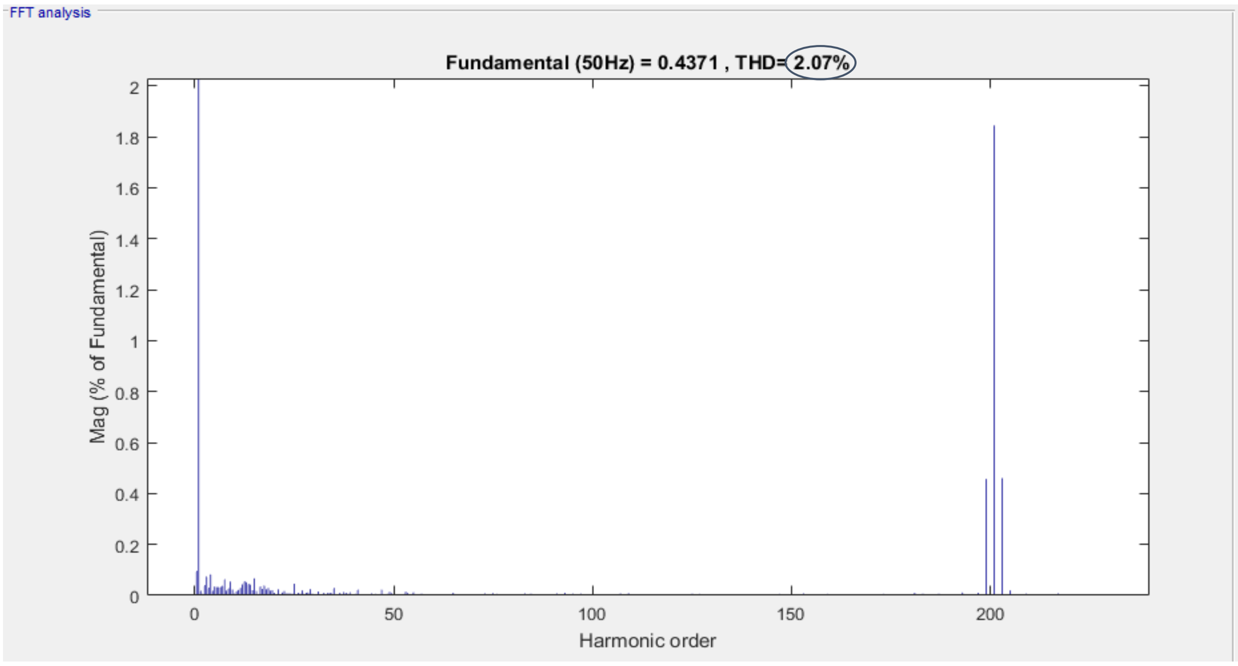


Figure 76 Simulink current THD "Bipolar"

- THD_v

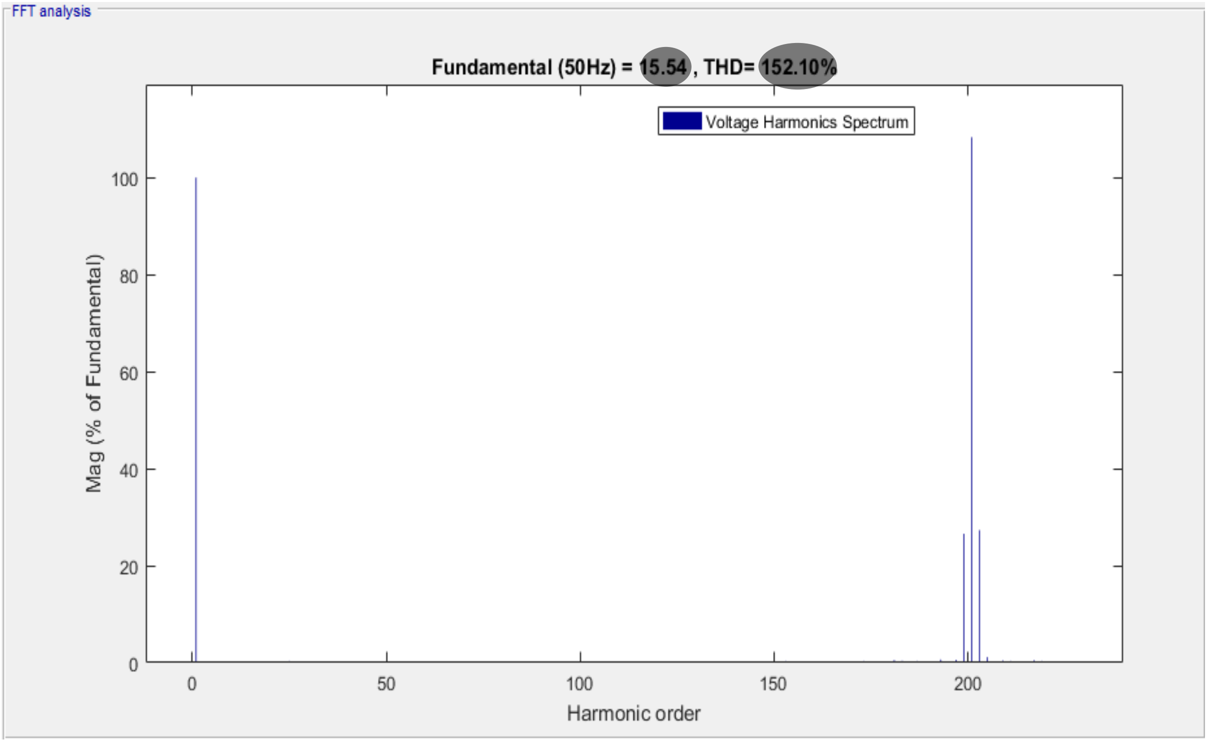


Figure 78 Simulink Voltage THD "Bipolar"

Actual THD

- THD_i

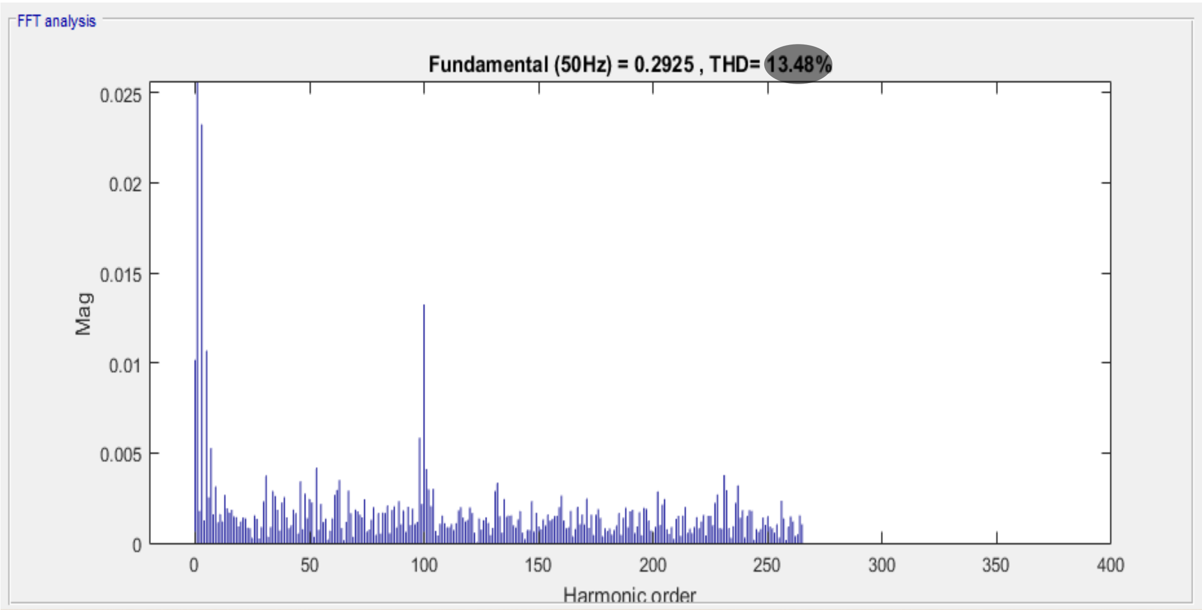


Figure 77 Actual Current THD "Bipolar"

- THD_v

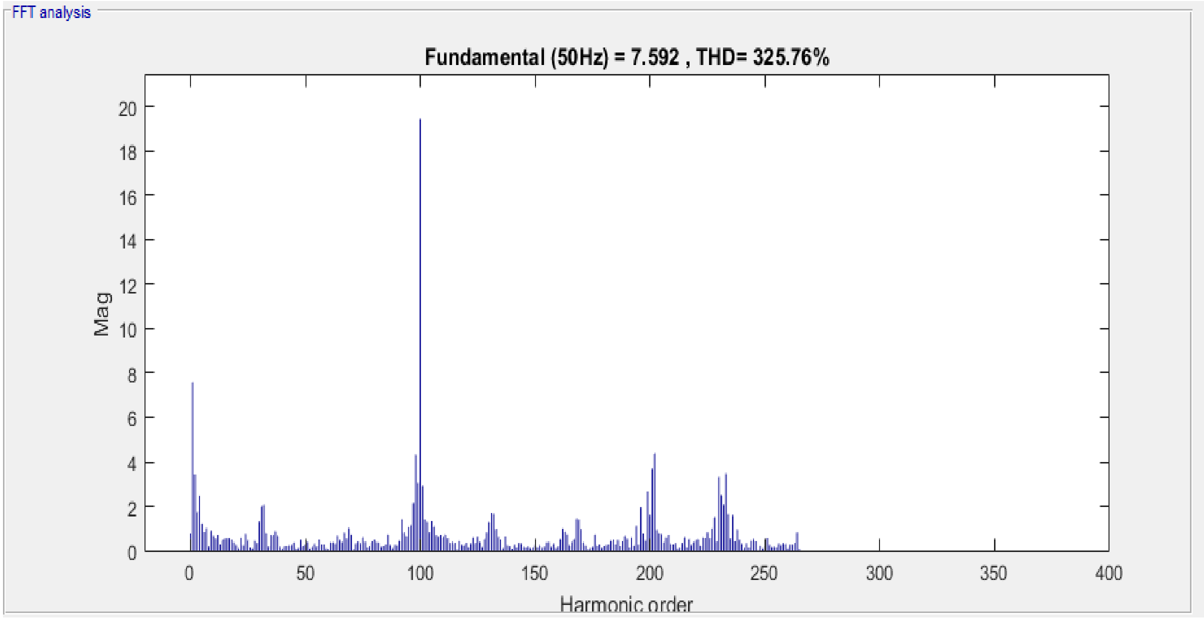


Figure 79 Actual Voltage THD "Bipolar"

Unipolar Technique

It’s another type of PWM technique, results in lower harmonics than Bipolar as it has 2 reference waves “sine & -sine “compare them with Sawtooth carrier to make gate signals.

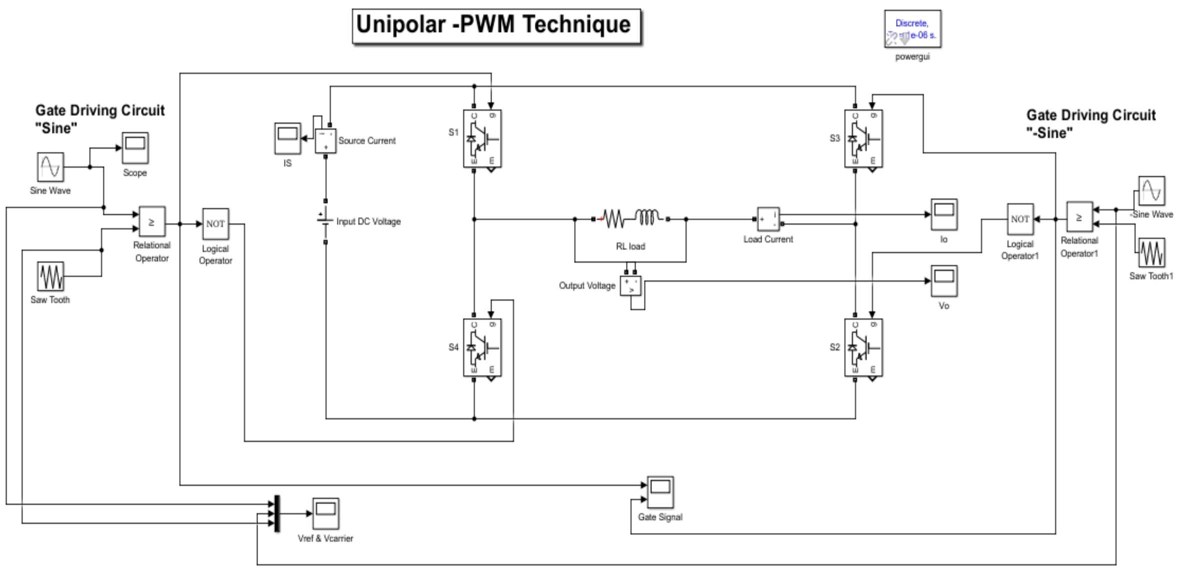


Figure 80 Model of Unipolar PWM

Setting Inputs

Take $f_{ref} = 50\ HZ$, and it’s better to take m_f as even number.

So, Take $m_f = 200$, $\therefore f_{sw} = 10000\ HZ$

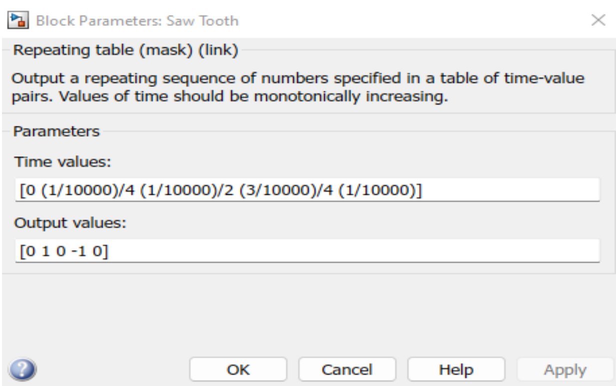


Figure 81 Parameters of Sawtooth "Unipolar"

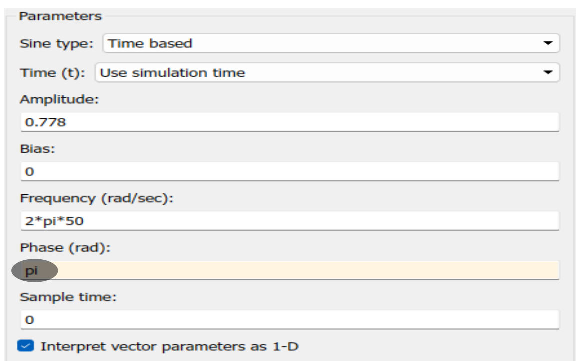


Figure 82 parameters of -sine reference "Unipolar"

Simulation Waveforms

- ## Gate Signals

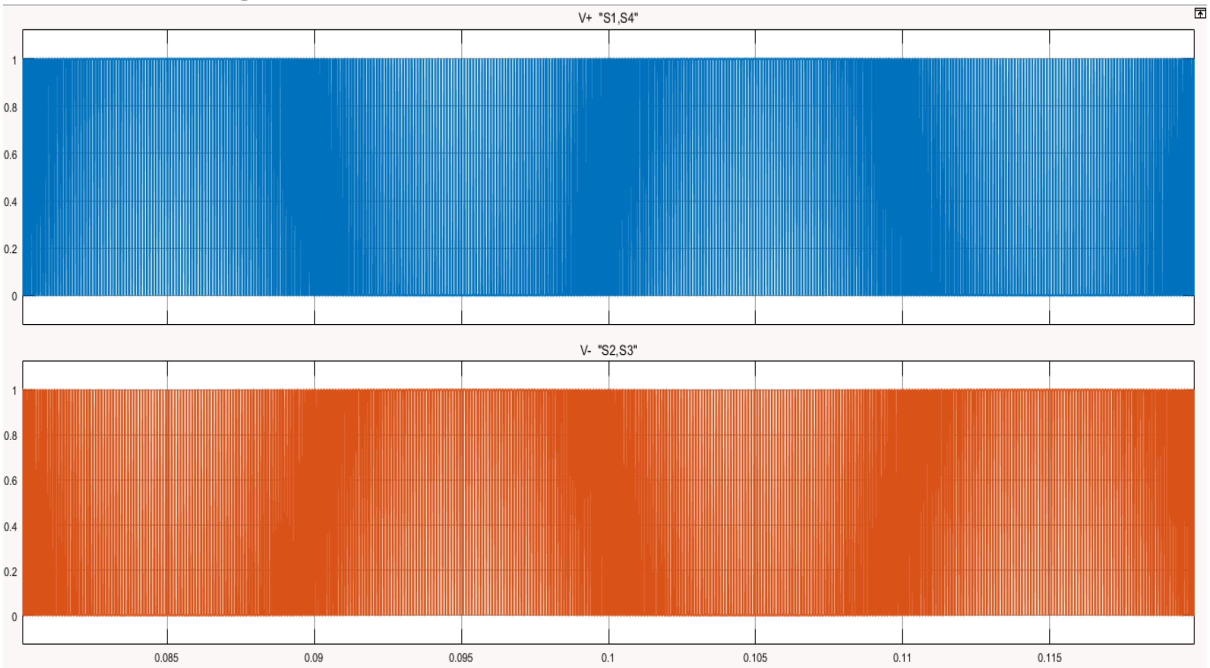


Figure 83 Gate Signals "Unipolar"

- ## References vs Carrier

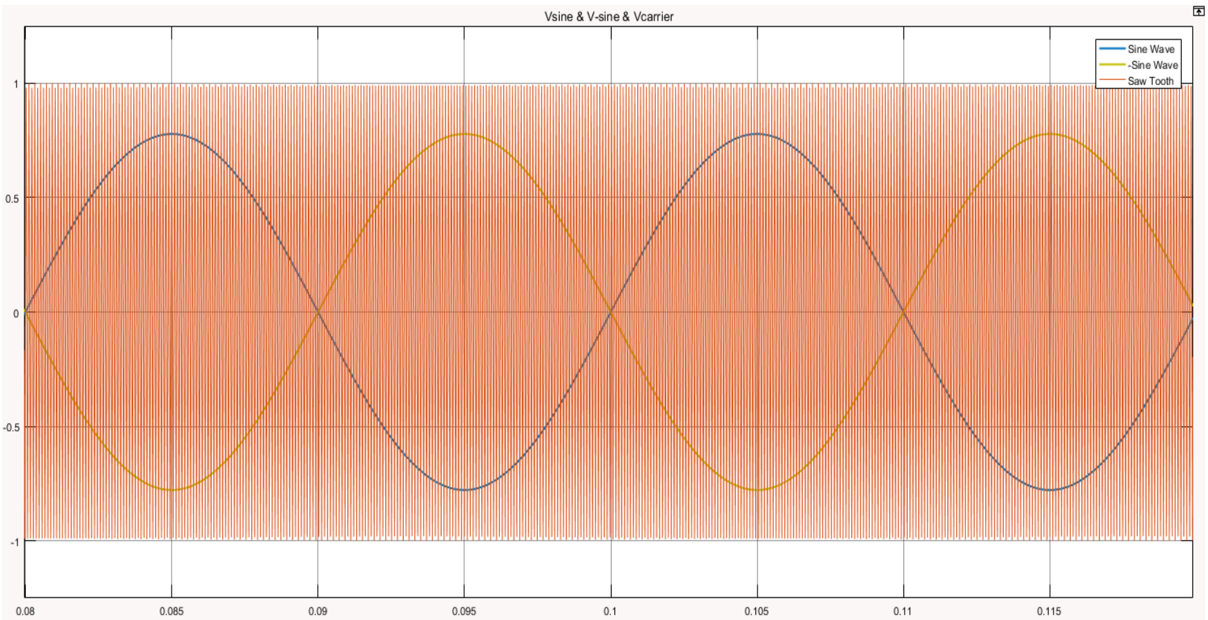


Figure 84 References vs Carrier "Unipolar"

- **Source Current**

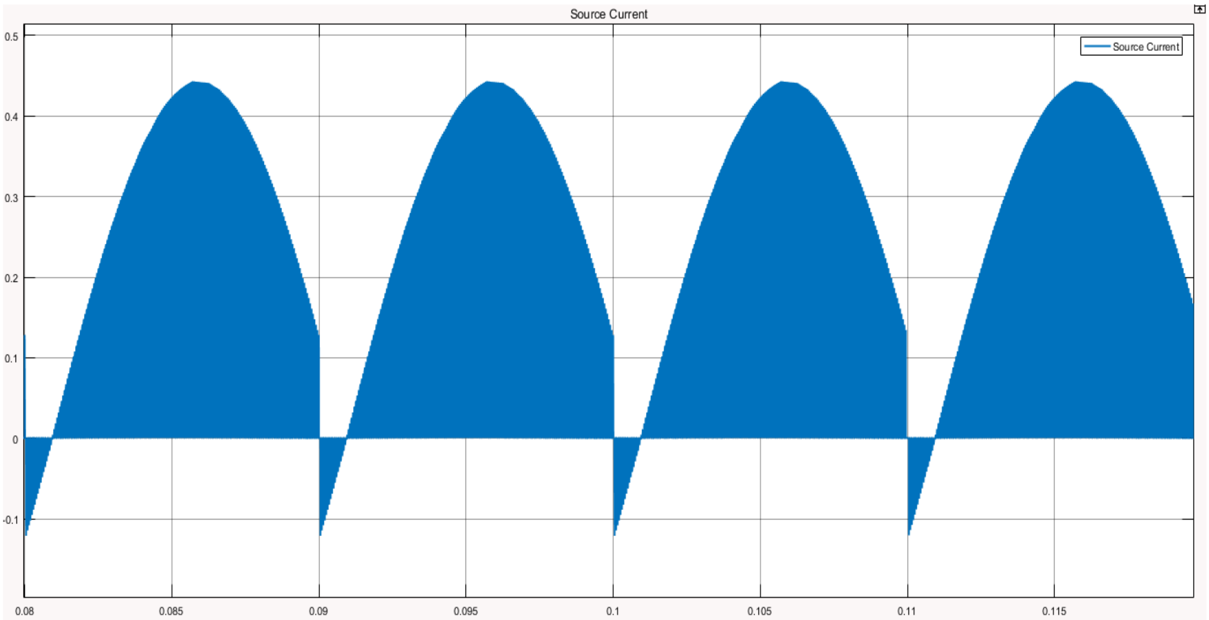


Figure 85 Source Current "Unipolar"

- **Load Current**

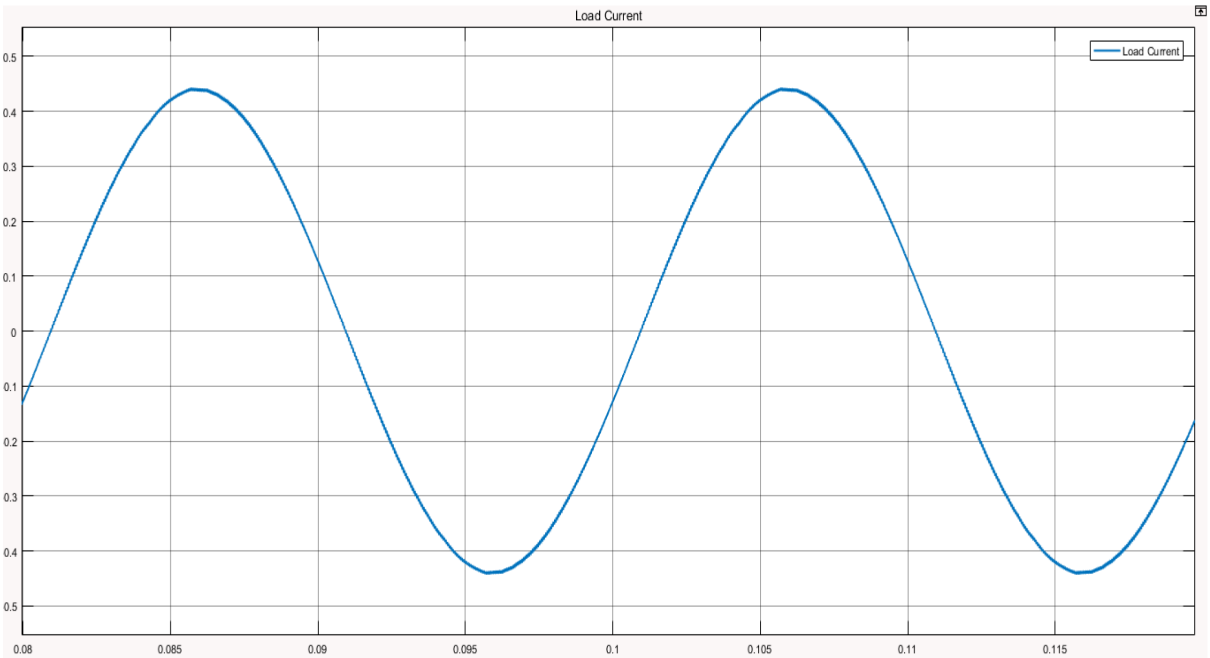


Figure 86 Load Current "Unipolar"

- **Load Voltage**

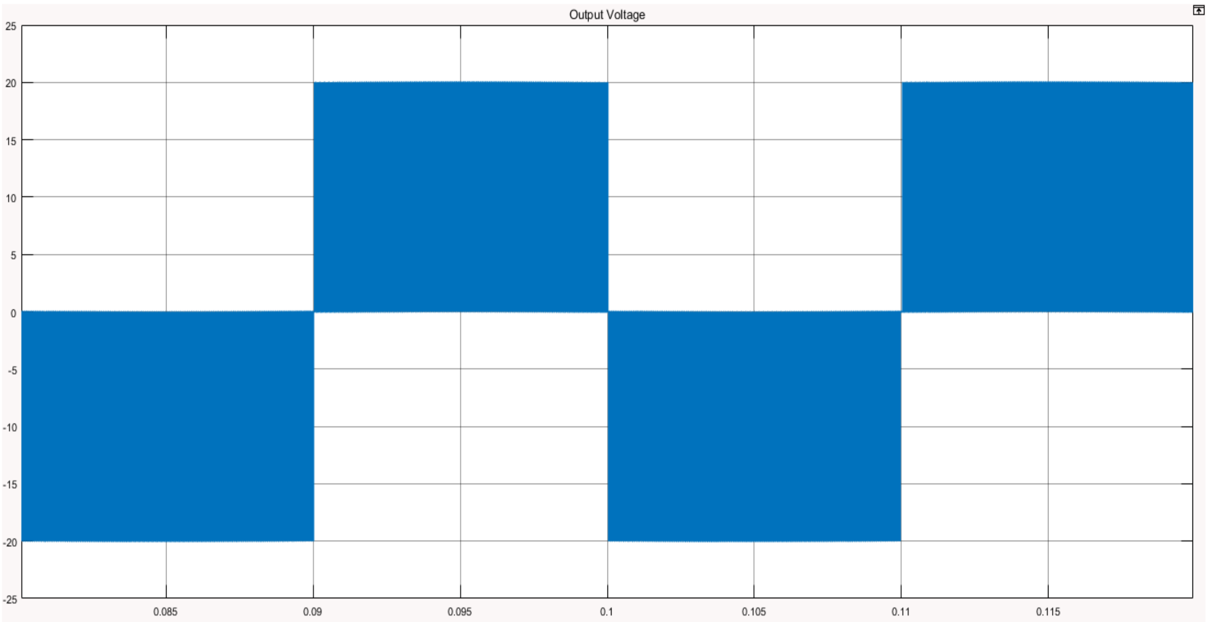


Figure 87 Load Voltage"Unipolar"

Actual Reading

- **Output Current**

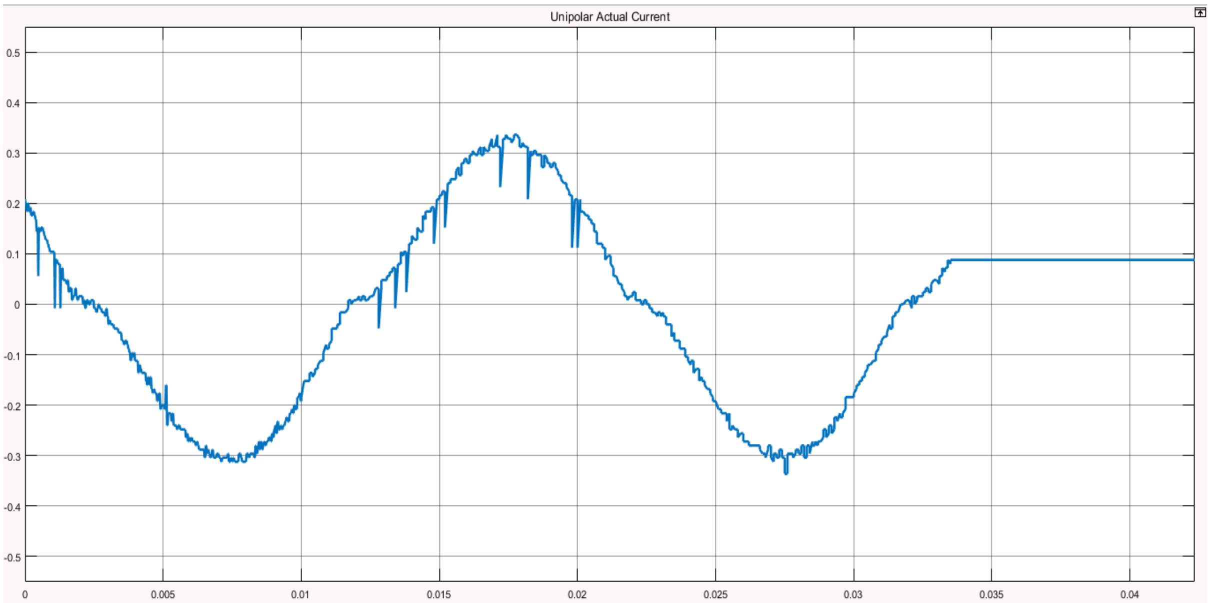


Figure 88 Actual Output Current "Unipolar"

- **Output Voltage**

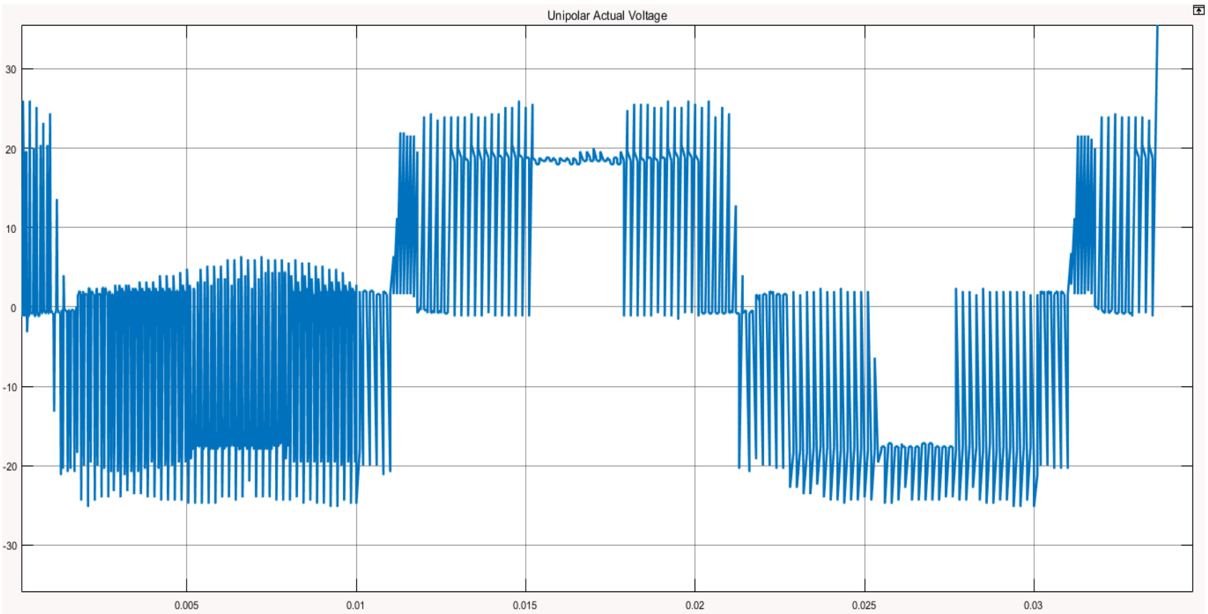


Figure 89 Actual Output Voltage "Unipolar"

Simulink THD

- THD_i

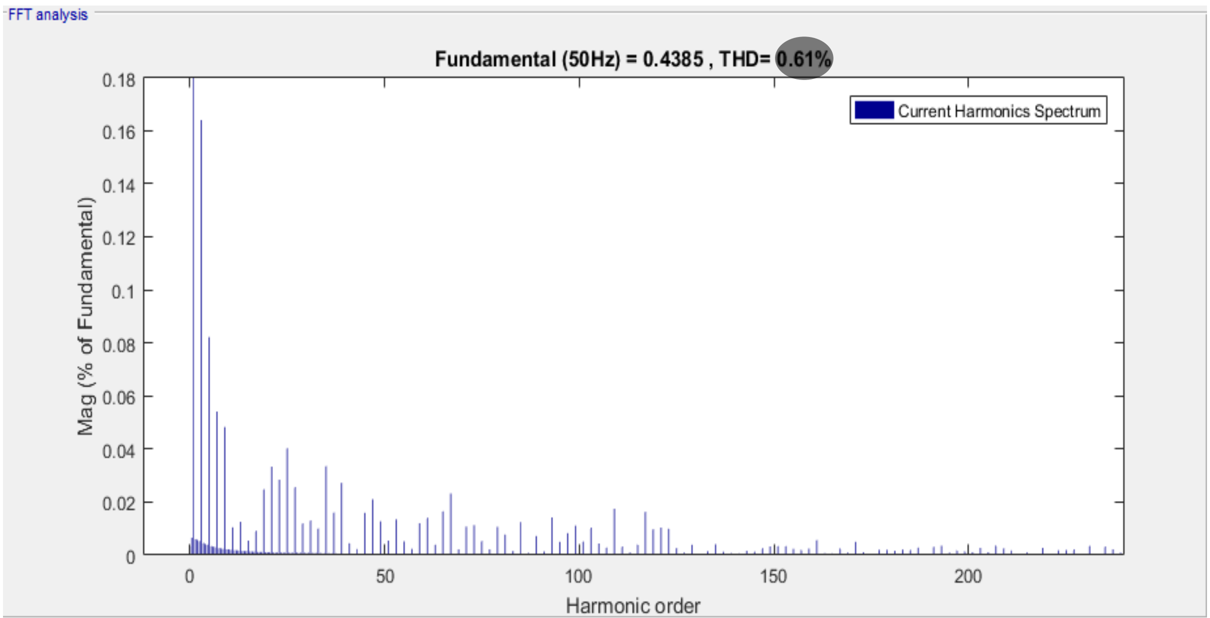


Figure 90 Simulink Current THD "Unipolar"

- THD_v

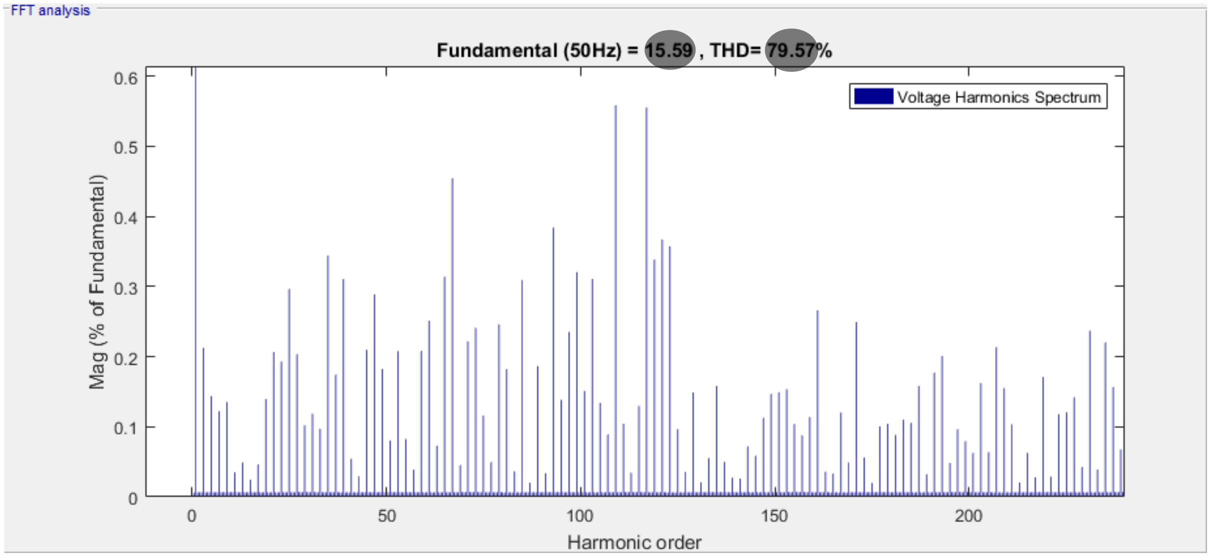


Figure 92 Simulink Voltage THD "Unipolar"

Actual THD

- THD_i

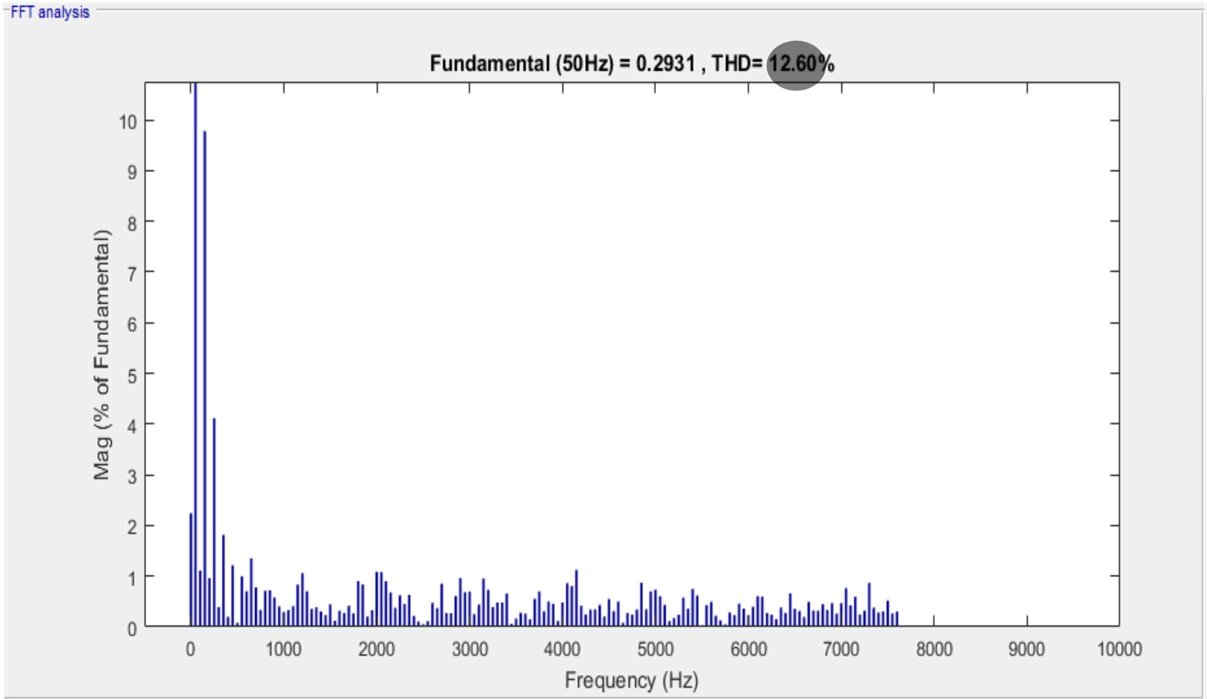


Figure 91 Actual Current THD "Unipolar"

- THD_v

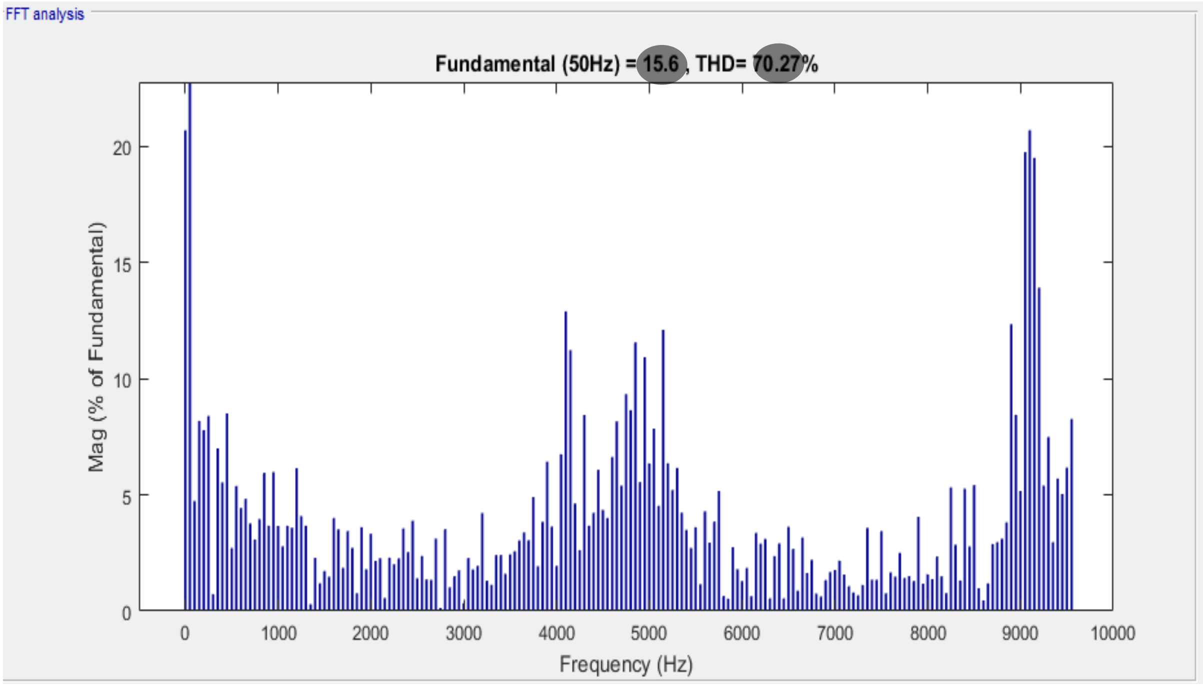


Figure 93 Actual Voltage THD "Unipolar"

Comments (Unipolar & Bipolar)

- It's Known That to get better performance when used Bipolar technique is to take m_f as odd number.
- As m_f is large number, there is little difference between using it as even or odd number.
- Unipolar has THD lower Than Bipolar as it is expected, as unipolar generate Harmonics at 2*Fsw which is high harmonic order so the effect of it will be smaller
- There is a large difference between Actual Value and Simulink Values because:
    1. Component Parameters: Deviations in component parameters between the simulated model and the actual hardware can lead to discrepancies. Parameters such as resistances, inductances
    2. Switching Devices: The performance of switching devices, such as MOSFETs, IGBTs, Diodes
    3. Non-Idealises: such as parasitic capacitances, inductances, and resistances.
    4. Noise and Disturbances, Temperature Effects, Temperature Effects.

I. Bipolar PWM design

I. SIMULINK Model

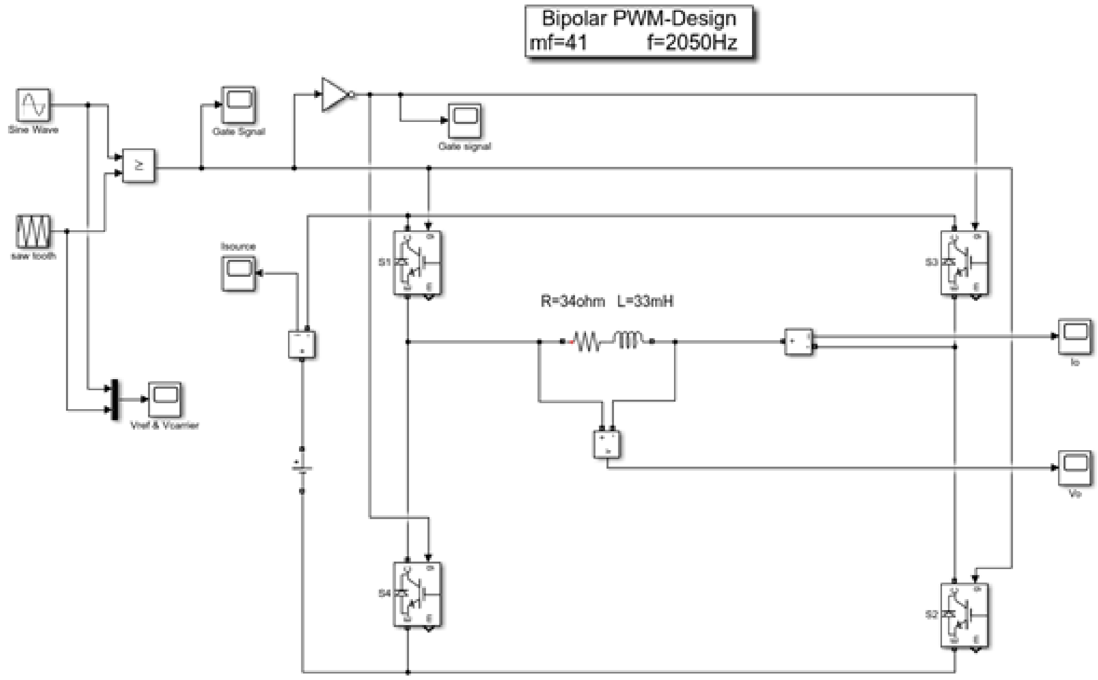


Figure 94 Model of Bipolar Design Technique

In order to achieve V1rms = $\frac{16}{\sqrt{2}}\ V$ and since Vdc = 20 V, we took modulation index Ma = 0.8 and for current THD ≤ 10%: We took $mf = 41$ which corresponds to frequency of carrier signal

$f_{s\omega} = 2050$ Hz achieving the requirements.

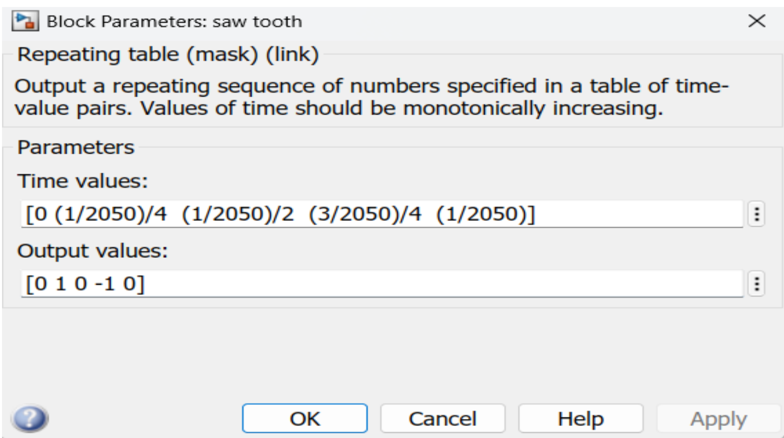


Figure 95 Parameter of reference signal "Bipolar Design"

II. Simulation Waveforms

III. Gate signal on switches 1 and 2

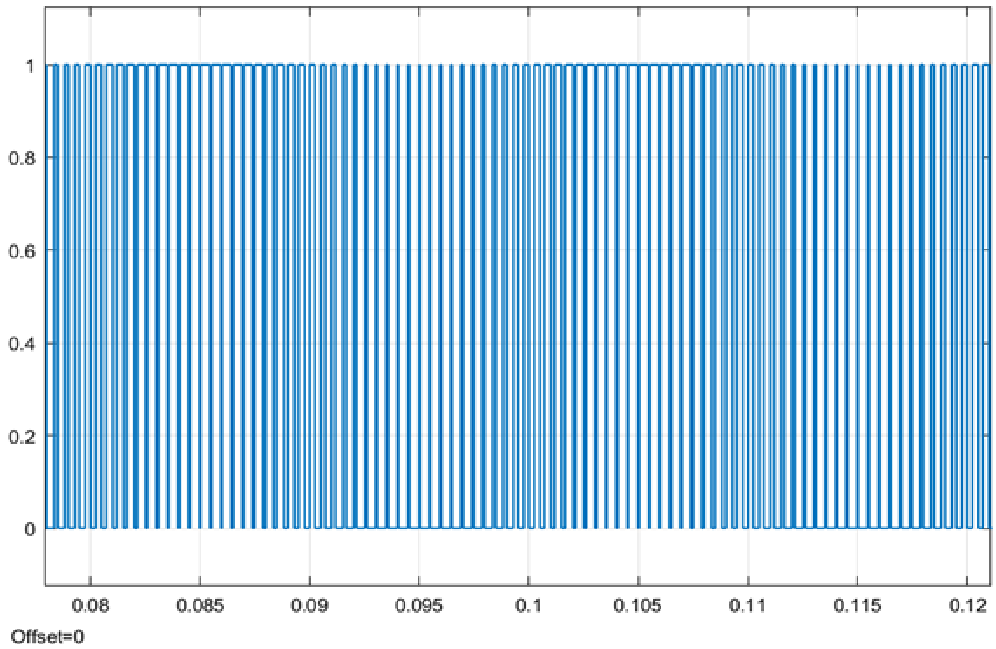


Figure 96 Gate Signal S1,S2 "Bipolar Design"

IV. Gate signal on switches 3 and 4

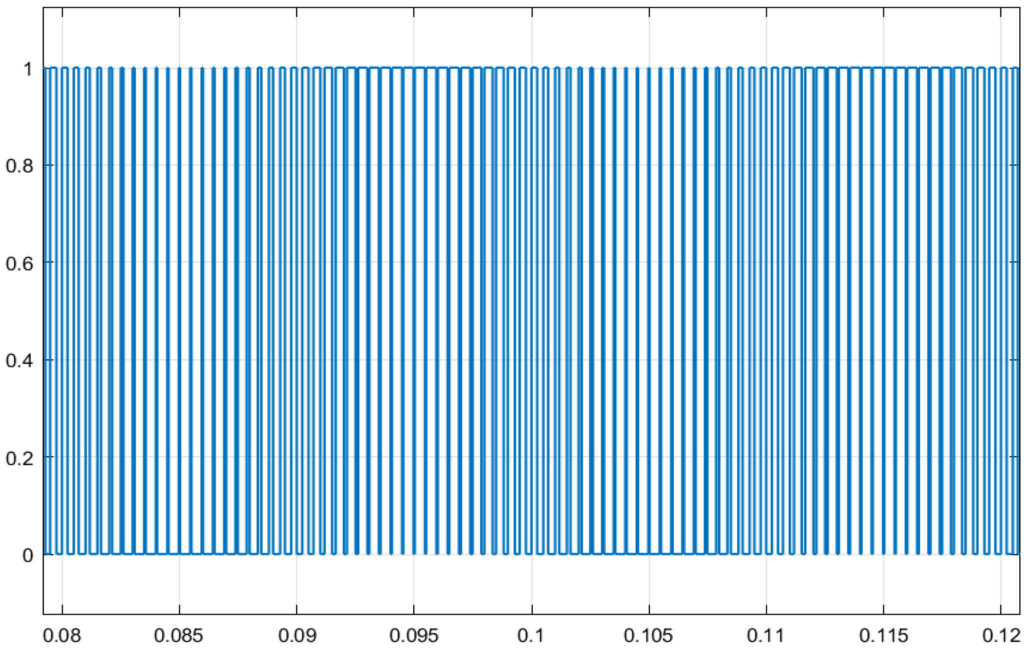


Figure 97 Gate Signal S3,S4 "Bipolar Design"

V.Dc current source

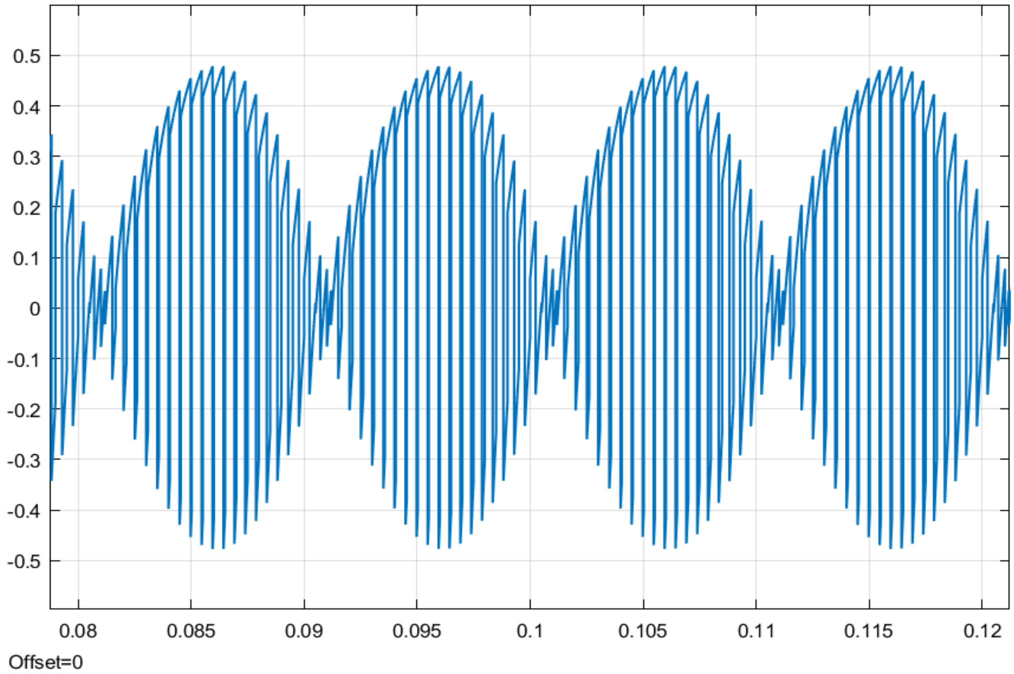


Figure 98 DC source current "Bipolar Design"

VI. Reference voltage signal & Carrier Voltage signal

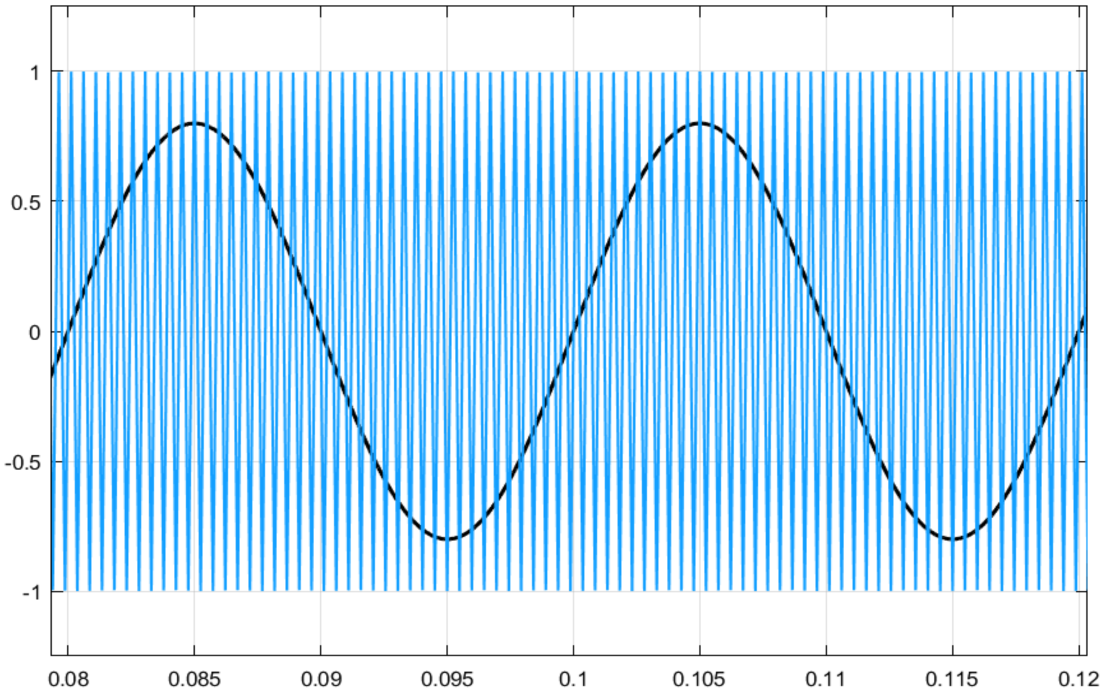


Figure 99 Vref and Vcarier "Bipolar Design"

VII. Load current

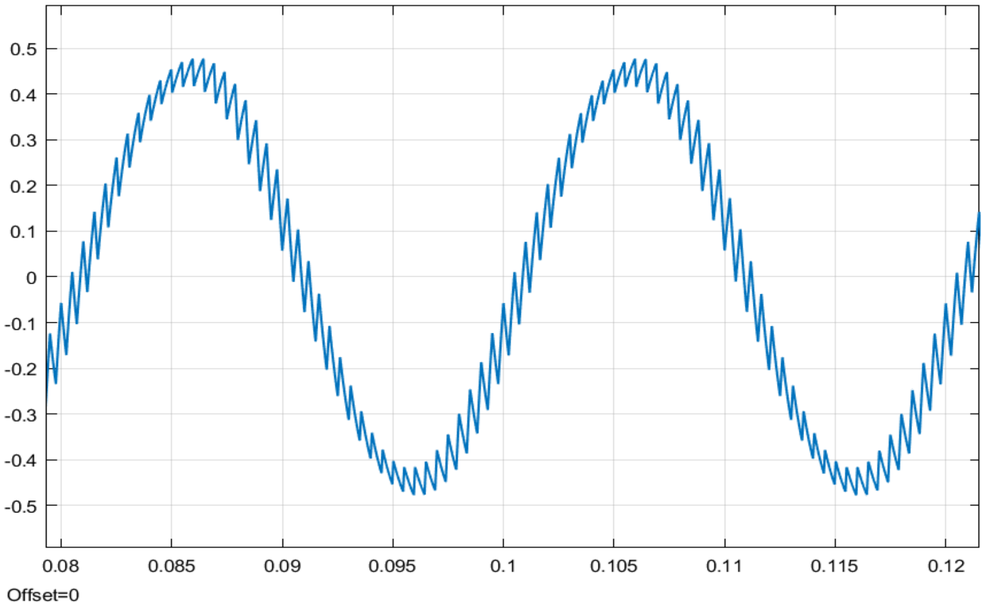


Figure 100 Load Current "Bipolar Design"

VIII. Load Voltage

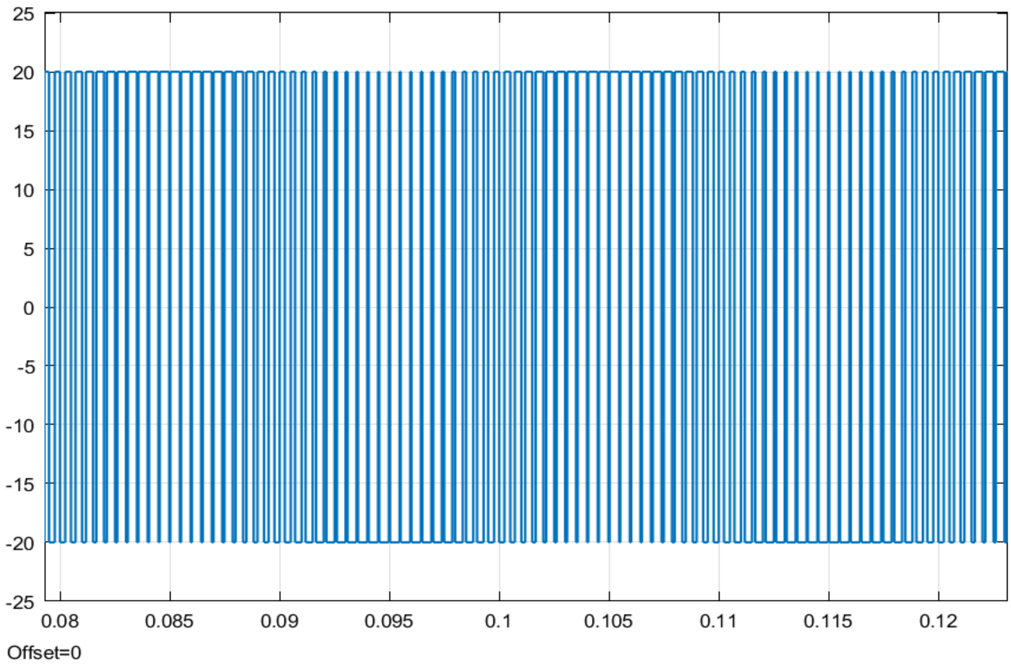


Figure 101 Load Voltage "Bipolar Design"

X. Current THD and harmonics

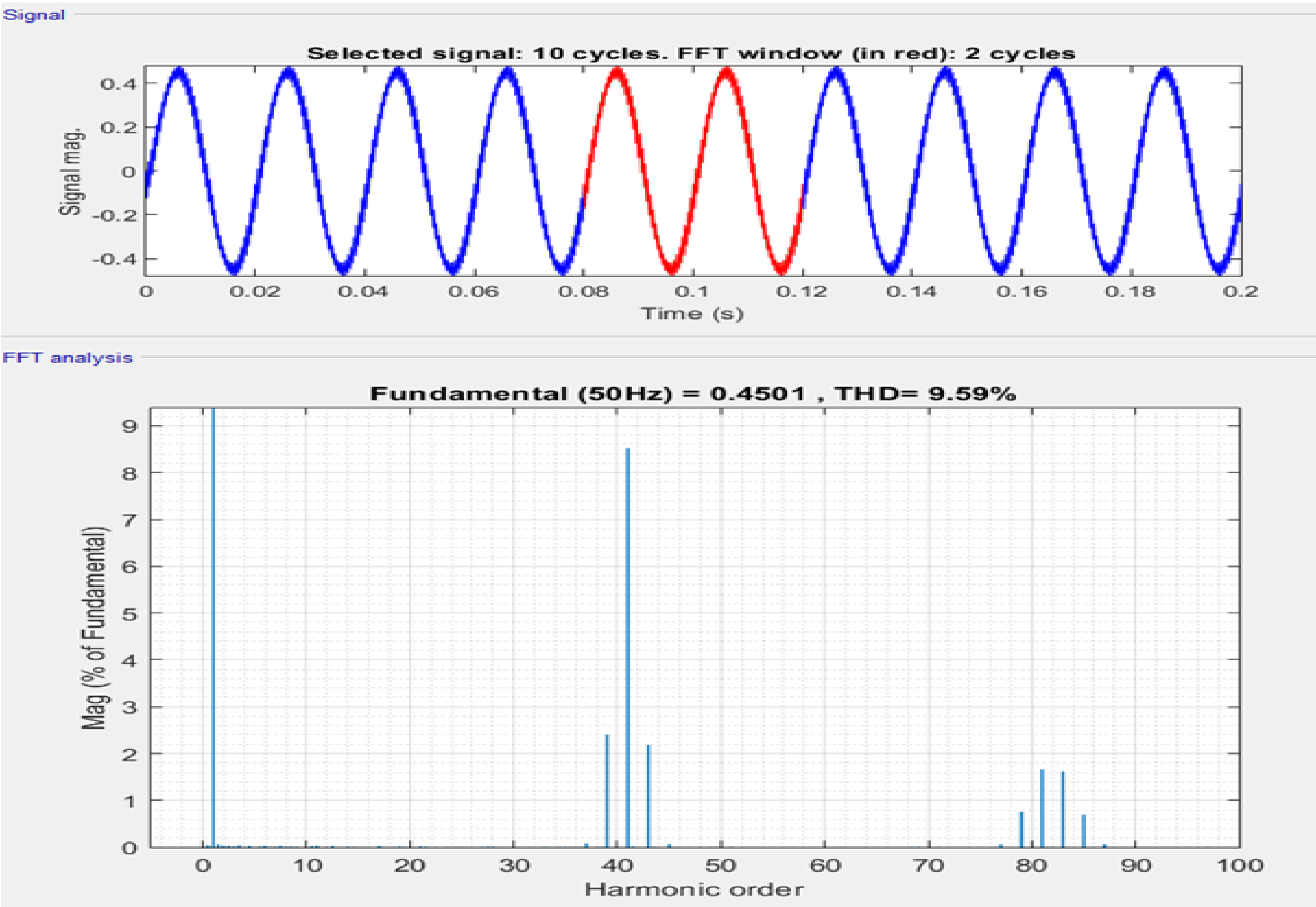


Figure 102 Current THD "Bipolar Design"

<u>Comment</u>:

FFT analysis showed that the fundamental frequency “f=50HZ” is reflected in order =1 as expected also Harmonics appeared in order of the chosen (mf = 40) and its multipliers (40n, n>1) as well as side frequencies which is “mf ± 1”

XI. Voltage THD and Harmonics

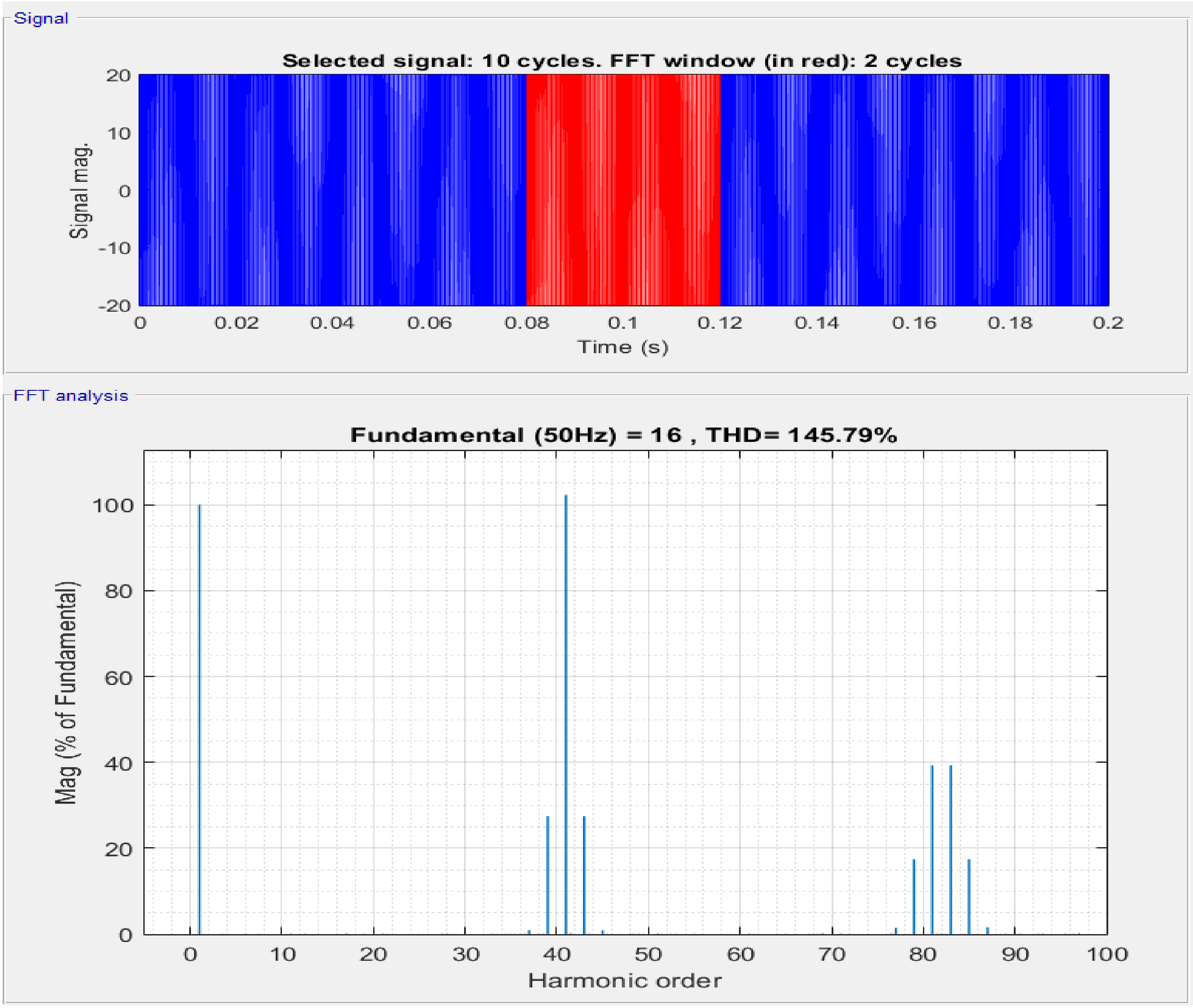


Figure 103 Voltage THD "Bipolar Design"

II. Unipolar single phase inverter design

I. SIMULINK Model

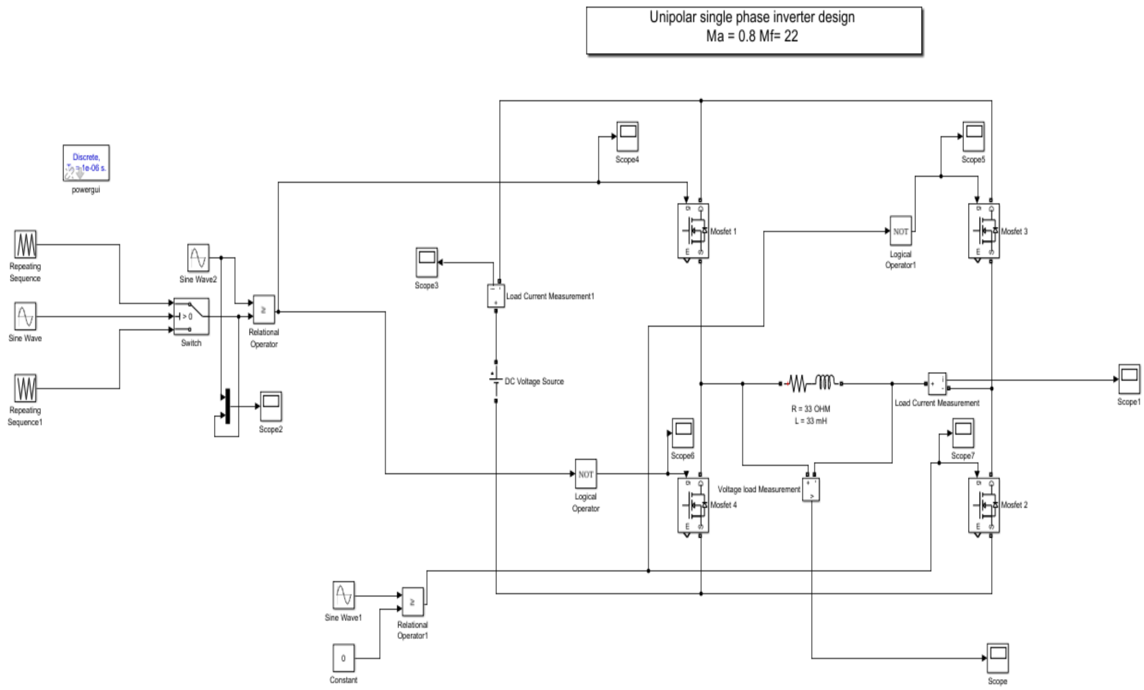


Figure 104 Model of Unipolar Design Technique

In order to achieve Vrms = $\frac{16}{\sqrt{2}}\,V$ and since Vdc = 20 V, we took modulation index Ma = 0.8, And for current THD < 10% We took MF = 22 with frequency of carrier = 1100 Hz

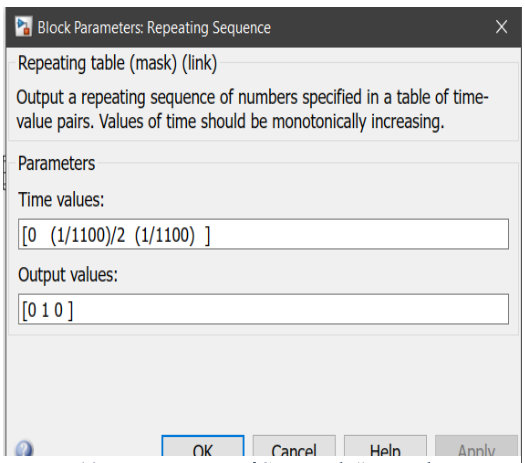


Figure 105 Parameters of Sawtooth "Unipolar Design"

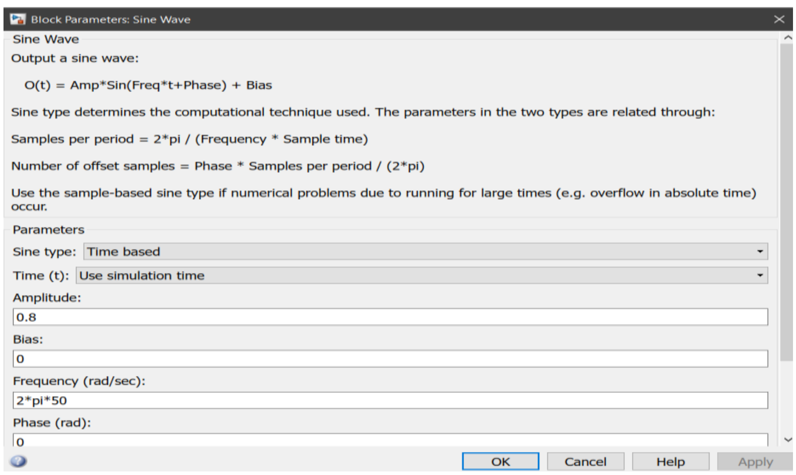


Figure 106 Parameter of reference signal "Unipolar Design"

II. Simulation Waveforms

In order to reduce switching losses, we used the technique in which switches 2 and 3 are given low frequency signal in which sine wave is compared to zero while switches 1 and 4 are given high frequency signal in which sine wave is compared with sawtooth carrier which frequency equal 1100 H. Note: All readings started from time 0.08 sec to 0.12 sec.

PWM Signal for switch 1 and 4

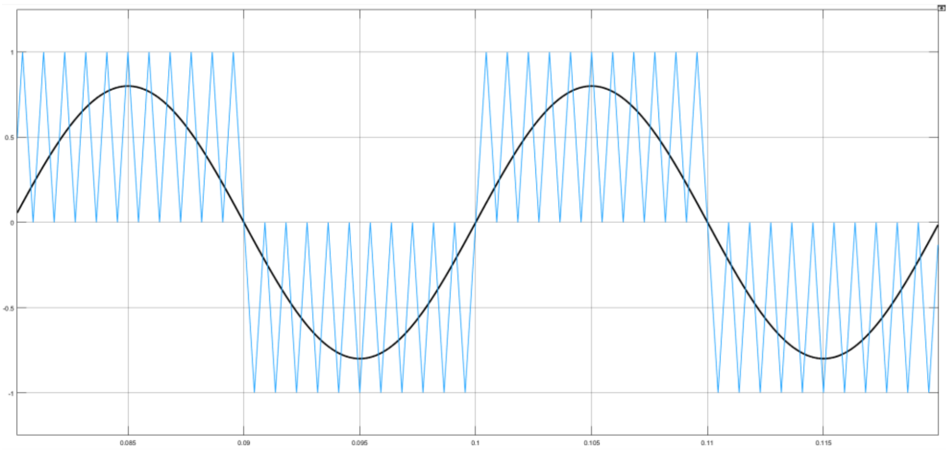


Figure 107 PWM signal for switches S1,S4 "Unipolar Design"

Switch 1 gate signal.

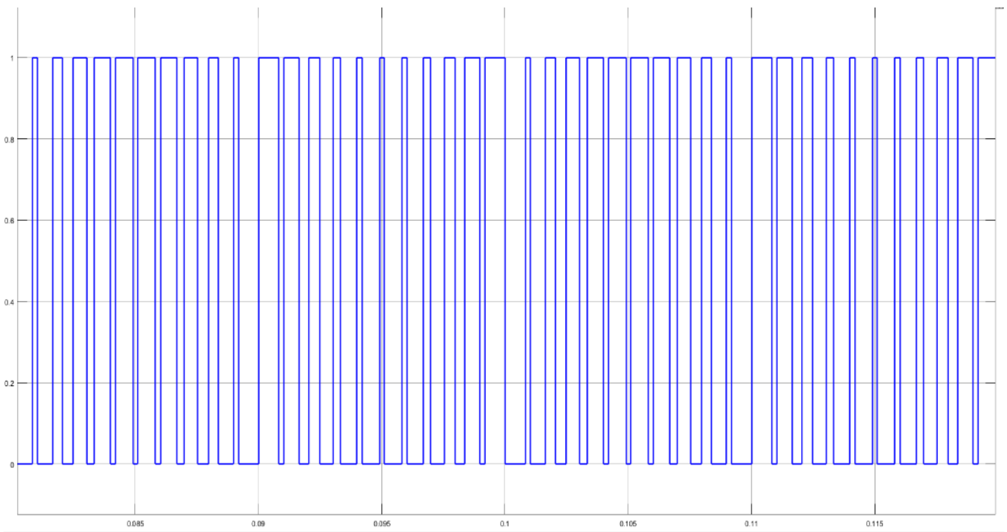


Figure 108 Switch 1 gate signal "Unipolar Design"

III. Switch 4 gate signal

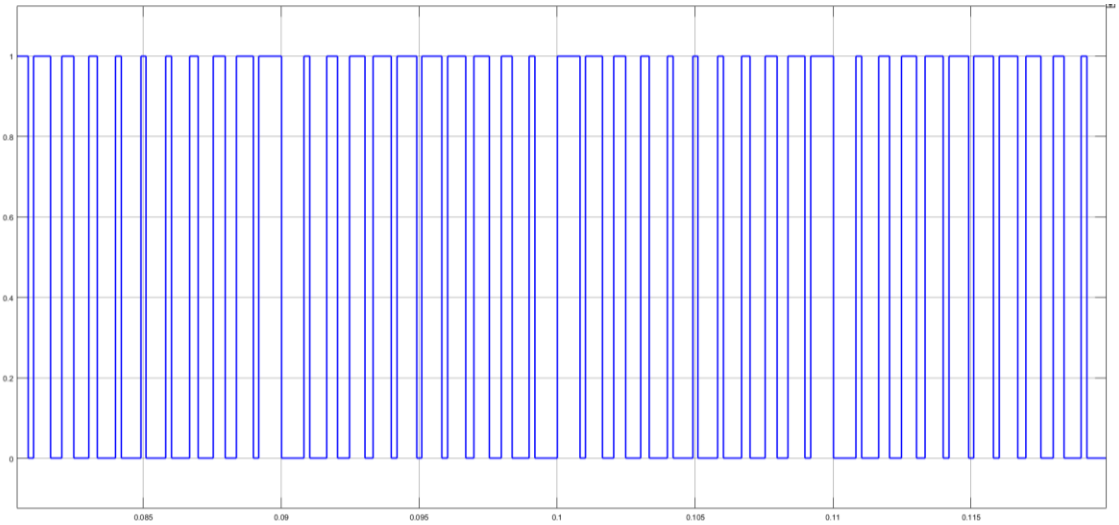


Figure 109 Switch 4 gate signal "Unipolar Design"

IV. Switch 2 gate signal

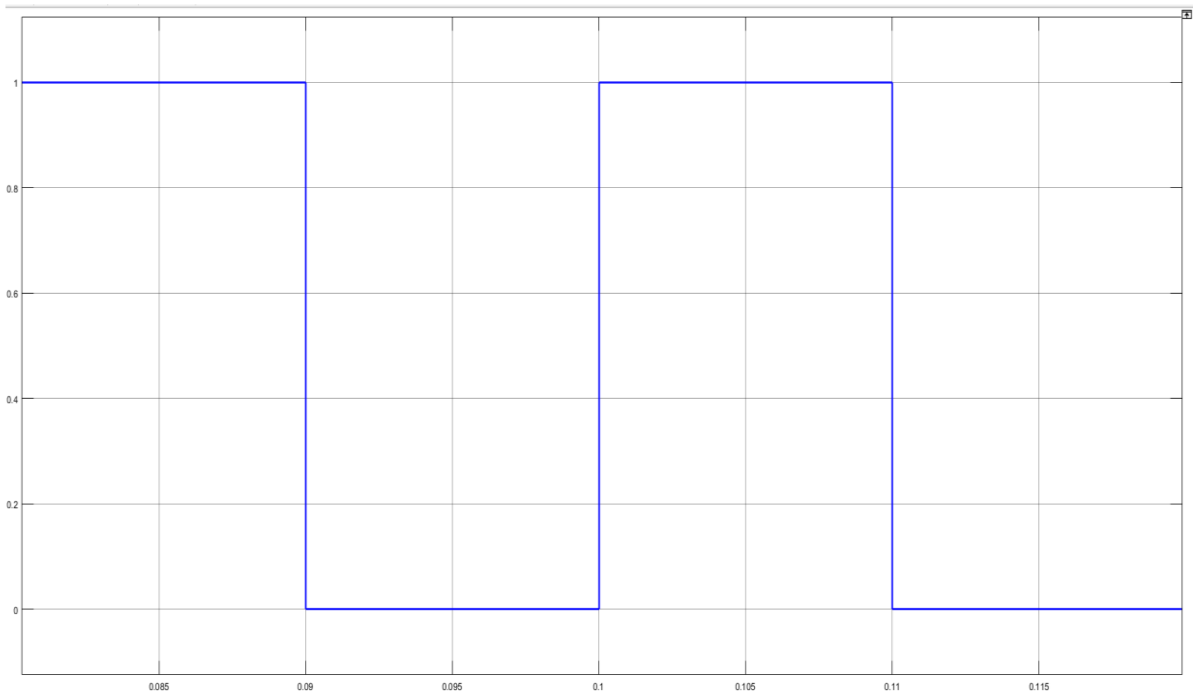


Figure 110 Switch 2 gate signal "Unipolar Design"

V. Switch 3 gate signal

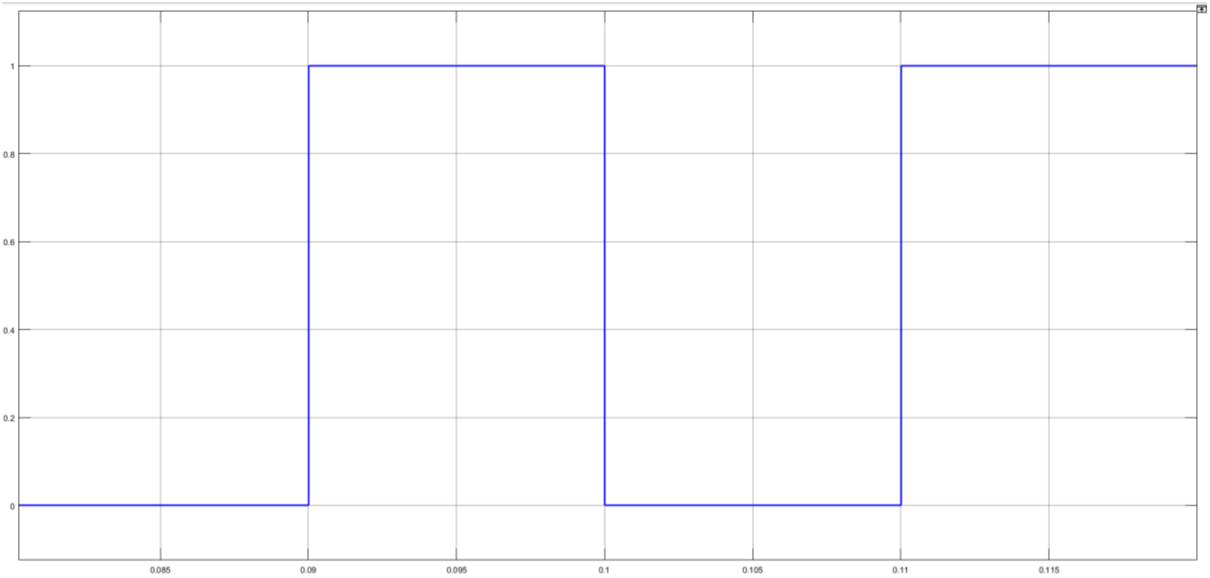


Figure 111 Switch 3 gate signal "Unipolar Design"

VI. Load voltage

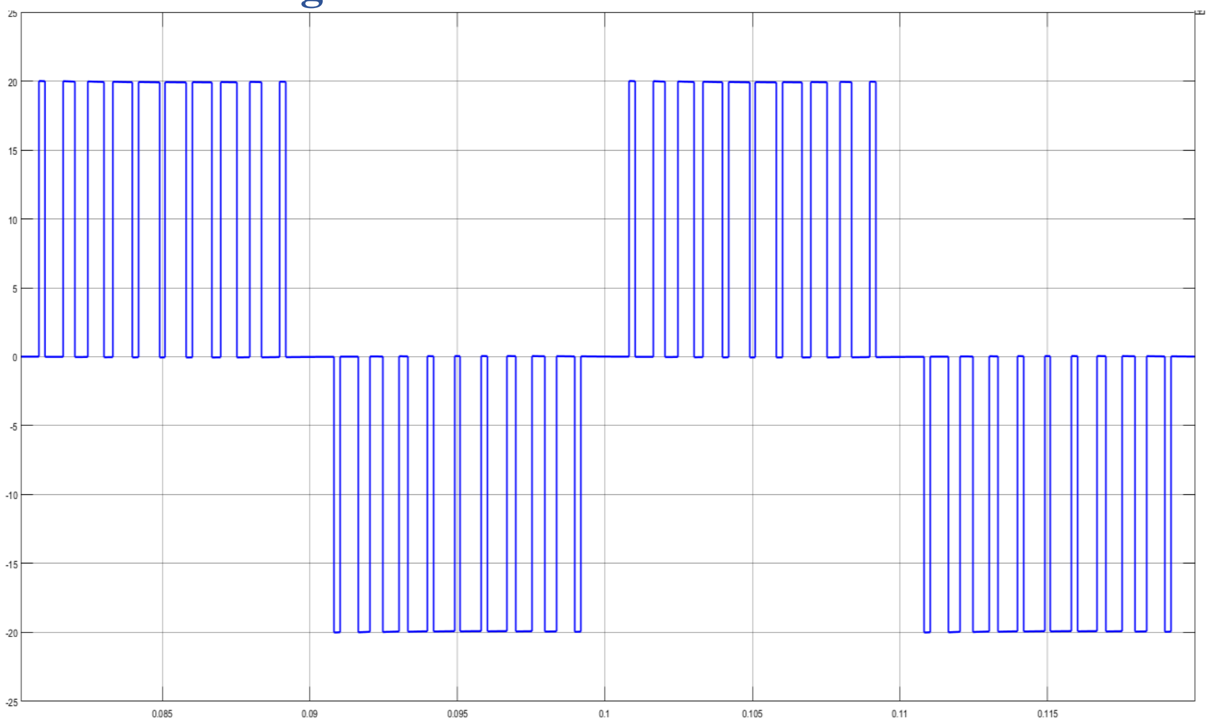


Figure 112 Load Voltage "Unipolar Design"

VII. Load current

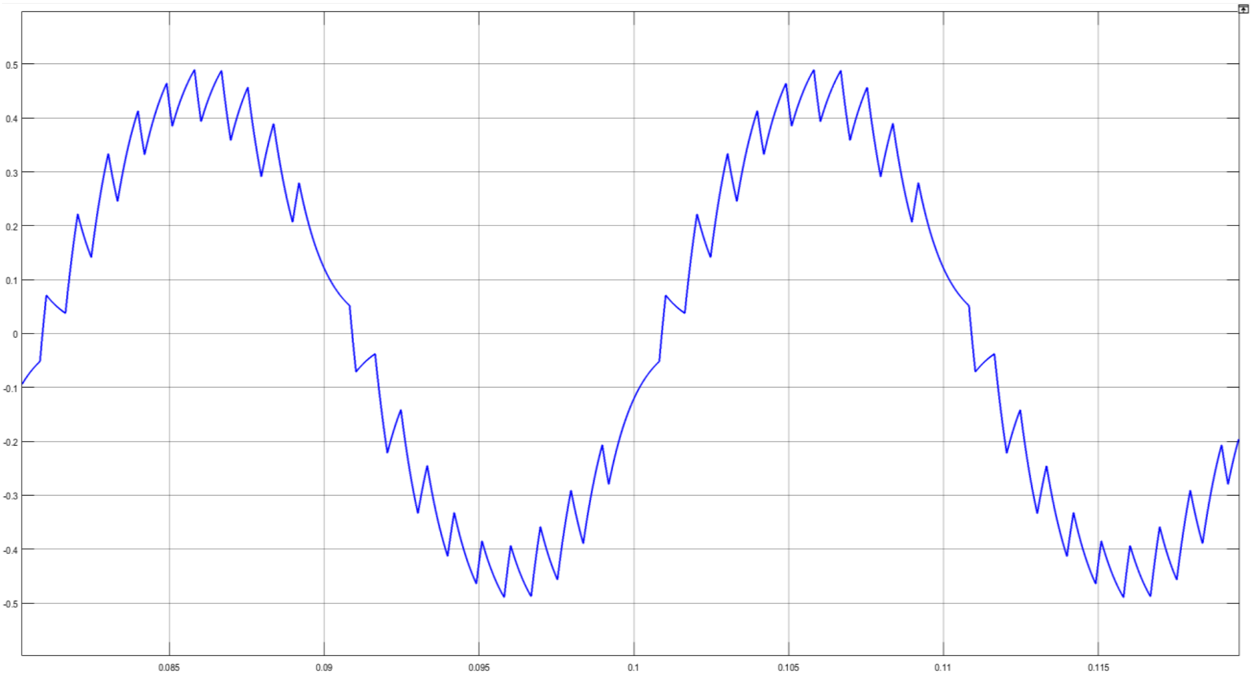


Figure 113 Load Current "Unipolar Design"

VIII. Supply current

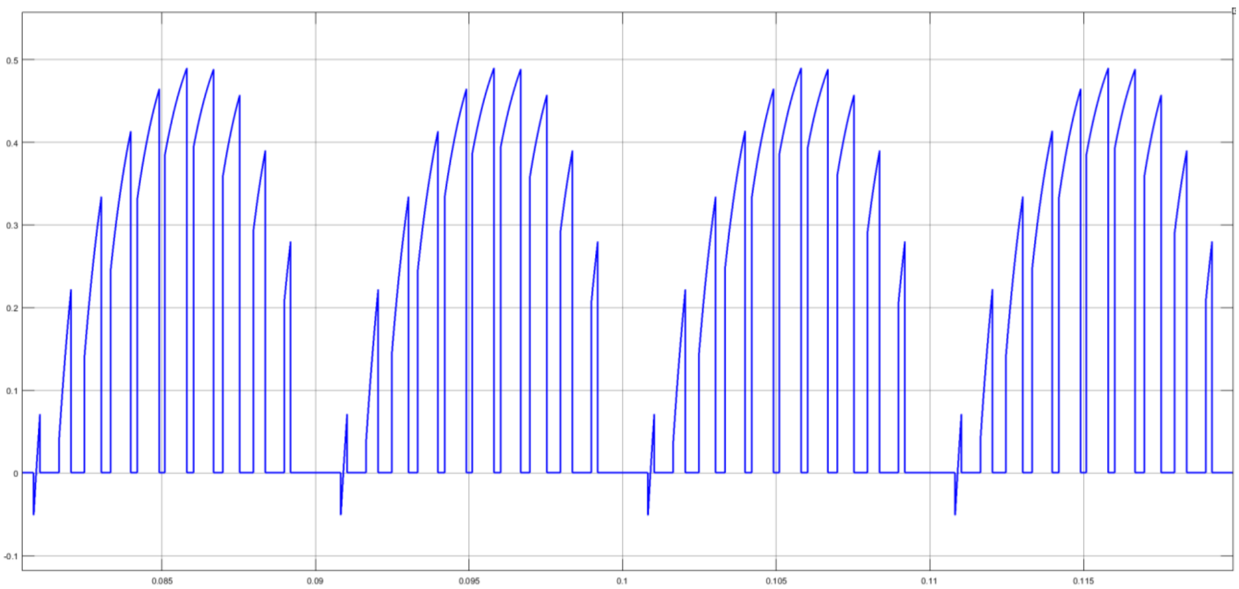


Figure 114 Supplpy current "Unipolar Design"

IX. Voltage fundamental and THD

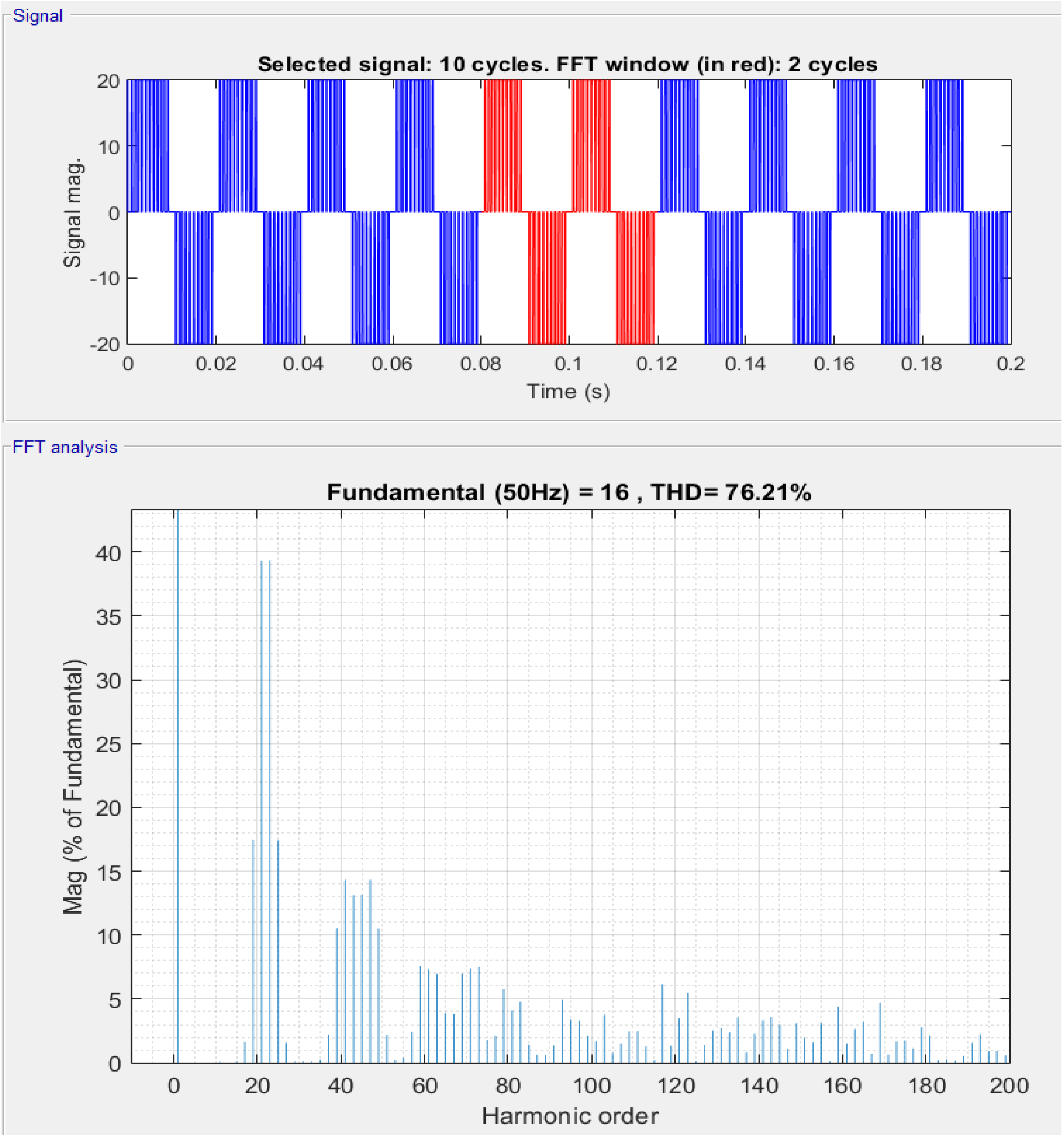
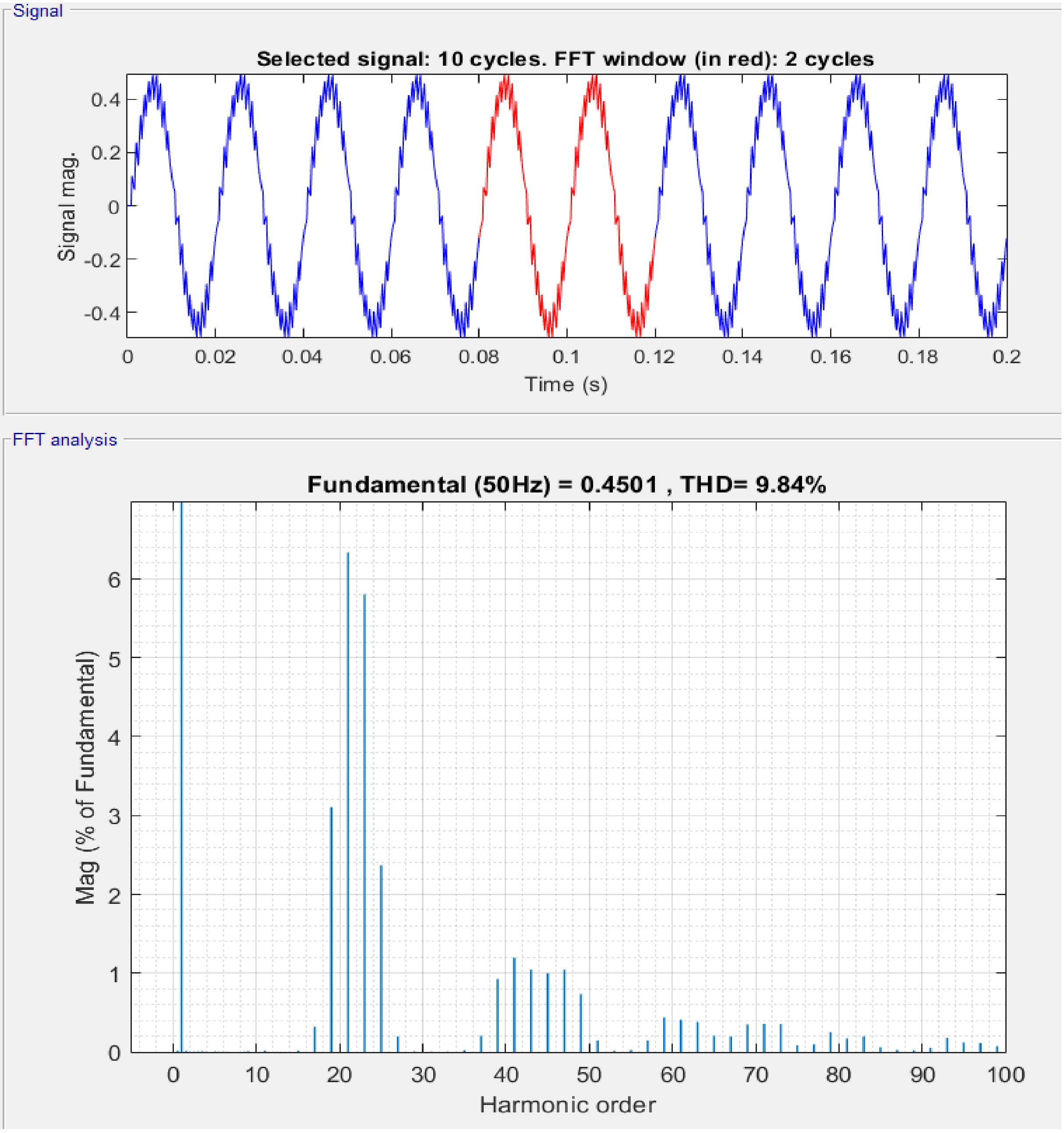


Figure 115 Voltage THD "Unipolar Design"

X. Current THD



Conclusion

Technique	**V1**		**THDv**		**THDi**	
	Sim.	**ACT.**	Sim.	ACT	Simulink	**Actual**
Square	25.46	23.1	48.34	51.15	29.44	30.34
Quasi	22.06	13.33	31.07	70.67	13.64	46.9
Optimized PWM	15.49	13.41	75.5	86	27.18	38.8
Multilevel	15.32		12.1		2.68	
Bipolar	15.54	7.592	152.1	325.76	2.07	13.48
Unipolar	15.59	15.6	79.57	70.27	0.61	12.6
Bipolar design	16		145.79		9.59	
Unipolar Design	16		76.21		9.84	