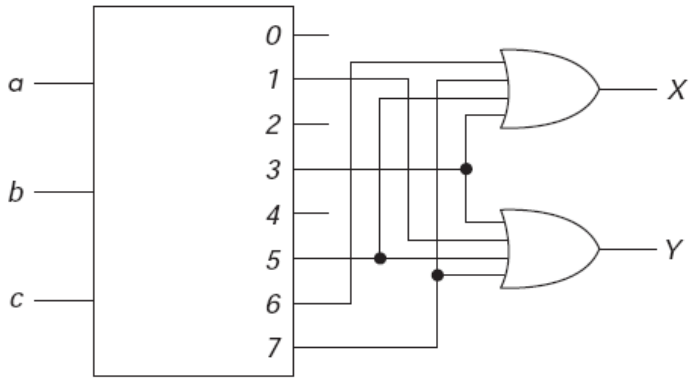
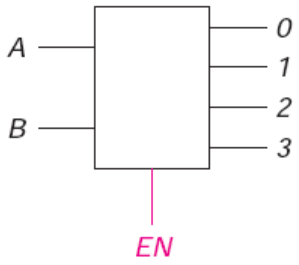
Chapter 5, problem 7: (10 pts) Consider the following circuit with an active high output decoder. Draw a truth table for X and Y in terms of a, b. and c.



Chapter 5, problem 8: (15 pts) We wish to design a decoder, with three inputs, x, y, z, and eight active high outputs, labeled 0, 1, 2, 3, 4, 5, 6, 7. There is no enable input required. (For example, if xyz = 011, then output 3 would be 1 and all other outputs would be 0.)
The only building block is a two-input, four output decoder (with an active high enable).

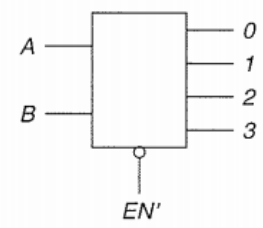
EN	*A*	*B*	*0*	*1*	*2*	*3*
0	X	X	0	0	0	0
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1



Chapter 5, problem 9: (10 pts) We want to implement a full adder: we'll call the inputs a, b, and c and the outputs s and c_{out}. As always, the adder is described by the following equations:

$$s(a, b, c) = \Sigma m(1, 2, 4, 7)$$
$$c_{out}(a, b, c) = \Sigma m(3, 5, 6, 7)$$

To implement all this, all we have available are two decoders (as shown below) and two OR gates. Inputs a and b are available both uncomplemented and complemented; c is available only uncomplemented. Show a block diagram for this system. Be sure to label all of the inputs to the decoders.



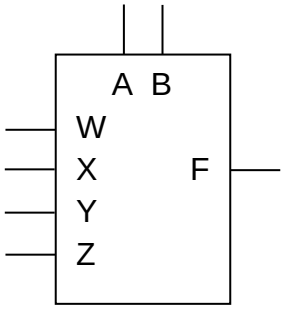
EN'	A	B	0	1	2	3
1	X	X	0	0	0	0
0	0	0	1	0	0	0
0	0	1	0	1	0	0
0	1	0	0	0	1	0
0	1	1	0	0	0	1

Chapter 5, problem 12: (10 pts) Implement the function

$$f(x, y, z) = \Sigma m(0, 1, 3, 4, 7)$$

using 2:1 multiplexers.

Chapter 5, problem 14: (5 pts) The following circuit includes a multiplexer with select inputs A and B, and data inputs W, X, Y, and Z. Write an algebraic equation for F.



Chapter 5, problem 15: (5 pts) For the following sets of functions, design a system

i. Using a ROM

a) $F(A,B,C) = \Sigma m(3,4,5,7)$
$G(A,B,C) = \Sigma m(1,3,5,6,7)$
$H(A,B,C) = \Sigma m(1,4,5)$

Chapter 5, problem 16: (10 pts) We have found a minimum sum of products expression for each of the two functions, F and G, minimizing them individually (no sharing):

F = W'X'Y' + XY'Z + W'Z
G = WY'Z + X'Y'

a) Implement them with a ROM.

c) For the same function, we have available as many of the decoders as described in the assignment as are needed plus 2 eight-input OR gates. Show a block diagram for this implementation. All inputs are available both uncomplemented and complemented.