Chapter 7, problem 2b: (40 pts) For the following state table, design the system using

i.) *D* flip flops
ii.) *SR* flip flops
iii.) *T* flip flops
iv.) *JK* flip flops

x	A	B	A*	B*	z
0	0	0	1	0	0
0	0	1	0	0	0
0	1	0	0	1	1
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	0	1	0
1	1	0	1	1	0
1	1	1	0	0	1

Show the equations for each and a block diagram for the *JK* design (using AND, OR, and NOT gates).

Chapter 7, problem 7a: (10 pts) Design a synchronous base-12 counter using D flip-flops.

Chapter 7, problem 8c: (10 pts) Design a synchronous counter that goes through the following sequence

6 5 4 1 2 3 and repeat

using JK and D flip flops. Show a state diagram, indicating what happens if it initially is in one of the unused states.

Chapter 7, problem 10a: (15 pts) Design a counter with two JK flip-flops (A and B) and an input (x) that counts 0 1 2 3 0 … when x = 0 and counts 0 1 2 0 … when x = 1. Design this assuming that x is never 1 when the count is 3. Show the minimum equations for each.

Chapter 7, problem 16: (10 + 10 pts) For each of the following problems show a state table or a state diagram.

a) A Moore system that produces a 1 output iff the input has been 0 for at least two consecutive clocks followed immediately by two or more consecutive 1's (five states).

c) A Mealy system that produces a 1 output iff the input has been 1 for three or more consecutive clock times or 0 for three or more consecutive clock times. When first turned on, it is in an initial state S_0 (There are four additional states.).