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Homework #6

Chapter 7, Problem 2b: for the following state table, design using:

(i) D flip flops
(ii) S R flip flops
(iii) T flip flops
(iv) J K flip flops

x	A	B	A*	B*	Z
0	0	0	1	0	0
0	0	1	0	0	0
0	1	0	0	1	1
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	0	1	0
1	1	0	1	1	0
1	1	1	0	0	1

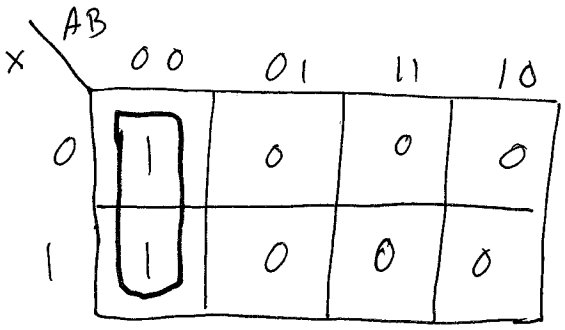
show equations for each and a block diagram for the JK design (using AND, OR, and NOT gates).

(i) D Flip Flop

A	B	A*	B*	A*	B*	D_A	D_B	D_A	D_B	X = 0	X = 1
0	0	1	0	1	1	1	0	1	1	0	0
0	1	0	0	0	1	0	0	0	1	0	0
1	0	0	1	1	1	0	1	0	1	1	0
1	1	0	0	0	0	0	0	0	0	1	1

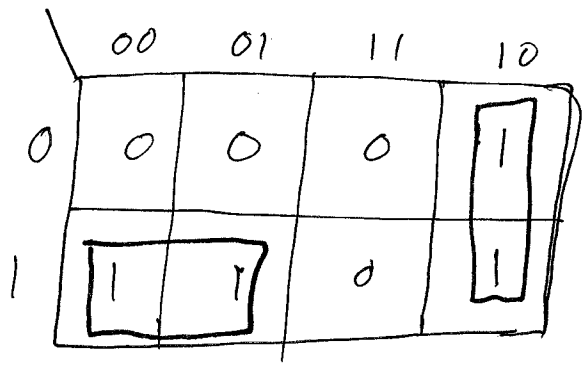
k-map

D_A



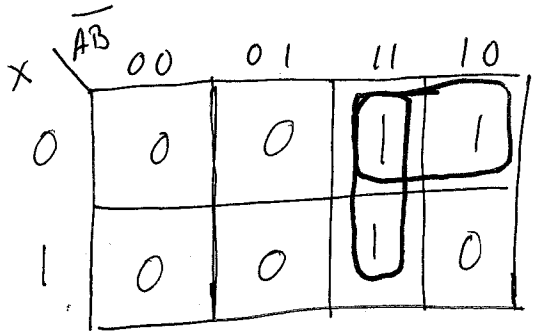
$D_A = \bar{A}\bar{B}$

D_B



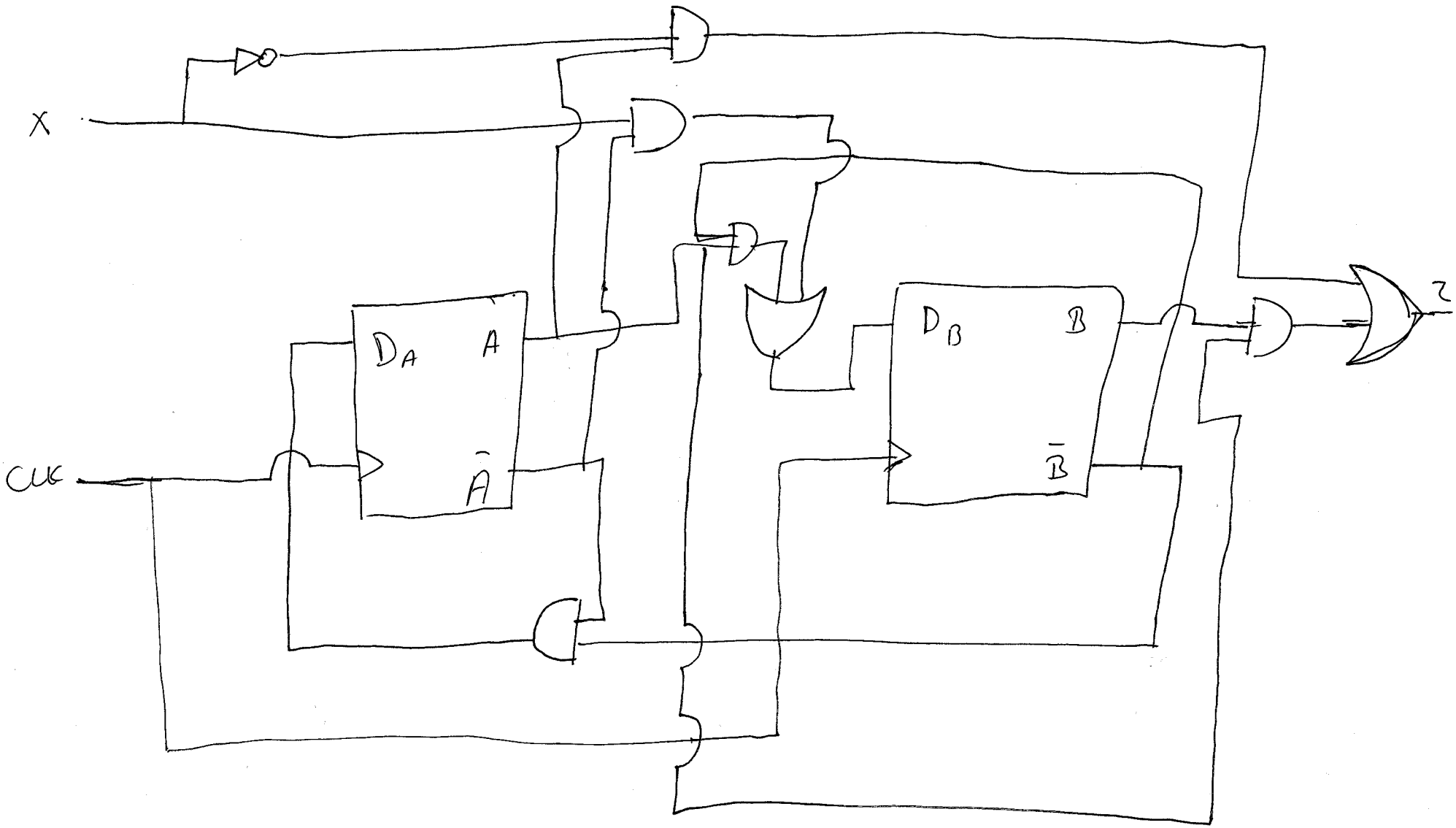
$D_B = X\bar{A} + A\bar{B}$

For output Z



$Z = AB + \bar{X}A$

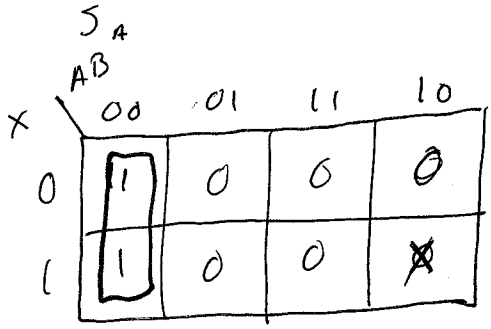
Circuit Diagram



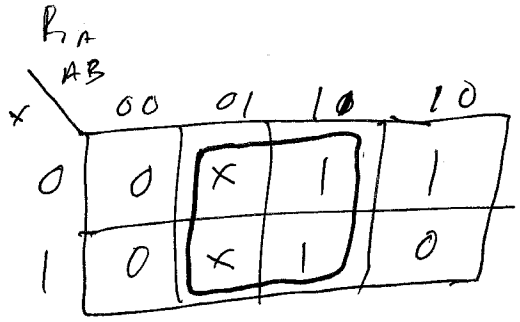
(ii) SR Flip flop

A	B	A*	B*	S_A	R_A	S_B	R_B	S_A	R_A	S_B	R_B	x=0	x=1
0	0	1	0	1	0	0	x	1	0	1	0	0	0
0	1	0	0	0	x	0	1	0	x	x	0	0	0
1	0	0	1	0	1	1	0	x	0	1	0	1	1
1	1	0	0	0	1	0	1	0	1	0	1	1	1

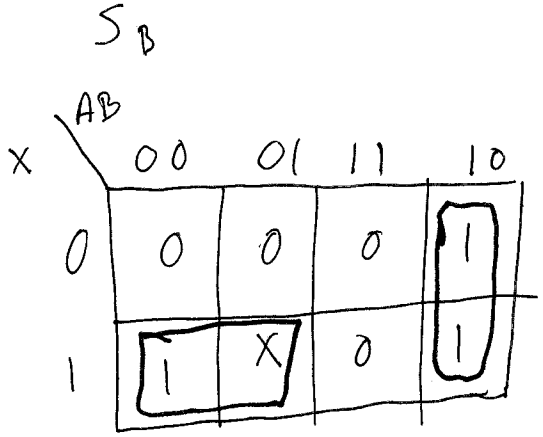
k-map



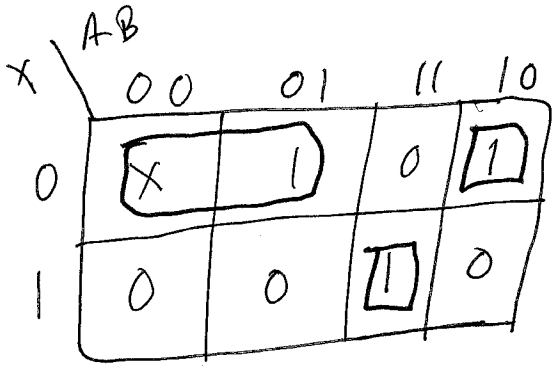
$S_A = \bar{A}\bar{B}$



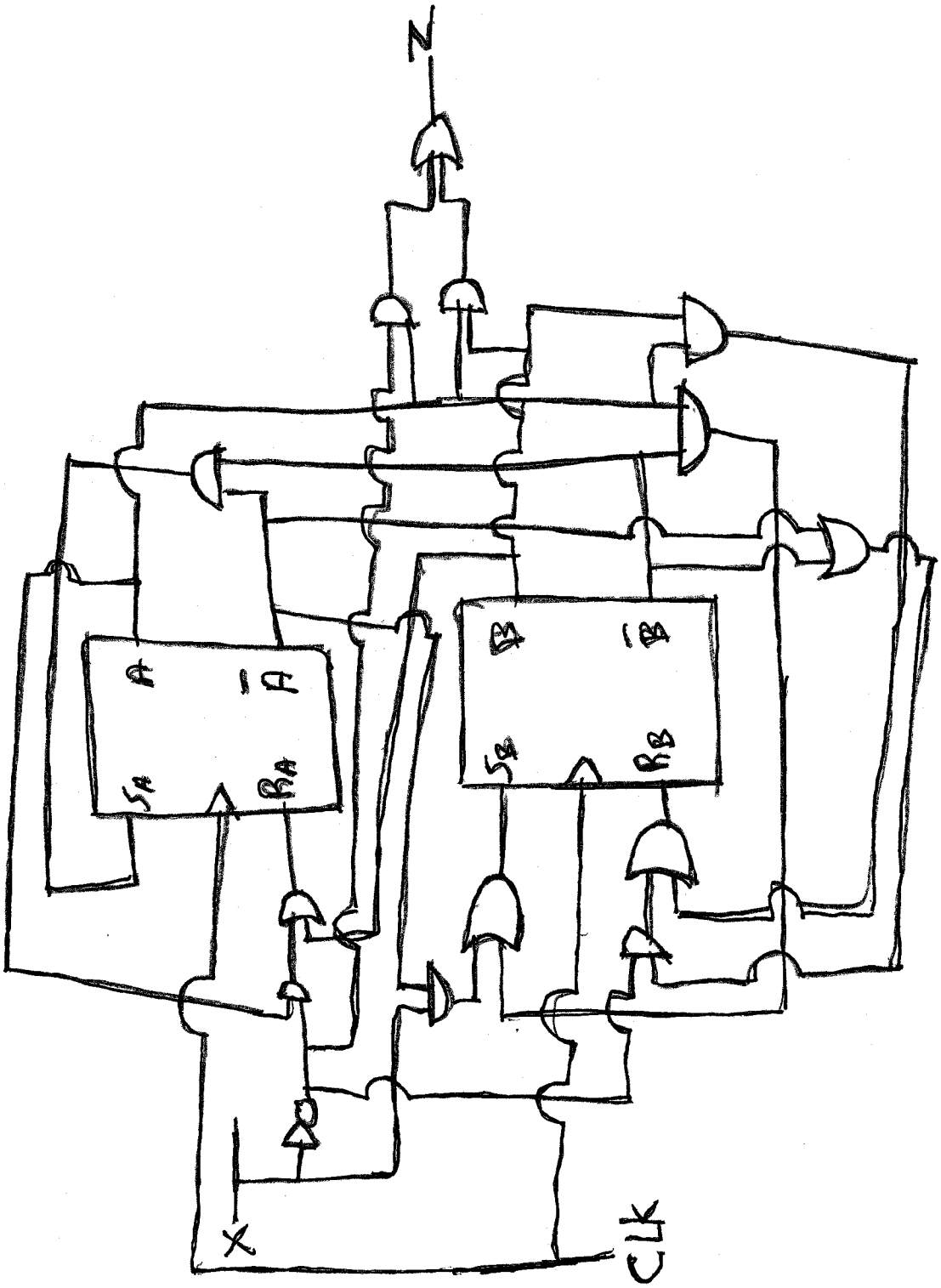
$R_A = B + \bar{X}A$



$S_B = A\bar{B} + X\bar{A}$



$R_B = \bar{X}\bar{A} + \bar{X}\bar{B} + XAB$


N
A
1A
SA
RA
B
1B
SB
RB
X
CLK

(iii) T- Flip Flop

A	B	A^*	B^*	A^*	B^*	T_A	T_B	T_A	T_B	x = 0	x = 1
0	0	1	0	1	1	1	0	1	1	0	0
0	1	0	0	0	1	0	1	0	0	0	0
1	0	0	1	1	1	1	1	0	1	1	0
1	1	0	0	0	0	1	1	1	1	1	1

k-Map

T_A

x \ AB	00	01	11	10
0	1	0	1	1
1	1	0	1	0

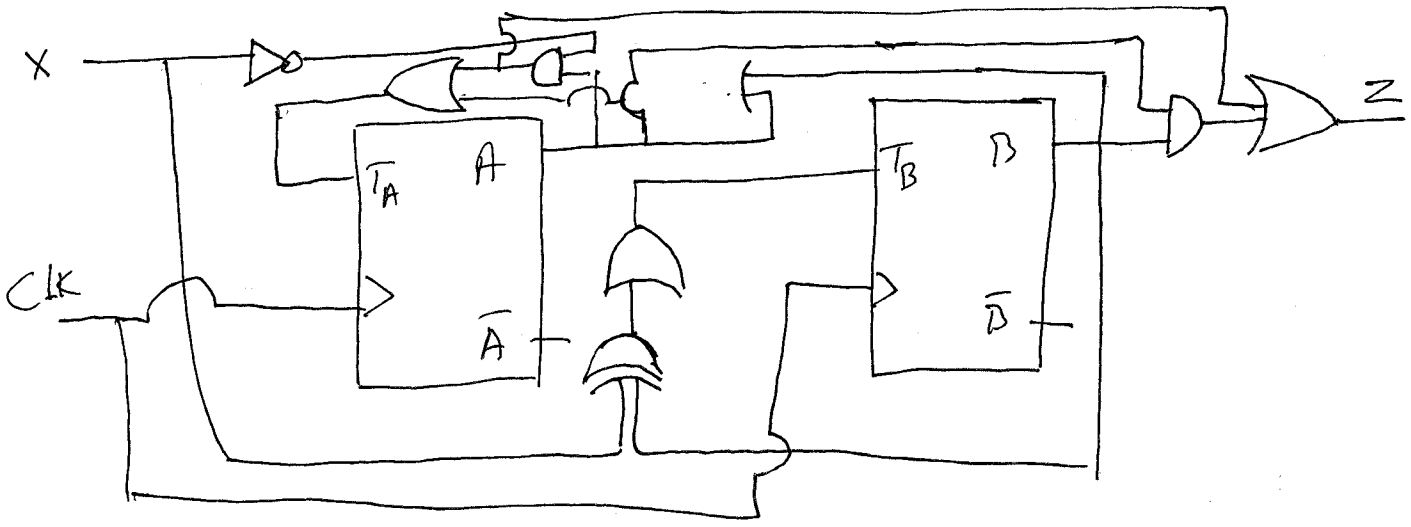
$T_A = \bar{A}\bar{B} + AB + \bar{x}A$

T_B

x \ AB	00	01	11	10
0	0	1	1	1
1	1	0	1	1

$T_B = AB + \bar{x}A$

circuit Diagram

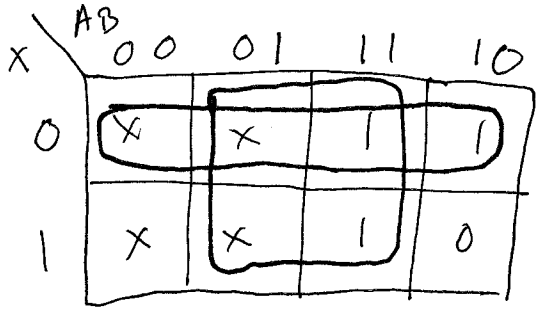


(iv) J K Flip-flop

A	B	A^*	B^*	A^*	B^*	J_A	K_A	J_B	K_B	J_A	K_B	J_B	K_B	x=0	x=1
0	0	1	0	1	1	1	x	0	x	1	x	1	x	0	0
0	1	0	0	0	1	0	x	x	1	0	x	x	0	0	0
1	0	0	1	1	1	x	1	1	x	x	0	1	x	1	0
1	1	0	0	0	0	x	1	0	1	x	1	x	1	1	1

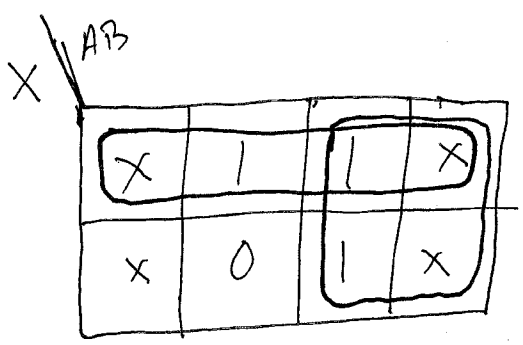
K-Map

K_A



$K_A = \bar{X} + B$

K_B



$K_B = \bar{X} + A$

J_A

X \ AB	00	01	11	10
0	1	0	x	x
1	1	0	x	x

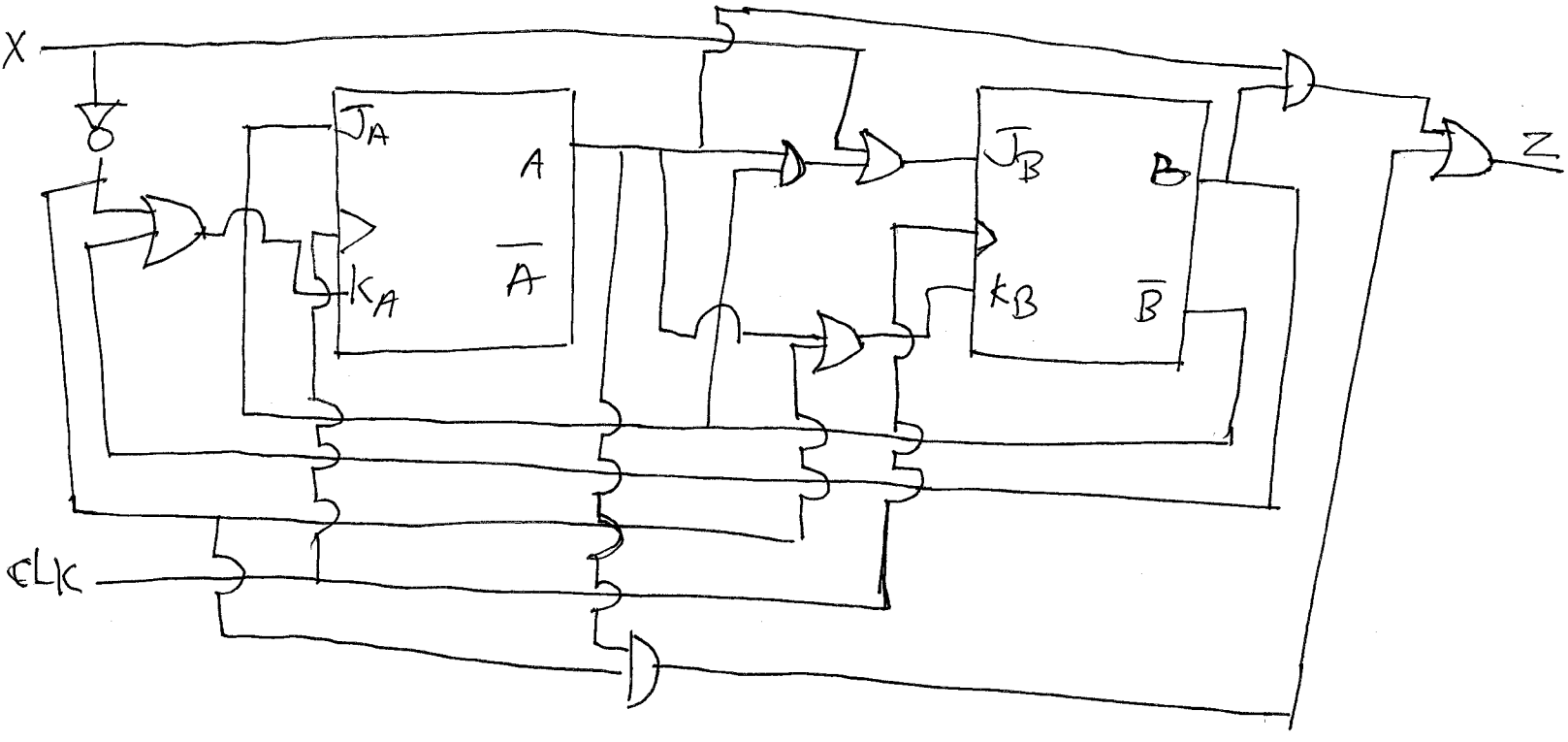
$J_A = \bar{B}$

J_B

X \ AB	00	01	11	10
0	0	x	0	1
1	1	x	x	1

$J_B = X + A\bar{B}$

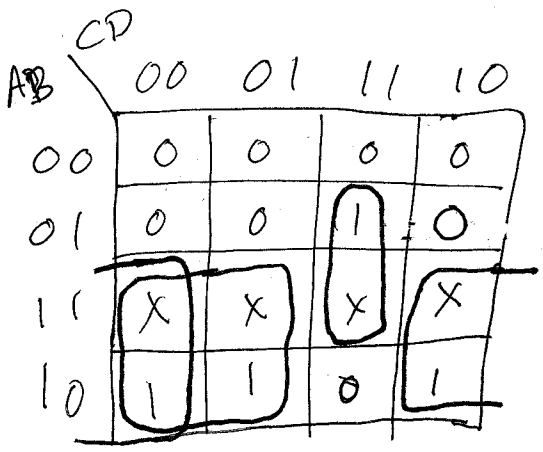
Circuit Diagram



Chapter 7, problem 7a: Design a synchronous base-12 counter using D-flip-flops.

Present state				Next state				Required D inputs			
A	B	C	D	A	B	C	D	D_A	D_B	D_C	D_D
0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	1	0	0	0	1	0	0	1	0
0	0	1	0	0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	1	0	1	0	0
0	1	0	0	0	1	0	0	0	1	0	1
0	1	0	1	0	1	0	1	0	1	1	0
0	1	1	0	0	1	1	0	0	1	1	1
0	1	1	1	0	1	1	1	1	0	0	0
1	0	0	0	1	0	0	0	1	0	0	1
1	0	0	1	1	0	0	1	1	0	1	0
1	0	1	0	1	0	1	0	1	0	1	1
1	0	1	1	1	0	1	1	0	1	0	0

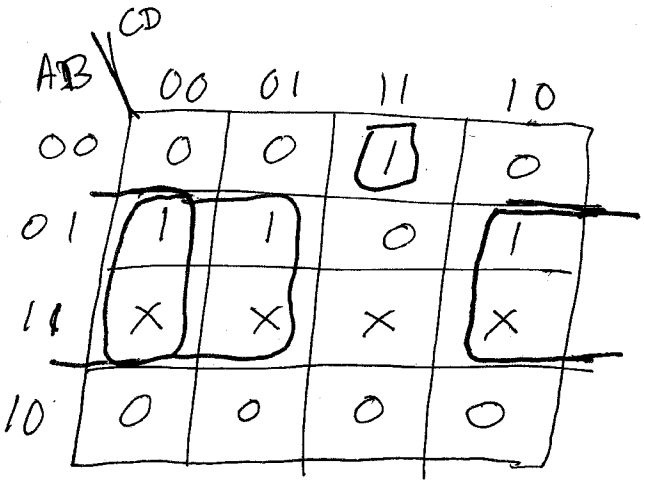
D_A



AB \ CD	00	01	11	10
00	0	0	0	0
01	0	0	1	0
11	X	X	X	X
10	1	1	0	1

$D_A = BCD + A\bar{C} + A\bar{D}$

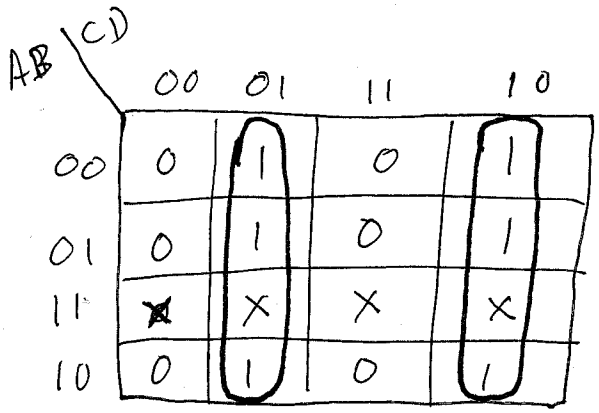
D_B



AB \ CD	00	01	11	10
00	0	0	1	0
01	1	1	0	1
11	X	X	X	X
10	0	0	0	0

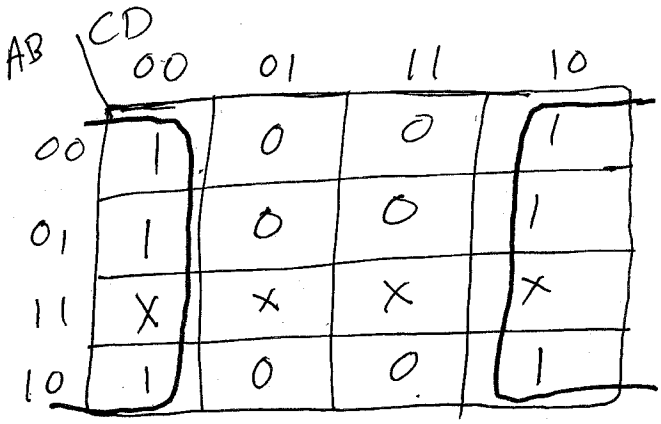
$D_B = A'B'CD + B\bar{D} + B\bar{C}$

D_C



AB \ CD	00	01	11	10
00	0	1	0	1
01	0	1	0	1
11	X	X	X	X
10	0	1	0	1

$D_C = \bar{C}D + \overline{C\bar{D}}$



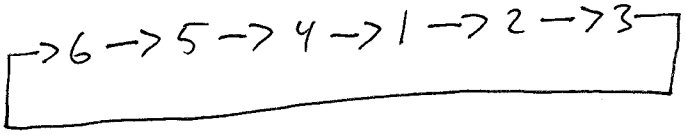
AB \ CD	00	01	11	10
00	1	0	0	1
01	1	0	0	1
11	X	X	X	X
10	1	0	0	1

$D_D = \overline{D}$

Chapter 7, Problem 8c: Design a synchronous counter that goes through the following sequence.

6 5 4 1 2 3 and repeat

using JK and D flip flops. Show a state diagram, indicating what happened if it initially is in one of the unused states



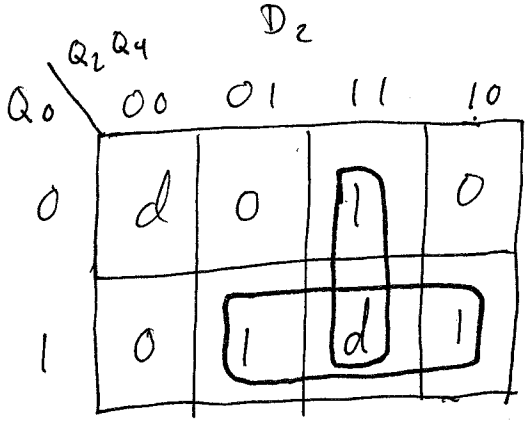
Flip flops: -3

Q_2	Q_1	Q_0	D_2	D_1	D_0
0	0	0	d	d	d
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	1	0	1
1	1	1	d	d	d

For D - Flip-flop

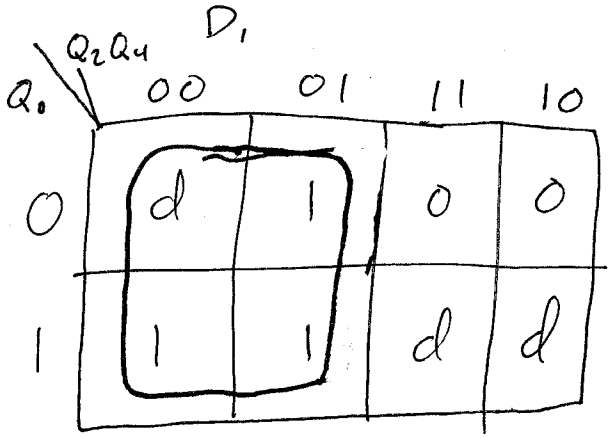
k-Map

D_2



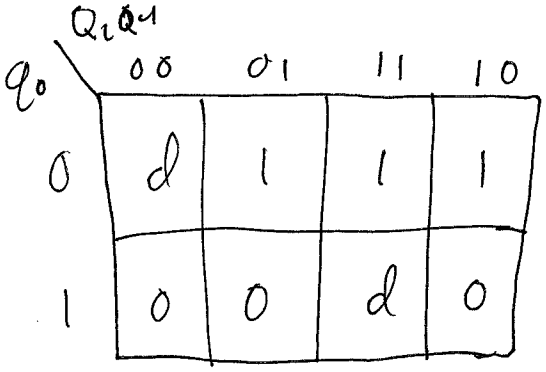
$D_2 = Q_2Q_4 + Q_0Q_4 + Q_2Q_0$

D_1

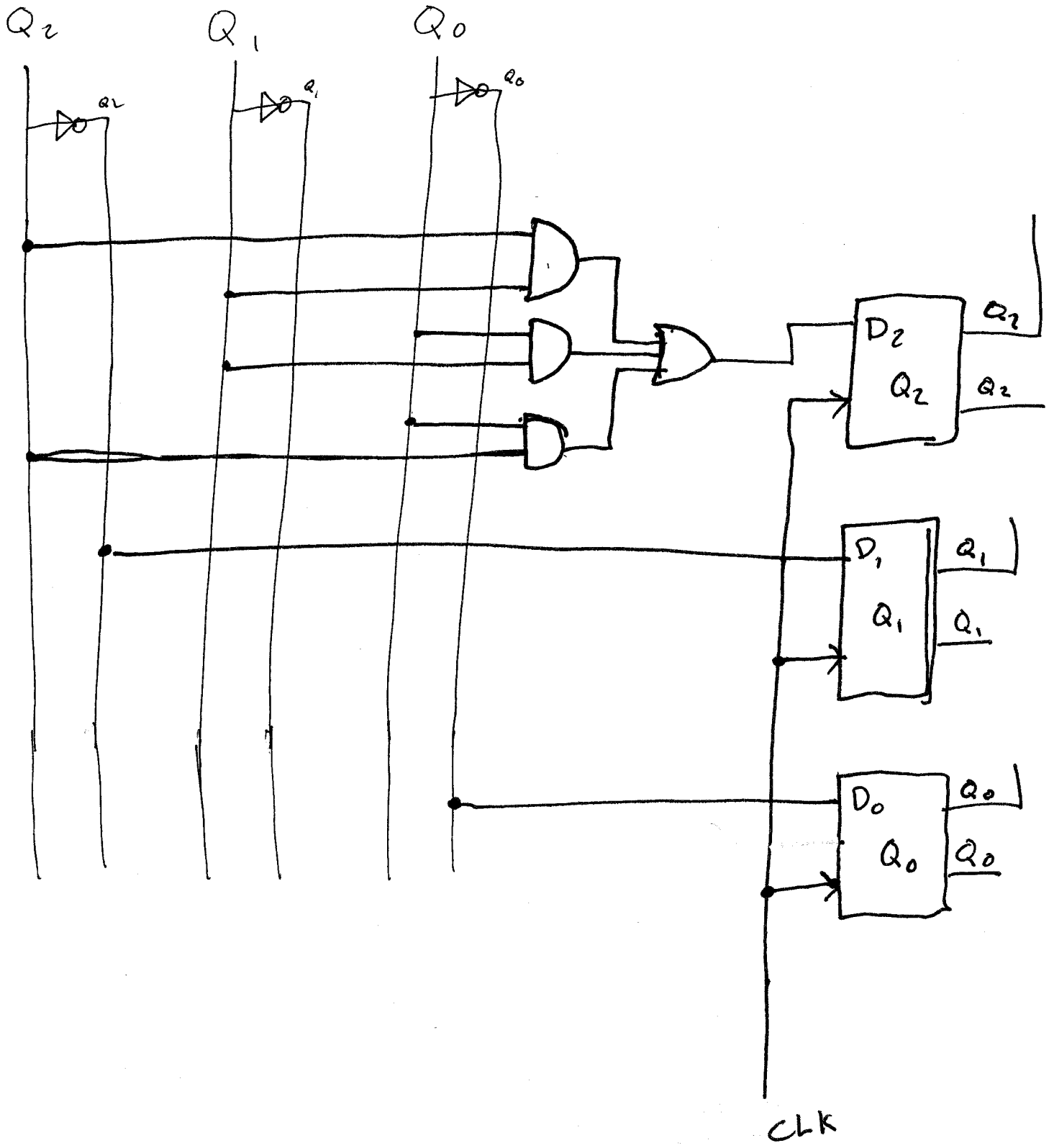


$D_1 = Q_2$

D_0



$D_0 = Q_0$


Q2
Q1
Q0
D2
Q2
D1
Q1
D0
Q0
CLK

JK Flip Flop

Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	J_2	K_2	J_1	K_1	J_0	K_0
0	0	0	d	d	d	d	d	d	d	d	d
0	0	1	0	1	0	0	d	1	d	d	1
0	1	0	0	1	1	0	d	d	0	1	d
0	1	1	1	1	0	1	d	d	0	d	1
1	0	0	0	0	1	d	1	0	d	1	d
1	0	1	1	0	0	d	0	0	d	d	1
1	1	0	1	0	1	d	0	d	1	1	d
1	1	1	d	d	d	d	d	d	d	d	d

J_2

Q_0 \ Q_2Q_1	00	01	11	10
0	d	0	d	d
1	0	1	d	d

$J_2 = Q_1 Q_0$

K_2

Q_0 \ Q_2Q_1	00	01	11	10
0	d	d	0	1
1	d	d	d	0

$K_2 = \bar{Q}_1 \bar{Q}_0$

J_1

Q_0 \ Q_2Q_4	00	01	11	10
0	d	d	d	0
1	1	d	d	0

$J_1 = \bar{Q}_2$

K_1

Q_0 \ Q_2Q_4	00	01	11	10
0	d	0	1	d
1	d	0	d	d

$K_1 = Q_2$

J_0

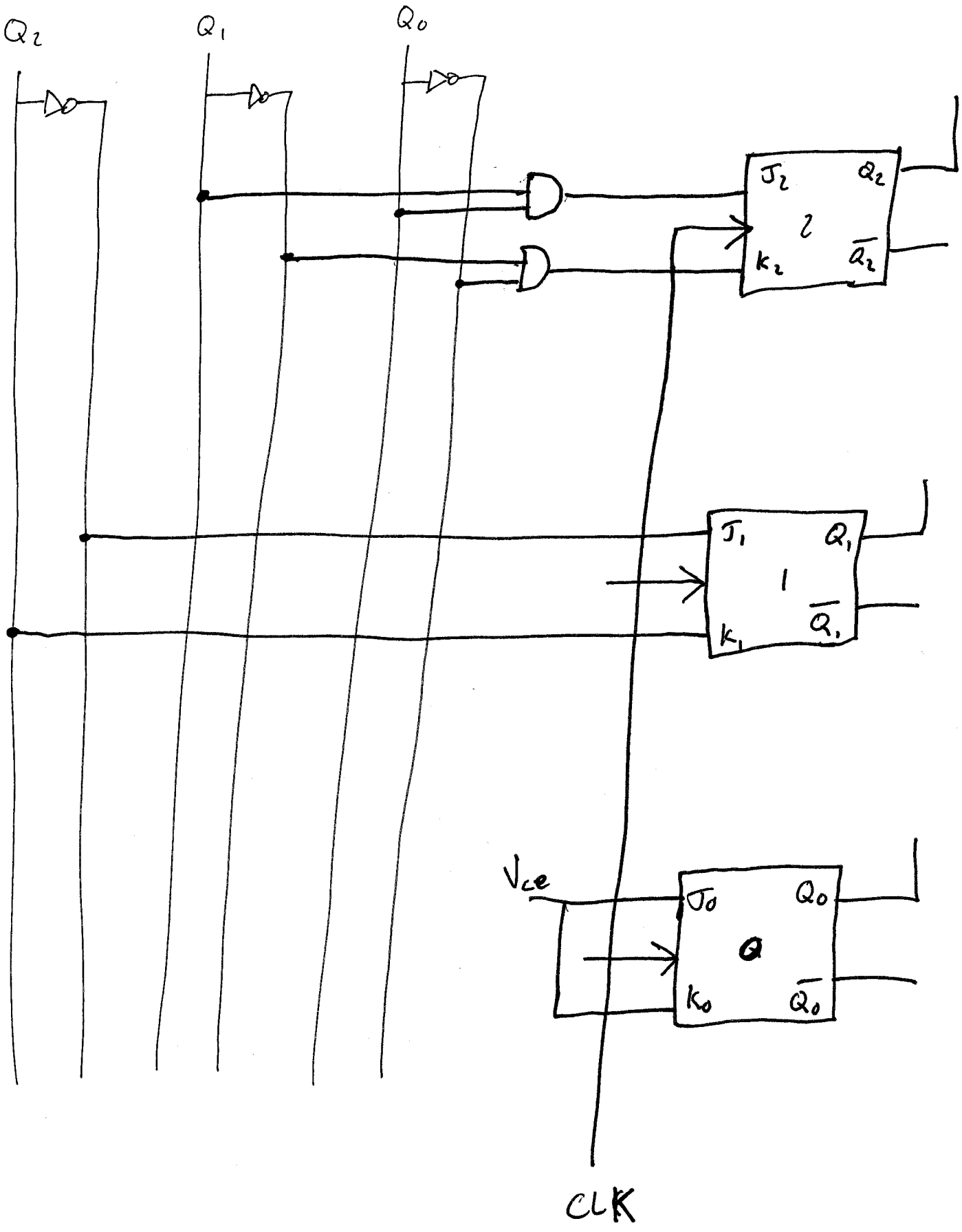
Q_0 \ Q_2Q_4	00	01	11	10
0	d	1	1	1
1	d	d	d	d

$J_0 = 1$

K_0

Q_0 \ Q_2Q_4	00	01	11	10
0	d	d	d	d
1	1	1	d	1

$K_0 = 1$

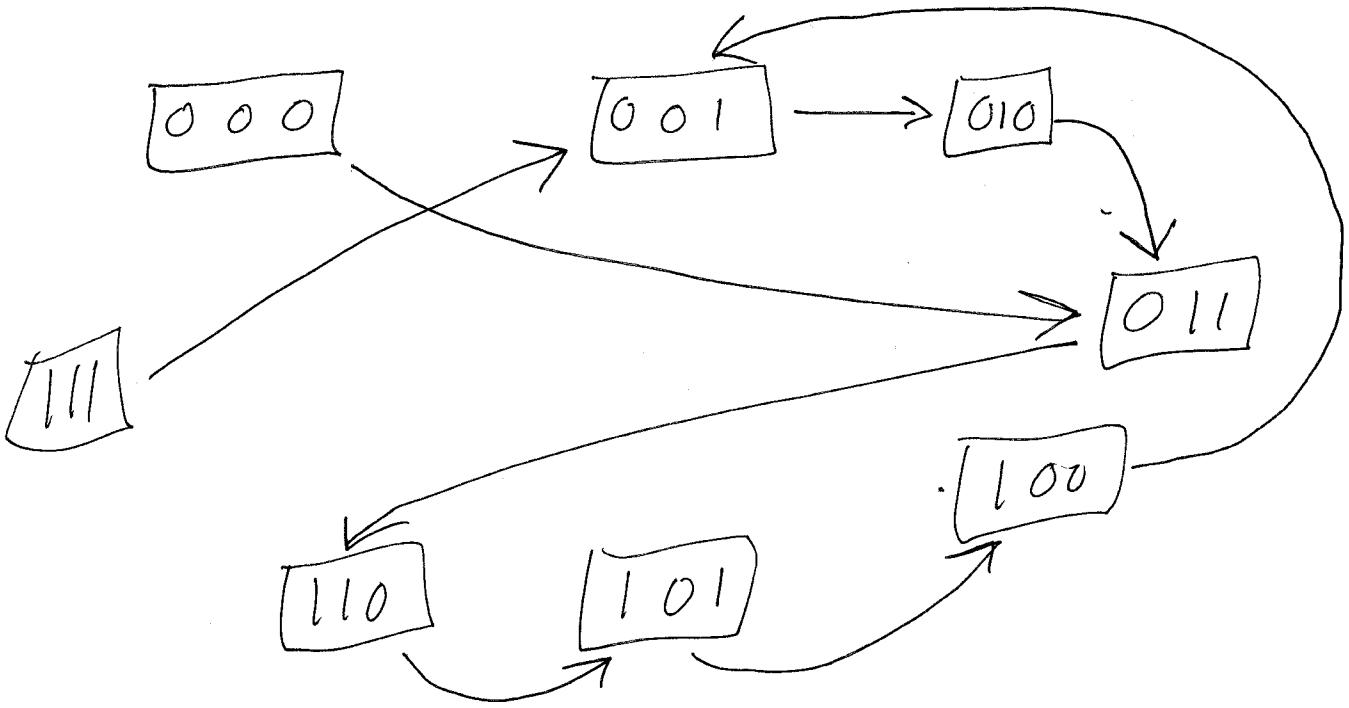

Q_2
Q_1
Q_0
J_2
Q_2
1
K_2
$\overline{Q_2}$
J_1
Q_1
1
K_1
$\overline{Q_1}$
V_{cc}
J_0
Q_0
1
K_0
$\overline{Q_0}$
CLK

$$D_2 = Q_2 Q_1 + Q_0 Q_1 + Q_2 Q_0$$

$$D_1 = \bar{Q}_2$$

$$D_0 = \overline{Q_0}$$

Q_2	Q_1	Q_0	D_2	D_1	D_0
0	0	0	0	1	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	1	0	1
1	1	1	1	0	0



Chapter 7, problem 10a: Design a counter with two JK flip-flops (A and B) and an input (x) that counts 0 1 2 3 0 ... when x = 0 and counts 0 1 2 0 when x = 1. Design this assuming that x is never 1 when the count is 3. Show minimum equations for each.

Truth Table =>

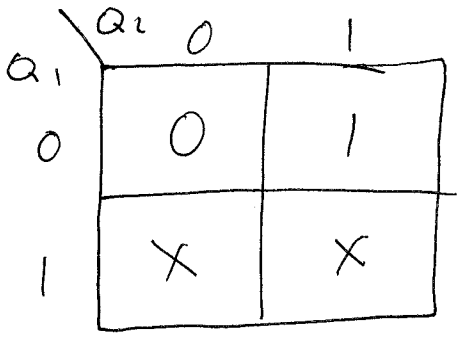
J	K	Q	$\bar{Q}$
0	0	Q	Q
0	1	0	1
1	0	1	0
1	1	$\bar{Q}$	$\bar{Q}$

Excitation Table =>

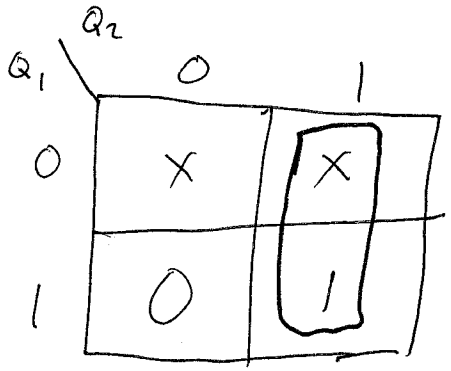
Q	$\bar{Q}$	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

2-Bit counter for $X = 0$

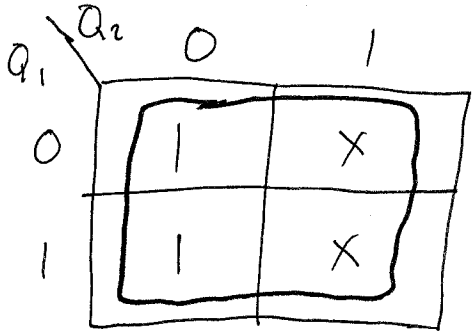
Q_1	Q_2	Q_1^*	Q_2^*	J_1	K_1	J_2	K_2
0	0	0	1	0	X	1	X
0	1	1	0	1	X	X	1
1	0	1	1	X	0	1	X
1	1	0	0	X	1	X	1



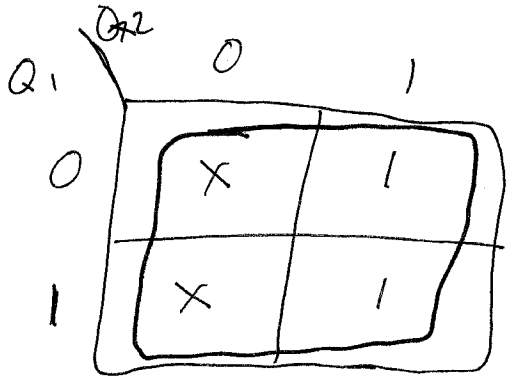
$J_1 = Q_2$



$K_1 = Q_2$



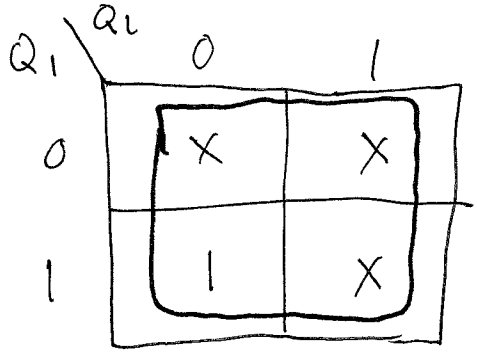
$J_2 = 1$



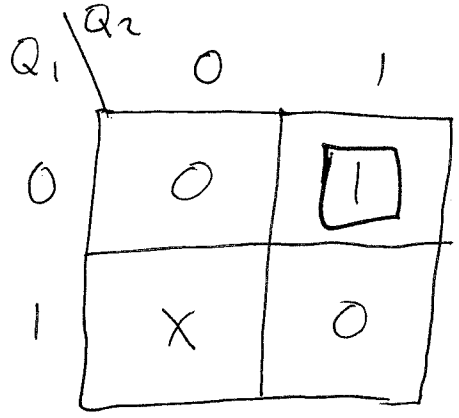
$K_2 = 1$

for $x = 1$

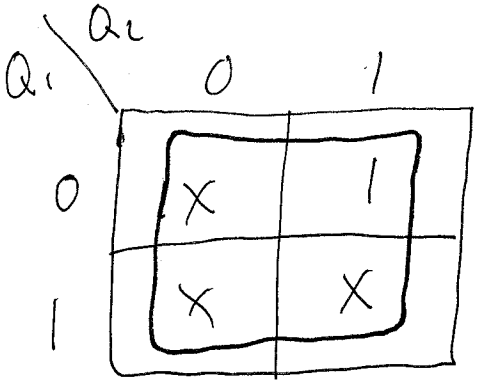
Q_1	Q_2	Q_1	Q_2	J_1	K_1	J_2	K_2
1	1	1	0	x	0	x	1
1	0	0	1	x	1	1	x
0	1	1	1	1	x	x	0
1	1	0	0	x	0	x	1



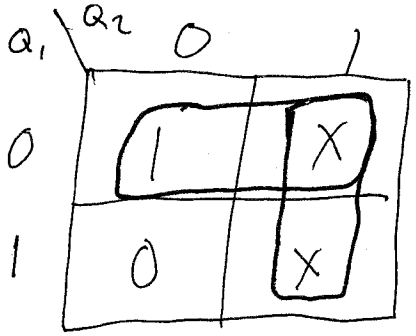
$J_1 = 1$



$K = \bar{Q}_1 Q_2$

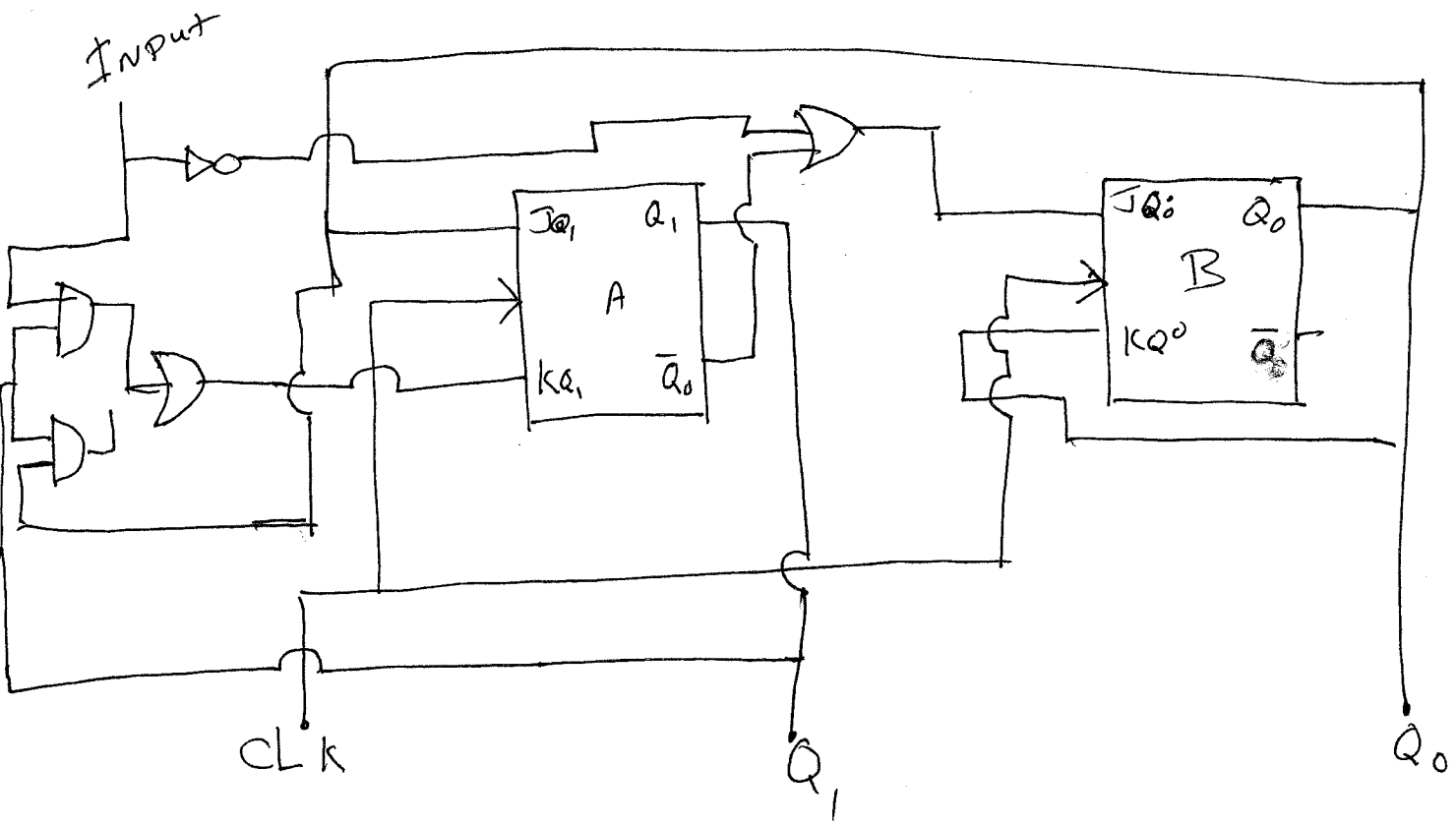


$J_2 = 1$



$K_2 = \bar{Q}_1 + Q_2$

Circuit



Chapter 7, Problem 16: For each of the following problems show a state table or a state diagram

(a) A moore system that produces a 1 output iff the input has been 0 for at least two consecutive clocks followed immediately by two or more consecutive 1's (five states)

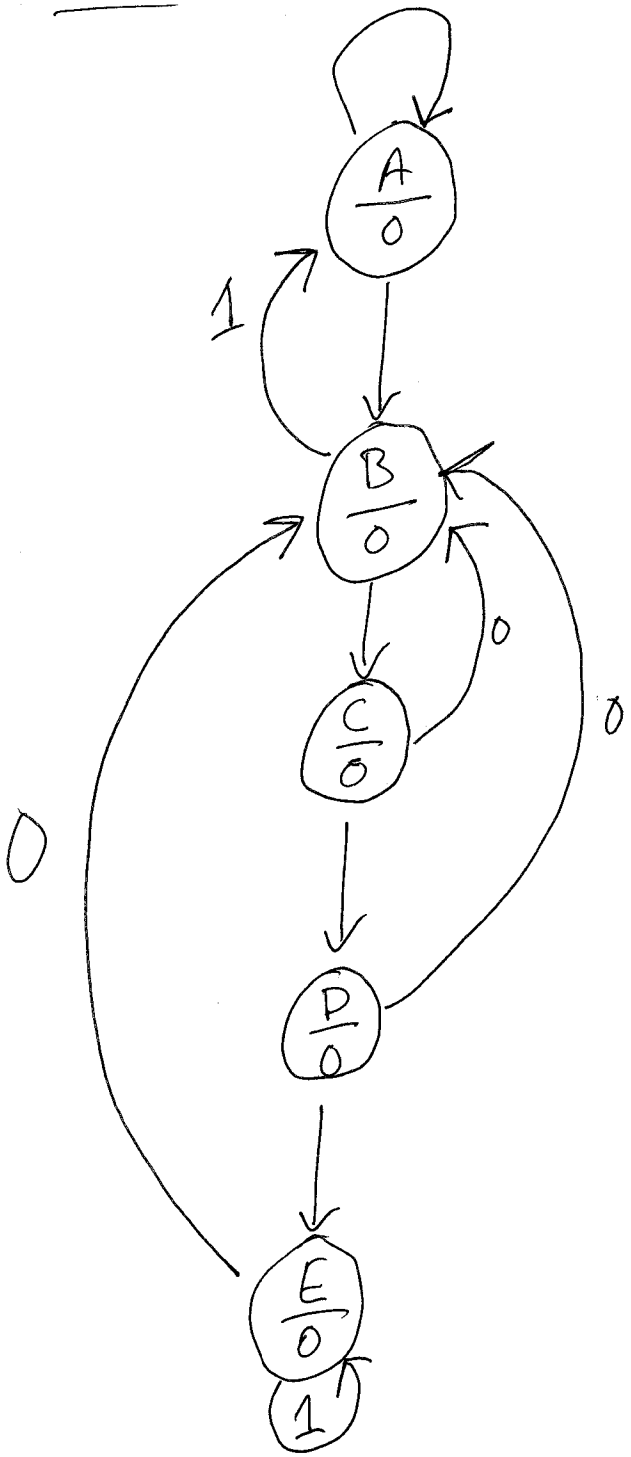
(c) A Mealy system that produces a 1 output iff the input has been 1 for three or more consecutive clock times or 0 for three or more consecutive clock times. When first turned on, it is in an initial state S_0. (There are four additional states).

(a)

X 0 1 0 0 1 0 0 1 1 0 0 0 1 0 1 0 0 0 1 1 1 1 0

Z 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 1 1 0 0

State Diagram



(b)

State	Meaning	A B C	X = 0	X = 1
S_0	Reset No "1" Received	0 0 0	0	0
S_1	Single "0" Received	0 0 1	0	0
S_2	Single "1" Received	0 1 0	0	0
S_3	Two or more "0" Received in sequence	0 1 1	1	0
S_4	Two or more "1" received in sequence	1 0 0	0	1

Transition Diagram