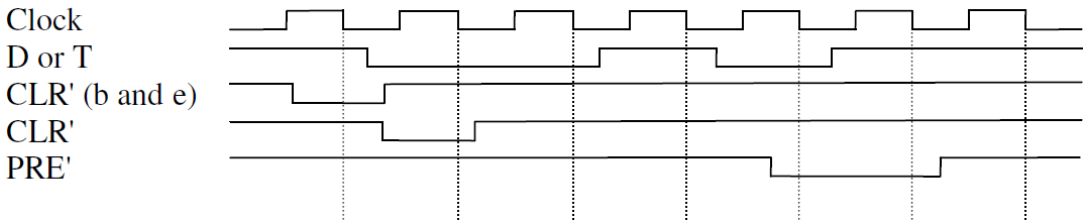
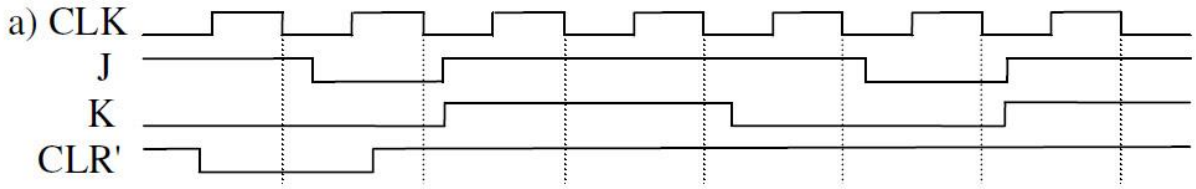
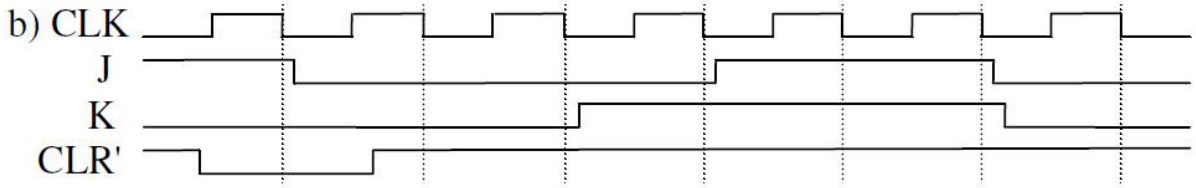
Chapter 6, problem 3c,d,e: (5 + 5 + 5 pts) For the input shown below, show the flip flop outputs.

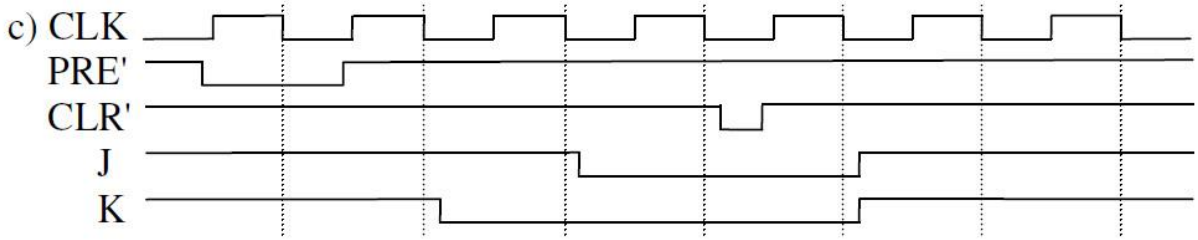
a. Assume that the flip flop is a D flip flop without a clear or preset.
b. Assume that the flip flop is a D flip flop with an active low clear.
c. Assume that the flip flop is a D flip flop with active low clear and preset inputs.
d. Assume that the flip flop is a T flip flop with the same input as part a, and that Q is initially 0.
e. Assume that the flip flop is a T flip flop with an active low clear and the same inputs as part b.



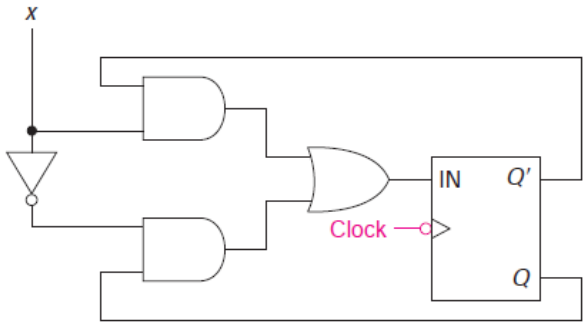
Chapter 6, problem 4: (15 pts) For a negative-edge triggered JK flip flop with active-low Preset and Clear inputs (74112), complete each individual timing diagram with the output Q:





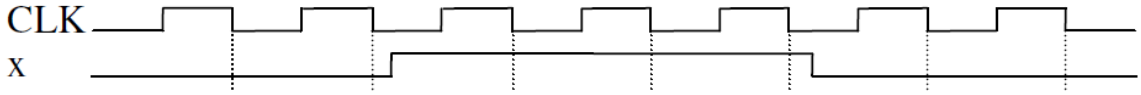


Chapter 6, problem 5: (10 pts) Considering the following circuit, complete the timing diagram if the flip flop is:



a) a D flip-flop (assume Q = 0 initially)

b) a T flip-flop (assume Q = 0 initially)



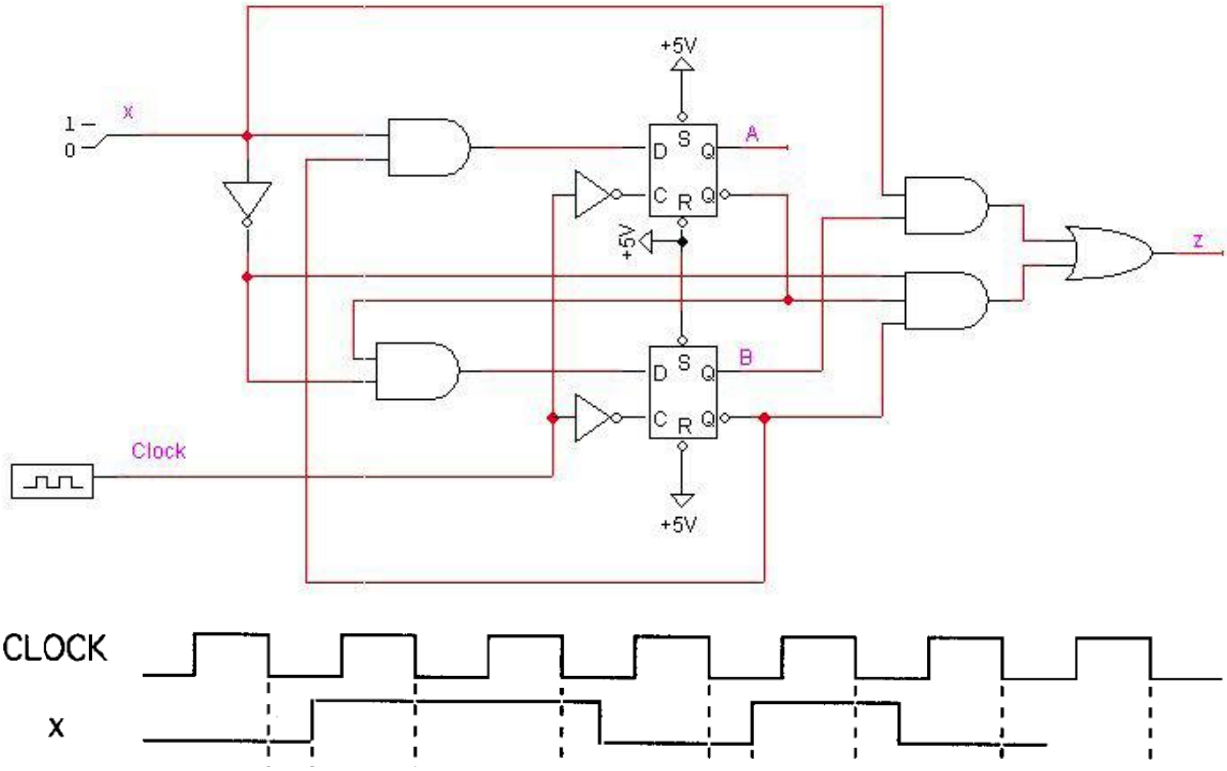
Chapter 6, problem 6: (10 pts) We have a new type of flip flop with inputs A and B. if A = 0, then Q* = B; if A = 1, Q* = B'.

a) Show the state diagram for this flip flop.

b) Write an equation for Q* in terms of A, B and Q.

Chapter 6, problem 7: (10 pts) For each of the following circuits, complete the timing diagram for the state of each flip flop and the output, where shown. All flip flops are trailing-edge triggered. For those circuits in which there is no clear input, assume each flip flop starts at 0.

(a)

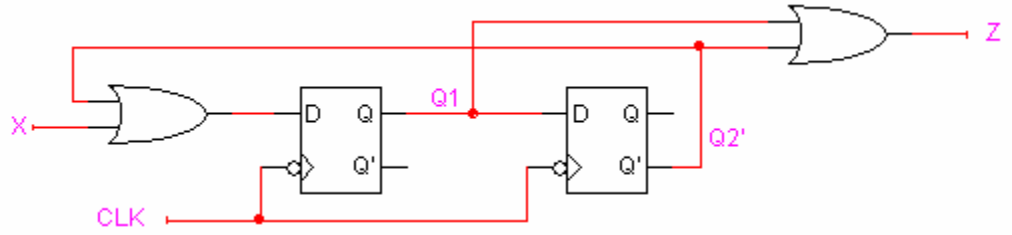


Chapter 6, problem 8: (10 pts) For the following circuit and input string:

i. Construct a state table (calling the states 00, 01, 10, 11).

ii. Show a timing trace for the flip-flops and the output as far as possible. Assume that the initial value of each flip flop is 0.

a)



x 001100110