EEE 120

Lab 0 Answer Sheet (Online Class)

Tutorial: Using Digital

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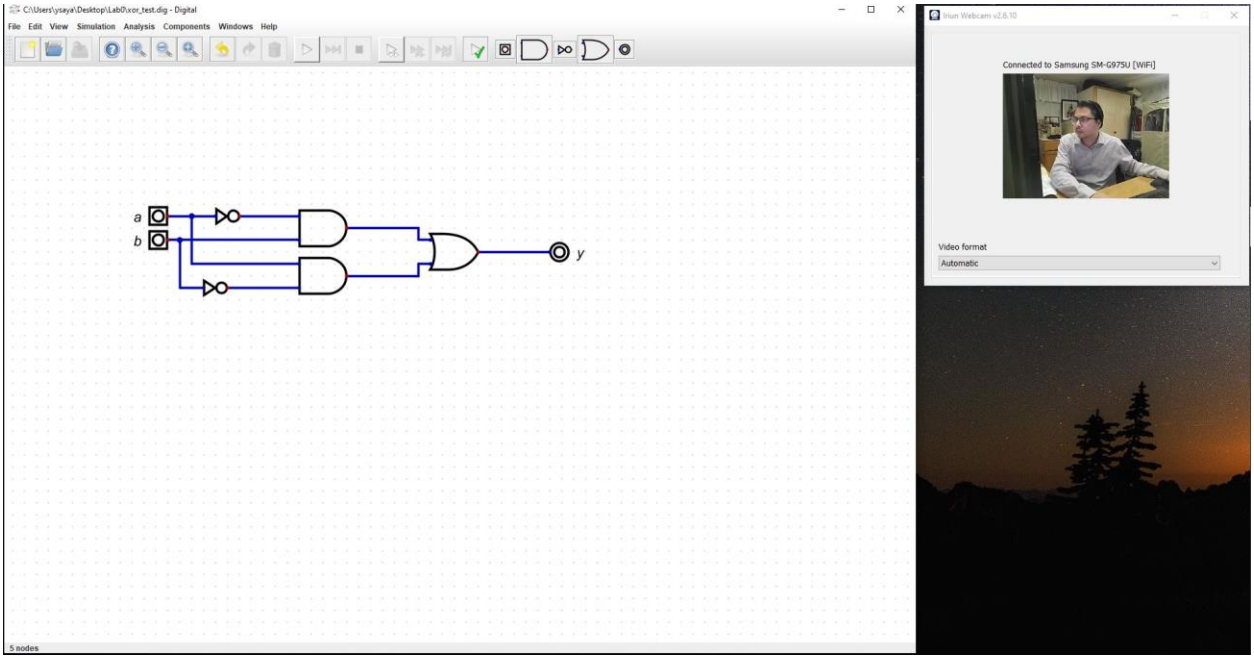
Semester/Year/Session (A/B): Spring 2022 Session A Date: 01/16/2022

Task 0-1: Build a 2-input XOR gate using AND/OR/NOT gates in Digital

Include a picture of your Digital circuit here:

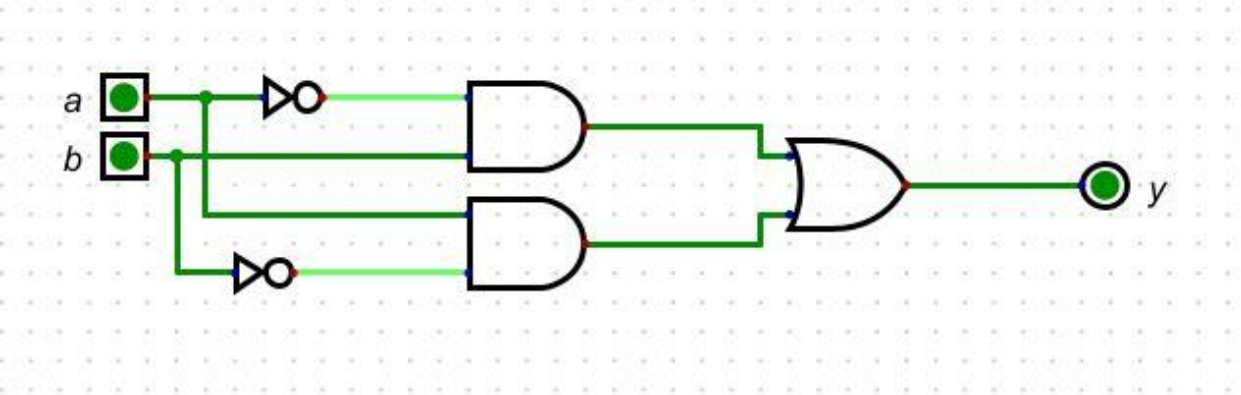


Please comment on the single biggest issue you were facing when designing the circuit.

The biggest issue is putting the a, b and y into the circuit. I had to re-read the directions on the assignment sheet to figure it out. I was looking for the symbols in the tabs.

Task 0-2: Simulate the design in visually in Digital

Include a picture of your simulated circuit here (only one picture with any combination of inputs you choose):



Try several input combinations from the truth table. Do you get the expected output when feeding these inputs? (Y/N) N

Task 0-3: Export the design and simulate in Verilog

Include a picture of your GTKWave simulation (timing diagram) here:

Please answer the following questions:

1. How do you expect the output of a 2-input XOR gate to behave? It's true when one input is true.
2. What tests did you perform to verify your logic circuit? I performed a waveform simulation to test the logic circuit.
3. Did the circuit behave as expected? If no, what was wrong? Yes, it did behave as expected.

Task 0-4: [Optional/Ungraded] Create a video and submit your report

[This task is useful to get partial credit if your schematic is not working. Take advantage of it to explain to the grader your understanding of the circuit. More importantly, explain where you think the mistake is in and what you would do if you were given more time to fix it.]

Record a short video showing your schematic in Digital and your waveforms in GTKWave. Be sure to show yourself in the video and show your screen. **Upload the video to your Google Drive (personal one or ASU one). Copy and paste the sharing link to that video here. Make sure the link is working and pointing to the correct video. Do NOT upload your video to YouTube.** If your circuit is not working as expected, explain in the video how it is not working and where you expect the mistake to be from.

Video Link:
https://drive.google.com/file/d/19mcuirmbZ_kn0YdVUdF14f1fwoGqBqrX/view?usp=sharing

At the beginning of your recording, say your name, the task number and circuit name. Be brief in your recording. Submit the completed template to Canvas.

Make sure all your files are in the Lab0 directory. Create a zip file of the Lab0 directory. Remember to turn in the zip file and your completed template on Canvas! Make sure you upload the template before the zip file.

LAB 0: LAB REPORT GRADE SHEET

Name Yengkong Sayaovong

Instructor Assessment

Grading Criteria	Max Points	Points Lost
Description of Assigned Tasks, Work Performed & Outcomes Met		
Task 0-1: Build a 2-input XOR gate using AND/OR/NOT gates in Intel Quartus	10	
Task 0-2: Simulate the design visually in Digital	10	
Task 0-3: Export the design and simulate in Verilog	20	
Task 0-4: Create a video and submit your report	0	
Lab Score (40 points total)	**Points Lost**	
	Late Lab	
	Lab Score	