Lab 0: Introduction to the EEE120/CSE120 Lab Tools

Prerequisites: Before beginning this lab, you must:

- Understand AND, OR, and NOT gates
- Understand the Exclusive-OR (XOR) logic function
- Know how to construct the XOR logic function using AND, OR, and NOT gates
- Have installed the required software on your computer (see separate instructions)

Equipment: Personal computer with the required software installed.

Files to download:

xor_stim.txt
xor_top.v

Objectives: When you have completed this lab, you will be able to:

- Create a new design and take it through the tool flow
- Design a digital logic circuit using gate primitives in schematic capture.
- Apply names to input and output signals.
- Export the schematic to Verilog.
- Simulate the circuit using a Verilog simulator.
- Create stimulus for the simulation.
- Create, and view, waveforms.

Introduction

The purpose of this lab is to get you acquainted as quickly as possible to the tool flow we'll be using in this course.

Task 0-1: Build a 2-input XOR gate using AND, OR, and NOT gates in Digital.

Create a folder named Lab0. We'll place all the files related to this lab in that folder.

Launch the Digital schematic entry tool, Digital.jar. It will open and you'll see the window on the following page. The use of the icons and menus in the window will be discussed as needed. Of course, you are always welcome to explore their uses – something you'll have to do on your own when out in industry!

NOTE: Digital.jar is not a normal application as it is based on Java. As a result, you may not be able to click on designs created by Digital to open them. You'll have to click on the Digital.jar icon. It may be simpler to put this on your Dock on Mac or create a convenient alias in Windows. Alternatively, from a command line, you can execute the command:

java -jar Digital.jar &

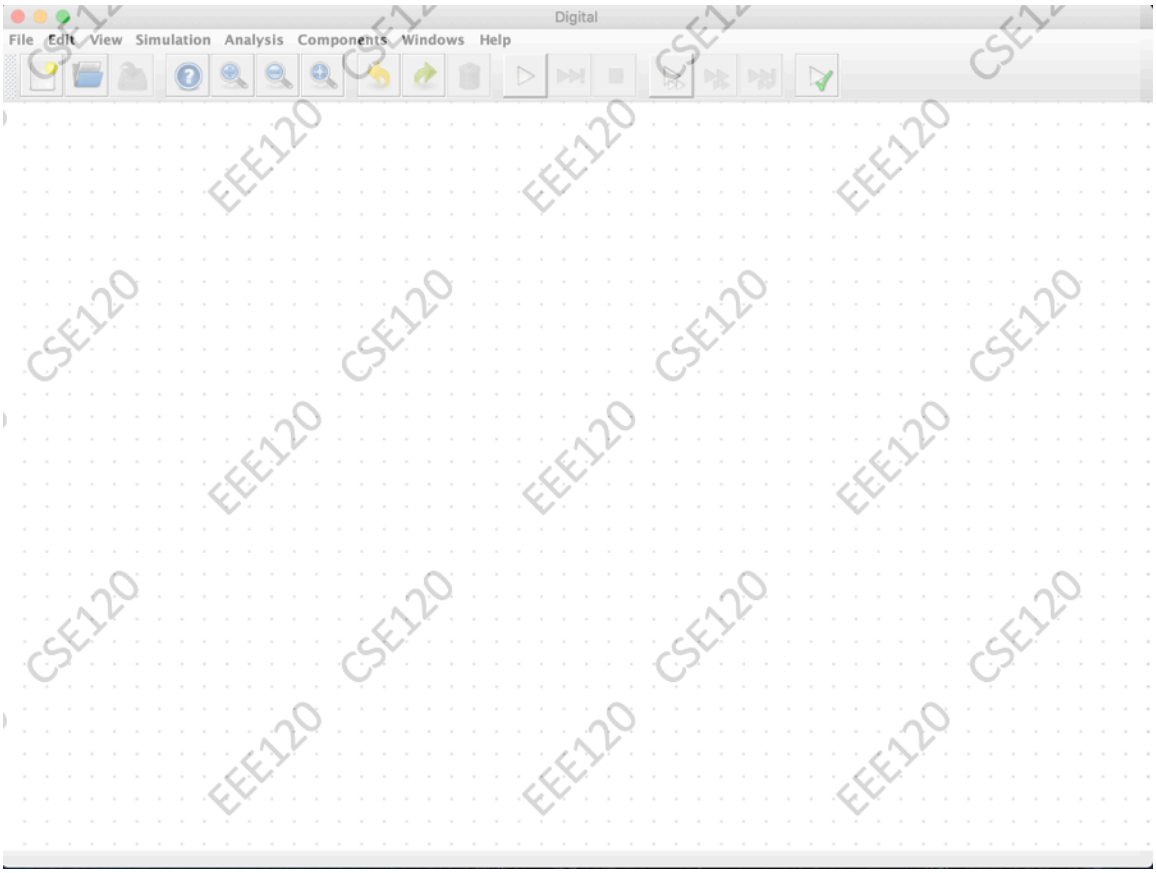

Figure 1. The Digital schematic entry window on startup.

This will work if you execute this in the folder where Digital.jar is located. The '&' at the end of the command causes Digital to run in the background so that you are still able to use the same terminal to do other things.

Otherwise, you must supply the path to Digital.jar. This example shows how to launch it if Digital.jar is installed in the Applications directory on the Mac:

java -jar /Applications/Digital/Digital.jar &

If Digital is elsewhere, then you'll need to supply the appropriate path.

Finally, if you've been working on your lab and save your file and want to reopen it later, you can add the name of the file:

java -jar /Applications/Digital/Digital.jar xor_test.dig &

We'll show you how to save your work down below.

A few tips. You can zoom in and out with the magnifying glass. Under the "View" menu, is the selection "Fit to Window" which will zoom to the level where your entire design will fit. (You

may find that “scrolling” up and down on your mouse will also zoom in and out!) If you’ve made a mistake, no worries – CMD-Z on Mac or CTRL-Z on Windows will undo changes. You can, as expected, copy and paste as well.

NOTE: If you quit Digital and want to start editing your design again, open Digital.jar and your design may appear, in which case you are good to go. Otherwise, under the File menu, select Open, navigate to your design file, which will end with .dig, and select it. Or, as shown above, start Digital from the command line in a terminal and specify the name of your .dig file.

If you try to open a file and can’t see it in the list but you know it’s there, type its name. As long as you’re in the correct directory, you should be able to open it. This is true for folder names as well. There is an issue with Digital/Java on some computers that makes some folders and files invisible in the area where you’d normally expect to see them. If this happens, type the name of the folder or file you would have selected in the “File Name” field and click Open.

Let’s now create the XOR function as shown in Figure 2.

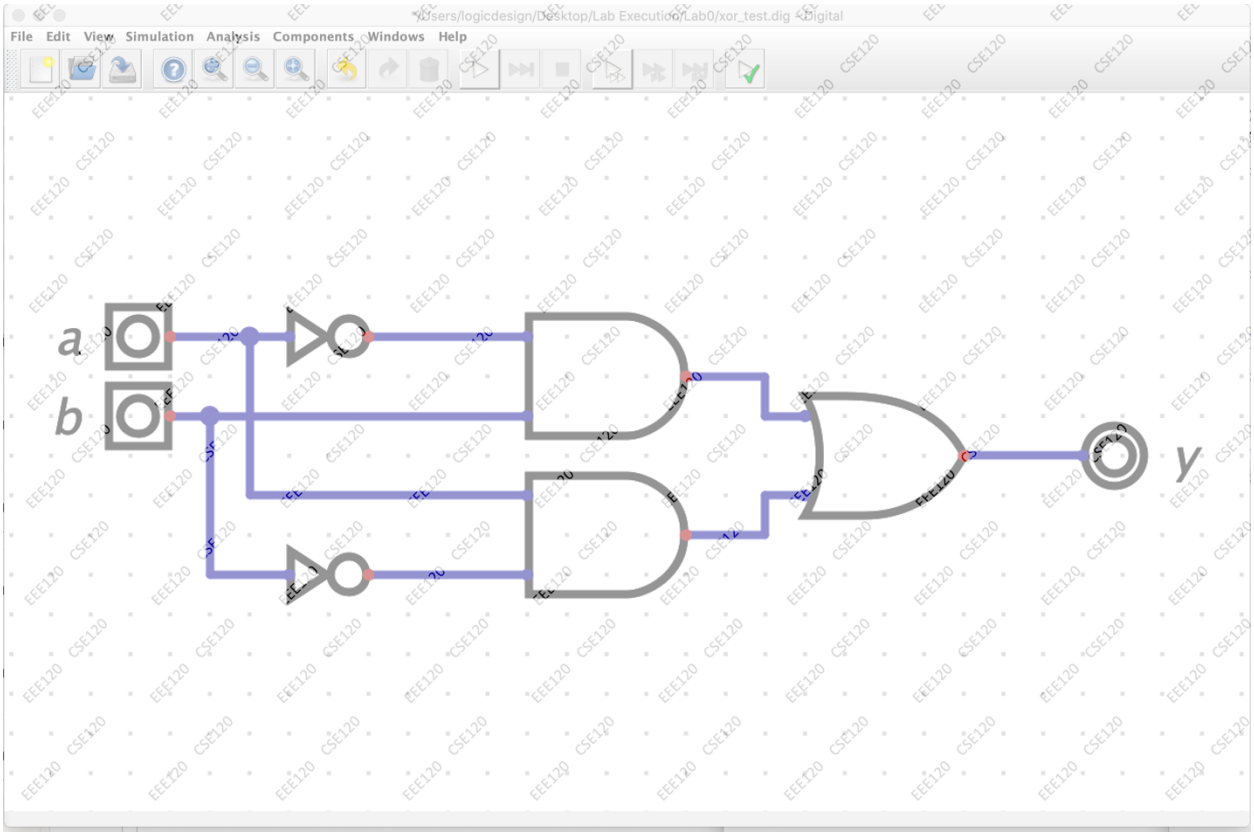

Figure 2. An Exclusive-OR built using AND, OR, and NOT gates.

First, let’s put in the AND gates. Click on the Components menu at the top of the window and select AND from the Logic submenu. An AND gate will appear as shown in Figure 3.

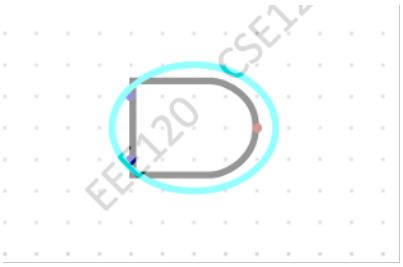

Figure 3. The AND gate appears in the window.

Click in the window where you want the AND gate to be placed. Then repeat these steps and place another AND gate below the first. You'll also notice that when you've used a component, an icon representing that component appears with the other icons near the top of the window. You can click on that icon to place another copy of the gate. Alternatively, you can select the first AND gate and duplicate it with CMD-d on Mac or CTRL-d on Windows, and then place the second AND gate. Finally, hitting the L key will allow you to place another copy of the last component you placed. Repeat these steps choosing an OR gate and two NOT gates so that your schematic is as shown in Figure 4. If you want to undo the most recent change, CMD-z on Mac or CTRL-z on Windows will do the trick.

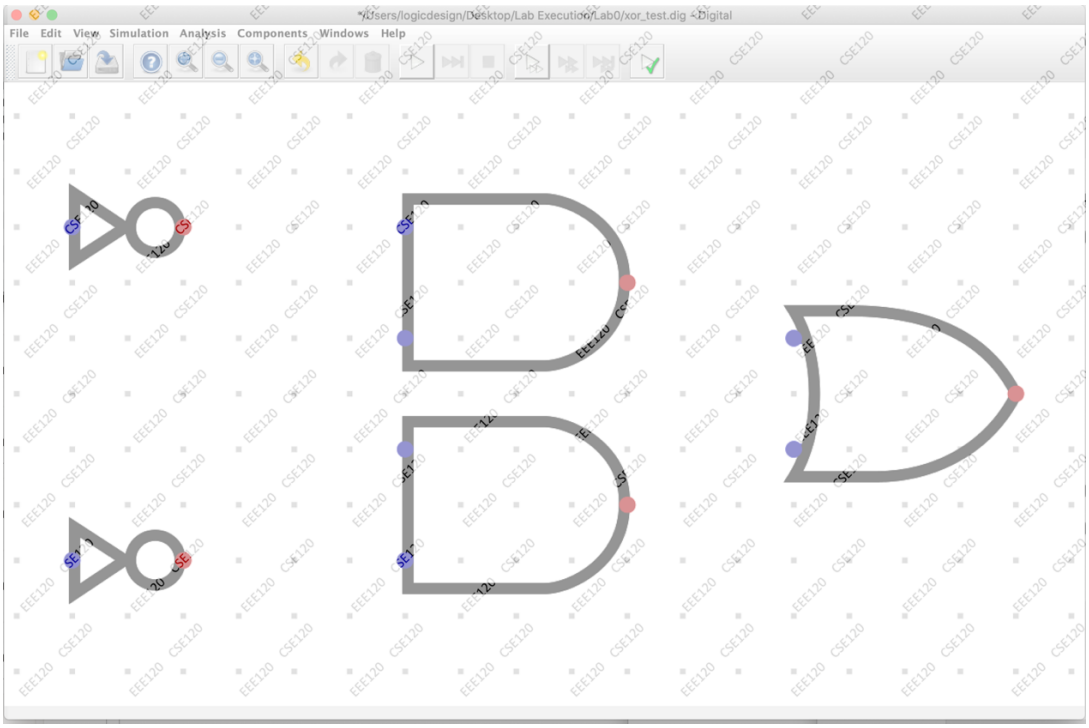

Figure 4. Logic gate placement.

Now we need to add the inputs and the output. Under the Components menu is another submenu, IO, which stands for Input Output. From this submenu, select the Input and place it in front of the upper inverter. Place another Input just below it. Then place an output to the right of the OR gate. For reference, see Figure 5. Notice that the shape of the input is square while the output is round.

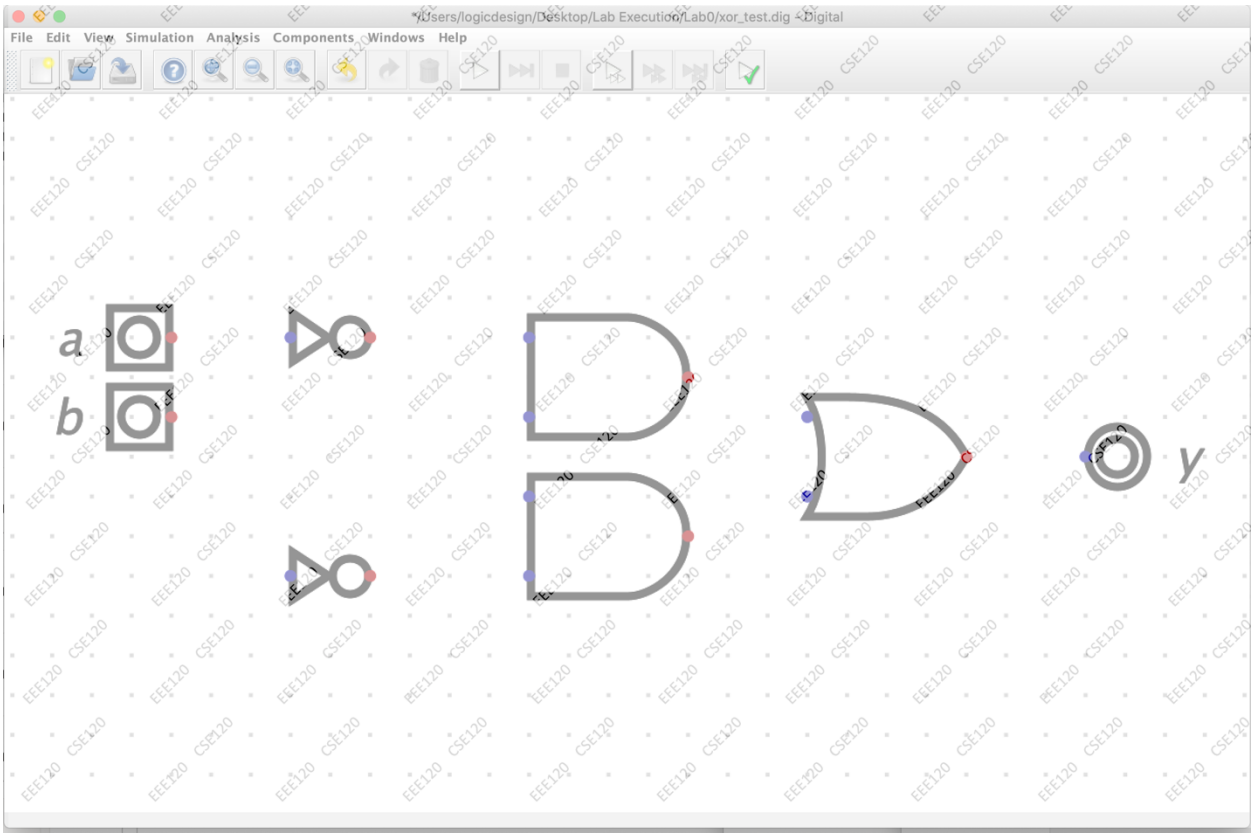

Figure 5. Input and Output pins have been added.

Next we need to connect the gates. Each of the items we've added have small colored pins on them. Red pins are outputs from the instances, blue pins are inputs. Click and release on a pin and move the mouse in the direction you want the connection to go. DO NOT CLICK AND DRAG! You must click and release – the wire will follow the mouse. If you want the wire to turn, click where you want the turn to be and head in a new direction. Finally, click on the pin of the gate you want to connect to. The wire will terminate when you click on another pin. When done, your design should look like the one in Figure 6. You can also terminate a wire at the last place you clicked by pressing the ESC key.

To connect a new wire to an existing wire, click on the existing wire where you want the connection to start and proceed as if you started on a pin.

Wires which cross each other but are not connected have no dot at the point where they cross. However, when wires which cross are connected, there is a dot.

Note: to delete a wire, use the mouse to select a region which includes at least one of the endpoints of the segment of the wire to be deleted. The segment(s) of the wire will then be highlighted and you can delete it. If you select a region where two wires are connected, as shown by a dot, then both wires will be deleted.

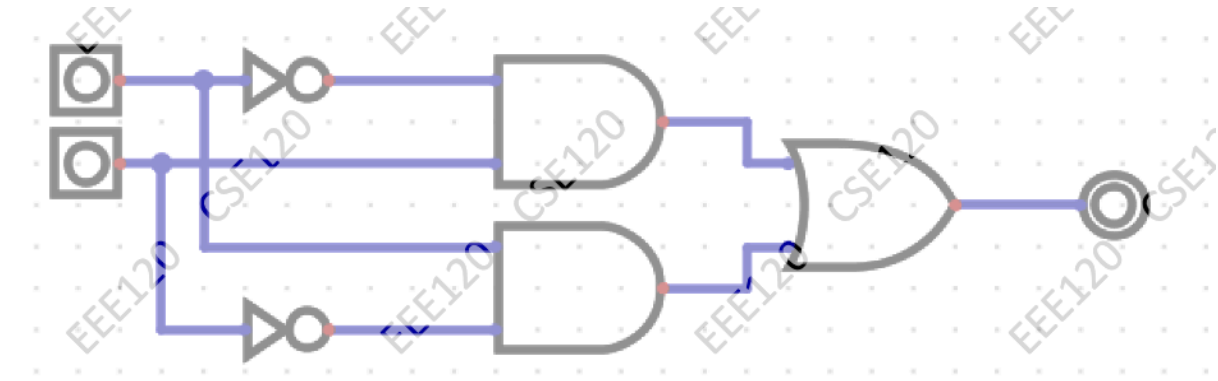

Figure 6. The wires have been added.

Finally, we need to name the inputs and the output. To bring up the window in Figure 7, right click on the upper input. On the Mac, holding the CTRL button, click on the upper input. In the Label field, name the input **a**.

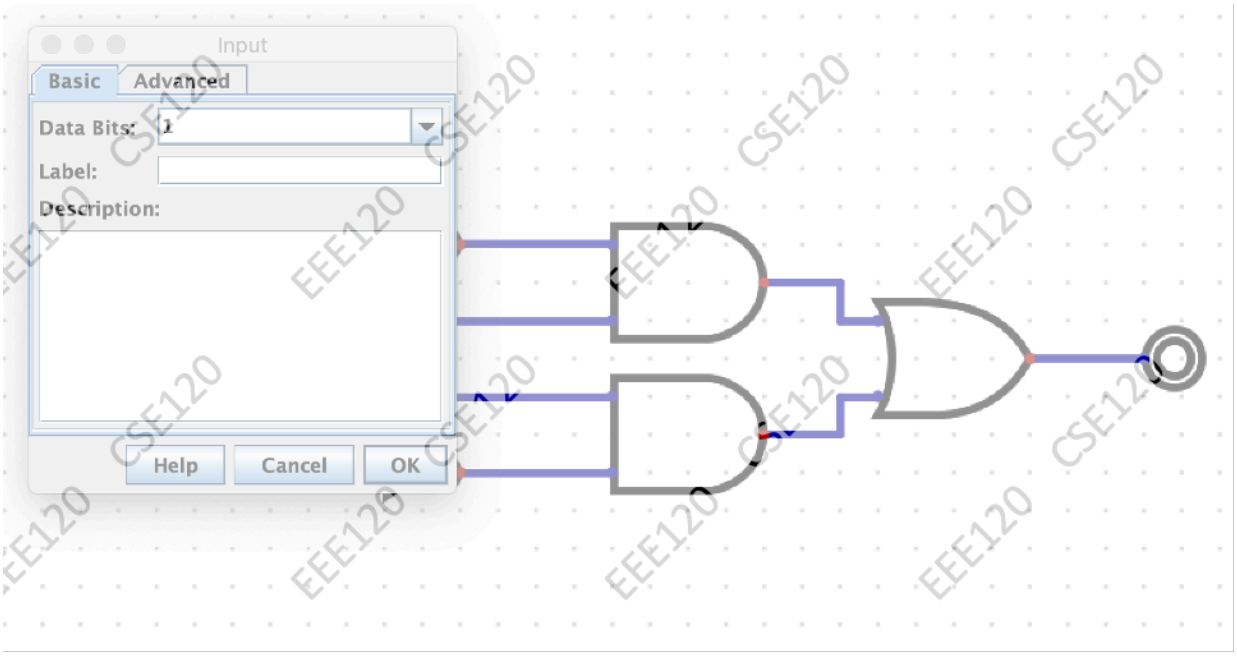

Figure 7. Configuring the input **a**.

In future, we may want to change the number of bits. However, in this lab, we'll leave that field alone and in the Label field put the letter **a**. Repeat the same steps for the other input, **b**, and the output, **y**. Your schematic should now be as shown in Figure 8.

IMPORTANT: In order for your simulations to work, you MUST use the names specified for inputs, outputs, and design files.

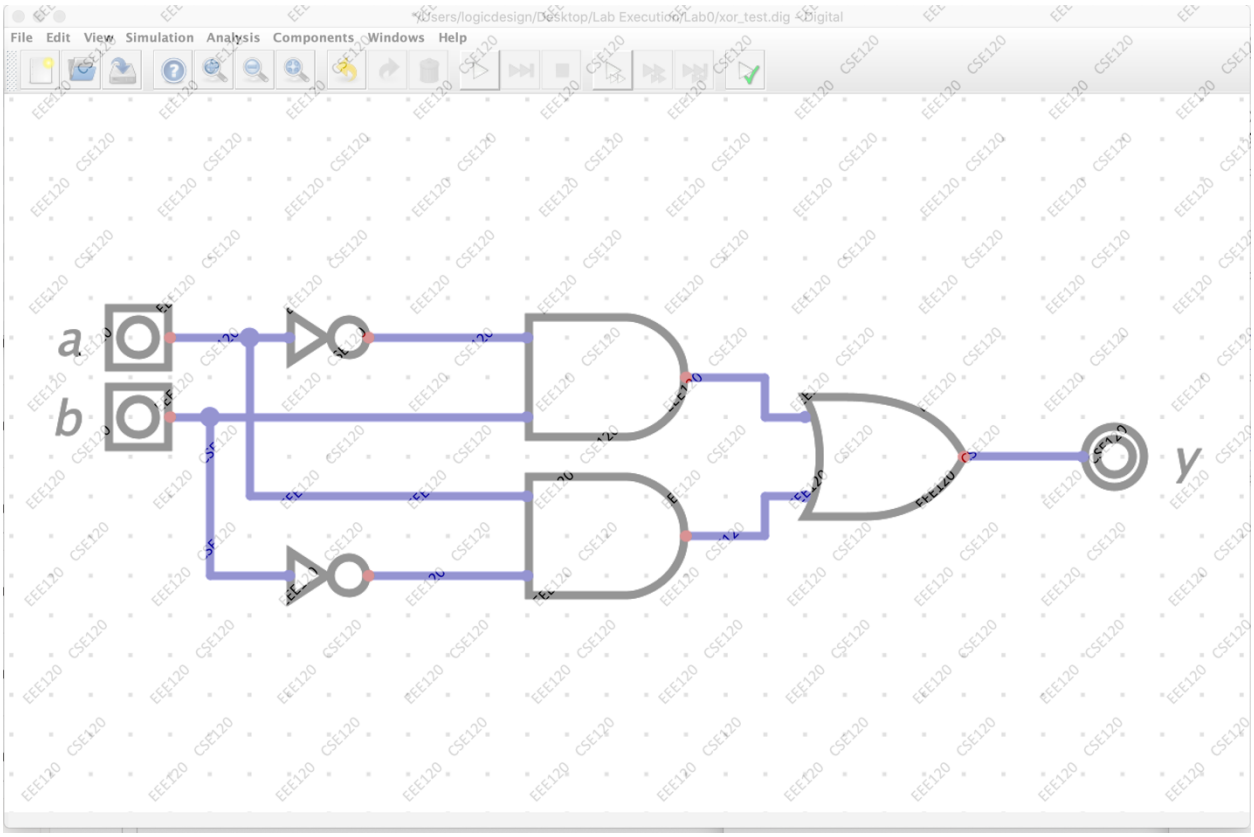

Figure 8. The completed schematic.

You've now completed your first schematic design. Nice job! Now, let's save it. On the Mac, hit CMD-s, on Windows CTRL-s, or select Save under the File menu. Name your file xor_test and click Save. Make sure the directory where it is saved is Lab0. You may have to click on the folder in the upper section of the window to select the folder. See Figure 9 for an example where you must click on the Lab0 folder, which is highlighted in the figure.

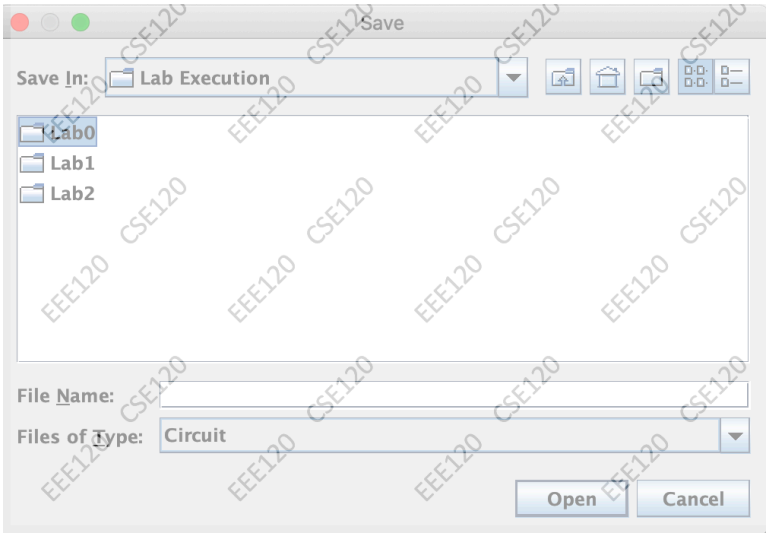

Figure 9. Saving your design.

Now, take a screenshot of your work to paste into the template. Make sure the screenshot includes the entire window, including the banner at the top which shows the path to your file.

Task 0-2: Simulate the design in visually in Digital.

Click on the Simulation menu and select Start of Simulation. A shortcut is to click on the triangle icon to the right of the trash icon. (If you hover over the icons below the menus at the top of the screen, text pops up to tell you what pressing that icon will do.) Press the one that says, "Starts the simulation of the circuit".

When the simulation starts, the wires will change from blue to green. Dark green means the wire is at logic 0. Light green means it is at logic one. (If you are color blind or would like to change the color scheme, select Settings under the Edit menu. There is a dropdown menu for Color-Scheme. Select the scheme you would like or create a custom scheme.)

Click on the inputs to change them. By watching the colors, you can see if the circuit is working as expected. While handy, we'll see in future labs that this is not a great way to verify a more complex circuit. When you are satisfied that the circuit is working, move on to the next task. End the simulation by clicking on the square icon two spots to the right of the triangle icon used to start the simulation or select Simulation->Stop Simulation.

Task 0-3: Export the design and simulate in Verilog.

Under the File menu, select Export->Export to Verilog. Since you named your design xor_test, the default name xor_test.v will be provided. Click save. You should now see the Verilog file on your computer.

You have been provided with two files: xor_top.v and xor_stim.txt. Make sure they are in the Lab0 folder. The xor_top.v file will instantiate your design, apply the test stimulus found in xor_stim.txt, and check the results against the expected responses which are also in xor_stim.txt. You may look in these files, but do not change them. In the future, you'll create your own stimulus and expected response files!

The xor_stim.txt file provides 8 bits per line since each of the hexadecimal digits represents 4 bits. We use 4 bits to make it easier to see the values at a glance. The left digit holds the expected output. The right digit is the stimulus to apply; that is, the input values. Since there are two inputs and one output, this means that 5 of the bits are not used. Table 1 shows how each bit is used.

Table 1: Bit definitions for xor_stim.txt.

Bit #	7:5	4	3:2	1	0
Meaning	unused	exp_y	unused	a	b

To run your simulation, you'll need to be in a command window. Navigating to the Lab0 folder will differ whether you are on Mac or on Windows:

On the Mac, open the Terminal program, which is found in /Applications/Utilities. Navigate using the cd command to the folder where your circuit is located. For example, if the Lab0 folder is on your Desktop, type "cd Desktop/Lab0" and you'll be where you need to be. If it's in your Documents folder in a subfolder named EEE120, type "cd Documents/EEE120/Lab0". To see what is in the current folder, type "ls". (That's a lower case L.)

On Windows, open the Command Prompt or Windows PowerShell. Navigate using the "cd" command to the folder where your circuit is located. For example, if the Lab0 folder is on your Desktop, type "cd Desktop/Lab0" and you'll be where you need to be. If it's in your Documents folder in a subfolder named EEE120, type "cd Documents/EEE120/Lab0". To see what is in the current folder, type "dir".

On both Windows and Mac you can use the tab key to auto-complete file and directory names and to browse through alternatives.

To simulate the design, type the following command in the terminal. Make sure the files xor_stim.txt and xor_top.v, which you were provided, are in the Lab0 directory.

iverilog -o xor.exe xor_test.v xor_top.v

iverilog will create an executable file called xor.exe. Now we need to run it by typing the following command in the terminal. On the Mac, type:

./xor.exe

On Windows, type:

vvp xor.exe

You should see the following output to the terminal:

```
VCD info: dumpfile xor_waves.vcd opened for output.
```

Finally, we need to look at the waves. On the Mac, launch the GTKWave application. Under File, select "Open New Tab". Alternatively, on Mac press CMD-T or on Windows CTRL-T. Select the file xor_waves.vcd. You may have to navigate to the Lab0 folder.

On Windows, type "gtkwave xor_waves.vcd".
Either way, the window shown in Figure 10 will appear.

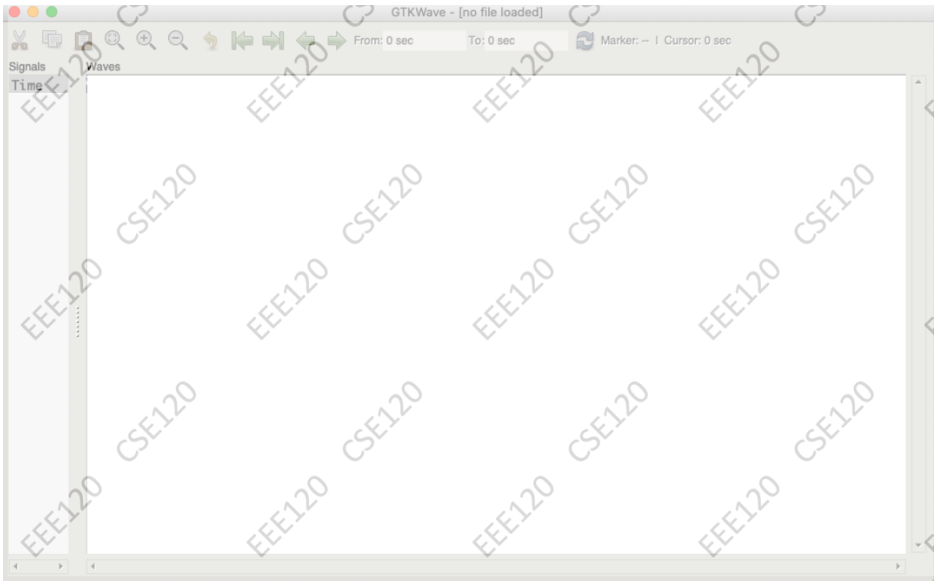

Figure 10. The waveform window.

Notice where it says xor_top in the upper left area. Click on the small triangle (on Mac) or the small + (on Windows) to the left of xor_top. You'll see xor_test. This is your design. This is the instance name we've given to your circuit. You can see the two inputs and the output of your circuit in the lower area on the left. If you double click on each of the signal names, waves will appear in the window. You can examine the waves to see if your circuit is behaving correctly. Figure 11 shows how your waves should appear.

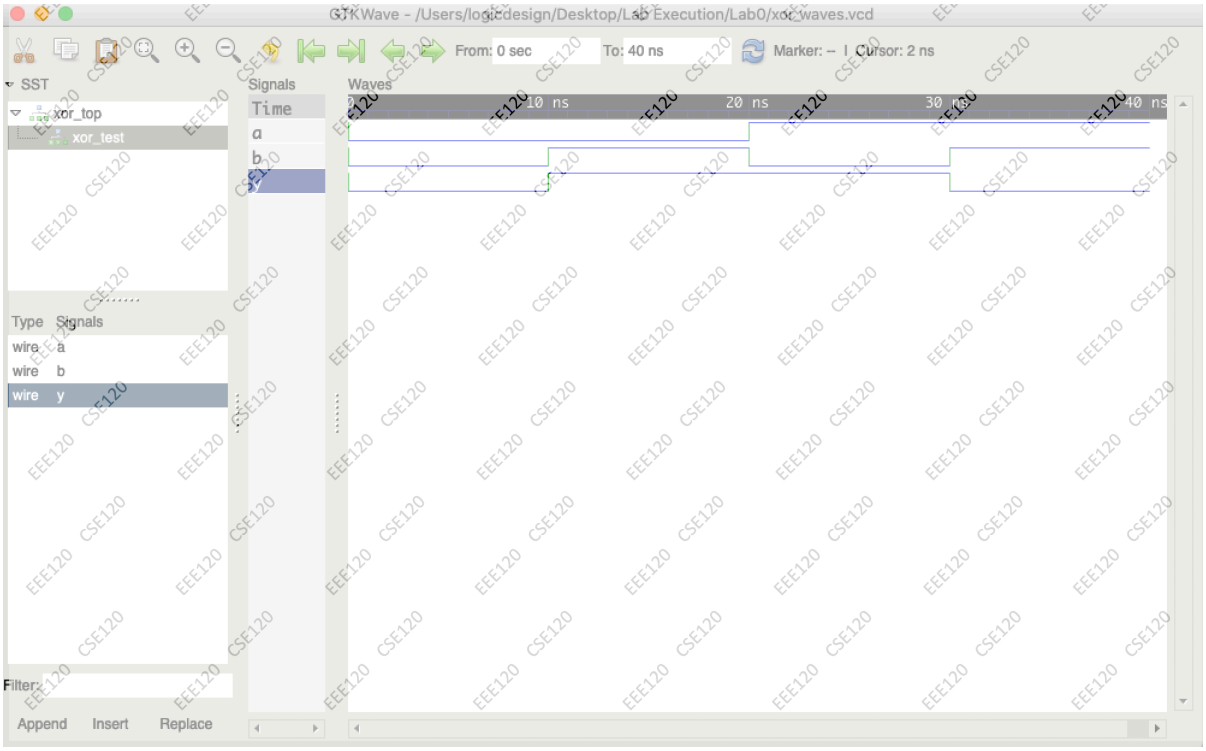

Figure 11. The XOR circuit waves.

NOTE: When you run GTKWaves, the background in the waves window will be black and the colors used for the waves will be different from that shown here. These have been modified for clarity in this document. There is no need for you to modify the colors to match. Leave them as is when copying and pasting into your template. This will be true for all future labs as well.

When you are satisfied that the waves are correct for the XOR function, take a screen shot of the entire window, including the path name at the top, and paste it into the template.

Task 0-4: Create a video and submit your report.

Create a video showing your schematic in Digital, and your waveforms. Be sure to show yourself in the video and show your screen. Place a link to the video on your ASU google drive. Be sure to set permissions so that everybody can see your video and paste the link into your template.

Make sure all of your files are in the Lab0 directory. Create a zip file of the Lab0 directory. Turn in the zip file and your completed template. (Double check that you turned in the completed template and NOT the blank one you downloaded. Unfortunately, turning in the wrong template file is a common mistake.)

Congratulations! You've completed Lab 0!