# EEE 120: Extra Credit Design Problem

Design a synchronous counter that counts up 0, 1, 2, 3, 0, 1, 2, 3, ... when an input x = 1, and down when x = 0 using
(a) D flip-flops.
(b) J-K flip-flops.

You need to show the state definition table, the state transition diagram, the state transition table, the K-maps for the respective logic functions and the schematic of the implementation using flip-flops and logic gates in (a) as well as the K-maps for the logic functions and the schematic in (b). **(5 points each, 35 points total)**

Note:

1) You can either create an electronic document and submit your answer in a **word** or **pdf** format.
2) Or you can work on a scratch paper and scan your answer with a scanner. If you don't have a scanner you may use a camera such as on a computer or a phone to take a picture. Transfer your picture to your computer and upload your picture in **.pdf** or **.jpg** format.
3) You are welcome to simulate your design using Logisim to verify its functionality but it is NOT required.