EE5801 Project Report

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***Abstract*—This document serves as the report for the EE5801 Time Domain Reflectometry (TDR) project. It explores the fundamental principles of TDR, its working mechanism, and its applications in fault detection and signal integrity analysis. In addition, the report examines how transmission lines can be modeled as discrete lumped elements in LTspice, providing insights into their behavior and simulation techniques.**

***Index Terms*—Time Domain Reflectometry, LTspice.**

I. Introduction

TIME Domain Reflectometry (TDR) is a cornerstone technique for diagnostic of impedance mismatches, faults, and discontinuities in transmission lines and the analysis of signal integrity in high-speed electronic systems. This project investigates the foundational principles of TDR through computational modeling, focusing on the lumped element approximation of transmission lines in LTspice and its implications for signal reflection, attenuation, and delay.

II. Time Domain Reflectometry

The basis of TDR is succinctly explained by the reflection coefficient equation:

$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{1}$$

where Z_L is the load impedance, and Z_0 is the characteristic impedance of the transmission line. A mismatch in impedance along the transmission line or at the end ($Z_L \neq Z_0$) results in a reflection.

TDR operates by sending a pulse down a transmission line and listening for reflections. By analyzing these reflections, impedance mismatches can be detected. The time difference between sending the pulse and receiving the reflection determines the location of the mismatch, while the waveform provides information about the type of mismatch.

Impedance mismatches can be caused by various cable faults, such as:

- Degradation of the insulator
- Breaks in the conductor
- Corroded joints and connectors

TDR is widely used in various fields due to its non-destructive testing nature. These includes:

- In-place preventive maintenance and fault troubleshooting of long cable runs where removal is impractical, such as underground cabling
- Surveillance countermeasures to detect wiretaps
- For verification of impedance-controlled lines on high-frequency printed circuit boards (PCBs) [1] [2]
- Fault localization in integrated circuits (ICs) [3]

III. Objective of Project

This project is focused on simulating a transmission line using lumped circuit elements. The simulation aims to investigate several key effects that impact the behavior and performance of the transmission line and reflecting back on what it would mean for the time domain reflectometry application:

- **Unit Cell Length:** Analyze the effect of the length of the lumped element unit cell on the overall simulation accuracy and behavior of the transmission line
- **Rise Time:** Explore how varying the rise time of the input signal influences the transmission line's transient behavior
- **Load Matching:** Study the impact of load matching, how mismatches can lead to reflections
- **Ferrite Bead Modeling:** Develop and incorporate a model for a ferrite bead, and assess its effect on the transmission line when placed in series at the midpoint

IV. Methodology

Modeling a transmission line with the lumped circuit model requires the transmission line to be divided into adequately fine (e.g. $\lambda/20$) unit cell of lumped circuit elements. Creating these circuits manually in the LTspice GUI may be feasible for slower rise time, however, for cases with extremely short rise times (e.g., 5 ps), it requires more than 30,000 LC segments. To address this, a Python script is implemented to automate the generation of LTspice circuit files. This script calculates key parameters such as the maximum frequency (using $f_{\text{max}} = 0.35/\text{trise}$) and the corresponding wavelength based on the relative permittivity. By dividing the wavelength by a specified fraction (e.g., $\lambda/20$), the script determines the segment length and total number of segments, automatically writing the circuit definitions, including subcircuit instantiations, source, and load elements into a LTspice .cir file.

To model the ferrite bead based on the given plot, an extraction of the measured impedance vs frequency data from the image is performed using PlotDigitizer and saved as a CSV file. The ferrite bead is then modeled with the following circuit and with the impedance calculated with the following formula where $\omega = 2\pi f$, L is the inductance, C is the capacitance, R is the resistance in the parallel branch, and R_s is the series resistance:

$$|Z| = \sqrt{\left(R_s + \frac{\frac{1}{R}}{\left(\frac{1}{R}\right)^2 + \left(\omega C - \frac{1}{\omega L}\right)^2}\right)^2 + \left(\frac{\omega C - \frac{1}{\omega L}}{\left(\frac{1}{R}\right)^2 + \left(\omega C - \frac{1}{\omega L}\right)^2}\right)^2} \tag{2}$$

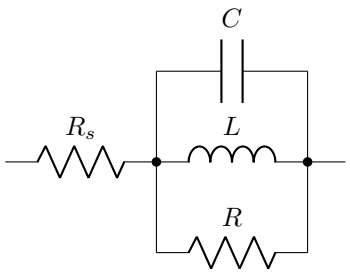

Fig. 1. Equivalent circuit diagram for the ferrite bead model.

Since inductance L, resistance R, and series resistance R_s are known to be 1.208 uH, 1.082 kΩ and 0.3 Ω, respectively, a Python script is used to sweep through a range of capacitance values and the mean square error (MSE) between the modeled impedance and the measured data can be computed. The capacitance that has the smallest MSE is selected as the best fit. A sweep between 1 pF to 2 pF is performed at 0.0001 pF step.

Implementation of these Python scripts and their outputs can all be found in this GitHub repository.

V. Results and Discussion

A. Question 2.1

The formula to obtain the characteristics of a two-wire transmission line of equal wire diameter, d, of separation, D and length, ℓ_t , is as shown:

$$C_{\text{p.u.l}} = \frac{\pi\epsilon_o\epsilon_r'}{\ln\left[\frac{D}{d}+\sqrt{\left(\frac{D}{d}\right)^2-1}\right]}\ \text{F/m} \tag{3}$$

$$L_{\text{p.u.l}} = \frac{\mu_o\mu_r}{\pi}\ln\left[\frac{D}{d}+\sqrt{\left(\frac{D}{d}\right)^2-1}\right]\ H/m \tag{4}$$

$$R_{\text{p.u.l}} = \frac{2R_{surface}}{\pi d} = \frac{2}{\sigma_{metal}\delta_{metal}\pi d}\,\Omega/m \tag{5}$$

$$G_{\text{p.u.l}} = \frac{\pi\omega\epsilon''}{\ln\left[\frac{D}{d}+\sqrt{\left(\frac{D}{d}\right)^2-1}\right]} = \frac{\pi\omega\epsilon_o\epsilon_r'\tan\left(\delta_{dieletric}\right)}{\ln\left[\frac{D}{d}+\sqrt{\left(\frac{D}{d}\right)^2-1}\right]}\ S/m \tag{6}$$

$$Z_0 = \sqrt{\frac{R_{\text{p.u.l}}+j\omega L_{\text{p.u.l}}}{G_{\text{p.u.l}}+j\omega C_{\text{p.u.l}}}}\,\Omega \tag{7}$$

$$\gamma = \alpha+j\beta = \sqrt{(R_{\text{p.u.l}}+j\omega L_{\text{p.u.l}})(G_{\text{p.u.l}}+j\omega C_{\text{p.u.l}})} \tag{8}$$

$$u_{\text{p}} = \frac{2\pi f}{\beta} \tag{9}$$

$$t_{\text{prop}} = \frac{\ell_t}{u_p} \tag{10}$$

where ϵ_o is the permittivity of free space, ϵ_r' is the relative permittivity, μ_o is the permeability of free space, μ_r is the relative permeability, R_{surface} is the surface resistance, σ_{metal} is the conductivity, δ_{metal} is the skin depth of the conductor, $\omega = 2\pi f$ is the angular frequency, ϵ'' is the dielectric loss factor, and $\tan(\delta_{\text{dielectric}})$ is the loss tangent.

The following parameters are given:

- d: $4\,mm$
- D: $10\,mm$
- length, ℓ_{t}: $69.25\,cm$
- ϵ_{r}': 2.4
- $\tan(\delta_{\text{dielectric}})$: 0.05
- μ_{r}: 1

Since the conductivity of the conductor is not given, is it taken to be a perfectly conducting conductor. Hence, the only losses are due to dielectric losses modeled by the conductance. Following eq. 3, 4, 5, 6, the transmission line characteristic is calculated to be:

- $C_{\text{p.u.l}}$: $42.609\,pF/m$
- $L_{\text{p.u.l}}$: $626.720\,nH/m$
- $R_{\text{p.u.l}}$: $0\,\Omega/m$
- $G_{\text{p.u.l}}$: $13.386\times f\,pS/m$

The characteristic impedance and propagation constant is then calculated based on eq. 7 and 8:

- $Z_{0,\text{ lossless}}$: $121.3\,\Omega$
- $\gamma_{\text{lossless}} = \beta$: $jf\times 3.2469\times 10^{-8}$
- $Z_{0,\text{ lossy}}$: $121.2\angle 1.431^\circ\,\Omega$
- γ_{lossy}: $f\times(8.1147\times 10^{-10}+j3.2479\times 10^{-8})$

Using eq. 9 and 10, the phase velocity and propagation time from one end to another end on the transmission line is then:

- $u_{\text{p, lossless}}$: $1.935\times 10^8\,m/s$
- $t_{\text{prop, lossless}}$: 3.6 ns
- $u_{\text{p, lossy}}$: $1.935\times 10^8\,m/s$
- $t_{\text{prop, lossless}}$: 3.6 ns

B. Question 2.2

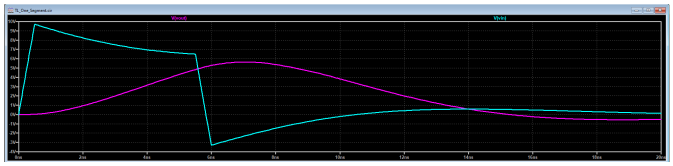

Fig. 2. Time domain plot with only one unit cell

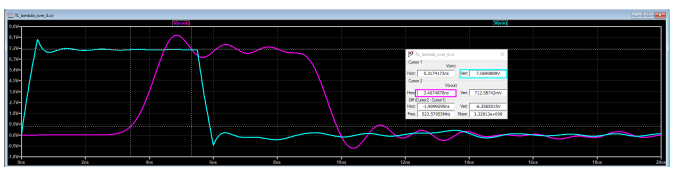

Fig. 3. Time domain plot with cell of $\lambda/4$

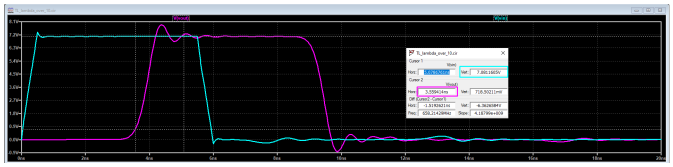

Fig. 4. Time domain plot with cell of $\lambda/10$

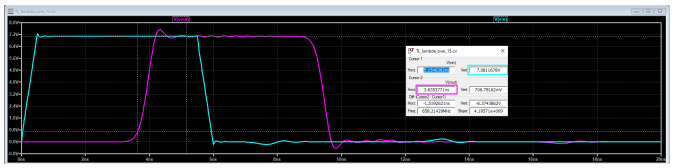

Fig. 5. Time domain plot with cell of $\lambda/15$

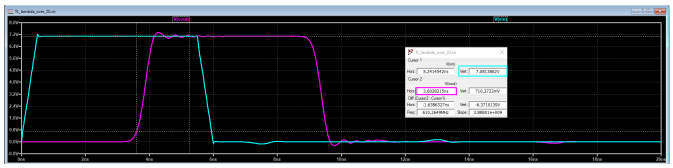

Fig. 6. Time domain plot with cell of $\lambda/20$

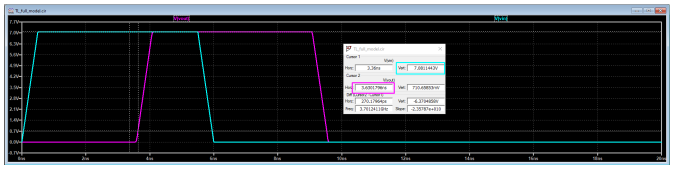

Fig. 7. Time domain plot with LTspice built-in transmission line model

This section explores the impact of unit cell length in the transmission line model. As a reference, the LTspice built-in transmission line model is simulated as well.

From Fig. 2 to Fig. 6, it is apparent that the approximation accuracy improves as the unit cell length decreases relative to the signal wavelength, though this increases computational time as shown in the simulation logs. For practical time-domain and magnitude approximations, division factors of 1/15 and 1/20 yield acceptable results, showing minimal rise-time error and rapidly decaying ringing giving readable steady-state values.

$$V_{\text{init}} = V_S \frac{Z_0}{Z_0 + Z_S} = 10\,\text{V} \times \frac{121.3}{121.3 + 50} \approx 7.08\,\text{V} \quad (11)$$

It can be observed that for all cases except the single unit cell configuration Fig. 2, when $R_L = Z_0$, reflections are eliminated and the input pulse amplitude follows the resistive divider relationship between the source impedance (Z_S) and characteristic impedance (Z_0) as described by eq. 11. The measured delay from start of pulse to output rise is approximately 3.6 ns, corresponding to the signal propagation time through the transmission line length,

C. Question 2.3

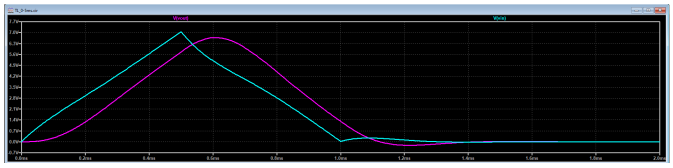

Fig. 8. Time domain plot with 0.5 ms rise time

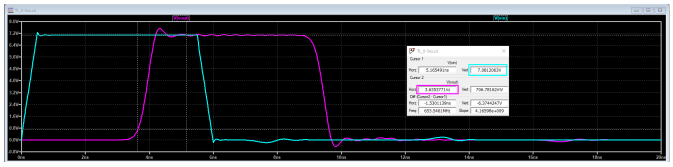

Fig. 9. Time domain plot with 0.5 ns rise time

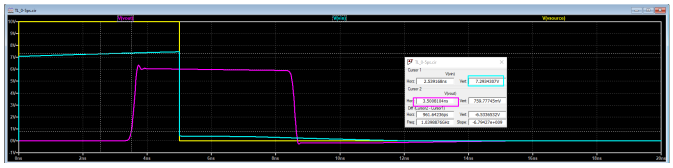

Fig. 10. Time domain plot with 0.5 ps rise time

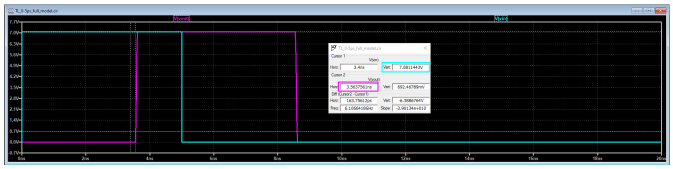

Fig. 11. Time domain plot with 0.5 ps rise time with LTspice built-in transmission line model

This section explores the impact of rise time with a fixed length of transmission line. Again, as a reference, the LTspice built-in transmission line model is simulated for the 5 ps case.

For the 0.5 ms rise time case, Fig. 8, the wavelength involved is much longer than the transmission line and the whole line can be considered as one lumped circuit. The 0.5 ns cases, Fig. 9, exhibit similar behavior to previous observations seen in section (V-B).

The 0.5 ps case, Fig. 10, required over 30,000 unit cells to satisfy the $\lambda/15$ requirement. This simulation required roughly 30 minutes computation time on a personal laptop, yet produced erroneous results including rising V_{near} transients which is not observed with LTspice's native model (0.163 s runtime), Fig. 11.

These results demonstrate that for TDR, the rise time requirements scale with cable length, shorter cables demand faster rise times to ensure the transmission line behavior is apparent.

D. Question 2.4

Fig. 12. Case A: Time domain plot with a matched load

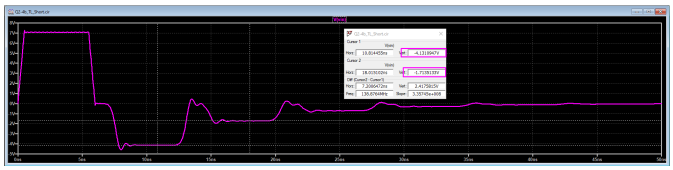

Fig. 13. Case B: Time domain plot with a short

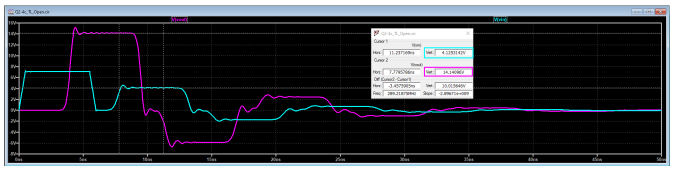

Fig. 14. Case C: Time domain plot with an open

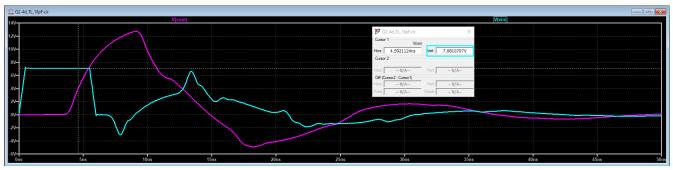

Fig. 15. Case D: Time domain plot with an 18 pF load

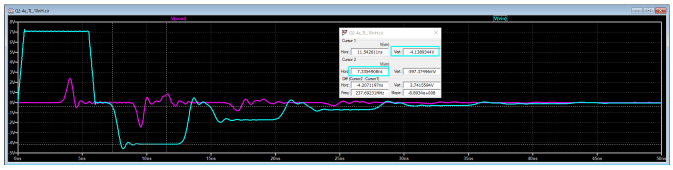

Fig. 16. Case E: Time domain plot with an 10 nH load

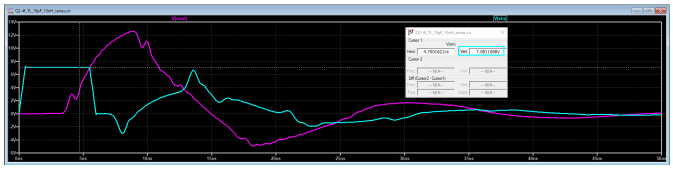

Fig. 17. Case F: Time domain plot with a series 18 pF and 10 nH load

This section explores the effect of load mismatch on the voltage seen from the input port of the transmission line.

The initial pulse height remains constant across all cases, determined by the voltage divider between source impedance (Z_S) and characteristic impedance (Z_0) as described by eq. 11.

Key observations for cases (A-F):

- **Timing Consistency**: V_{near} transitions due to reflection occur at $2 \times t_{\text{prop}}$ (7.2 ns for 3.6 ns propagation time):

$$t_{\text{reflect}} = 2 \times \frac{\ell_{\text{t}}}{u_p} \approx 7.2\,\text{ns} \tag{12}$$

- **Case A** Fig.12 ($R_L = Z_0$): Minimal reflections (slight imperfect matching causes minor artifacts)
- **Case B** Fig.13 (Short): $\Gamma_L = -1$ creates full inversion at load. Reflection at source ($\Gamma_S = \frac{Z_S - Z_0}{Z_S + Z_0} = -0.416$) produces:

$$V_{\text{near 2nd}} = -7.08 + (7.08 \times 0.416) \approx -4.09\,\text{V} \tag{13}$$

- **Case C** Fig.14 (Open): Similar as case B but voltage wave sign will not invert at load, but at input end, so the sign of wave observed is alternating between positive and negative at the input
- **Cases D-F**: Frequency-dependent Γ_L complicates waveforms:
  - **Case D** Fig.15 (Capacitive load): for low frequency, the cap acts like open, while for the higher frequency content, it acts like a short or lower impedance. Overall will get a mix of both both signs of Γ_L, resulting waveform more complicated than the others
  - **Case E** Fig.16 (Inductive load): Most of the frequency content in the pulse are low frequency, where the inductor impedance is low, below 50 Ω for those below f_{max}, hence it acts very similar to the short case B
  - **Case F** Fig.17: Since the inductor impedance is low, capacitor's behavior will dominate, this case acts similar to the case D

These results shows that for TDR, where reflection due to cable faults are sought after, the transmission line should be load matched to avoid any additional reflection that may affect the result.

E. Question 2.5

This section explores how clamping a ferrite bead on the two wire transmission line would affect its behavior.

Following the procedure outlined in section IV, the best fit capacitance is determined to be 1.6579 pF. Fig. 18 shows that the modeled ferrite bead fit the measured impedance fairly well.

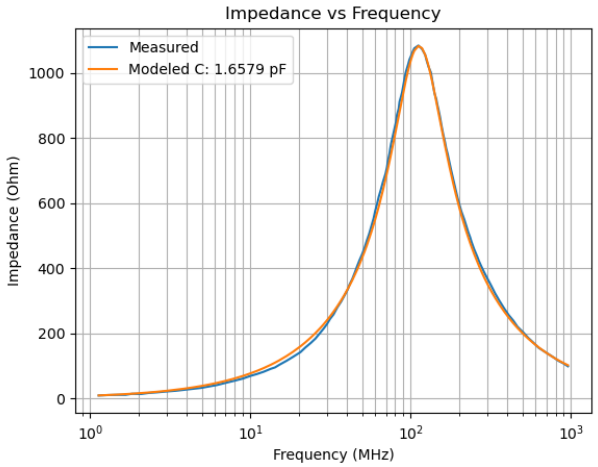

Fig. 18. Plot of measured and modeled ferrite bead impedance

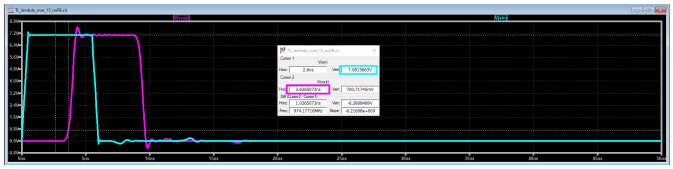

Fig. 19. Time domain plot without ferrite bead

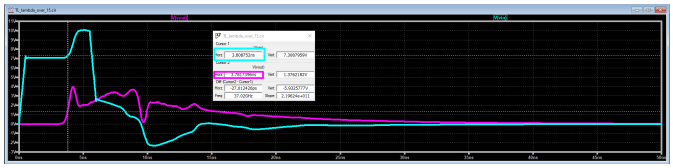

Fig. 20. Time domain plot with ferrite bead

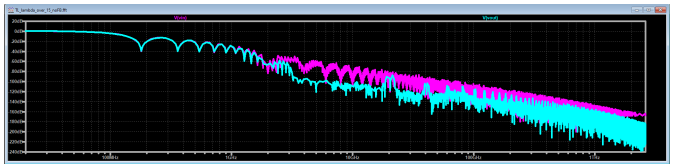

Fig. 21. Frequency domain plot without ferrite bead

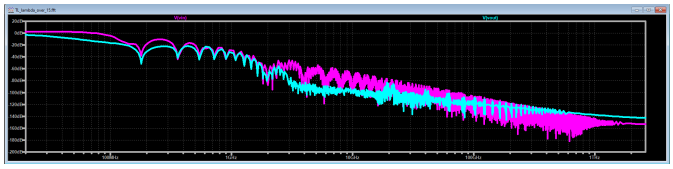

Fig. 22. Frequency domain plot with ferrite bead

Comparing time-domain plots with/without ferrite beads, Fig. 19 and Fig 20, reveals key observations:

- Impedance discontinuities from the ferrite bead induce reflections despite matched load conditions ($R_L = Z_0$)
- With the ferrite bead placed at the transmission line midpoint, the round-trip midpoint reflection delay matches the one-way propagation time
- This shows how TDR could use the impedance discontinuities to localize faults along a cable

Frequency-domain plots with/without ferrite beads, Fig. 21 and Fig 22, provide additional insights into the impact of the ferrite bead on the transmission line.:

- Spectral content above 1 GHz remains nearly identical between configurations
- Differ the most near 100 MHz, where the impedance of the ferrite bead is high, and hence the frequency content in this region is attenuated the most

VI. Conclusion

This project successfully demonstrated the modeling of transmission line behavior using lumped element approximations in LTspice. Insights to TDR are gained, such as the need for a matched load to prevent extra reflections and how impedance discontinuity along the line can be detected. Implementation of Python automation for SPICE model generation proved essential for handling extremely high unit cell count requirements.

References

[1] "TDR Testing Services." [Online]. Available: http://circuittechservices.com/services/tdr-test/#:~:text=TDR%20test%20applies%20a%20very,tester%20as%20well%20as%20graphed.

[2] "How a PCB Manufacturer Verifies Controlled Impedance," Cadence PCB Resources, [Online]. Available: https://resources.pcb.cadence.com/blog/how-a-pcb-manufacturer-verifies-controlled-impedance

[3] D. Abessolo-Bidzo, P. Poirier, P. Descamps and B. Domenges, "Failure localization in IC packages using time domain reflectometry: technique limitations and possible improvements," Proceedings of the 12th International Symposium on the Physical and Failure Analysis of Integrated Circuits, 2005. IPFA 2005., Singapore, 2005, pp. 318-322, doi: 10.1109/IPFA.2005.1469187. keywords: Integrated circuit packaging;Reflectometry;Impedance;Failure analysis;Packaging machines;Pins;Reflection;Semiconductor device packaging;Bandwidth;Wire