Release Notes for S32K3 Real-Time Drivers AUTOSAR 4.4

Version 3.0.0 P01

31 March 2023 **Release notes**

1 Getting Started

1.1 Package content

This release contains the NXP S32K3 Real-Time Drivers Version 3.0.0 P01:

- "eclipse/plugins/<mod>_TS_T40D34M30I0R0" directories - Tresos Plugins, 1 per module.
- "SW32K3_RTD_4.4_3.0.0_P01_D2303.exe"
- "SW32K3_RTD_4.4_3.0.0_P01_D2303_ReleaseNotes.pdf" - This file.
- "SW32K3_RTD_4.4_3.0.0_P01_D2303_SCR.txt"
- "SW32K3_RTD_4.4_3.0.0_P01_D2303_DS_updatesite.zip"
- "SW32K3_RTD_4.4_3.0.0_P01_D2303_SafetyPackage.zip" - contains FMEA reports and Safety Manual.
- "SW32K3_RTD_4.4_3.0.0_D2303_P01_QualityPackage.zip"
- Various other files: GettingStarted.htm start page and associated images, the license.txt EULA file and the Uninstall.exe utility for removing the RTD installation.

1.2 Installation Design Studio

1.2.1 Bundled in S32 Design Studio

S32 RTD is delivered bundled in the S32 Design Studio. In this case, it's already configured and ready to use. New S32DS project wizard and New S32DS project from Example can be used to create S32 RTD based projects.

1.2.2 Delivered as an extension for S32 Design Studio

S32 RTD is delivered as an Update Site for S32 Design Studio "*S32DS 3.5 Service Pack 1 EAR4 Build 230307 and S32M27x_SP2_CD*". In this case, it must be installed by opening Help -> S32 Design Studio Extensions and Updates -> Add Update Sites and selecting the archive file containing the S32 RTD software and then check the S32 RTD software package to be installed and continue the installation process. After it is installed, New S32DS project wizard and New S32DS project from Example can be used to create S32 RTD based projects.

1.3 Installation EB Tresos

Follow the installer steps. By default the installer will create a link between the installation target directory and a selected EB Tresos installation. If you choose not to create a link, you can later create one manually or you can copy all "<mod>_TS_T40D34M30I0R0" directories and .JAR files to the "<Tresos Install Path>\plugins" directory.

2 Release Specifics

The S32K3 Real-Time Drivers Version 3.0.0 P01 is AUTOSAR 4.4 compliant. The AUTOSAR Configuration ARXML specification takes precedence over AUTOSAR SWS PDF Specifications if there are discrepancies.

The S32K3 Real-Time Drivers Version 3.0.0 P01 can be used also in non-AUTOSAR environment, as a collection of peripheral drivers designed to simplify and accelerate application development on NXP microcontrollers.

2.1 Release Details

This is the NXP S32K3 Real-Time Drivers release Version 3.0.0 P01 added FEE, FLS, EEP drivers supporting AUTOSAR 4.4 with functionalities and tests on S32K358, S32K396, S32K311, S32K342, S32K312, S32K344 and S32M276.

This release contains a deviation from AUTOSAR recommended version check inside source files for more details.

This release has EAR qualification for S32M276, S32K358 and RTM qualification for S32K358, S32K396, S32K311, S32K342, S32K312, S32K344.

RTM qualified drivers can be used in production.

EAR qualified drivers are not intended for production use.

This release was developed and tested using:

- Silicon P32K358GVS 0P14E CTZF2233B.
- Silicon P32K396EHMJBS OP40E QAD2222F.
- Silicon P32K311HVS 0P98C CTZA2242B.
- Silicon P32K344EHVMMS 1P55A CTSB2128B.
- Silicon P32K312NHVPBS 0P09C CTZM2132B.
- Silicon P32K342EHVPBE 0P97C CTZM2139A.
- Silicon P32M276CH MKHS 0P73G CTZA2305A.
- Silicon P32M276LH MKHS 0P73G CTZA2305B.
- Mini Module XS32K3X8CVB-Q289 PCB 53108 RevX3 SCH RevA1 .
- Mini Module XS32K396-BGA-DC PCB 54614 RevX1 SCH RevA.
- Mini Module XS32K3X2CVB-Q100 PCB 48306 RevX1 SCH RevA.
- Mini Module XS32K3XXCVB-Q257 PCB 47020 RevA1 SCH RevX2.
- Mini Module XS32K3X2CVB-Q172 PCB 48307 RevX1 SCH RevA.
- Mother Board X-S32K3XXX-MB PCB 47386 RevA SCH RevA.
- Mother Board X-S32K2XX-MB PCB 31431 RevX3 SCH RevB.
- Mother Board X-S32X-MB version A PCB 54935 RevX1 SCH RevA.
- EVB S32K3X4EVB-Q257 PCB 47827 RevX1 SCH RevA.
- EVB S32K3X4EVB-Q172 PCB 51972 RevA SCH RevA.
- EVB S32K312EVB-Q172 PCB 50892 RevA SCH RevB.
- EVB XS32M2XXCVB-Q064 PCB 53099 RevX1 SCH RevA.

In all source files, Software Version values are checked (major, minor, patch). AUTOSAR release or SWS versions are not checked during preprocessing/template generation.

The correct SWS versions are exported by each module.

The functions contained in the Dem, Det, EcuC, EcuM, Rte and interface plugins are sample stub functions.

These functions should be replaced by the user developed code during integration.

The Resource module is needed to select the MCU derivative.

The derivatives supported can be found in the Resource module definition file, parameter 'ResourceSubderivative'.

The following limitations are present in this release:

Known limitation on S32 Design Studio:

- Due to low SRAM memory space on S32K310, S32K311, S32K312, S32K322, S32K341, S32K342, S32M274 and S32M276 derivatives, users should select FLASH profile to create new project on S32 Design Studio.

Known issue with IAR compiler, all RTD drivers:

- Warning regarding stack usage is thrown for reference implementations of core exceptions in startup files when drivers are compiled with IAR. These functions are provided as reference code and can be replace/modified by the application.
- Usage of IAR compiler option "-enable_stack_usage " will issue warnings regarding uncalled functions (eg : interrupt handlers). This should be disregarded.
- IAR cannot analyze stack usage for function in .s file and the function with indirect call(function pointer).

Known issue with GCC compiler, all RTD drivers:

- Warning regarding enum size is thrown by the linker due to usage of "-fno-short-enums" option: "use of enum values across objects may fail". The drivers do not use any library enum types - no functional impact.

Known issue for PE Micro debug plugins in Design Studio:

- Debugging an application in RAM might fail if another application is present in target flash (debug communication lost during startup, MCU boots the application in flash). Workaround proposed: erase flash before loading an application in RAM; this can be done with the following command launched in the PE for example GDB Server console: "pegdbserver_console.exe -device=NXP_S32K3xx_S32K344 -programmingtype=3 -runafterprogramming=0 -interface=USBMULTILINK -startserver -singlesession -quitafterprogramming -flashobjectfile=path_to_a_srec_or_elf_file".

RTD Header Files reference

Table 1. RTD Header Files reference

Derivatives	RTD Header files
S32K396	Available
S32K358	Available
S32K344	Available
S32K324	Available
S32K314	Available
S32K342	Available
S32K341	Available
S32K322	Available

Table 1. RTD Header Files reference*...continued*

Derivatives	RTD Header files
S32K312	Available
S32K311	Available
S32M276	Available

2.2 Used Documentation

This release was developed and tested with the following documents:

Table 2. Reference Manuals

Document Title	Version and Date
S32K3xx Reference Manual	Rev.6 Draft B, 01/2023
S32K3xx Data Sheet	Rev. 6 — 11/2022
S32M27x Reference Manual	Rev.2 Draft A, 02/2023
S32M2xx Data Sheet	Rev. 2 RC — 12/2022
S32K39 and S32K37 Reference Manual	Rev.2 Draft A, 11/2022
S32K396 Data Sheet	Rev. 1.1 — 08/2022

Table 3. Implemented Errata

Document Title	Maskset	Date
S32K358 Mask Set Errata for Mask	0P14E	Rev. 28, 9/2022
S32K311 Mask Set Errata for Mask	0P98C	Rev. 6, 3/2023
S32K396 Mask Set Errata for Mask	0P40E	Rev. DEC2022, 12/2022
S32K312 Mask Set Errata for Mask	0P09C	Rev. 25, 4/2022
S32K342 Mask Set Errata for Mask	0P97C	Rev. 10, 11/2022
S32K3x4 Mask Set Errata for Mask	0P55A/1P55A	Rev. 14, 10/2022

2.3 Supported Derivatives

The software described in this document is intended to be used with the following microcontroller devices of NXP:

- s32k310_mqfp100.
- s32k310_lqfp48.
- s32k311_mqfp100 / MWCT2015S_mqfp100.
- s32k311_lqfp48.
- s32k312_mqfp100 / MWCT2016S_mqfp100.
- s32k312_mqfp172 / MWCT2016S_mqfp172.
- s32k314_mqfp172.
- s32k314_mapbga257.
- s32k322_mqfp100 / MWCT2D16S_mqfp100.
- s32k322_mqfp172 / MWCT2D16S_mqfp172.
- s32k324_mqfp172 / MWCT2D17S_mqfp172.
- s32k324_mapbga257.
- s32k341_mqfp100.
- s32k341_mqfp172.
- s32k342_mqfp100.
- s32k342_mqfp172.
- s32k344_mqfp172.

- s32k344_mapbga257.
- s32k394_mapbga289.
- s32k396_mapbga289.
- s32k358_mqfp172.
- s32k358_mapbga289.
- s32k328_mqfp172.
- s32k328_mapbga289.
- s32k338_mqfp172.
- s32k338_mapbga289.
- s32k348_mqfp172.
- s32k348_mapbga289.
- s32m274_lqfp64.
- s32m276_lqfp64.

The mapping between MWCT2xxxS parts and S32K3XX is showed in the table below:

Table 4. Derivatives mapping

MWCT2xxxS derivative	S32K3 derivative
MWCT2D17S_MQFP172	S32K324_MQFP172
MWCT2D16S_MQFP100	S32K322_MQFP100
MWCT2D16S_MQFP172	S32K322_MQFP172
MWCT2016S_MQFP172	S32K312_MQFP172
MWCT2016S_MQFP100	S32K312_MQFP100
MWCT2015S_MQFP100	S32K311_MQFP100

Note: MWCT part numbers contain NXP confidential IP for Qi Wireless Power and they tested with:

- P32K344EHVMMS 1P55A CTSB2128B (and in S32K324 configuration).
- P32K312NHVPBS 0P09C CTZM2132B.
- P32K311HVS 0P98C CTZA2242B.

2.4 Modules Configuration

2.4.1 EB Tresos

Modules configurations were developed and tested using the Tresos Configuration Tool version "*EB Tresos Studio 29.0.0 b220329-0119*"

Configuration definition files were developed according to AUTOSAR R21-11, AUTOSAR_EcucParamDef.arxml

A folder named "<mod>_TS_TtDdMmIiRr" exists for each delivered module (<mod>). It is called a Tresos plugin for the module. A plugin contains the AUTOSAR module definition file (epd), the Tresos Xpath Data Model module definition file (xdm), the module user and integration manuals, the module configuration generation template source files, and the module driver static source files. Additional necessary Tresos specific tooling files are also included.

Plugin Encoding: <mod>_TS_TtDdMmIiRr

Important change related to the plugin notation:
- "m" = coding major and minor version number, can contain 1 or more digits
- "i" = patch number.
The major version number will be left out, if it is "0", in this case "m" contains 1 digit only,

otherwise it contains 2 digits

For this release:

- t=40, CortexM Architecture
- d=34, S32K3XX (derivative)
- m=30, Release major and minor version
- i=0, Release patch version
- r=0, Reserved

2.4.2 S32 Design Studio

Configuration components were developped using "*S32DS 3.5 Service Pack 1 EAR4 Build 230307 and S32M27x_SP2_CD*".

The components are split in three tools inside S32 Design Studio: Pins Tool, Clocks Tool, Peripherals tool which enable the generation of configuration structures to be used by both Autosar and low-level drivers.

2.5 Support and Driver Plugins Delivered

Table 5. Support and Driver Plugins Delivered

Plugin	Low level interface	SW Version	Description
ADC	Bctu_Ip, Adc_Sar_Ip, Sdadc_Ip	sw version 3.0.0	Driver, Analog to Digital Conversion
BASE	N/A	sw version 3.0.0	Base Module, General AUTOSAR and Hardware Specific register files
CAN	FlexCAN	sw version 3.0.0	Driver, Controller Area Network
CRC	Crc_Ip	sw version 3.0.0	Driver, Cyclic Redundancy Check
CRYPTO	Hse_Ip	sw version 3.0.0	Driver, Cryptographic Operations
DIO	Siul2_Dio	sw version 3.0.0	Driver, Digital Input Output
ETH	GMAC	sw version 3.0.0	Driver, Ethernet
EEP	Sd_Emmc_Ip	sw version 3.0.0 P01	Driver, EEPROM
FEE	N/A	sw version 3.0.0 P01	Driver, Flash EEPROM Emulation
FLS	C40_Ip, Pflash_Ip, Qspi_Ip	sw version 3.0.0 P01	Driver, Flash
GPT	Emios_Gpt, Pit, Rtc, Stm	sw version 3.0.0	Driver, General Purpose Timer
I2C	FlexIO_I2C, LPI2C	sw version 3.0.0	Driver, Inter-Integrated Circuit
I2S	FlexIO_I2S, Sai_Ip	sw version 3.0.0	Driver, Inter-IC Sound
ICU	Emios_Icu, Cmp, Siul2_Icu, Wkpu	sw version 3.0.0	Driver, Input Capture Unit
LIN	FlexIo_Lin, LPUART	sw version 3.0.0	Driver, Local Interconnect Network
MCL	Cache_Ip, Dma_Ip, Lcu_Ip, Trgmux_Ip, Emios_Mcl, FlexIO_Mcl	sw version 3.0.0	Driver, Microcontroller Library
MCU	Clock_Ip, Power_Ip, Ram_Ip, Siul2_Mcu, Emios_Mcu	sw version 3.0.0	Driver, Microcontroller Unit
OCU	Emios_Ocu	sw version 3.0.0	Driver, Output Control Unit
PLATFORM	startup, IntCtrl_Ip, Intm_Ip, Mpu_M7_Ip	sw version 3.0.0	Driver, Platform
PORT	Siul2_Port, Tspc_Port	sw version 3.0.0	Driver, Port
PWM	Emios_Pwm, FlexIo_Pwm	sw version 3.0.0	Driver, Pulse Width Modulation

Table 5. Support and Driver Plugins Delivered*...continued*

Plugin	Low level interface	SW Version	Description
RESOURCE	N/A	sw version 3.0.0	Resource Module, Required by all other modules to select MCU derivative
RM	Xbar_Ip, Xrdc_Ip, Mpu_M7, Sema42_Ip, Xbic_Ip, Pflash_Ip, Virt_Wrapper_Ip, IntCtrl_Ip, Dma_Ip	sw version 3.0.0	Resource Module, Resource Manager
SENT	FlexIo_Sent	sw version 3.0.0	Driver, Single edge nibble transmission
SPI	FlexIO_Spi, Lpspi	sw version 3.0.0	Driver, Serial Peripheral Interface
UART	FlexIo_UART, LPUART	sw version 3.0.0	Driver, None
ZIPWIRE	N/A	sw version 3.0.0	Driver, Zipwire
AE	Hvm_Ip, Ae_Ip	sw version 3.0.0	Driver, Watchdog
WDG	Swt_Ip, AeWdog_Ip	sw version 3.0.0	Driver, Watchdog
GDU	Gdu_Ip	sw version 3.0.0	Driver, None
OCOTP	Mem_Otp_Ip	sw version 3.0.0	Driver, None
LINTRCV	N/A	sw version 3.0.0	Driver, None
CANTRCV	N/A	sw version 3.0.0	Driver, None
DPGA	Dpga_Ip	sw version 3.0.0	Driver, None
CANIF	N/A	sw version 3.0.0	Support Stub, Controller Area Network Interface
CRYIF	N/A	sw version 3.0.0	Support stub, Crypto Interface
CSM	N/A	sw version 3.0.0	Support stub, Crypto Service Manager
DEM	N/A	sw version 3.0.0	Support Stub, Diagnostic Event Manager
DET	N/A	sw version 3.0.0	Support Stub, Development Error Tracer
ECUC	N/A	sw version 3.0.0	Support Stub, ECU Configuration
ECUM	N/A	sw version 3.0.0	Support Stub, ECU State Manager
ETHIF	N/A	sw version 3.0.0	Support Stub, Ethernet Interface
ETHTRCV	N/A	sw version 3.0.0	Support stub, Ethernet Transceiver
ETHSWT	N/A	sw version 3.0.0	Support stub, Ethernet Switch
LINIF	N/A	sw version 3.0.0	Support Stub, Local Interconnect Network Interface
MEMIF	N/A	sw version 3.0.0	Support Stub, Memory Interface
OS	N/A	sw version 3.0.0	Support stub, Operating System
RTE	N/A	sw version 3.0.0	Support Stub, only for Schedule Manager
WDGIF	N/A	sw version 3.0.0	Support Stub, Watchdog Interface

2.6 Module Plugin Folder Structure

Table 6. Module Plugin Folder Structure

Folder or file	Description
<mod>_TS_TtDdMmIiRr\anchors.xml	Tresos Configuration tooling documentation data file
<mod>_TS_TtDdMmIiRr\plugin.xml	Tresos Configuration tooling data file
<mod>_TS_TtDdMmIiRr\ant_generator.xml	Tresos Configuration tooling data file
<mod>_TS_TtDdMmIiRr\autosar\<mod>.epd	Module Parameter Definition in AUTOSAR format
<mod>_TS_TtDdMmIiRr\config\<mod>.xdm	Module Parameter Definition in Tresos XDM format
<mod>_TS_TtDdMmIiRr\config_ext\<mod>PreConfiguration.xdm	Module Parameter Default Configuration in Tresos XDM format[1]
<mod>_TS_TtDdMmIiRr\doc\AUTOSAR_RTD_<mod>_IM.pdf	Module Integration Manual
<mod>_TS_TtDdMmIiRr\doc\AUTOSAR_RTD_<mod>_UM.pdf	Module User's Manual
<mod>_TS_TtDdMmIiRr\generate_PB	Post-build source files (only if applicable)

Table 6. Module Plugin Folder Structure*...continued*

Folder or file	Description
<mod>_TS_TtDdMmIiRr\generate_PB\src	Post-build source file templates (only if applicable)
<mod>_TS_TtDdMmIiRr\generate_PB\include	Post-build source file header templates (only if applicable)
<mod>_TS_TtDdMmIiRr\generate_LT	Link-time source files (only if applicable)
<mod>_TS_TtDdMmIiRr\generate_LT\src	Link-time source file templates (only if applicable)
<mod>_TS_TtDdMmIiRr\generate_LT\include	Link-time source file templates (only if applicable)
<mod>_TS_TtDdMmIiRr\generate_PC\	Pre-compile source files
<mod>_TS_TtDdMmIiRr\generate_PC\src	Pre-compile source files templates
<mod>_TS_TtDdMmIiRr\generate_PC\include	Pre-compile source files templates
<mod>_TS_TtDdMmIiRr\generate_swcd	Module BSWMD file
<mod>_TS_TtDdMmIiRr\include\	Module driver header files
<mod>_TS_TtDdMmIiRr\META-INF	Tresos Configuration tooling data and signature files
<mod>_TS_TtDdMmIiRr\src\	Module driver source files[2]

Notes:

[1] Not available for all plugins.

[2] The Support Stub Resource contains the "resource" folder instead of the "src" folder.

2.7 Compiler Options

This release was developed and tested with:

- NXP GCC 10.2.0 20200723
- Green Hills Multi 7.1.6d / Compiler 2021.1.4
- IAR ANSI C/C++ Compiler v.8.50.10 (safety version)
- Wind River Diab Compiler v7.0.4 (for S32K358 and S32K328, S32K338, S32K348, S32K312)

2.7.1 DIAB Compiler/Linker/Assembler Options

Table 7. Compiler Options

Option	Description
-tARMCORTEXM7MG:simple	Selects target processor (hardware single-precision, software double-precision floating-point)
-mthumb	Selects generating code that executes in Thumb state
-std=c99	Follows the C99 standard for C
-Oz	Like -O2 with further optimizations to reduce code size
-g	Generates DWARF 4.0 debug information
-fstandalone-debug	Emits full debug info for all types used by the program
-Wstrict-prototypes	Warn if a function is declared or defined without specifying the argument types
-Wsign-compare	Produce warnings when comparing signed type with unsigned type
Wdouble-promotion	Give a warning when a value of type float is implicitly promoted to double
-Wunknown-pragmas	Issues a warning for unknown pragmas
-Wundef	Warns if an undefined identifier is evaluated in an #if directive. Such identifiers are replaced with zero

Table 7. Compiler Options*...continued*

Option	Description
-Wextra	Enables some extra warning flags that are not enabled by '-Wall'
-Wall	Enables all of the most useful warnings (for historical reasons this option does not literally enable all warnings)
-pedantic	Emits a warning whenever the standard specified by the -std option requires a diagnostic
-Werror=implicit-function-declaration	Generates an error whenever a function is used before being declared
-fno-common	Compile common globals like normal definitions
-fno-signed-char	Char is unsigned
-fno-trigraphs	Do not process trigraph sequences
-V	Displays the current version number of the tool suite
-c	Stop after assembly and produce an object file for each source file
-DS32K3XX	Predefine DS32K3XX as a macro, with definition 1
-DS32K344	Predefine DS32K344 as a macro, with definition 1
-DDIAB	Predefine DIAB as a macro, with definition 1
-DUSE_SW_VECTOR_MODE	Predefine USE_SW_VECTOR_MODE as a macro, with definition 1. By default, the drivers are compiled to handle interrupts in Software Vector Mode.
-DD_CACHE_ENABLE	Predefine D_CACHE_ENABLE as a macro, with definition 1. Enables data cache initalization in source file system.c under the Platform driver
-DI_CACHE_ENABLE	Predefine I_CACHE_ENABLE as a macro, with definition 1. Enables instruction cache initalization in source file system.c under the Platform driver
-DENABLE_FPU	Predefine ENABLE_FPU as a macro, with definition 1. Enables FPU initalization in source file system.c under the Platform driver
-DMCAL_ENABLE_USER_MODE_SUPPORT	Predefine MCAL_ENABLE_USER_MODE_SUPPORT as a macro, with definition 1. Allows drivers to be configured in user mode.

Table 8. Assembler Options

Option	Description
-mthumb	Selects generating code that executes in Thumb state
-Xpreprocess-assembly	Invokes C preprocessor on assembly files before running the assembler
-Xassembly-listing	Produces an .lst assembly listing file
-c	Stop after assembly and produce an object file for each source file

Table 9. Linker Options

Option	Description
-e Reset_Handler	Make the symbol Reset_Handler be treated as a root symbol and the start label of the application
linker_script_file.dld	Use linker_script_file.dld as the linker script. This script replaces the default linker script (rather than adding to it)

Table 9. Linker Options*...continued*

Option	Description
-m30	m2 + m4 + m8 + m16
-Xstack-usage	Gathers and display stack usage at link time
-Xpreprocess-lecl	Perform pre-processing on linker scripts
-Llibrary_path	Points to the libraries location for ARMV7EMMG to be used for linking
-lc	Links with the standard C library
-lm	Links with the math library

2.7.2 GCC Compiler/Linker/Assembler Options

Table 10. Compiler Options

Option	Description
-mcpu=cortex-m7	Targeted ARM processor for which GCC should tune the performance of the code
-mthumb	Generates code that executes in Thumb state
-mlittle-endian	Generate code for a processor running in little-endian mode
-mfpu=fpv5-sp-d16	Specifies the floating-point hardware available on the target
-mfloat-abi=hard	Specifies the floating-point ABI to use. "hard" allows generation of floating-point instructions and uses FPU-specific calling conventions
-std=c99	Specifies the ISO C99 base standard
-Os	Optimize for size. Enables all -O2 optimizations except those that often increase code size
-ggdb3	Produce debugging information for use by GDB using the most expressive format available, including GDB extensions if at all possible. Level 3 includes extra information, such as all the macro definitions present in the program
-Wall	Enables all the warnings about constructions that some users consider questionable, and that are easy to avoid (or modify to prevent the warning), even in conjunction with macros
-Wextra	This enables some extra warning flags that are not enabled by -Wall
-pedantic	Issue all the warnings demanded by strict ISO C. Reject all programs that use forbidden extensions. Follows the version of the ISO C standard specified by the aforementioend -std option.
-Wstrict-prototypes	Warn if a function is declared or defined without specifying the argument types
-Wundef	Warn if an undefined identifier is evaluated in an #if directive. Such identifiers are replaced with zero
-Wunused	Warn whenever a function, variable, label, value, macro is unused
-Werror=implicit-function-declaration	Make the specified warning into an error. This option throws an error when a function is used before being declared
-Wsign-compare	Warn when a comparison between signed and unsigned values could produce an incorrect result when the signed value is converted to unsigned.
-Wdouble-promotion	Give a warning when a value of type float is implicitly promoted to double

Table 10. Compiler Options*...continued*

Option	Description
-fno-short-enums	Specifies that the size of an enumeration type is at least 32 bits regardless of the size of the enumerator values.
-funsigned-char	Let the type char be unsigned by default, when the declaration does not use either signed or unsigned
-funsigned-bitfields	Let a bit-field be unsigned by default, when the declaration does not use either signed or unsigned
-fomit-frame-pointer	Omit the frame pointer in functions that don't need one. This avoids the instructions to save, set up and restore the frame pointer; on many targets it also makes an extra register available.
-fno-common	Makes the compiler place uninitialized global variables in the BSS section of the object file. This inhibits the merging of tentative definitions by the linker so you get a multiple-definition error if the same variable is accidentally defined in more than one compilation unit
-fstack-usage	Makes the compiler output stack usage information for the program, on a per-function basis
-fdump-ipa-all	Enables all inter-procedural analysis dumps
-c	Stop after assembly and produce an object file for each source file
-DS32K3XX	Predefine S32K3XX as a macro, with definition 1
-DS32K344	Predefine S32K344 as a macro, with definition 1
-DGCC	Predefine GCC as a macro, with definition 1
-DUSE_SW_VECTOR_MODE	Predefine USE_SW_VECTOR_MODE as a macro, with definition 1. By default, the drivers are compiled to handle interrupts in Software Vector Mode.
-DD_CACHE_ENABLE	Predefine D_CACHE_ENABLE as a macro, with definition 1. Enables data cache initalization in source file system.c under the Platform driver
-DI_CACHE_ENABLE	Predefine I_CACHE_ENABLE as a macro, with definition 1. Enables instruction cache initalization in source file system.c under the Platform driver
-DENABLE_FPU	Predefine ENABLE_FPU as a macro, with definition 1. Enables FPU initalization in source file system.c under the Platform driver
-DMCAL_ENABLE_USER_MODE_SUPPORT	Predefine MCAL_ENABLE_USER_MODE_SUPPORT as a macro, with definition 1. Allows drivers to be configured in user mode.

Table 11. Assembler Options

Option	Description
-Xassembler-with-cpp	Specifies the language for the following input files (rather than letting the compiler choose a default based on the file name suffix)
-mcpu=cortex-m7	Targeted ARM processor for which GCC should tune the performance of the code
-mthumb	Generates code that executes in Thumb state
-c	Stop after assembly and produce an object file for each source file

Table 12. Linker Options

Option	Description
-Wl,-Map,filename	Produces a map filer
-T linkerfile	Use linkerfile as the linker script. This script replaces the default linker script (rather than adding to it)
--entry=Reset_Handler	Specifies that the program entry point is Reset_Handler
-nostartfiles	Do not use the standard system startup files when linking
-mcpu=cortex-m7	Targeted ARM processor for which GCC should tune the performance of the code
-mthumb	Generates code that executes in Thumb state
-mfpu=fpv5-sp-d16	Specifies the floating-point hardware available on the target
-mfloat-abi=hard	Specifies the floating-point ABI to use. "hard" allows generation of floating-point instructions and uses FPU-specific calling conventions
-mlittle-endian	Generate code for a processor running in little-endian mode
-ggdb3	Produce debugging information for use by GDB using the most expressive format available, including GDB extensions if at all possible. Level 3 includes extra information, such as all the macro definitions present in the program
-lc	Link with the C library
-lm	Link with the Math library
-lgcc	Link with the GCC library

2.7.3 GHS Compiler/Linker/Assembler Options

Table 13. Compiler Options

Option	Description
-cpu=cortexm7	Selects target processor: Arm Cortex M7
-thumb	Selects generating code that executes in Thumb state
-fpu=vfpv5_d16	Specifies hardware floating-point using the v5 version of the VFP instruction set, with 16 double-precision floating-point registers
-fsingle	Use hardware single-precision, software double-precision FP instructions
-C99	Use (strict ISO) C99 standard (without extensions)
--ghstd=last	Use the most recent version of Green Hills Standard mode (which enables warnings and errors that enforce a stricter coding standard than regular C and C++)
-Osize	Optimize for size
--gnu_asm	Enables GNU extended asm syntax support
-dual_debug	Generate DWARF 2.0 debug information
-G	Generate debug information
-keeptempfiles	Prevents the deletion of temporary files after they are used. If an assembly language file is created by the compiler, this option will place it in the current directory instead of the temporary directory
-Wimplicit-int	Produce warnings if functions are assumed to return int
-Wshadow	Produce warnings if variables are shadowed
-Wtrigraphs	Produce warnings if trigraphs are detected
-Wundef	Produce a warning if undefined identifiers are used in #if preprocessor statements
--unsigned_chars	Let the type char be unsigned, like unsigned char

Table 13. Compiler Options*...continued*

Option	Description
--unsigned_fields	Bitfelds declared with an integer type are unsigned
--no_commons	Allocates uninitialized global variables to a section and initializes them to zero at program startup
--no_exceptions	Disables C++ support for exception handling
--no_slash_comment	C++ style // comments are not accepted andgenerate errors
--prototype_errors	Controls the treatment of functions referenced or called when no prototype has been provided
--incorrect_pragma_warnings	Controls the treatment of valid #pragma directives that use the wrong syntax
-c	Stop after assembly and produce an object file for each source file
-DS32K3XX	Predefine S32K3XX as a macro, with definition 1
-DS32K344	Predefine S32K344 as a macro, with definition 1
-DGHS	Predefine GHS as a macro, with definition 1
-DUSE_SW_VECTOR_MODE	Predefine USE_SW_VECTOR_MODE as a macro, with definition 1. By default, the drivers are compiled to handle interrupts in Software Vector Mode.
-DD_CACHE_ENABLE	Predefine D_CACHE_ENABLE as a macro, with definition 1. Enables data cache initalization in source file system.c under the Platform driver
-DI_CACHE_ENABLE	Predefine I_CACHE_ENABLE as a macro, with definition 1. Enables instruction cache initalization in source file system.c under the Platform driver
-DENABLE_FPU	Predefine ENABLE_FPU as a macro, with definition 1. Enables FPU initalization in source file system.c under the Platform driver
-DMCAL_ENABLE_USER_MODE_SUPPORT	Predefine MCAL_ENABLE_USER_MODE_SUPPORT as a macro, with definition 1. Allows drivers to be configured in user mode.

Table 14. Assembler Options

Option	Description
-cpu=cortexm7	Selects target processor: Arm Cortex M7
-preprocess_assembly_files	Controls whether assembly files with standard extensions such as .s and .asm are preprocessed
-list	Creates a listing by using the name and directory of the object file with the .lst extension
-c	Stop after assembly and produce an object file for each source file

Table 15. Linker Options

Option	Description
-T linker_script_file.ld	Use linker_script_file.ld as the linker script. This script replaces the default linker script (rather than adding to it)
-e Reset_Handler	Make the symbol Reset_Handler be treated as a root symbol and the start label of the application
-map	Produce a map file

Table 15. Linker Options*...continued*

Option	Description
-keepmap	Controls the retention of the map file in the event of a link error
-Mn	Generates a listing of symbols sorted alphabetically/ numerically by address
-delete	Instructs the linker to remove functions that are not referenced in the final executable. The linker iterates to find functions that do not have relocations pointing to them and eliminates them
-ignore_debug_references	Ignores relocations from DWARF debug sections when using -delete. DWARF debug information will contain references to deleted functions that may break some third-party debuggers
-Llibrary_path	Points to library_path (the libraries location) for thumb2 to be used for linking
-larch	Link architecture specific library
-lstartup	Link run-time environment startup routines. The source code for themodules in this library is provided in the src/libstartup directory
-lind_sd	Link language-independent library, containing support routines for features such as software floating point, run-time error checking, C99 complex numbers, and some general purpose routines of the ANSI C library
-v	Prints verbose information about the activities of the linker, including the libraries it searches to resolve undefined symbols
-keep=C40_Ip_AccessCode	Avoid linker remove function C40_Ip_AccessCode from Fls module because it is not referenced explicitly

2.7.4 IAR Compiler/Linker/Assembler Options

Table 16. Compiler Options

Option	Description
--cpu=Cortex-M7	Targeted ARM processor for which IAR should tune the performance of the code
--cpu_mode=thumb	Generates code that executes in Thumb state
--endian=little	Generate code for a processor running in little-endian mode
--fpu=FPv5-SP	Use this option to generate code that performs floating-point operations using a Floating Point Unit (FPU). Single-precision variant.
-e	Enables all IAR C language extensions
-Ohz	Optimize for size. the compiler will emit AEABI attributes indicating the requested optimization goal. This information can be used by the linker to select smaller or faster variants of DLIB library functions
--debug	Makes the compiler include debugging information in the object modules. Including debug information will make the object files larger
--no_clustering	Disables static clustering optimizations. Static and global variables defined within the same module will not be arranged so that variables that are accessed in the same function are close to each other

Table 16. Compiler Options*...continued*

Option	Description
--no_mem_idioms	Makes the compiler not optimize certain memory access patterns
--no_explicit_zero_opt	Do not treat explicit initializations to zero of static variables as zero initializations
--require_prototypes	Force the compiler to verify that all functions have proper prototypes. Generates an error otherwise
--no_wrap_diagnostics	Does not wrap long lines in diagnostic messages
--diag_suppress=Pa050	Suppresses diagnostic message Pa050
-DS32K3XX	Predefine S32K3XX as a macro, with definition 1
-DS32K344	Predefine S32K344 as a macro, with definition 1
-DIAR	Predefine IAR as a macro, with definition 1
-DUSE_SW_VECTOR_MODE	Predefine USE_SW_VECTOR_MODE as a macro, with definition 1. By default, the drivers are compiled to handle interrupts in Software Vector Mode.
-DD_CACHE_ENABLE	Predefine D_CACHE_ENABLE as a macro, with definition 1. Enables data cache initalization in source file system.c under the Platform driver
-DI_CACHE_ENABLE	Predefine I_CACHE_ENABLE as a macro, with definition 1. Enables instruction cache initalization in source file system.c under the Platform driver
-DENABLE_FPU	Predefine ENABLE_FPU as a macro, with definition 1. Enables FPU initalization in source file system.c under the Platform driver
-DMCAL_ENABLE_USER_MODE_SUPPORT	Predefine MCAL_ENABLE_USER_MODE_SUPPORT as a macro, with definition 1. Allows drivers to be configured in user mode.

Table 17. Assembler Options

Option	Description
--cpu Cortex-M7	Targeted ARM processor for which IAR should generate the instruction set
--cpu_mode thumb	Selects the thumb mode for the assembler directive CODE
-g	Disables the automatic search for system include files
-r	Generates debug information

Table 18. Linker Options

Option	Description
--map filename	Produces a map file
--config linkerfile	Use linkerfile as the linker script. This script replaces the default linker script (rather than adding to it)
--cpu=Cortex-M7	Selects the ARM processor variant to link the application for
--fpu=FPv5-SP	Use this option to generate code that performs floating-point operations using a Floating Point Unit (FPU). Single-precision variant.
--entry _start	Treats _start as a root symbol and start label
--enable_stack_usage	Enables stack usage analysis. If a linker map file is produced, a stack usage chapter is included in the map file

Table 18. Linker Options*...continued*

Option	Description
--skip_dynamic_initialization	Dynamic initialization (typically initialization of C++ objects with static storage duration) will not be performed automatically during application startup
--no_wrap_diagnostics	Does not wrap long lines in diagnostic messages

2.8 Examples and Demos

The drivers provide a set of examples. For details, please refer to Examples\... \readme.txt file from each driver folder.

3 Known Issues for S32K3 RTD 3.0.0 P01

3.1 Known Issues for 3.0.0

ID	Headline
ARTD-61591	[S32K3XX] [MEM_EXFLS] Bulk data read is not stable on K358, on HyperFlash board
ARTD-61572	[WDG] The Wdg_Example_S32M276 project build warning on S32DS
ARTD-61349	[I2C] Mismatch the define value between Requirement and Driver code
ARTD-61185	[S32K3] PwmEmiosBufRef error when S32CT is used in Turkish
ARTD-61124	[Integration][PORT] Pins tool: Incorrect build version
ARTD-61100	[Crypto] Remove the HSE interface file from the Crypto driver plugin
ARTD-61095	[S32K3XX] Crypto: Fix remaining Cwe/Misra/His warnings
ARTD-61009	[MCL] Fix INTEGER_OVERFLOW violation in CWE report
ARTD-60920	[Mcu] SXOSC is not available in 100 pin and 48 pin packages
ARTD-60460	[OCU] Fix VSMD rule TpsEcuc_08033 violation, for OcuHWSpecificSettingsRef parameter
ARTD-60454	[gpt] S32K312 STM timer Call back not triggered in s32k3 RTD version 2.0.3
ARTD-60442	[MCU] Range of SWG_CLK is different between EB and CT
ARTD-60374	[S32K3XX 3.0.0][Port] No error when enable invert control in input mode
ARTD-59912	[ZIPWIRE] Function should do nothing after DET error
ARTD-59682	[CRYPTO] Incorrect OID for SECP521
ARTD-59451	[ZIPWIRE] Blocking function return BUSY due to transfer is not done
ARTD-59283	[CRYPTO] Fix remain finding for code review checklist rule 29, 46, 47
ARTD-58529	[MemAcc] Services still return OK after retry reached 0
ARTD-56166	[ZIPWIRE] Initialize Slave failure in HIGH_SPEED_MODE
ARTD-54994	[FLS] [S32K3] Fls_Write potential bug
ARTD-54548	[Mcu] Cannot enable CMU_5 on S32K3xx
ARTD-54102	[SPI][S32K3xx][FLEXIO] Master CS is only continuous between datas in channel but not between channels in job
ARTD-52748	[UART] Not match number of instance between .xls file and RM on S32K396

ID	Headline
ARTD-52623	[CAN] Wrong idHit value
ARTD-47333	[SPI][S32K311] Readding feature and fix: Example Flexio slave reports Rx overrun error at the last Rx frame
ARTD-46975	[S32K3XX] [FLS] Bulk data read is not stable on K358, on HyperFlash board
ARTD-41757	S32K3 RTD component version shown error
ARTD-40410	[S32DS] Debug failed with NPW S32K396 attached RTD + IAR Toolchain
ARTD-38119	[GMAC][SAF85xx] Fatal Bus Error detected when receiving Eth frame at high throughput
ARTD-29346	[Mcu] Validation error due to missing PreConfiguredConfiguration
ARTD-29053	[ADC] 2 DMA request in parallel from both ADC and CTU when starting a CTU control mode conversion after a SW one-shot single access mode group finishes
ARTD-29049	[BASE] USE_CAN_MODULE and USE_LIN_MODULE generated as STD_OFF even if Can and Lin are present in project
ARTD-28743	[Pins tool] Check all the bitfields in MSCRs again, show as N/A for unavailable cases for S32K3, S32XX and S32ZE
ARTD-25729	[icu] To investigate if global config variables should be declared with const keyword
ARTD-25728	[gpt] To investigate if global config variables should be declared with const keyword
ARTD-8089	[I2S] For I2S over SAI the DMA transferred data is incorrect when FIFO packing enabled
ARTD-8063	[MCL] Can not jump to callback when major interrupt did not configure consistently with each element
ARTD-7913	[MCU] Fix VSMD errors related to XPath expression for MIN attributes - resource file not found
ARTD-61276	[LINTRCV][VSMD] Fix waring and Error in VSMD report
ARTD-60618	[S32M27x][Pins tool] Missing TSPC, ADC Interleave configuration
ARTD-60403	[SPI]The reentrant problem about Lpspi_Ip_IrqTx/RxDmaHandler
ARTD-60141	[MCU] Low power modes of S32Kxx cannot operate as expected

4 Changes List for S32K3 RTD 3.0.0 P01

4.1 Change List for 3.0.0 p01

ID	Subtype	Headline and Description
ARTD-25946	Bug	[FEE] Warnings of zero-initialized variables with complier IAR Detailed description (how to reproduce it): When building Fee driver with IAR compiler, there are some warnings appear, because of zero-initialized variables still have explicit zero-initializers Root cause: there was an incorrect fixing for{color}{color:#172b4d} compiler warning, it did not follow the rule of zero-initialized variables in "CLEARED" memory sections [https://bitbucket.sw.nxp.com/projects/ARTD/repos/fee/pull-requests/117/diff#generic/src/Fee.c] Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: There are compiler warning on IAR Expected behavior: There are no warnings Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Remove all explicit zero-initializers in the "CLEARED" memory sections. Following the guidline in the ticket: https://jira.sw.nxp.com/browse/ARTD-12239
ARTD-54375	Bug	[FEE] - UM Memory dump example has incorrect information Detailed description (how to reproduce it): In User Manual document, section 3.6.2 Memory Dump Example: One group of two clusters is configured: # The first cluster has start address 0x10000. # The second cluster has start address 0x18000. !image-2023-02-03-13-16-09-282.png|width=767,height=295! However, the size of first cluster is 0x10000.It will overlap in the memory of the second clusters. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Start address of 2nd cluster in this example is not correct, will leads to the confusion for customer . It should be change to 0x20000 Expected behavior: Start address of 2nd cluster in this example is not correct, will leads to the confusion for customer . It should be change to 0x20000 Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A

ID	Subtype	Headline and Description
ARTD-55453	Bug	[fls] [GENERAL] PLUGINS_DIR should point to RTD plugin folder instead of EB Tresos plugin folder in readme.txt Detailed description (how to reproduce it): In readme.txt file, the following sentence: PLUGINS_DIR The path to the Tresos plugins directory !john_floros_0-1653582301493.png|width=696,height=261! In fact, PLUGINS_DIR should point to RTD plugin folder instead of EB Tresos plugin folder in readme.txt Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: PLUGINS_DIR points to EB Tresos plugin folder in readme.txt, which is incorrect. Expected behavior: PLUGINS_DIR should point to RTD plugin folder instead of EB Tresos plugin folder in readme.txt. PLUGINS_DIR The path to the RTD plugins directory Ex: PLUGINS_DIR = C:/NXP/SW32_RTD/eclipse/plugins Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: PLUGINS_DIR should point to RTD plugin folder : PLUGINS_DIR The path to the RTD plugins directory Ex: PLUGINS_DIR = C:/NXP/SW32_RTD/eclipse/plugins
ARTD-55321	Bug	[S32K3XX] [FLS] Qspi_lp_Abort has no prototype Detailed description (how to reproduce it): Qspi_lp_Abort has no prototype, so iar compiler cannot build tests Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Fls_TS_020 Observed behavior: as description Expected behavior: build successfully Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: add prototype
ARTD-55731	New Feature	[S32K3 3.0.0] Eep : added feature to enable/disable CRC Configuration Check (req CPR_RTD_00678.eep) NewWorkDescription: Eep S32K3 3.0.0 has the new req CPR_RTD_00678.eep uncover. CPR_RTD_00678.eep: An optional, vendor specific parameter shall disable consistency check through CRC of the flash descriptor. Rationale: If the image is already authenticated, the CRC configuration check is not required. Requirement source: CPR_RTD_00678.eep (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Added feature to enable/disable CRC Configuration Check to cover this requirement.

ID	Subtype	Headline and Description
ARTD-59210	Bug	[S32K3XX] [FLS] Update the return value to fix test build and run fail Detailed description (how to reproduce it): wrong the the return value. !image-2023-03-09-09-37-23-076.png! Preconditions: Test Case ID (internal TC that caught the defect) optional: Fls_TS_000 Observed behavior: wrong the the return value Expected behavior: test pass Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-59951	Bug	[S32K3 3.0.0] [EEP] Compiler warning when enable multicore Detailed description (how to reproduce it): When user enable multicore support, compiler report there warning in Rm_Sema42_ChannelType Preconditions: Eep driver have no waring in all configuration case Test Case ID (internal TC that caught the defect) optional: Eep_TS_001 Observed behavior: When user enable multicore support, compiler report there warning in Rm_Sema42_ChannelType Expected behavior: Eep driver have no waring in all configuration case Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: n/A
ARTD-60480	Bug	[S32K3 3.0.0][EEP] Remove redundant codes which support HS200 HS400 in S32K3XX platform Detailed description (how to reproduce it): S32K3XX do not support high speed HS200/HS400 (1v8 mode), this feature has been barrier in driver code to isolate by define and validate in interface. But it will impact to CCOV in test side. Need use M4 to remove redundant codes which support HS200 HS400 in S32K3XX platform Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: CCOV in test side is low Expected behavior: CCOV in test side is high Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Remove redundant codes which support HS200 HS400 in S32K3XX platform

ID	Subtype	Headline and Description
ARTD-25882	Bug	[FLS] Write data error when the data size will go over the sector boundary Detailed description (how to reproduce it): when writing data on a sector in asynchronous mode and if this data length causes spanning, it will causes errors. After code analyze, this is a bug which the low level driver process a wrong sector index when the write data need to cross sectors. And this issue exist in both K1 and K3 RTD. Preconditions: write data in async mode, and the write data size will across the sector edge. Test Case ID (internal TC that caught the defect) optional: None Observed behavior: write data error Expected behavior: Write data normally Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: add the index variable when the case happened in the low level driver, can refer to the MCAL code.
ARTD-26477	Bug	[FLS] [QSPI] SEQID is treated as a LUT index Detailed description (how to reproduce it): In the functions mentioned below the lut parameter is actually a sequence ID, and not a LUT index: Qspi_Ip_IpWrite}} Qspi_Ip_IpRead}} Qspi_Ip_IpCommand}} Besides the confusion, the functional defect is that the parameter is checked against the maximum number of LUT registers: DEV_ASSERT_QSPI(lut < QuadSPI_LUT_COUNT);}} Preconditions: none Test Case ID (internal TC that caught the defect) optional: no TC Observed behavior: the check is too permissive Expected behavior: we should differentiate between the id of the sequence and the index of the LUT register Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Besides the functional change proposed below, a better naming of the parameters would be suited: DEV_ASSERT_QSPI(SeqId < QuadSPI_LUT_COUNT / FEATURE_QSPI_LUT_SEQUENCE_SIZE);}}
ARTD-26603	Bug	[Fls][S32ZE_EAR_080] Remove include "Os.h" in Fls.h for avoiding build failed re-declared function Detailed description (how to reproduce it): Since Os.h has been updated as https://bitbucket.sw.nxp.com/projects/ARTD/repos/os/pull-requests/35/diff#generic/include/Os.h: Build failed occure (re-declare ResumeAllInterrupts() and SuspendAllInterrupts()) on GHS if USER_MODE enable . Preconditions: Osif_Internal.h defines the above APIs already Test Case ID (internal TC that caught the defect) optional: All test build on GHS with USER_MODE enable Observed behavior: Build failed on GHS. Expected behavior: Fls.h shall be updated Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA

ID	Subtype	Headline and Description
ARTD-28180	Bug	[FLS][S32K3XX] Issue in data write using C40 flash (lack of end boundary check for input paramerter) Detailed description (how to reproduce it): If FLS address is 8 bytes aligned for ex:(0x500010) and data length is 128 bytes , in that case data is written from 0x500010 to 0x50007F keeping last 16 bytes unchanged. Observed behavior: Only 112 bytes are written from 0x500010 to 0x50007F Expected behavior: Data should be written from 0x500010 to 0x50008F i.e 128 bytes Proposed solution optional: [....]
ARTD-47525	New Feature	[FLS] RTD driver memory resource reduction NewWorkDescription: Implement RTD driver memory optimizations. Implementation of Change Request AAI-1345 Compiler used: IAR Requirement source: Customer Request Proposed solution optional: Implement proposals agreed on change request, as per conclusions provided in ppt documents attached to current ticket and AAI-1345. More details available in tickets dedicated for memory optimizations analysis, cloned for each driver from ARTD-43887. Update driver UserManual, UML design and examples accordingly. If new requirements are created, run traceability to ensure the new requirements are covered. Attach to this ticket an xlsx document with memory size before and after optimizations.

4.2 Change List for 3.0.0

ID	Subtype	Headline and Description
ARTD-8787	Bug	Performing an RTD update through updatesite clears the PlatformIntegration installation When installing the RTD update site, PlatformIntegration installation is cleared and needs to be reinstalled.
ARTD-9657	New Feature	[BUILD_ENV] Create a .dox page for all IMs to clarify the OsIf timeout approach NewWorkDescription: Clarify for the users the OS initialization issue (sys timers not available before OS is initialized) and their options. Requirement source: N/A (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Create a .dox page to clarify the OsIf timeout approach and modify the ToC in rtd_docgen so that it will be automatically included by all IMs.
ARTD-9987	Bug	[ICU][S32DS] Errors are reported when configuring multiple variants in DS There are two mainly problem with S32DS when configuring many variant: Firstly, when i switch between variants (VS0,VS1, VS2) the node in IcuGeneral section in S32DS interface also change. This section should be not changeable when user switch to other VS. Secondly, some error with output configuration as the attached picture. Adittionally, checking with test suite Icu_TS_DS_M04 contains 10 config set.

ID	Subtype	Headline and Description
ARTD-14052	New Feature	[I3C] Add support for Master Request NewWorkDescription: Master Request Please refer to initial analysis done in https://nxp1.sharepoint.com/:x:/s/Zebra/EedqZRWa0ElLk5-n2OhCB8MByBV0CEBRFInle2wexrt_0g?e=TP6TXV Check if requirement available or need any updates Create/update dev test Add section/update UM Update UML if required If examples already available, update examples with any eventual new nodes Requirement source: RM.pdf Proposed solution optional: [...]
ARTD-15063	New Feature	RTD MCAL Example project makefile optimization For the example projects included in the RTD MCAL, the GCC compiler will rebuild all files even if only one source file is modified a little bit. Is it possible to optimize the make file or the build script file so that only the modified source files are built when we run the "make build" command?

ID	Subtype	Headline and Description
ARTD-15712	New Feature	[port] Enable ECPD generation for IP components (CPR_RTD_00544) Note: This feature must be implemented by all the modules for which this ticket was cloned (including CDDs). No clone shall be closed with "Not Applicable" or "No Action Taken". How to implement: # Add "options_expr" tags (containing all the necessary options) for the fields of the IP component(s). Please refer to the slides covering "EPD Generation" in Reference #2 below. # To ensure that the ECPD is generated only for your component, modify line 512 in "mcu_data/components/PlatformSDK_S32K3_2021_08/system/codegenerator.js" as follows: {code:javascript} if (configComponent.isOptionSet("ecucDefinitionCollection") && (configComponent.getId() === "Gmac")) { where you can replace "Gmac" with the ID of your IP component. # Check that there are no errors reported in the Problems view and that the ECPD has been generated in Code Preview. How to validate: # Manually create an EBT plugin using the previously generated ECPD. To achieve this: ## Unzip [^Ip_TS_T40D34M10I0R0.zip] in the "output/eclipse/plugins" folder of your K3 work tree / repository. ## Open "Ip_TS_T40D34M10I0R0/plugin.xml" and replace all occurrences of "Gmac" with the ID of your IP component. # Create an EBT project (File > New > Configuration Project > Project Name: TstIp > Next > ECU ID: someId; Target: CORTEXM/S32K3XX > Finish) and add the previously created module (Right click on TstIp in Project Explorer > Module Configurations... > Double click on your module > OK) CHECKPOINT 1: The module should have been successfully imported into the project. # Go to S32DS and create a valid project using your IP component (or use an already existing one). {*}{color:#FF0000}Please assign a value other than the default value to each setting to avoid default values in this configuration{color}{*}. Rename your IP component instance and discard the "_1" prefix (e.g. "Gmac_1" > "Gmac"): !screenshot-1.png! # Generate the [LT/PB]Cfg.h/.c files of your IP component and save them somewhere to avoid overwriting them in a later step. We'll call this set of files {_}OriginalGenerateFiles{_}. # Generate the ECVD file for your IP component instance (Global Settings > EcvdGenerationMethod = INDIVIDUAL > EcvdOutputPath = <EcvdOutputDir> > Click on the "Generate Configuration" button) # Import the previously generated ECVD file in your EBT project (Right click on TstIp in Project Explorer > Im and Exporters... > Green Button > Next > File Name: <Browse and select the ECVD file> > Next > Enable path mapping > Finish > Run Importer) CHECKPOINT 2: The ECVD file should have been successfully applied to your module. # Save (CTRL S) and generate the project (Right click on TstIp in Project Explorer > Generate Project) to trigger the EPC generation. CHECKPOINT 3: The EPC file should have been successfully generated (TstIp/output/output/<Ip>.epc) # Import the previously generated EPC file in your S32DS project (File > Import > Import ECU Configuration > Path: <EpcOutputDir> > Check "Merge into current configuration" > Check "Check ECUC-MODULE-DEF" value > CHECKPOINT 4: The EPC file should have been successfully imported into your S32DS project. If you get the error "The required modules are not available for the current configuration" it means that the ECUC-MODULE-DEF check has failed and you're not properly using M4_XDM_AR_PKG_NAME in your IP component. # Generate again the [LT/PB]Cfg.h/.c files of your IP component and save them somewhere without overwriting the previous set of files. We'll call this new set of files {_}ImportedGenerateFiles{_}. # Compare the OriginalGenerateFiles set with the ImportedGenerateFiles set. CHECKPOINT 5: The comparison should be binary identical. There should be no single difference between the two set of files. Requirements covered by this ticket: CPR_RTD_00544 EA_RTD_00107 EA_RTD_00108 References: # [^Ethernet.template] # [https://nxp1.sharepoint.com/:p:/s/Zebra/EaMbpShSxPVAq7amkzZx3NMB1LWDlRvDlnrzP1m0TZ9elQ?e=erB0sH] (Relevant chapters: "9. EPD Importer Replacing the lost GNU M4 macros", "10. EPD Generation", "11. EPC Importer", "12. EPC Generation") Legend: EPD ECU Parameter Definition (Schema) Used by EBT ECPD ECU Configuration Parameter Definition (Schema) Used by S32CT EPC ECU Parameter Configuration (Configuration File) Used by EBT ECVD ECU Configuration Value Description (Configuration File) Used by S32CT For S32K3, for mapping file, because un-matching about peripherals between EB and Pins tool, so peripheral in mapping files was modified manually with mixing between upper and lowercase: eMIOS, JTAG_TRACEnoETM...
ARTD-17295	New Feature	[I3C] Add development test for multiple variants NewWorkDescription: Add development test for multiple variants For rest of new features, the dev tests must be added on new feature ticket (even if will not be run automatically because requires 2 boards setup)

ID	Subtype	Headline and Description
ARTD-19058	New Feature	[ETH][NETC] Implement scatter gather on transmission NewWorkDescription: Allow sending multiple buffer pointers using a single Send command. For example: buffer1 = headers of the frame (dest mac, src mac, eth type, tcp header, etc.) buffer2 = payload One single send command will bring the 2 buffers together in one single frame Requirement source: Internal requirement (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Use the buffer descriptor chaining feature to do this
ARTD-19252	Bug	[CRYPTO] Fix remain finding for code review checklist Fix remain finding for rule 6, 10, 29, 46, 47 at ARTD-16954. Rule 6, 10: https://teams.microsoft.com/l/message/19:ffb5bcb3ccf94d4cb64209a2b0fe242f@thread.tacv2/1630979638112?tenantId=686ea1d3-bc2b-4c6f-a92c-d99c5c301635&groupId=f9decd68-7b74-4101-a4d2-ad54e86f727f&parentMessageId=1630979638112&teamName=Zebra&channelName=Group%200&createdTime=1630979638112 Rule 46, 47: https://teams.microsoft.com/l/message/19:ffb5bcb3ccf94d4cb64209a2b0fe242f@thread.tacv2/1630415151959?tenantId=686ea1d3-bc2b-4c6f-a92c-d99c5c301635&groupId=f9decd68-7b74-4101-a4d2-ad54e86f727f&parentMessageId=1630415151959&teamName=Zebra&channelName=Group%200&createdTime=1630415151959 Rule 29: Currently the rule 29 is not followed in code, the notation used for most of the variables and parameters, if not all, is Hungarian notation, this happened because the code was imported from MCAL to RTD and provided clear information about the variable/parameter type. !image-2021-11-08-16-18-31-180.png|thumbnail!
ARTD-19289	New Feature	[UART] - Support Loopback mode on Uart driver NewWorkDescription: Support Loopback mode transfer Requirement source: RM.pdf Proposed solution optional: Add a check in configurator in order to put the driver in loopback or not Configure the driver accordingly Add testcase to validate the feature.

ID	Subtype	Headline and Description

ARTD-20015	New Feature	[gpt] incorrect PIT channel interrupt flag cause interrupt missing
		
		Detailed description (how to reproduce it):
		
		in RTD LLD API function Pit_Ip_ProcessCommonInterrupt()* (file Pit_Ip.c_*), the PIT channel interrupt flag clear should be called after checking & confirming its corresponding interrupt flag is actually set to avoid interrupt missing:
		
		Preconditions:
		[...]
		
		Test Case ID (internal TC that caught the defect) optional:
		[...]
		
		Observed behavior:
		
		original codes with incorrect interrupt flag clear:
		
		static void Pit_Ip_ProcessCommonInterrupt(uint8 instance, uint8 channel)
		{
		uint32 flagEnable = 0U;
		uint32 interruptEnable = 0U;
		
		/*Checks for spurious interrupts*/
		flagEnable = Pit_Ip_GetInterruptFlags(instance, channel);
		interruptEnable = Pit_Ip_GetInterruptBit(instance, channel);
		/ Clear interrupt flag /
		Pit_Ip_ClearInterruptFlag(instance, channel);
		
		if ((1U == flagEnable) && (1U == interruptEnable))
		{
		#if (PIT_IP_CHANGE_NEXT_TIMEOUT_VALUE == STD_ON)
		Pit_Ip_bIsChangedTimeout = FALSE;
		#endif
		/ Call upper layer handler /
		if((TRUE == Pit_Ip_u32ChState[instance][channel].chInit) && \
		(NULL_PTR != Pit_Ip_u32ChState[instance][channel].callback))
		{
		Pit_Ip_u32ChState[instance][channel].callback(Pit_Ip_u32ChState[instance][channel].callbackParam);
		}
		}
		}
		
		Expected behavior:
		
		should be correctted as below*:
		
		static void Pit_Ip_ProcessCommonInterrupt(uint8 instance, uint8 channel)
		{
		uint32 flagEnable = 0U;
		uint32 interruptEnable = 0U;
		
		/*Checks for spurious interrupts*/
		flagEnable = Pit_Ip_GetInterruptFlags(instance, channel);
		interruptEnable = Pit_Ip_GetInterruptBit(instance, channel);
		
		if ((1U == flagEnable) && (1U == interruptEnable))
		{
		#if (PIT_IP_CHANGE_NEXT_TIMEOUT_VALUE == STD_ON)
		Pit_Ip_bIsChangedTimeout = FALSE;
		#endif
		
		/ Clear interrupt flag /
		Pit_Ip_ClearInterruptFlag(instance, channel);
		
		/ Call upper layer handler /
		if((TRUE == Pit_Ip_u32ChState[instance][channel].chInit) && \
		(NULL_PTR != Pit_Ip_u32ChState[instance][channel].callback))
		{
		Pit_Ip_u32ChState[instance][channel].callback(Pit_Ip_u32ChState[instance][channel].callbackParam);
		}
		}
		}
		
		Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)
		
		Proposed solution optional:
		[...]

ID	Subtype	Headline and Description
ARTD-20021	Bug	[S32K3xx] Project S32K342 attach sdk RTD 2.0.0 then update code build fail with Ram configuration Step: 1.Create project S32K342 and attach sdk RTD 2.0.0 2. Open S32CT tool > set some config to Pin/Clock/Peripheral tool > Update code 3. Build Ram Observed behavior: 3. Project build fail with error Building target: k342.elf Invoking: Standard S32DS C Linker arm-none-eabi-gcc o "k342.elf" "@k342.args" e:/nxp/s32ds.3.4/b211123sp3/s32ds/build_tools/gcc_v10.2/gcc-10.2-arm32-eabi/bin/../lib/gcc/arm-none-eabi/10.2.0/../../../../arm-none-eabi/bin/real-ld.exe: warning: e:/nxp/s32ds.3.4/b211123sp3/s32ds/build_tools/gcc_v10.2/gcc-10.2-arm32-eabi/bin/../lib/gcc/arm-none-eabi/10.2.0/../../../../arm-none-eabi/lib/thumb/v7e-m+fp/hard\libc_nano.a(lib_a-memmove.o) uses variable-size enums yet the output is to use 32-bit enums; use of enum values across objects may fail e:/nxp/s32ds.3.4/b211123sp3/s32ds/build_tools/gcc_v10.2/gcc-10.2-arm32-eabi/bin/../lib/gcc/arm-none-eabi/10.2.0/../../../../arm-none-eabi/bin/real-ld.exe: warning: e:/nxp/s32ds.3.4/b211123sp3/s32ds/build_tools/gcc_v10.2/gcc-10.2-arm32-eabi/bin/../lib/gcc/arm-none-eabi/10.2.0/../../../../arm-none-eabi/lib/thumb/v7e-m+fp/hard\libc_nano.a(lib_a-memset.o) uses variable-size enums yet the output is to use 32-bit enums; use of enum values across objects may fail e:/nxp/s32ds.3.4/b211123sp3/s32ds/build_tools/gcc_v10.2/gcc-10.2-arm32-eabi/bin/../lib/gcc/arm-none-eabi/10.2.0/../../../../arm-none-eabi/bin/real-ld.exe: k342.elf section `.heap' will not fit in region `int_sram' e:/nxp/s32ds.3.4/b211123sp3/s32ds/build_tools/gcc_v10.2/gcc-10.2-arm32-eabi/bin/../lib/gcc/arm-none-eabi/10.2.0/../../../../arm-none-eabi/bin/real-ld.exe: section .acfls_code_rom LMA [20408488,204084bb] overlaps section .non_cacheable LMA [20408000,2040869b] e:/nxp/s32ds.3.4/b211123sp3/s32ds/build_tools/gcc_v10.2/gcc-10.2-arm32-eabi/bin/../lib/gcc/arm-none-eabi/10.2.0/../../../../arm-none-eabi/bin/real-ld.exe: section .non_cacheable VMA [20408000,2040869b] overlaps section .heap VMA [20406488,20408487] e:/nxp/s32ds.3.4/b211123sp3/s32ds/build_tools/gcc_v10.2/gcc-10.2-arm32-eabi/bin/../lib/gcc/arm-none-eabi/10.2.0/../../../../arm-none-eabi/bin/real-ld.exe: region `int_sram' overflowed by 5360 bytes collect2.exe: error: ld returned 1 exit status make: [makefile:40: k342.elf] Error 1 "make j6 all" terminated with exit code 2. Build might be incomplete. Expected behavior: 3. Project build successfully or note to document as know issue
ARTD-20032	New Feature	[RM] XRDC shall allow locking the XRDC registers (follow up ticket) NewWorkDescription: ZSE platform provides 11 instances of XRDC, this feature need to be updated more to simplify driver code. !image-2021-11-30-13-52-23-248.png! Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Support locking the XRDC configured registers, as a configuration option. Could be done by having some extra masks or in a separate step at the end of init.
ARTD-22020	New Feature	[ETH]Add infix support in the Eth driver NewWorkDescription: Add infix support in the Eth driver Requirement source: Planned activity (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: For having separate and independent namespaces, drivers with the defined multiplicity greater than 1 need to have their name extended with an infix. Steps: Outside of the driver: Add in Base a new MemMap Eth_43_NETC_MemMap.h generated for the new naming Add in Rte new SchM files Schm_Eth_43_NETC,c and Schm_Eth_43_NETC.h generated for the new naming In the driver: Add in the HLD and IPW M4 tags that will be replaced with the infix The files need to be renamed, the types, the functions, etc. Do not rename the types and defines that are specified in Eth_GeneralTypes. Those need to keep their name, as they will be used as defined by all Eth drivers (if more drivers are present in a project) Update the xdm file to change the package name and use the short_name of the driver instead of MODULE_NAME where needed Update the mak file of the driver to rename all files and to propagate the m4_infix_value in all needed files In the tests: Change the xdm configuration for the tests to use the new format Change the mak file of the tests to compile the correct plugin folder Create a wrapper file Eth.h which includes Eth_43_NETC.h and redefines all needed macros, typedefs and functions to point to the newly named entities

ID	Subtype	Headline and Description
ARTD-23123	New Feature	[ADC] Workaround for incorrect data of first channel if using CTU or Injected sw/hw trigger NewWorkDescription: Need workaround for issue with incorrect data of first channel of a chain when conversion triggered by CTU or sw/hw injected mode. Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: NA

ID	Subtype	Headline and Description
ARTD-23614	Bug	[Base] -fdump-ipa-all shall not be used in project setting by default Detailed description (how to reproduce it): See the report from Mike and an internal user below for DS3.4 Seems the makefile generator for GCC ARM is enabling a GCC developer option, fdump-ipa-all. This option dumps internal GCC optimization information – not useful to the user. In this case, a user is getting an error. I suppose in most cases, the dump file would be created and destroyed without the user ever knowing it was created. Since this is a GCC developer option, no user would ever have any use for it, so it is a bit mysterious why it should show up in projects. I searched some of my 3.4 projects and found the flag in the some of the projects' arg files. … I"C:/Users/nxa10550/workspaceS32DS.3.4/project.zip_expanded/Crypto_Aes_Enc_Dec/generate/src" I"C:/Users/nxa10550/workspaceS32DS.3.4/project.zip_expanded/Crypto_Aes_Enc_Dec/generate/include" Os fshort-enums funsigned-char fstack-usage fdump-ipa-all fomit-frame-pointer Looking a bit closer – could this have come from an RTD project imported from somewhere else because the "Other optimization flags" string field is apparently set. ./.cproject: <option id="gnu.c.compiler.option.optimization.flags.1148268502" name="Other optimization flags" superClass="gnu.c.compiler.optio n.optimization.flags" useByScannerDiscovery="false" value="-fshort-enums funsigned-char fstack-usage fdump-ipa-all fomit-frame-pointer fno-zero-initialized-in-bss" valueType="string"/> This appears also in a new application project see attached email. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: see above Expected behavior: see above Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA

ID	Subtype	Headline and Description
ARTD-23790	Bug	[ADC] Self-test does not validate data Detailed description (how to reproduce it): ERR_x error flag only will happen only when enable STAWxR[AWDE] and data in STDR1 is out of range between STAWxR[THRH] and STAWxR[THRL] !screenshot-1.png|thumbnail! Current implementation is just checking ERR_x in Adc_Sar_CheckSelfTestProgress without enabling STAWxR[AWDE] Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: NA Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-24108	Bug	[I3c] HDR-DDR sync master write not working for buffer sizes larger than 16 Detailed description (how to reproduce it): Build and run TS_014 and TS_015. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: Sync write is not working for buffer sizes larger than FIFO_SIZE. Expected behavior: Sync write is works for buffer sizes larger than FIFO_SIZE. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-24139	Bug	[GPT] PIT 64bit Lifetime Timer not supported Detailed description (how to reproduce it): I want to use PIT 64bit Lifetime Timer as a free-running 64 bit counter. I have 2 issues to configure it so using the GTP driver: 1) Setting LDVAL to 0xFFFFFFFF. The driver sets 0xFFFFFFF{*}+E+{*}, if 0xffffffff is provided. The driver does not accept 0. The driver accepts 32-bit value only, so 0x100000000 cannot be provided as well. There is no way to set LDVAL to 0xFFFFFFFF. 2) Setting the chain mode The Tresos “ChainMode” option is not applied to the hw register. Preconditions: tresos.png Test Case ID (internal TC that caught the defect) optional: n/a Observed behavior: observed.png Expected behavior: expected.png Proposed solution optional: A special on/off option for "64bit Lifetime free-running counter", which configures channel 0 and 1 accordingly.

ID	Subtype	Headline and Description
ARTD-24155	New Feature	[ADC] Multiple triggering unit support NewWorkDescription: Currently both Autosar and non-Autosar drivers/modules are hardcoded to work with a single CTU/BCTU unit. S32K396 and S32E27/S32S27 have more than one triggering unit available so modifications are required to the drivers in order to support these platforms. Requirement source: S32K396RM_Rev1_Draft_H.pdf S32E27RM_Rev1DraftAI.pdf Proposed solution optional: NA
ARTD-24454	Bug	[MCU] When setting Mcu Register Values Optimization is enable, mcu can not init Detailed description (how to reproduce it): When setting Mcu Register Values Optimization is enable, MCU can not init !screenshot-1.png|thumbnail! Issue2: Improvement generation script: 2 list MCU.CMU_FC.Address.List}} and {{MCU.CMU_FC.List}} contain same information: cmuInstance and cmuMonitorname.-> using string operation and add function macro to use 1 list only try "constrains" to avoid using multiple #IF to check McuCmuName Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: hardfault when call MCU_initclock() Expected behavior: MCU_initclock() run fine Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc. Proposed solution optional: [...]
ARTD-24504	New Feature	[S32CT] Prepare environment for multiple configurations support NewWorkDescription: Prepare environment for multiple configurations support Requirement source: [SRS_BSW_00405] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Prepare environment for multiple configurations support
ARTD-24518	Bug	[I3c] InBandInterrupt address is always 0 in Get Ibi Address Callback when DynamicAddressAssignment is done at Init Detailed description (how to reproduce it): Build TS_0010 and TS_011. Set I3C_IP_ENABLE_DAA_INIT_TIME = STD_ON and run the tests. Preconditions: Set I3C_IP_ENABLE_DAA_INIT_TIME = STD_ON Test Case ID (internal TC that caught the defect) optional: TS_010, TS_011 Observed behavior: Get IBI Address callback returns IbiAddress = 0, even if all IBI data bytes are correctly received by the master. Expected behavior: Get IBI Address callback returns correct IbiAddress. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: None

ID	Subtype	Headline and Description
ARTD-24536	Bug	[ADC] Self-test does not validate data Detailed description (how to reproduce it): ERR_x error flag only will happen only when enable STAWxR[AWDE] and data in STDR1 is out of range between STAWxR[THRH] and STAWxR[THRL] !screenshot-1.png|thumbnail! Current implementation is just checking ERR_x in Adc_Sar_CheckSelfTestProgress without enabling STAWxR[AWDE] Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: NA Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-24541	Bug	[S32K3 2.0.0][SENT] DMA can not get all serial msg when receive from all channel at the same time Detailed description (how to reproduce it): I created a test to receive many serial msg from 8 channels at the same time by using DMA. But it missed some serial msg from some channel. When use DMA buffer = 1, the test sometimes pass, sometimes fail. When use DMA buffer > 1, the test always fail. Preconditions: Using DMA to receive many serial frames from many channel at the same time. Test Case ID (internal TC that caught the defect) optional: TS_22 Observed behavior: NA Expected behavior: NA Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-25284	Bug	[MCU] Incorrect default frequency value for CORE_CLOCK on S32K312 Detailed description (how to reproduce it): Incorrect default frequency value for CORE_CLOCK on S32K312 Max frequency of CORE_CLOCK on S32K312 is 120Mhz, but in clocks tool default value of CORE_CLOCK is 160Mhz Preconditions: Create new project for S32K312 on S32CT > move to clocks tool Test Case ID (internal TC that caught the defect) optional: Mcu_TC_COT_003 Observed behavior: Frequency CORE_CLOCK is 160Mhz Expected behavior: Frequency CORE_CLOCK is 120Mhz Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update range of CORE_CLOCK maximum is 120Mhz

ID	Subtype	Headline and Description
ARTD-25461	Bug	[I2S] SAI DMA transfer counts limited by 32767, but no assert/warning by RTD Detailed description (how to reproduce it): [Invoke "void Sai_Ip_Send(const uint8 u8Instance, const uint8 const aData[], const uint32 u32Count)" with more than 32767 counts] Preconditions: [SAI work in DMA transfer mode] Test Case ID (internal TC that caught the defect) optional: [SFDC CN 00456190] Observed behavior: [Only part of the u32Count can be transfered, the DMA TCD major loop counts CITTER[0-14] which will cut lower 15-bits width of the total "u32Count"] Expected behavior: [all of the u32Count data can be transfered, or a warning/assert to indicate the input param out of range] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [Software divided the source data to multiple slices, and ensure each of the slice data counts under the "DMA mode, 32767 counts" limitation]
ARTD-25493	New Feature	[gpt] RTC_IP_TICKS_PER_SECOND is always 0 on EB project Our leader customer continental needs to use RTC to get time and wakeup function on EB project. They found RTC_IP_TICKS_PER_SECOND in Rtc_Ip_Cfg.h was not equal to the value of GptChannelTickFrequency on EB, it was always 0 on generated codes from EB which would influence some RTC IP functions, for example, in RTC_IP_TicksToSeconds(), the RTC_IP_TICKS_PER_SECOND = 0 will be divisor, it's unreasonable. It's very inconvinient for them to modify this macro definition manually on their system each time. The RTC_IP_TICKS_PER_SECOND could be auto-generated by EB.
ARTD-25548	New Feature	[mcu] Check requirements, documentation and code for Mcu_GetPowerModeState API Mcu_GetPowerModeState API is visible on multiple platforms, and may be confusing because it is not implemented on all platforms. This functionality doesn't exist or may not be applicable for all platforms. To be checked: 1. If there is any requirement for this API and where is the requirement applied to. 2. What is the scope of this API, if the description in the driver code is correct, and to what platforms this applies. 3. If the API can be included by using an M4 macro with parameter defined in resource or makefile. If not, to be checked whether this API can be disabled in configuration, not allowing the user to activate it. A note to be added in this case to the Tresos/DS field, to explain why the field is disabled. 4. If a note in the UM/IM may be useful or not. See attached email thread for more information.
ARTD-25553	Bug	[I2S] Build fail multi-core when use VariantPreCompile Detailed description (how to reproduce it): Build a multi-core test with Precompile mode Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: I2s_TC_FCT_9000 Observed behavior: Build fail with log: !image-2022-03-28-17-49-09-674.png! Expected behavior: Build pass Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]

ID	Subtype	Headline and Description
ARTD-25591	Bug	[MCU] Get frequency of FIRC_CLK is wrong Detailed description (how to reproduce it): Get frequency of FIRC_CLK is wrong when McuFircDivSel is different Div_by_1 in the fist clock config Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: Get frequency of FIRC_CLK is correct Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update code in Clock_Ip_Cfg_Defines.h in EBT and CT: #define CLOCK_IP_FIRC_FREQUENCY ([!"(num:i(McuModuleConfiguration/McuClockSettingConfig/*[1]/McuFIRC/McuFIRC_Frequency))"!]U) to #define CLOCK_IP_FIRC_FREQUENCY 48000000U
ARTD-25719	Bug	[PORT] Memory section is not closed in Port_Ipw.c Detailed description (how to reproduce it): In the file Port_Ipw.c, a memory section (PORT_START_SEC_CODE) is opened in line 167, but it is not closed at the end. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: In the file Port_Ipw.c, a memory section (PORT_START_SEC_CODE) is opened in line 167, but it is not closed at the end. Expected behavior: Add PORT_STOP_SEC_CODE to close the code section. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-25732	New Feature	[adc] Rename Base to BaseNXP in EBT and OsIf to BaseNXP in S32CT NewWorkDescription: Actions that need to be taken: All schema files have to be updated (.xdm, .component) Effort mitigated by attached script Testing makefiles (with dependency on Base) have to be updated (in theory, only in common.mak) Effort mitigated by attached script All test configuration files for Base have to be updated: For XDM configuration files Effort mitigated by attached script For MEX configuration files Manually performed (the script can't help here since the structure of OsIf has been drastically changed in S32CT to match the one from EBT) Have to update input.json files if they are referencing Base Effort mitigated by attached script Requirement source: EB Request (refer to linked tickets) (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Copy the attached script in the root directory of your driver's repository and execute it from there in Cygwin (./RenameBase.sh) Re-configure OsIf in the MEX configuration files. Regenerate examples to check that everything is working fine again.

ID	Subtype	Headline and Description
ARTD-25733	New Feature	[build_env] Rename Base to BaseNXP in EBT and OsIf to BaseNXP in S32CT NewWorkDescription: Actions that need to be taken: All schema files have to be updated (.xdm, .component) Effort mitigated by attached script Testing makefiles (with dependency on Base) have to be updated (in theory, only in common.mak) Effort mitigated by attached script All test configuration files for Base have to be updated: For XDM configuration files Effort mitigated by attached script For MEX configuration files Manually performed (the script can't help here since the structure of OsIf has been drastically changed in S32CT to match the one from EBT) Have to update input.json files if they are referencing Base Effort mitigated by attached script Requirement source: EB Request (refer to linked tickets) (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Copy the attached script in the root directory of your driver's repository and execute it from there in Cygwin (./RenameBase.sh) Re-configure OsIf in the MEX configuration files. Regenerate examples to check that everything is working fine again.
ARTD-25734	New Feature	[can] Rename Base to BaseNXP in EBT and OsIf to BaseNXP in S32CT NewWorkDescription: Actions that need to be taken: All schema files have to be updated (.xdm, .component) Effort mitigated by attached script Testing makefiles (with dependency on Base) have to be updated (in theory, only in common.mak) Effort mitigated by attached script All test configuration files for Base have to be updated: For XDM configuration files Effort mitigated by attached script For MEX configuration files Manually performed (the script can't help here since the structure of OsIf has been drastically changed in S32CT to match the one from EBT) Have to update input.json files if they are referencing Base Effort mitigated by attached script Requirement source: EB Request (refer to linked tickets) (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Copy the attached script in the root directory of your driver's repository and execute it from there in Cygwin (./RenameBase.sh) Re-configure OsIf in the MEX configuration files. Regenerate examples to check that everything is working fine again.
ARTD-25735	New Feature	[crc] Rename Base to BaseNXP in EBT and OsIf to BaseNXP in S32CT NewWorkDescription: Actions that need to be taken: All schema files have to be updated (.xdm, .component) Effort mitigated by attached script Testing makefiles (with dependency on Base) have to be updated (in theory, only in common.mak) Effort mitigated by attached script All test configuration files for Base have to be updated: For XDM configuration files Effort mitigated by attached script For MEX configuration files Manually performed (the script can't help here since the structure of OsIf has been drastically changed in S32CT to match the one from EBT) Have to update input.json files if they are referencing Base Effort mitigated by attached script Requirement source: EB Request (refer to linked tickets) (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Copy the attached script in the root directory of your driver's repository and execute it from there in Cygwin (./RenameBase.sh) Re-configure OsIf in the MEX configuration files. Regenerate examples to check that everything is working fine again.
ARTD-25736	New Feature	[crypto] Rename Base to BaseNXP in EBT and OsIf to BaseNXP in S32CT NewWorkDescription: Actions that need to be taken: All schema files have to be updated (.xdm, .component) Effort mitigated by attached script Testing makefiles (with dependency on Base) have to be updated (in theory, only in common.mak) Effort mitigated by attached script All test configuration files for Base have to be updated: For XDM configuration files Effort mitigated by attached script For MEX configuration files Manually performed (the script can't help here since the structure of OsIf has been drastically changed in S32CT to match the one from EBT) Have to update input.json files if they are referencing Base Effort mitigated by attached script Requirement source: EB Request (refer to linked tickets) (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Copy the attached script in the root directory of your driver's repository and execute it from there in Cygwin (./RenameBase.sh) Re-configure OsIf in the MEX configuration files. Regenerate examples to check that everything is working fine again.

ID	Subtype	Headline and Description
ARTD-25741	New Feature	[dio] Rename Base to BaseNXP in EBT and OsIf to BaseNXP in S32CT NewWorkDescription: Actions that need to be taken: All schema files have to be updated (.xdm, .component) Effort mitigated by attached script Testing makefiles (with dependency on Base) have to be updated (in theory, only in common.mak) Effort mitigated by attached script All test configuration files for Base have to be updated: For XDM configuration files Effort mitigated by attached script For MEX configuration files Manually performed (the script can't help here since the structure of OsIf has been drastically changed in S32CT to match the one from EBT) Have to update input.json files if they are referencing Base Effort mitigated by attached script Requirement source: EB Request (refer to linked tickets) (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Copy the attached script in the root directory of your driver's repository and execute it from there in Cygwin (./RenameBase.sh) Re-configure OsIf in the MEX configuration files. Regenerate examples to check that everything is working fine again.
ARTD-25745	New Feature	[eth] Rename Base to BaseNXP in EBT and OsIf to BaseNXP in S32CT NewWorkDescription: Actions that need to be taken: All schema files have to be updated (.xdm, .component) Effort mitigated by attached script Testing makefiles (with dependency on Base) have to be updated (in theory, only in common.mak) Effort mitigated by attached script All test configuration files for Base have to be updated: For XDM configuration files Effort mitigated by attached script For MEX configuration files Manually performed (the script can't help here since the structure of OsIf has been drastically changed in S32CT to match the one from EBT) Have to update input.json files if they are referencing Base Effort mitigated by attached script Requirement source: EB Request (refer to linked tickets) (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Copy the attached script in the root directory of your driver's repository and execute it from there in Cygwin (./RenameBase.sh) Re-configure OsIf in the MEX configuration files. Regenerate examples to check that everything is working fine again.
ARTD-25750	New Feature	[gpt] Rename Base to BaseNXP in EBT and OsIf to BaseNXP in S32CT NewWorkDescription: Actions that need to be taken: All schema files have to be updated (.xdm, .component) Effort mitigated by attached script Testing makefiles (with dependency on Base) have to be updated (in theory, only in common.mak) Effort mitigated by attached script All test configuration files for Base have to be updated: For XDM configuration files Effort mitigated by attached script For MEX configuration files Manually performed (the script can't help here since the structure of OsIf has been drastically changed in S32CT to match the one from EBT) Have to update input.json files if they are referencing Base Effort mitigated by attached script Requirement source: EB Request (refer to linked tickets) (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Copy the attached script in the root directory of your driver's repository and execute it from there in Cygwin (./RenameBase.sh) Re-configure OsIf in the MEX configuration files. Regenerate examples to check that everything is working fine again.
ARTD-25751	New Feature	[i2c] Rename Base to BaseNXP in EBT and OsIf to BaseNXP in S32CT NewWorkDescription: Actions that need to be taken: All schema files have to be updated (.xdm, .component) Effort mitigated by attached script Testing makefiles (with dependency on Base) have to be updated (in theory, only in common.mak) Effort mitigated by attached script All test configuration files for Base have to be updated: For XDM configuration files Effort mitigated by attached script For MEX configuration files Manually performed (the script can't help here since the structure of OsIf has been drastically changed in S32CT to match the one from EBT) Have to update input.json files if they are referencing Base Effort mitigated by attached script Requirement source: EB Request (refer to linked tickets) (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Copy the attached script in the root directory of your driver's repository and execute it from there in Cygwin (./RenameBase.sh) Re-configure OsIf in the MEX configuration files. Regenerate examples to check that everything is working fine again.

ID	Subtype	Headline and Description
ARTD-25752	New Feature	[i2s] Rename Base to BaseNXP in EBT and OsIf to BaseNXP in S32CT NewWorkDescription: Actions that need to be taken: All schema files have to be updated (.xdm, .component) Effort mitigated by attached script Testing makefiles (with dependency on Base) have to be updated (in theory, only in common.mak) Effort mitigated by attached script All test configuration files for Base have to be updated: For XDM configuration files Effort mitigated by attached script For MEX configuration files Manually performed (the script can't help here since the structure of OsIf has been drastically changed in S32CT to match the one from EBT) Have to update input.json files if they are referencing Base Effort mitigated by attached script Requirement source: EB Request (refer to linked tickets) (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Copy the attached script in the root directory of your driver's repository and execute it from there in Cygwin (./RenameBase.sh) Re-configure OsIf in the MEX configuration files. Regenerate examples to check that everything is working fine again.
ARTD-25755	New Feature	[lin] Rename Base to BaseNXP in EBT and OsIf to BaseNXP in S32CT NewWorkDescription: Actions that need to be taken: All schema files have to be updated (.xdm, .component) Effort mitigated by attached script Testing makefiles (with dependency on Base) have to be updated (in theory, only in common.mak) Effort mitigated by attached script All test configuration files for Base have to be updated: For XDM configuration files Effort mitigated by attached script For MEX configuration files Manually performed (the script can't help here since the structure of OsIf has been drastically changed in S32CT to match the one from EBT) Have to update input.json files if they are referencing Base Effort mitigated by attached script Requirement source: EB Request (refer to linked tickets) (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Copy the attached script in the root directory of your driver's repository and execute it from there in Cygwin (./RenameBase.sh) Re-configure OsIf in the MEX configuration files. Regenerate examples to check that everything is working fine again.
ARTD-25756	New Feature	[mcl] Rename Base to BaseNXP in EBT and OsIf to BaseNXP in S32CT NewWorkDescription: Actions that need to be taken: All schema files have to be updated (.xdm, .component) Effort mitigated by attached script Testing makefiles (with dependency on Base) have to be updated (in theory, only in common.mak) Effort mitigated by attached script All test configuration files for Base have to be updated: For XDM configuration files Effort mitigated by attached script For MEX configuration files Manually performed (the script can't help here since the structure of OsIf has been drastically changed in S32CT to match the one from EBT) Have to update input.json files if they are referencing Base Effort mitigated by attached script Requirement source: EB Request (refer to linked tickets) (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Copy the attached script in the root directory of your driver's repository and execute it from there in Cygwin (./RenameBase.sh) Re-configure OsIf in the MEX configuration files. Regenerate examples to check that everything is working fine again.
ARTD-25757	New Feature	[mcu] Rename Base to BaseNXP in EBT and OsIf to BaseNXP in S32CT NewWorkDescription: Actions that need to be taken: All schema files have to be updated (.xdm, .component) Effort mitigated by attached script Testing makefiles (with dependency on Base) have to be updated (in theory, only in common.mak) Effort mitigated by attached script All test configuration files for Base have to be updated: For XDM configuration files Effort mitigated by attached script For MEX configuration files Manually performed (the script can't help here since the structure of OsIf has been drastically changed in S32CT to match the one from EBT) Have to update input.json files if they are referencing Base Effort mitigated by attached script Requirement source: EB Request (refer to linked tickets) (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Copy the attached script in the root directory of your driver's repository and execute it from there in Cygwin (./RenameBase.sh) Re-configure OsIf in the MEX configuration files. Regenerate examples to check that everything is working fine again.

ID	Subtype	Headline and Description
ARTD-25763	New Feature	[port] Rename Base to BaseNXP in EBT and OsIf to BaseNXP in S32CT NewWorkDescription: Actions that need to be taken: All schema files have to be updated (.xdm, .component) Effort mitigated by attached script Testing makefiles (with dependency on Base) have to be updated (in theory, only in common.mak) Effort mitigated by attached script All test configuration files for Base have to be updated: For XDM configuration files Effort mitigated by attached script For MEX configuration files Manually performed (the script can't help here since the structure of OsIf has been drastically changed in S32CT to match the one from EBT) Have to update input.json files if they are referencing Base Effort mitigated by attached script Requirement source: EB Request (refer to linked tickets) (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Copy the attached script in the root directory of your driver's repository and execute it from there in Cygwin (./RenameBase.sh) Re-configure OsIf in the MEX configuration files. Regenerate examples to check that everything is working fine again.
ARTD-25765	New Feature	[pwm] Rename Base to BaseNXP in EBT and OsIf to BaseNXP in S32CT NewWorkDescription: Actions that need to be taken: All schema files have to be updated (.xdm, .component) Effort mitigated by attached script Testing makefiles (with dependency on Base) have to be updated (in theory, only in common.mak) Effort mitigated by attached script All test configuration files for Base have to be updated: For XDM configuration files Effort mitigated by attached script For MEX configuration files Manually performed (the script can't help here since the structure of OsIf has been drastically changed in S32CT to match the one from EBT) Have to update input.json files if they are referencing Base Effort mitigated by attached script Requirement source: EB Request (refer to linked tickets) (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Copy the attached script in the root directory of your driver's repository and execute it from there in Cygwin (./RenameBase.sh) Re-configure OsIf in the MEX configuration files. Regenerate examples to check that everything is working fine again.
ARTD-25767	New Feature	[rm] Rename Base to BaseNXP in EBT and OsIf to BaseNXP in S32CT NewWorkDescription: Actions that need to be taken: All schema files have to be updated (.xdm, .component) Effort mitigated by attached script Testing makefiles (with dependency on Base) have to be updated (in theory, only in common.mak) Effort mitigated by attached script All test configuration files for Base have to be updated: For XDM configuration files Effort mitigated by attached script For MEX configuration files Manually performed (the script can't help here since the structure of OsIf has been drastically changed in S32CT to match the one from EBT) Have to update input.json files if they are referencing Base Effort mitigated by attached script Requirement source: EB Request (refer to linked tickets) (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Copy the attached script in the root directory of your driver's repository and execute it from there in Cygwin (./RenameBase.sh) Re-configure OsIf in the MEX configuration files. Regenerate examples to check that everything is working fine again.
ARTD-25768	New Feature	[sent] Rename Base to BaseNXP in EBT and OsIf to BaseNXP in S32CT NewWorkDescription: Actions that need to be taken: All schema files have to be updated (.xdm, .component) Effort mitigated by attached script Testing makefiles (with dependency on Base) have to be updated (in theory, only in common.mak) Effort mitigated by attached script All test configuration files for Base have to be updated: For XDM configuration files Effort mitigated by attached script For MEX configuration files Manually performed (the script can't help here since the structure of OsIf has been drastically changed in S32CT to match the one from EBT) Have to update input.json files if they are referencing Base Effort mitigated by attached script Requirement source: EB Request (refer to linked tickets) (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Copy the attached script in the root directory of your driver's repository and execute it from there in Cygwin (./RenameBase.sh) Re-configure OsIf in the MEX configuration files. Regenerate examples to check that everything is working fine again.

ID	Subtype	Headline and Description
ARTD-25859	New Feature	[GPT]: The value of macro: RTC_IP_TICKS_PER_SECOND is 0, and it will cause error Detailed description (how to reproduce it): The macro's (RTC_IP_TICKS_PER_SECOND) value is 0 regardless of whether we have configured the RTC or not. but this macro is used in code and is used as the denominator of a division operation, then it will cause an error. !image-2022-04-12-16-19-59-153.png! !image-2022-04-12-16-20-23-156.png! !image-2022-04-12-16-20-46-050.png! !image-2022-04-12-16-21-08-737.png! Preconditions: None Test Case ID (internal TC that caught the defect) optional: None Observed behavior: system crash Expected behavior: the macro (RTC_IP_TICKS_PER_SECOND) value should not be 0 when we configured RTC in GPT module. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: None
ARTD-25873	New Feature	[eth] Rename OsIf to BaseNXP in S32CT NewWorkDescription: Actions that need to be taken: All schema files have to be updated (.xdm, .component) Effort mitigated by attached script Testing makefiles (with dependency on Base) have to be updated (in theory, only in common.mak) Effort mitigated by attached script All test configuration files for Base have to be updated: For XDM configuration files Effort mitigated by attached script For MEX configuration files Manually performed (the script can't help here since the structure of OsIf has been drastically changed in S32CT to match the one from EBT) Have to update input.json files if they are referencing Base Effort mitigated by attached script Requirement source: EB Request (refer to linked tickets) (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Copy the attached script in the root directory of your driver's repository and execute it from there in Cygwin (./RenameBase.sh) Re-configure OsIf in the MEX configuration files. Regenerate examples to check that everything is working fine again.
ARTD-25882	Bug	[FLS] Write data error when the data size will go over the sector boundary Detailed description (how to reproduce it): when writing data on a sector in asynchronous mode and if this data length causes spanning, it will causes errors. After code analyze, this is a bug which the low level driver process a wrong sector index when the write data need to cross sectors. And this issue exist in both K1 and K3 RTD. Preconditions: write data in async mode, and the write data size will across the sector edge. Test Case ID (internal TC that caught the defect) optional: None Observed behavior: write data error Expected behavior: Write data normally Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: add the index variable when the case happened in the low level driver, can refer to the MCAL code.

ID	Subtype	Headline and Description
ARTD-25893	New Feature	[RM] Move MPU IP to Platform NewWorkDescription: According to the SOW, it was decided to move the Mpu Ip (Mpu_M7, Mpu_M33, Smpu) from RM to Platform https://nxp1.sharepoint.com/:w:/r/sites/Zebra/_layouts/15/Doc.aspx?sourcedoc= %7B7CCDA70E-A524-4353-B765-555A665E295B%7D&file=S32%20RTD%20for%20S32ZSE %200.8.0%20SOW.docx&action=default&mobileredirect=true&cid=8bdb9bbc-3ec2-498a-8a2b-70a6c7b42b23 Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Move Mpu_Ip (Mpu_M7, Mpu_M33, Smpu) code, configuration and requirements from Rm to Platform
ARTD-25914	New Feature	[base] Rename Base to BaseNXP in EBT and OsIf to BaseNXP in S32CT NewWorkDescription: Actions that need to be taken: All schema files have to be updated (.xdm, .component) Effort mitigated by attached script Testing makefiles (with dependency on Base) have to be updated (in theory, only in common.mak) Effort mitigated by attached script All test configuration files for Base have to be updated: For XDM configuration files Effort mitigated by attached script For MEX configuration files Manually performed (the script can't help here since the structure of OsIf has been drastically changed in S32CT to match the one from EBT) Have to update input.json files if they are referencing Base Effort mitigated by attached script Requirement source: EB Request (refer to linked tickets) (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Copy the attached script in the root directory of your driver's repository and execute it from there in Cygwin (./RenameBase.sh) Re-configure OsIf in the MEX configuration files. Regenerate examples to check that everything is working fine again.
ARTD-25940	New Feature	[RM] Move MPU Requirements to Platform NewWorkDescription: Move Mpu, Mpu_M7 and Smpu IP requirements from RM to Platform. Remove Mpu HLD requirements from RM Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Move Mpu, Mpu_M7 and Smpu IP requirements from RM to Platform. Remove Mpu HLD requirements from RM
ARTD-25946	Bug	[FEE] Warnings of zero-initialized variables with complier IAR Detailed description (how to reproduce it): When building Fee driver with IAR compiler, there are some warnings appear, because of zero-initialized variables still have explicit zero-initializers Root cause: there was an incorrect fixing for{color}{color:#172b4d} compiler warning, it did not follow the rule of zero-initialized variables in "CLEARED" memory sections [https://bitbucket.sw.nxp.com/projects/ARTD/repos/fee/pull-requests/117/diff#generic/src/Fee.c] Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: There are compiler warning on IAR Expected behavior: There are no warnings Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Remove all explicit zero-initializers in the "CLEARED" memory sections. Following the guidline in the ticket: https://jira.sw.nxp.com/browse/ARTD-12239

ID	Subtype	Headline and Description
ARTD-25966	Bug	[MCU]Boot mode can't be normal in special case. Detailed description (how to reproduce it): Boot Mode can't be Normal Mode because the register DCMRWF5 still keep value different 0 at the field BOOT_MODE. This caused by SOC_PREPARE_FAST_STANDBY called before SOC_PREPARE_STANDBY called. Preconditions: SOC_PREPARE_FAST_STANDBY called before SOC_PREPARE_STANDBY called. Test Case ID (internal TC that caught the defect) optional: Mcu_Example_Low_Power_Cycling_S32K344 Observed behavior: DCMRWF5 still keep value of fast standby instead of value reset. Expected behavior: DCMRWF5 need be 0 in Normal standby. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: If BootMode is Normal, need to reset value of register IP_DCM_GPR->DCMRWF5
ARTD-25997	Bug	[CAN] fail to check constraint for CAN_1 when enabled multicore / S32CT Detailed description (how to reproduce it): A> Create S32Z project / s32ct Enable multicores Add CAN_0, then fix constraints Add CAN_1, => expectation: constraint log instead of anonymous code-generate error B> Add EcucPartition_0 to CanEcucPartitionRef CAN_0 refer to EcucPartition_One (instead of EcucPartition_0) => contraint log should be displayed C> Missing constraint for checking mcl channel and dma_callback_name. Please add constraint for this as in EB. For 24 instances this is necessary feature Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: A> !image-2022-04-19-18-21-47-015.png|thumbnail! [...] B> No contraint log was displayed Expected behavior: A> constraint log instead of anonymous code-generate error B> contraint log should be displayed Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A

ID	Subtype	Headline and Description
ARTD-26056	Bug	[can] constraint for dma channel check should be support / IpFlexCAN Detailed description (how to reproduce it): Create s32z project / IPL layer Add Flexcan_0 and enable dma Add Flexcan_1 and enable dma By default the values of dma channel is the same as 0 value => no error indicate when all controllers have same dma_channel value Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: !image-2022-04-22-11-25-00-962.png|thumbnail! Expected behavior: for fields that need distinct value, constraint should be implemented. For example as the implementation for "FlexCan Configuration Name" Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-26084	Bug	[Port]: the memory section don't match the variable type, it will cause the compile result abnormal when compile with IAR Detailed description (how to reproduce it): when I compiling the code with IAR, the binary file include a block which the address belongs to RAM area. it will cause download failed. after analysis the code, it caused by the code in Port.c. After I remove the initial value which showed in the picture, the compile result will not show the block 3. !image-2022-04-26-14-29-44-797.png! !image-2022-04-26-14-30-48-463.png! Preconditions: compile with IAR Test Case ID (internal TC that caught the defect) optional: None Observed behavior: the compile binary file abnormal Expected behavior: without data which belongs to RAM areas Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: optimize the initialization value or change the section

ID	Subtype	Headline and Description
ARTD-26188	New Feature	[i2c] CPR_RTD_00028 is replaced by CPR_RTD_00664 NewWorkDescription: Requirement CPR_RTD_00028 is rejected and replaced by CPR_RTD_00664: "ISR shall check whether its respective interrupt status flag and interrupt enable flag are set; i.e. whether the interrupt is not spurious. If at least one of the flags is not set, then the interrupt is spurious and the ISR shall not treat the event (return immediately). Rationale: A spurious interrupt is considered when there is a glitch in the hardware mechanisms that trigger the CPU exception. Drivers must ensure only relevant events are treated and spurious ones are discarded." Check and update (if needed) the driver implementation to be according to CPR_RTD_00664. Update FMEA and include also Adrian Herea (Safety Manager) to the review. Requirement source: cPRT {*}Proposed solution{*}: The rationale behind the update is to not consider as spurious the events that may otherwise be treated in a different context (e.g. polling mode) and for which the interrupt enable bit is not set. For interrupt lines shared by multiple events, it should be possible for some of the events to be treated by the ISR, while other to be left uncleared so that they can be treated in the thread (as long as they have the interrupt enabled bit cleared, meaning the interrupt is disabled). The update required here would be to only clear the flags for the events that are enabled and leave the others untouched, as long as they are managed by the driver in a different context. The consequence of that would be to allow multiple events that have separate interrupt enable bits but share a single interrupt line to function both in "interrupt" and "polling" modes simultaneously. Hence, the clearing of the flag should only happen if the condition "(interrupt_enable && interrupt_flag)" is true, otherwise it is assumed that the flag is handled outside the ISR. The rationale applies only for drivers that handle hardware resources that share interrupt lines, but the correct implementation of the ISR logic should be checked for all drivers.
ARTD-26190	New Feature	[i2s] CPR_RTD_00028 is replaced by CPR_RTD_00664 NewWorkDescription: Requirement CPR_RTD_00028 is rejected and replaced by CPR_RTD_00664: "ISR shall check whether its respective interrupt status flag and interrupt enable flag are set; i.e. whether the interrupt is not spurious. If at least one of the flags is not set, then the interrupt is spurious and the ISR shall not treat the event (return immediately). Rationale: A spurious interrupt is considered when there is a glitch in the hardware mechanisms that trigger the CPU exception. Drivers must ensure only relevant events are treated and spurious ones are discarded." Check and update (if needed) the driver implementation to be according to CPR_RTD_00664. Update FMEA and include also Adrian Herea (Safety Manager) to the review. Requirement source: cPRT {*}Proposed solution{*}: The rationale behind the update is to not consider as spurious the events that may otherwise be treated in a different context (e.g. polling mode) and for which the interrupt enable bit is not set. For interrupt lines shared by multiple events, it should be possible for some of the events to be treated by the ISR, while other to be left uncleared so that they can be treated in the thread (as long as they have the interrupt enabled bit cleared, meaning the interrupt is disabled). The update required here would be to only clear the flags for the events that are enabled and leave the others untouched, as long as they are managed by the driver in a different context. The consequence of that would be to allow multiple events that have separate interrupt enable bits but share a single interrupt line to function both in "interrupt" and "polling" modes simultaneously. Hence, the clearing of the flag should only happen if the condition "(interrupt_enable && interrupt_flag)" is true, otherwise it is assumed that the flag is handled outside the ISR. The rationale applies only for drivers that handle hardware resources that share interrupt lines, but the correct implementation of the ISR logic should be checked for all drivers.

ID	Subtype	Headline and Description

ARTD-26206	New Feature	S32K3xx, RTD LPSPI Async Transmit
		
		I have modified the LPSPI_Ip_HalfDuplexTransfer_S32K344 example to have Async transfer from the Master.
		
		/ Master transmits data in half-duplex mode by sync method /
		//Lpspi_Ip_SyncTransmitHalfDuplex(&MASTER_EXTERNAL_DEVICE, TxMasterBuffer, NUMBER_OF_BYTES, LPSPI_IP_HALF_DUPLEX_TRANSMIT, TIMEOUT);
		Lpspi_Ip_AsyncTransmitHalfDuplex(&MASTER_EXTERNAL_DEVICE, TxMasterBuffer, NUMBER_OF_BYTES, LPSPI_IP_HALF_DUPLEX_TRANSMIT, NULL_PTR);
		
		do
		{
		status_master = Lpspi_Ip_GetStatus(MASTER_EXTERNAL_DEVICE.Instance);
		}
		while(status_master != LPSPI_IP_IDLE);
		
		While the transmit function returns SUCCESS, the GetStatus function keeps returning LPSPI_IP_BUSY, and I don’t see anything on the bus (clock is idle).

ARTD-26199	New Feature	[gpt] CPR_RTD_00028 is replaced by CPR_RTD_00664 NewWorkDescription: Requirement CPR_RTD_00028 is rejected and replaced by CPR_RTD_00664: "ISR shall check whether its respective interrupt status flag and interrupt enable flag are set; i.e. whether the interrupt is not spurious. If at least one of the flags is not set, then the interrupt is spurious and the ISR shall not treat the event (return immediately). Rationale: A spurious interrupt is considered when there is a glitch in the hardware mechanisms that trigger the CPU exception. Drivers must ensure only relevant events are treated and spurious ones are discarded." Check and update (if needed) the driver implementation to be according to CPR_RTD_00664. Update FMEA and include also Adrian Herea (Safety Manager) to the review. Requirement source: cPRT {*}Proposed solution{*}: The rationale behind the update is to not consider as spurious the events that may otherwise be treated in a different context (e.g. polling mode) and for which the interrupt enable bit is not set. For interrupt lines shared by multiple events, it should be possible for some of the events to be treated by the ISR, while other to be left uncleared so that they can be treated in the thread (as long as they have the interrupt enabled bit cleared, meaning the interrupt is disabled). The update required here would be to only clear the flags for the events that are enabled and leave the others untouched, as long as they are managed by the driver in a different context. The consequence of that would be to allow multiple events that have separate interrupt enable bits but share a single interrupt line to function both in "interrupt" and "polling" modes simultaneously. Hence, the clearing of the flag should only happen if the condition "(interrupt_enable && interrupt_flag)" is true, otherwise it is assumed that the flag is handled outside the ISR. The rationale applies only for drivers that handle hardware resources that share interrupt lines, but the correct implementation of the ISR logic should be checked for all drivers.
ARTD-26239	New Feature	[ETH][GMAC][ENET] - Add External Buffers transmission in HLD NewWorkDescription: Define a methodology to use the External Buffers Management in HLD. Define a configuration checkbox in order to configure External/Internal buffers management. Define an HLD API Eth_SendFrame which must perform a transmission using the frame buffer as a parameter. This API must be available only when External Buffers feature is in use. The new API for transmit in HLD will have parameters for controller index, priority, pointer to start of frame (not payload), length of the whole frame (not just payload) and transmit confirmation (TBD) Test the feature using multiple packets.
ARTD-26253	Bug	[LIN-S32ZSE] Can't generate code - undefine variable "LinMasterNodeUsed" in EB tresos Detailed description (how to reproduce it): when generate code be used SLAVE node for module LIN. In EB tresos variable "LinMasterNodeUsed " undefine in file Lin_Defines !image-2022-05-05-11-20-17-475.png! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional Lin_TC_FCT_0215,Lin_TC_FCT_0216,Lin_TC_FCT_0217,Lin_TC_FCT_0218,Lin_TC_FCT_0219 Observed behavior: N/A Expected behavior: define variable "LinMasterNodeUsed " Proposed solution optional: N/A

ID	Subtype	Headline and Description
ARTD-26271	Bug	Spi_SetupEB should follow AUTOSAR spec Detailed description (how to reproduce it): In current spi driver, the API is Std_ReturnType Spi_SetupEB (Spi_ChannelType Channel, Spi_DataBufferType SrcDataBufferPtr, Spi_DataBufferType DesDataBufferPtr, Spi_NumberOfDataType Length); Spi_DataBufferType SrcDataBufferPtr should be const Spi_DataBufferType SrcDataBufferPtr to follow AUTOSAR spec !image-2022-05-05-17-18-49-897.png|width=504,height=239! Preconditions: None Test Case ID (internal TC that caught the defect) optional: None Observed behavior: wrong API prototype Expected behavior: correct API prototype Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]

ID	Subtype	Headline and Description
ARTD-26299	New Feature	[dio] Add support for multiple configurations in S32CT NewWorkDescription: Previously, we limited the number of functional groups (multiple configurations) to 1. Now we want to add support for multiple configurations (in the form of post-build variants and classic functional groups) so that we can also replicate in S32CT the module configurations from EB Tresos in which there are two or more post-build variants. Requirement source: SRS_BSW_00405 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Read the newly introduced section ("13. Multiple Configurations") in the following presentation: [NXP_RTD_AUTOSAR_S32CT_V2|https://nxp1.sharepoint.com/:p:/r/sites/Zebra/Shared%20Documents/Configuration%20(code,%20DS,%20EB,%20etc)/NXP_RTD_AUTOSAR_S32CT_V2.pptx?d=w28a51ba3c45240f5abb6a6933671dcd3&csf=1&web=1&e=r7YbFB] Make sure you have added the SYNC_VALUE and SYNC_SIZE options to each component setting that requires it (as suggested in the presentation, you can use [epdimp2ct|https://nxp1.sharepoint.com/:f:/s/Zebra/EprWldG7fTNPgdoXtWTgmIsBn1Xo56J_qJQGC37m92ax9A?e=ivi58c] to automate this task as long as you have a matching EPD for your component) Apply the changes shown in the source code references. The main points are: {noformat} [!IF "var:defined('postBuildVariant')"!]{noformat} translates to {noformat} if (useFgInfix()){noformat} The file names and configuration structures should not contain the variant infix when there's no selected post-build variant (actually, most of the changes you'll see in the references are done just to support this use-case) Sanity Check: Check that your driver can be successfully built in all three scenarios: ## ComponentGenerationMethod = EcucPostBuildVariants and VARIANT_NO = 0 ## ComponentGenerationMethod = EcucPostBuildVariants and VARIANT_NO > 1 (VARIANT_NO == 1 is the base case from which you started) ## ComponentGenerationMethod = FunctionalGroups (with at least 2 FGs configured in the project) Extensive Testing: By default, EB Tresos cannot generate variant aware EPC files without throwing a null pointer exception. To get around this limitation, the dreisoft.tresos.autosar2 plugin must be patched. To do this, download one of the two attached archives, depending on your EBT version, and extract it in <ebt_root_dir>/plugins. # Go to your driver's plugin, open {_}plugin.xml{_}, search for {_}id="EPCGenerator"{_}, and set the value of parameter "allVariants" to {_}"true"{_}. This will enable variant aware EPC file generation for your module. # Create a configuration with at least two post-build variants. The project will need EcuC for post-build variants to be enabled. The configuration should ideally use different values for nodes with postBuildVariantValue=TRUE and different list elements for nodes with postBuildVariantMultiplicity=TRUE. This will ensure that errors in variant handling can be easily caught later on while doing the diffs. # Generate the EPC files by right clicking on your project's configuration and select "Generate Project". If the 1st step has been carried out correctly, there will be a "PostBuildSelectableVariants.arxml" file in <project_root_dir>/output/output and your module's EPC file, lying inside the same directory, will contain lots of "VARIATION-POINT" elements. # Open S32DS and select File > Import > S32 Configuration Tools > Import ECU Configuration. Browse to the location where your EPC files are located within the EBT project and select at least your module's EPC file, EcuC's EPC file and PostBuildSelectableVariants.arxml. Check the "Import the configuration as a new one" radio button and select the processor / package / sdk version accordingly. # Go to the "Global settings" panel and make sure that ComponentGenerationMethod=EcucPostBuildVariants in the System component. # Select "Update Code" to generate your S32DS project files. Perform a comparison/diff of the generated files between S32DS and EBT. These files should be pretty much identical (sans whitespace or formatting) # Go to the "Global settings" panel again to generate the ECVD files (EcvdGenerationMethod=INDIVIDUAL, browse a location for EcvdOutputPath and click on the Generate Configuration button). Compare/diff your module's EPC file with your module's ECVD file. These files should be pretty much identical (sans whitespace or formatting) # The above steps tested the EBT->S32DS compatibility. To also test the S32DS->EBT compatibility, do the above steps in reverse. That is, start from an S32DS project with post-build variants, generate the ECVD files, import them into EBT, compare again the generated files and the configuration files.

ID	Subtype	Headline and Description
ARTD-26310	New Feature	[i2s] Add support for multiple configurations in S32CT NewWorkDescription: Previously, we limited the number of functional groups (multiple configurations) to 1. Now we want to add support for multiple configurations (in the form of post-build variants and classic functional groups) so that we can also replicate in S32CT the module configurations from EB Tresos in which there are two or more post-build variants. Requirement source: SRS_BSW_00405 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Read the newly introduced section ("13. Multiple Configurations") in the following presentation: [NXP_RTD_AUTOSAR_S32CT_V2|https://nxp1.sharepoint.com/:p:/r/sites/Zebra/Shared%20Documents/Configuration%20(code,%20DS,%20EB,%20etc)/NXP_RTD_AUTOSAR_S32CT_V2.pptx?d=w28a51ba3c45240f5abb6a6933671dcd3&csf=1&web=1&e=r7YbFB] Make sure you have added the SYNC_VALUE and SYNC_SIZE options to each component setting that requires it (as suggested in the presentation, you can use [epdimp2ct|https://nxp1.sharepoint.com/:f:/s/Zebra/EprWldG7fTNPgdoXtWTgmIsBn1Xo56J_qJQGC37m92ax9A?e=ivi58c] to automate this task as long as you have a matching EPD for your component) Apply the changes shown in the source code references. The main points are: {noformat} [!IF "var:defined('postBuildVariant')"!]{noformat} translates to {noformat} if (useFgInfix()){noformat} The file names and configuration structures should not contain the variant infix when there's no selected post-build variant (actually, most of the changes you'll see in the references are done just to support this use-case) Sanity Check: Check that your driver can be successfully built in all three scenarios: ## ComponentGenerationMethod = EcucPostBuildVariants and VARIANT_NO = 0 ## ComponentGenerationMethod = EcucPostBuildVariants and VARIANT_NO > 1 (VARIANT_NO == 1 is the base case from which you started) ## ComponentGenerationMethod = FunctionalGroups (with at least 2 FGs configured in the project) Extensive Testing: By default, EB Tresos cannot generate variant aware EPC files without throwing a null pointer exception. To get around this limitation, the dreisoft.tresos.autosar2 plugin must be patched. To do this, download one of the two attached archives, depending on your EBT version, and extract it in <ebt_root_dir>/plugins. # Go to your driver's plugin, open {_}plugin.xml{_}, search for {_}id="EPCGenerator"{_}, and set the value of parameter "allVariants" to {_}"true"{_}. This will enable variant aware EPC file generation for your module. # Create a configuration with at least two post-build variants. The project will need EcuC for post-build variants to be enabled. The configuration should ideally use different values for nodes with postBuildVariantValue=TRUE and different list elements for nodes with postBuildVariantMultiplicity=TRUE. This will ensure that errors in variant handling can be easily caught later on while doing the diffs. # Generate the EPC files by right clicking on your project's configuration and select "Generate Project". If the 1st step has been carried out correctly, there will be a "PostBuildSelectableVariants.arxml" file in <project_root_dir>/output/output and your module's EPC file, lying inside the same directory, will contain lots of "VARIATION-POINT" elements. # Open S32DS and select File > Import > S32 Configuration Tools > Import ECU Configuration. Browse to the location where your EPC files are located within the EBT project and select at least your module's EPC file, EcuC's EPC file and PostBuildSelectableVariants.arxml. Check the "Import the configuration as a new one" radio button and select the processor / package / sdk version accordingly. # Go to the "Global settings" panel and make sure that ComponentGenerationMethod=EcucPostBuildVariants in the System component. # Select "Update Code" to generate your S32DS project files. Perform a comparison/diff of the generated files between S32DS and EBT. These files should be pretty much identical (sans whitespace or formatting) # Go to the "Global settings" panel again to generate the ECVD files (EcvdGenerationMethod=INDIVIDUAL, browse a location for EcvdOutputPath and click on the Generate Configuration button). Compare/diff your module's EPC file with your module's ECVD file. These files should be pretty much identical (sans whitespace or formatting) # The above steps tested the EBT->S32DS compatibility. To also test the S32DS->EBT compatibility, do the above steps in reverse. That is, start from an S32DS project with post-build variants, generate the ECVD files, import them into EBT, compare again the generated files and the configuration files.

ID	Subtype	Headline and Description
ARTD-26311	New Feature	[i3c] Add support for multiple configurations in S32CT NewWorkDescription: Previously, we limited the number of functional groups (multiple configurations) to 1. Now we want to add support for multiple configurations (in the form of post-build variants and classic functional groups) so that we can also replicate in S32CT the module configurations from EB Tresos in which there are two or more post-build variants. Requirement source: SRS_BSW_00405 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Read the newly introduced section ("13. Multiple Configurations") in the following presentation: [NXP_RTD_AUTOSAR_S32CT_V2|https://nxp1.sharepoint.com/:p:/r/sites/Zebra/Shared%20Documents/Configuration%20(code,%20DS,%20EB,%20etc)/NXP_RTD_AUTOSAR_S32CT_V2.pptx?d=w28a51ba3c45240f5abb6a6933671dcd3&csf=1&web=1&e=r7YbFB] Make sure you have added the SYNC_VALUE and SYNC_SIZE options to each component setting that requires it (as suggested in the presentation, you can use [epdimp2ct|https://nxp1.sharepoint.com/:f:/s/Zebra/EprWldG7fTNPgdoXtWTgmIsBn1Xo56J_qJQGC37m92ax9A?e=ivi58c] to automate this task as long as you have a matching EPD for your component) Apply the changes shown in the source code references. The main points are: {noformat} [!IF "var:defined('postBuildVariant')"!]{noformat} translates to {noformat} if (useFgInfix()){noformat} The file names and configuration structures should not contain the variant infix when there's no selected post-build variant (actually, most of the changes you'll see in the references are done just to support this use-case) Sanity Check: Check that your driver can be successfully built in all three scenarios: ## ComponentGenerationMethod = EcucPostBuildVariants and VARIANT_NO = 0 ## ComponentGenerationMethod = EcucPostBuildVariants and VARIANT_NO > 1 (VARIANT_NO == 1 is the base case from which you started) ## ComponentGenerationMethod = FunctionalGroups (with at least 2 FGs configured in the project) Extensive Testing: By default, EB Tresos cannot generate variant aware EPC files without throwing a null pointer exception. To get around this limitation, the dreisoft.tresos.autosar2 plugin must be patched. To do this, download one of the two attached archives, depending on your EBT version, and extract it in <ebt_root_dir>/plugins. # Go to your driver's plugin, open {_}plugin.xml{_}, search for {_}id="EPCGenerator"{_}, and set the value of parameter "allVariants" to {_}"true"{_}. This will enable variant aware EPC file generation for your module. # Create a configuration with at least two post-build variants. The project will need EcuC for post-build variants to be enabled. The configuration should ideally use different values for nodes with postBuildVariantValue=TRUE and different list elements for nodes with postBuildVariantMultiplicity=TRUE. This will ensure that errors in variant handling can be easily caught later on while doing the diffs. # Generate the EPC files by right clicking on your project's configuration and select "Generate Project". If the 1st step has been carried out correctly, there will be a "PostBuildSelectableVariants.arxml" file in <project_root_dir>/output/output and your module's EPC file, lying inside the same directory, will contain lots of "VARIATION-POINT" elements. # Open S32DS and select File > Import > S32 Configuration Tools > Import ECU Configuration. Browse to the location where your EPC files are located within the EBT project and select at least your module's EPC file, EcuC's EPC file and PostBuildSelectableVariants.arxml. Check the "Import the configuration as a new one" radio button and select the processor / package / sdk version accordingly. # Go to the "Global settings" panel and make sure that ComponentGenerationMethod=EcucPostBuildVariants in the System component. # Select "Update Code" to generate your S32DS project files. Perform a comparison/diff of the generated files between S32DS and EBT. These files should be pretty much identical (sans whitespace or formatting) # Go to the "Global settings" panel again to generate the ECVD files (EcvdGenerationMethod=INDIVIDUAL, browse a location for EcvdOutputPath and click on the Generate Configuration button). Compare/diff your module's EPC file with your module's ECVD file. These files should be pretty much identical (sans whitespace or formatting) # The above steps tested the EBT->S32DS compatibility. To also test the S32DS->EBT compatibility, do the above steps in reverse. That is, start from an S32DS project with post-build variants, generate the ECVD files, import them into EBT, compare again the generated files and the configuration files.

ID	Subtype	Headline and Description
ARTD-26328	New Feature	[sent] Add support for multiple configurations in S32CT NewWorkDescription: Previously, we limited the number of functional groups (multiple configurations) to 1. Now we want to add support for multiple configurations (in the form of post-build variants and classic functional groups) so that we can also replicate in S32CT the module configurations from EB Tresos in which there are two or more post-build variants. Requirement source: SRS_BSW_00405 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Read the newly introduced section ("13. Multiple Configurations") in the following presentation: [NXP_RTD_AUTOSAR_S32CT_V2|https://nxp1.sharepoint.com/:p:/r/sites/Zebra/Shared%20Documents/Configuration%20(code,%20DS,%20EB,%20etc)/NXP_RTD_AUTOSAR_S32CT_V2.pptx?d=w28a51ba3c45240f5abb6a6933671dcd3&csf=1&web=1&e=r7YbFB] Make sure you have added the SYNC_VALUE and SYNC_SIZE options to each component setting that requires it (as suggested in the presentation, you can use [epdimp2ct|https://nxp1.sharepoint.com/:f:/s/Zebra/EprWldG7fTNPgdoXtWTgmIsBn1Xo56J_qJQGC37m92ax9A?e=ivi58c] to automate this task as long as you have a matching EPD for your component) Apply the changes shown in the source code references. The main points are: {noformat} [!IF "var:defined('postBuildVariant')"!]{noformat} translates to {noformat} if (useFgInfix()){noformat} The file names and configuration structures should not contain the variant infix when there's no selected post-build variant (actually, most of the changes you'll see in the references are done just to support this use-case) Sanity Check: Check that your driver can be successfully built in all three scenarios: ## ComponentGenerationMethod = EcucPostBuildVariants and VARIANT_NO = 0 ## ComponentGenerationMethod = EcucPostBuildVariants and VARIANT_NO > 1 (VARIANT_NO == 1 is the base case from which you started) ## ComponentGenerationMethod = FunctionalGroups (with at least 2 FGs configured in the project) Extensive Testing: By default, EB Tresos cannot generate variant aware EPC files without throwing a null pointer exception. To get around this limitation, the dreisoft.tresos.autosar2 plugin must be patched. To do this, download one of the two attached archives, depending on your EBT version, and extract it in <ebt_root_dir>/plugins. # Go to your driver's plugin, open {_}plugin.xml{_}, search for {_}id="EPCGenerator"{_}, and set the value of parameter "allVariants" to {_}"true"{_}. This will enable variant aware EPC file generation for your module. # Create a configuration with at least two post-build variants. The project will need EcuC for post-build variants to be enabled. The configuration should ideally use different values for nodes with postBuildVariantValue=TRUE and different list elements for nodes with postBuildVariantMultiplicity=TRUE. This will ensure that errors in variant handling can be easily caught later on while doing the diffs. # Generate the EPC files by right clicking on your project's configuration and select "Generate Project". If the 1st step has been carried out correctly, there will be a "PostBuildSelectableVariants.arxml" file in <project_root_dir>/output/output and your module's EPC file, lying inside the same directory, will contain lots of "VARIATION-POINT" elements. # Open S32DS and select File > Import > S32 Configuration Tools > Import ECU Configuration. Browse to the location where your EPC files are located within the EBT project and select at least your module's EPC file, EcuC's EPC file and PostBuildSelectableVariants.arxml. Check the "Import the configuration as a new one" radio button and select the processor / package / sdk version accordingly. # Go to the "Global settings" panel and make sure that ComponentGenerationMethod=EcucPostBuildVariants in the System component. # Select "Update Code" to generate your S32DS project files. Perform a comparison/diff of the generated files between S32DS and EBT. These files should be pretty much identical (sans whitespace or formatting) # Go to the "Global settings" panel again to generate the ECVD files (EcvdGenerationMethod=INDIVIDUAL, browse a location for EcvdOutputPath and click on the Generate Configuration button). Compare/diff your module's EPC file with your module's ECVD file. These files should be pretty much identical (sans whitespace or formatting) # The above steps tested the EBT->S32DS compatibility. To also test the S32DS->EBT compatibility, do the above steps in reverse. That is, start from an S32DS project with post-build variants, generate the ECVD files, import them into EBT, compare again the generated files and the configuration files.

ID	Subtype	Headline and Description
ARTD-26330	New Feature	[spi] Add support for multiple configurations in S32CT NewWorkDescription: Previously, we limited the number of functional groups (multiple configurations) to 1. Now we want to add support for multiple configurations (in the form of post-build variants and classic functional groups) so that we can also replicate in S32CT the module configurations from EB Tresos in which there are two or more post-build variants. Requirement source: SRS_BSW_00405 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Read the newly introduced section ("13. Multiple Configurations") in the following presentation: [NXP_RTD_AUTOSAR_S32CT_V2|https://nxp1.sharepoint.com/:p:/r/sites/Zebra/Shared%20Documents/Configuration%20(code,%20DS,%20EB,%20etc)/NXP_RTD_AUTOSAR_S32CT_V2.pptx?d=w28a51ba3c45240f5abb6a6933671dcd3&csf=1&web=1&e=r7YbFB] Make sure you have added the SYNC_VALUE and SYNC_SIZE options to each component setting that requires it (as suggested in the presentation, you can use [epdimp2ct|https://nxp1.sharepoint.com/:f:/s/Zebra/EprWldG7fTNPgdoXtWTgmIsBn1Xo56J_qJQGC37m92ax9A?e=ivi58c] to automate this task as long as you have a matching EPD for your component) Apply the changes shown in the source code references. The main points are: {noformat} [!IF "var:defined('postBuildVariant')"!]{noformat} translates to {noformat} if (useFgInfix()){noformat} The file names and configuration structures should not contain the variant infix when there's no selected post-build variant (actually, most of the changes you'll see in the references are done just to support this use-case) Sanity Check: Check that your driver can be successfully built in all three scenarios: ## ComponentGenerationMethod = EcucPostBuildVariants and VARIANT_NO = 0 ## ComponentGenerationMethod = EcucPostBuildVariants and VARIANT_NO > 1 (VARIANT_NO == 1 is the base case from which you started) ## ComponentGenerationMethod = FunctionalGroups (with at least 2 FGs configured in the project) Extensive Testing: By default, EB Tresos cannot generate variant aware EPC files without throwing a null pointer exception. To get around this limitation, the dreisoft.tresos.autosar2 plugin must be patched. To do this, download one of the two attached archives, depending on your EBT version, and extract it in <ebt_root_dir>/plugins. # Go to your driver's plugin, open {_}plugin.xml{_}, search for {_}id="EPCGenerator"{_}, and set the value of parameter "allVariants" to {_}"true"{_}. This will enable variant aware EPC file generation for your module. # Create a configuration with at least two post-build variants. The project will need EcuC for post-build variants to be enabled. The configuration should ideally use different values for nodes with postBuildVariantValue=TRUE and different list elements for nodes with postBuildVariantMultiplicity=TRUE. This will ensure that errors in variant handling can be easily caught later on while doing the diffs. # Generate the EPC files by right clicking on your project's configuration and select "Generate Project". If the 1st step has been carried out correctly, there will be a "PostBuildSelectableVariants.arxml" file in <project_root_dir>/output/output and your module's EPC file, lying inside the same directory, will contain lots of "VARIATION-POINT" elements. # Open S32DS and select File > Import > S32 Configuration Tools > Import ECU Configuration. Browse to the location where your EPC files are located within the EBT project and select at least your module's EPC file, EcuC's EPC file and PostBuildSelectableVariants.arxml. Check the "Import the configuration as a new one" radio button and select the processor / package / sdk version accordingly. # Go to the "Global settings" panel and make sure that ComponentGenerationMethod=EcucPostBuildVariants in the System component. # Select "Update Code" to generate your S32DS project files. Perform a comparison/diff of the generated files between S32DS and EBT. These files should be pretty much identical (sans whitespace or formatting) # Go to the "Global settings" panel again to generate the ECVD files (EcvdGenerationMethod=INDIVIDUAL, browse a location for EcvdOutputPath and click on the Generate Configuration button). Compare/diff your module's EPC file with your module's ECVD file. These files should be pretty much identical (sans whitespace or formatting) # The above steps tested the EBT->S32DS compatibility. To also test the S32DS->EBT compatibility, do the above steps in reverse. That is, start from an S32DS project with post-build variants, generate the ECVD files, import them into EBT, compare again the generated files and the configuration files.

ID	Subtype	Headline and Description
ARTD-26332	New Feature	[uart] Add support for multiple configurations in S32CT NewWorkDescription: Previously, we limited the number of functional groups (multiple configurations) to 1. Now we want to add support for multiple configurations (in the form of post-build variants and classic functional groups) so that we can also replicate in S32CT the module configurations from EB Tresos in which there are two or more post-build variants. Requirement source: SRS_BSW_00405 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Read the newly introduced section ("13. Multiple Configurations") in the following presentation: [NXP_RTD_AUTOSAR_S32CT_V2|https://nxp1.sharepoint.com/:p:/r/sites/Zebra/Shared%20Documents/Configuration%20(code,%20DS,%20EB,%20etc)/NXP_RTD_AUTOSAR_S32CT_V2.pptx?d=w28a51ba3c45240f5abb6a6933671dcd3&csf=1&web=1&e=r7YbFB] Make sure you have added the SYNC_VALUE and SYNC_SIZE options to each component setting that requires it (as suggested in the presentation, you can use [epdimp2ct|https://nxp1.sharepoint.com/:f:/s/Zebra/EprWldG7fTNPgdoXtWTgmIsBn1Xo56J_qJQGC37m92ax9A?e=ivi58c] to automate this task as long as you have a matching EPD for your component) Apply the changes shown in the source code references. The main points are: {noformat} [!IF "var:defined('postBuildVariant')"!]{noformat} translates to {noformat} if (useFgInfix()){noformat} The file names and configuration structures should not contain the variant infix when there's no selected post-build variant (actually, most of the changes you'll see in the references are done just to support this use-case) Sanity Check: Check that your driver can be successfully built in all three scenarios: ## ComponentGenerationMethod = EcucPostBuildVariants and VARIANT_NO = 0 ## ComponentGenerationMethod = EcucPostBuildVariants and VARIANT_NO > 1 (VARIANT_NO == 1 is the base case from which you started) ## ComponentGenerationMethod = FunctionalGroups (with at least 2 FGs configured in the project) Extensive Testing: By default, EB Tresos cannot generate variant aware EPC files without throwing a null pointer exception. To get around this limitation, the dreisoft.tresos.autosar2 plugin must be patched. To do this, download one of the two attached archives, depending on your EBT version, and extract it in <ebt_root_dir>/plugins. # Go to your driver's plugin, open {_}plugin.xml{_}, search for {_}id="EPCGenerator"{_}, and set the value of parameter "allVariants" to {_}"true"{_}. This will enable variant aware EPC file generation for your module. # Create a configuration with at least two post-build variants. The project will need EcuC for post-build variants to be enabled. The configuration should ideally use different values for nodes with postBuildVariantValue=TRUE and different list elements for nodes with postBuildVariantMultiplicity=TRUE. This will ensure that errors in variant handling can be easily caught later on while doing the diffs. # Generate the EPC files by right clicking on your project's configuration and select "Generate Project". If the 1st step has been carried out correctly, there will be a "PostBuildSelectableVariants.arxml" file in <project_root_dir>/output/output and your module's EPC file, lying inside the same directory, will contain lots of "VARIATION-POINT" elements. # Open S32DS and select File > Import > S32 Configuration Tools > Import ECU Configuration. Browse to the location where your EPC files are located within the EBT project and select at least your module's EPC file, EcuC's EPC file and PostBuildSelectableVariants.arxml. Check the "Import the configuration as a new one" radio button and select the processor / package / sdk version accordingly. # Go to the "Global settings" panel and make sure that ComponentGenerationMethod=EcucPostBuildVariants in the System component. # Select "Update Code" to generate your S32DS project files. Perform a comparison/diff of the generated files between S32DS and EBT. These files should be pretty much identical (sans whitespace or formatting) # Go to the "Global settings" panel again to generate the ECVD files (EcvdGenerationMethod=INDIVIDUAL, browse a location for EcvdOutputPath and click on the Generate Configuration button). Compare/diff your module's EPC file with your module's ECVD file. These files should be pretty much identical (sans whitespace or formatting) # The above steps tested the EBT->S32DS compatibility. To also test the S32DS->EBT compatibility, do the above steps in reverse. That is, start from an S32DS project with post-build variants, generate the ECVD files, import them into EBT, compare again the generated files and the configuration files.
ARTD-26350	New Feature	[SPI] Add a note in UM to guide users configure correctly the priority of DMA ISR NewWorkDescription: In DMA mode, the priority of DMA ISR which is configured by Platform should be follow the order of priority as below: DMA ISR of TX channel is more important than DMA ISR of RX channel For more details, see the email in attachment Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Add a note in UM to guide users configure correctly the priority of DMA ISR (Driver usage and configuration tips)

ID	Subtype	Headline and Description
ARTD-26448	New Feature	[mcu] CPR_RTD_00028 is replaced by CPR_RTD_00664 NewWorkDescription: Requirement CPR_RTD_00028 is rejected and replaced by CPR_RTD_00664: "ISR shall check whether its respective interrupt status flag and interrupt enable flag are set; i.e. whether the interrupt is not spurious. If at least one of the flags is not set, then the interrupt is spurious and the ISR shall not treat the event (return immediately). Rationale: A spurious interrupt is considered when there is a glitch in the hardware mechanisms that trigger the CPU exception. Drivers must ensure only relevant events are treated and spurious ones are discarded." Check and update (if needed) the driver implementation to be according to CPR_RTD_00664. Update FMEA and include also Adrian Herea (Safety Manager) to the review. Requirement source: cPRT {*}Proposed solution{*}: The rationale behind the update is to not consider as spurious the events that may otherwise be treated in a different context (e.g. polling mode) and for which the interrupt enable bit is not set. For interrupt lines shared by multiple events, it should be possible for some of the events to be treated by the ISR, while other to be left uncleared so that they can be treated in the thread (as long as they have the interrupt enabled bit cleared, meaning the interrupt is disabled). The update required here would be to only clear the flags for the events that are enabled and leave the others untouched, as long as they are managed by the driver in a different context. The consequence of that would be to allow multiple events that have separate interrupt enable bits but share a single interrupt line to function both in "interrupt" and "polling" modes simultaneously. Hence, the clearing of the flag should only happen if the condition "(interrupt_enable && interrupt_flag)" is true, otherwise it is assumed that the flag is handled outside the ISR. The rationale applies only for drivers that handle hardware resources that share interrupt lines, but the correct implementation of the ISR logic should be checked for all drivers.
ARTD-26450	Bug	[SENT] [S32K3] There are some issues for SENT 2.0.0 of K3 RTD. Detailed description (how to reproduce it): 1.DMA buffer always overflow See below screenshot, the address of DMA buffer is from 0x20431BF8 to 0x20431C6F. Address 0x20431C70 is not included in buffer, but it is filled with a captured value. !image-2022-05-12-10-53-31-571.png! 2.Nibble/frame may be missed because SENT data processing is very easily impacted by other tasks. (See attachment) The minimum nibble length is 12 ticks (i.e., 36 us for 3 us tick length, or 19.86 us for 1.655 us tick length), which means the data processing of SENT must be less than 12 ticks to prevent buffer overflow and frame missing. Generally, the data processing of SENT is shorter than 12 ticks if there was no other tasks, or the depth of DMA buffer is not very deep. However, if a prioritized task happened while SENT ISR was ongoing, it is possible that the time of SENT data processing would be prolonged to more than 12 ticks. In case of multi-channel, if the depth of DMA is significant, the ISR of SENT may block each other, causing nibble/frame missing. 3. For multi-channel SENT configured, signal edge may be missed because flag is wrongly cleared. See right screenshot of Flexio_Mcl_Ip_Irq.c (in attachment), suppose one signal edge has come, and SW has run into ISR. At present, if another signal edge comes between point ① and {*}②{*}, the flag triggered by the latter edge will not be recorded in point ① and will be cleared in point {*}②{*}. Because of that, the unrecorded flag will not be recognized in point {*}③{*}, which means no data processing, resulting in one nibble/frame missing. For multi-channel SENT configured, it happens very frequently (see test results in attachment). By the way, {+}it seems that Shifter flag and Pin flag clearing has the same problem{+}. Please find the details in attachment. Preconditions: Please find the details in attachment. Test Case ID (internal TC that caught the defect) optional: None Observed behavior: Please find the details in attachment. Expected behavior: Please find the details in attachment. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Please find the Proposed solution in attachment.

ID	Subtype	Headline and Description
ARTD-26477	Bug	[FLS] [QSPI] SEQID is treated as a LUT index Detailed description (how to reproduce it): In the functions mentioned below the lut parameter is actually a sequence ID, and not a LUT index: Qspi_lp_IpWrite}} Qspi_lp_IpRead}} Qspi_lp_IpCommand}} Besides the confusion, the functional defect is that the parameter is checked against the maximum number of LUT registers: DEV_ASSERT_QSPI(lut < QuadSPI_LUT_COUNT);}} Preconditions: none Test Case ID (internal TC that caught the defect) optional: no TC Observed behavior: the check is too permissive Expected behavior: we should differentiate between the id of the sequence and the index of the LUT register Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Besides the functional change proposed below, a better naming of the parameters would be suited: DEV_ASSERT_QSPI(SeqId < QuadSPI_LUT_COUNT / FEATURE_QSPI_LUT_SEQUENCE_SIZE);}}
ARTD-26542	Bug	[SPI] RTD 200 LPSPI baudrate The CT (S32DS3.4 RTD 2.0.0) does not allow setting the LPSPI baudrate to 20MHz. !image-2022-05-16-13-07-10-971.png|thumbnail! But according to the datasheet and even to the CT description, it is possible: !image-2022-05-16-13-06-00-951.png|thumbnail!

ARTD-26591	Bug	[SPI] LPSPI IP does not output correct SpiTimeCs2Cs values
		
		Description frovided by teldevice DFAE:
		
		I'm using S32K3 RTD v2.0.0 with the following update to S32DS v3.4.
		S32K3 RTD AUTOSAR 4.4 Version 2.0.0 (version: 2.0.0)
		S32K3xx development package (version:3.4.3)
		
		If I set SpiBaudrate to 10000000 (1Mbps) and SpiTimeCs2Cs to 0.0000064 (6.4us) in LPSPI_0, the actual Cs2Cs is only 3.228us.
		
		Upon further investigation, I found that ConfigTools is outputting incorrect settings. Since LPSPI_0 operates at 80MHz(12.5ns), to get Cs2Cs2 to 6.4us, DBT should be (6.4us/12.5ns)-2=510 cycles. But, the maximum value of DBT is 255, so PRESCALE should be 1. However PRESCALE is still 0 and the value of DBT is wrong.
		I believe this is a bug. Could you please fix this bug?
		
		/ Lpspi_lp_DeviceAttributes_SpiExternalDevice_Master Device Attribute Configuration of Spi*/
		const Lpspi_lp_ExternalDeviceType Lpspi_lp_DeviceAttributes_SpiExternalDevice_Master_Instance_0_BOARD_InitPeripherals =
		{
		0U, / Instance /
		(uint32)(LPSPI_CCR_SCKPCS(79U) LPSPI_CCR_PCSSCK(79U) LPSPI_CCR_SCKDIV(78U) LPSPI_CCR_DBT(255U)), / ccr /
		(uint32)(LPSPI_TCR_WIDTH(0U) LPSPI_TCR_CPOL(1U) LPSPI_TCR_CPHA(1U) LPSPI_TCR_PRESCALE(0U)
		LPSPI_TCR_PCS(0U) LPSPI_TCR_CONT(0U)) / TCR /
		
		#if (STD_ON == LPSPI_IP_HALF_DUPLEX_MODE_SUPPORT)
		,(uint32)0U / This device do not support half duplex mode /
		#endif
		, &Lpspi_lp_DeviceParamsCfg_BOARD_InitPeripherals[0U]
		};

ID	Subtype	Headline and Description
ARTD-26603	Bug	[Fls][S32ZE_EAR_080] Remove include "Os.h" in Fls.h for avoiding build failed re-declared function Detailed description (how to reproduce it): Since Os.h has been updated as https://bitbucket.sw.nxp.com/projects/ARTD/repos/os/pull-requests/35/diff#generic/include/Os.h: Build failed occure (re-declare ResumeAllInterrupts() and SuspendAllInterrupts()) on GHS if USER_MODE enable . Preconditions: Osif_Internal.h defines the above APIs already Test Case ID (internal TC that caught the defect) optional: All test build on GHS with USER_MODE enable Observed behavior: Build failed on GHS. Expected behavior: Fls.h shall be updated Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-26656	Bug	[SPI/DMA] Incorrect configuration sequence in AsyncTransmitFast() for SPI fast transfer mode. Detailed description (how to reproduce it): [Using SPI fast transfer mode. and call Lpspi_Ip_AsyncTransmitFast(), Then the DMA hardware SBE error will occur. This error is caused by incorrect configuration sequence. We should configure DMA first and enable the DMA request.] !image-2022-05-23-10-39-41-303.png! Preconditions: [Using SPI fast transfer mode] Observed behavior: [SBE error on DMA channel] !image-2022-05-23-10-49-55-556.png! Proposed solution*_ [Fix this bug in subsequent RTD version.]
ARTD-26677	Bug	CLONE - S32K3 Config tool - SPI driver window crash Detailed description (how to reproduce it): Open Spi_HaldDuplexTransfer_S32K344 example and open config tool. Select SPI peripheral and SpiDriver tab: !image-2022-05-23-09-42-56-687.png! scroll down to SpiHwUnit and switch CSIB0 to SSIB2 or higher: !image-2022-05-23-09-44-50-972.png! After that switch to any other Tab and back to SpiDriver tab. The window layout is broken: !image-2022-05-23-09-46-44-274.png! Preconditions: Packages installed S32K3 development package v3.4.3, S32K3 RTD Autosar 4.4 version 2.0.0.

ID	Subtype	Headline and Description
ARTD-26764	Bug	[spi] Review missing or incomplete IM Multcore support chapter Detailed description (how to reproduce it): Each IM needs to contain chapter "5.8 Multicore support", in which it needs to list: the multicore type the multicore type per IP, in case there are any differences the list of all assumption any other details a user might need to understand how it can use it, in a natural language, any vendor specific details, etc. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Missing and/or incomplete information Expected behavior: Any user to be able to understand the implementation details and the integration steps required for using a module in multicore context. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Review and update the IMs with the following information in Chapter "5.8 Multicore support" the multicore type the multicore type per IP, in case there are any differences the list of all assumption any other details a user might need to understand how it can use it, in a natural language, any vendor specific details, etc. Check for reference IMs from modules like: ADC, THERMAL, CRYPTO, etc. Note: some modules have this chapter missing (like DIO, PORT, FR), others have it incomplete (MCL, EEP, FLS) others would benefit from more details. Note2: even if the testing is missing for a release, it is useful to have this chapter as a statement for the implementation design.
ARTD-26809	Bug	[LIN][S32K1XX/S32K3XX] Lin driver is still waking up with signal < 150 us Detailed description (how to reproduce it): In Lin Specification Package, Both Master and Slave node shall detect the wake up signal (a dominant pulse longer than 150 us) But the Lin driver is still waking up with signal < 150 us. Preconditions: First, Call Lin_GoToSleep or Lin_GoToSleepInternal function. Then, Send the wake up pulse < 150 us Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Lin driver is still waking up with signal < 150 us Expected behavior: Lin driver is only waking up with signal > 150 us Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Solution for this issue is to use timer and UART edge detection interrupts to detect and measure the wake up signal.

ID	Subtype	Headline and Description
ARTD-26817	Bug	[MCU] When setting Mcu Register Values Optimization is enable, mcu can not init Detailed description (how to reproduce it): When setting Mcu Register Values Optimization is enable, MCU can not init !screenshot-1.png|thumbnail! Issue2: Improvement generation script: 2 list MCU.CMU_FC.Address.List}} and {{MCU.CMU_FC.List}} contain same information: cmuInstance and cmuMonitorname.-> using string operation and add function macro to use 1 list only try "constrains" to avoid using multiple #IF to check McuCmuName Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: hardfault when call MCU_initclock() Expected behavior: MCU_initclock() run fine Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc. Proposed solution optional: [...]
ARTD-26824	Bug	Incorrect Baud Rate while configuring LPUART Detailed description (how to reproduce it): Configure LPUART for Baud Rate 921600 and do following settings !image-2022-05-27-19-51-02-116.png! Preconditions: None Test Case ID (internal TC that caught the defect) optional: None Observed behavior: Wrong actual baud rate value in configuration !image-2022-05-27-19-51-47-794.png! Expected behavior: Actual baud rate should be whatever configured like 921600 Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-26849	Bug	[Platform] The exception entry in linker files for R52 and A53 should be aligned with 2^11 Detailed description (how to reproduce it): The exception entry in linker files for R52 and A53 should be aligned with 2^11 !image-2022-05-30-15-33-26-310.png! It should be pushed at top of a memory region to avoid wasting memory Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: NA Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA

ID	Subtype	Headline and Description
ARTD-26945	New Feature	[SENT] [S32K3] Add support for status nibble in CRC computation NewWorkDescription: Some sensors include the status nibble in the CRC computation −Currently, it's not possible to use some sensors that compute the CRC over the whole nibble set (including status nibble). A new feature (configuration option) is required to add support for this. −Another improvement topic would be the CRC handling. The spec requires 2 types of CRC (RECOMMENDED/LEGACY), the only difference being the extra shift of a zero frame into the CRC pipeline. The standard also recommends 3 different computation methods, however, the 256 element table is intended for certain microcontrollers lacking specific HW features (XOR, not applicable on K3). The suggestion is to use the 16 element table for both LEGACY/RECOMMENDED, thus saving 256 bytes of memory and improving the performance. Requirement source: Customer Request (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: !image-2022-05-31-12-09-05-976.png!
ARTD-27051	New Feature	[ICU] Update format of testcase Detailed description (how to reproduce it): Update test cases to new format, that can be use by "Auto Collect Comment From Commit" tool. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: N/A Expected behavior: N/A Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-27081	New Feature	[S32K3XX] PLATFORM: Remove MSCM configuration NewWorkDescription: PLATFORM: Remove MSCM configuration Requirement source: PLATFORM: Remove MSCM configuration (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: PLATFORM: Remove MSCM configuration
ARTD-27097	New Feature	[CRYPTO] Fix CWE violations NewWorkDescription: Fix CWE violations found in the following reports. Bamboo build(artifacts): [https://bamboo3.sw.nxp.com/browse/ARTD-CIC225-13/artifact] Requirement source: [NA] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Double check and fix CWE violations, what cannot be fixed will be added in the CWE deviation

ID	Subtype	Headline and Description
ARTD-27729	Bug	[PORT]Symbolic name of PortPin generated wrong Detailed description (how to reproduce it): The issue with the symbolic names of PortPinId according to TPS_ECUC_02108 in AUTOSAR_TPS_ECUConfiguration.pdf. The sample port configuratiuon this leads to the generation result: #define PortConfigSet_PortContainer_0_PortPin_0 0 But according to TPS_ECUC_02108, it must be like this: #define PortConf_PortPin_PortPin_0 0 The short name EcucParamConfContainerDef of the declaring module is PortPin and the short name of the EcuCContainerValue container, which holds the symbolicNameValue configuration parameter value, is PortPin_0 Preconditions: the name generated of the Port module must be: #define PortConf_PortPin_PortPin_0 0 Test Case ID (internal TC that caught the defect) optional: None Observed behavior: #define PortConfigSet_PortContainer_0_PortPin_0 0 Expected behavior: #define PortConf_PortPin_PortPin_0 0 Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: The current name is a deviation from Autosar and must be marked if it shall be used. Add the constraint for duplication of Port Pin Name
ARTD-27900	Bug	[SPI] Incorrect max value of baudrate on S32K312 and S32K311 Detailed description (how to reproduce it): Reference manual: S32K314, S32K324, S32K344, S32K322, and S32K342 supports data rate up to 20 Mbps, S32K312 and S32K311 supports data rate up to 15 Mbps. Only one LPSPI instance support 20 MHz in loopback mode that is LPSPI0. Datasheet: LPSPI0 support up to 20MHz on fast pin. IOMUX doc: Fast pin wasn't supported on S32K311 and S32K312 SPI driver: All derivative can use 20MHz baudrate if using LPSPI0 master in loopback mode Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: See above Expected behavior: Max baudrate of SPI master mode on S32K311 and S32K312 are 15MHz Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: See above
ARTD-27933	New Feature	[CAN] While using FlexCAN timestamp feature, the message buffers should be unlocked within each 20 CAN bits NewWorkDescription: when review RM for K396(ARTD-27064), one note for timestamp, which should be investigated. !image-2022-06-21-14-02-36-357.png! Requirement source: None (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [....]

ID	Subtype	Headline and Description
ARTD-28056	Bug	[WDG] ServiceIdType is not match with AUTOSAR specification. Detailed description (how to reproduce it): [Wrong the service ID with function Wdg_SetTriggerCondition !image-2022-06-23-14-37-32-924.png|thumbnail! and Autosar spec !image-2022-06-23-14-51-09-227.png|thumbnail!] Preconditions: [Autosar specification link https://www.autosar.org/fileadmin/user_upload/standards/classic/19-11/AUTOSAR_SWS_WatchdogDriver.pdf] Test Case ID (internal TC that caught the defect) optional: [Review] Observed behavior: [Wrong WDG service ID] Expected behavior: [Correct the service ID. This should impact to the bswmd report, dox.... So you need to check report again.] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]

ID	Subtype	Headline and Description
ARTD-28119	New Feature	[SPI] Request for changing RTD driver of SPI on S32K3XX Detailed description (how to reproduce it): [Background] The followings are slave device specifications. For getting data length, CS must be assert from command to slave response continuingly. The data length changes depending on the time. So, they execute “Lpspi_lp_SyncTransmit()“ 2 times. (1st is command for getting data length, 2nd is for slave response.) So, my customer use GPIO as CS. [Phenomenon] CLK changes between 1st “Lpspi_lp_SyncTransmit()“ and 2nd “Lpspi_lp_SyncTransmit()“. Lpspi_lp_SyncTransmit calls Lpspi_TransmitTxInit() > IP Reset to cover ERRATA 050456 !image-2022-06-27-09-43-41-626.png! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: !image-2022-06-27-09-44-04-721.png! CLK changes between 1st “Lpspi_lp_SyncTransmit()“ and 2nd “Lpspi_lp_SyncTransmit()“. [Affection] If CLK is not corrected, it is necessary to receive the maximum number of data each time. The size of the data varies greatly from a few bytes to 100 bytes. Obtaining the maximum data size each time would take a considerable amount of processing time, making it systematically unacceptable. Expected behavior: Workaround for ERRATA 050456 shouldn't reset CLK Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Requirement source: N/A Proposed solution optional: Change the code for the other workaround instead of resetting the IP !image-2022-06-27-09-48-53-542.png!
ARTD-28205	New Feature	[adc] Update copyright template NewWorkDescription: Replace : “(c) Copyright \{year range\} NXP Semiconductors All Rights Reserved.” with : Copyright \{year range\} NXP !screenshot-2.png|thumbnail! to !screenshot-3.png|thumbnail! Requirement source: as described in “Updating Copyright Years” topic on this guide https://confluence.sw.nxp.com/display/OSS/File+Headers+-+Copyright+and+License+Information). (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: as above

ID	Subtype	Headline and Description
ARTD-28210	New Feature	[i2s] Update copyright template NewWorkDescription: Replace : “(c) Copyright \{year range\} NXP Semiconductors All Rights Reserved.” with : Copyright \{year range\} NXP !screenshot-2.png|thumbnail! to !screenshot-3.png|thumbnail! Requirement source: as described in “Updating Copyright Years” topic on this guide https://confluence.sw.nxp.com/display/OSS/File+Headers+-+Copyright+and+License+Information). (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: as above
ARTD-28180	Bug	[FLS][S32K3XX] Issue in data write using C40 flash (lack of end boundary check for input paramerter) Detailed description (how to reproduce it): If FLS address is 8 bytes aligned for ex:(0x500010) and data length is 128 bytes , in that case data is written from 0x500010 to 0x50007F keeping last 16 bytes unchanged. Observed behavior: Only 112 bytes are written from 0x500010 to 0x50007F Expected behavior: Data should be written from 0x500010 to 0x50008F i.e 128 bytes Proposed solution optional: [....]
ARTD-28179	Bug	[S32K3][SENT] There is an issue in tick length adjustment. Detailed description (how to reproduce it): It can be find in Flexio_Sent_Ip.c that the AdjustedTick is a static variable. That means the adjustment of different channel use the same adjusted variable. When multi Sent channels who have different tick length are set, partial channels cannot extract data correctly, mostly resulting in CRC error. !image-2022-06-28-15-46-12-390.png! Customer ZLG reported this issue. Preconditions: When multi Sent channels who have different tick length are set. Test Case ID (internal TC that caught the defect) optional: None Observed behavior: Partial channels cannot extract data correctly, mostly resulting in CRC error. Expected behavior: All channels can extract data correctly Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: The static variable AdjustedTick* should be an array to storage all channels' adjusted value, respectively.

ID	Subtype	Headline and Description
ARTD-28240	New Feature	[icu] Update copyright template NewWorkDescription: Replace : “(c) Copyright \{year range\} NXP Semiconductors All Rights Reserved.” with : Copyright \{year range\} NXP !screenshot-2.png|thumbnail! to !screenshot-3.png|thumbnail! Requirement source: as described in “Updating Copyright Years” topic on this guide https://confluence.sw.nxp.com/display/OSS/File+Headers+-+Copyright+and+License+Information). (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: as above
ARTD-28593	Bug	[pwm] RTD have bugs with code generation and driver implementation in SW32ZE_RTD_4.4_0.8.0 version Detailed description (how to reproduce it): 1.FLEXPWM channel pair types macro implementation incorrect. In RM the complementary PWM pair should set with 0 and independent should set with 1. !image-2022-06-30-13-23-20-552.png|width=630,height=349! !image-2022-06-30-13-25-10-575.png! 2.PWM generate code is incorrect with the EB configuration: I configured two FLEXPWM instances but the generated instance count only is 1: !image-2022-06-30-13-32-00-390.png|width=1285,height=408! !image-2022-06-30-13-32-45-210.png! Preconditions: S32ZE_RTD_4.4_0.8.0 Test Case ID (internal TC that caught the defect) optional: NO Observed behavior: FLEXPWM initiation is incorrect and flexpwm EB generation code have incorrect macro. Expected behavior: FLEXPWM initiation and code generation should correct. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: modified the driver implementation and EB generation also should de changed.
ARTD-28588	New Feature	LIN driver reports LIN_ERR_SYNC and LIN_ERR_PID conforming to LIN J2602 protocol NewWorkDescription: LIN driver reporting LIN_ERR_SYNC and LIN_ERR_PID conforming to LIN J2602 protocol Requirement source: Proposed solution optional: N/A

ID	Subtype	Headline and Description
ARTD-28678	New Feature	[adc] Add support for multiple configurations in S32CT NewWorkDescription: Previously, we limited the number of functional groups (multiple configurations) to 1. Now we want to add support for multiple configurations (in the form of post-build variants and classic functional groups) so that we can also replicate in S32CT the module configurations from EB Tresos in which there are two or more post-build variants. Requirement source: SRS_BSW_00405 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Read the newly introduced section ("13. Multiple Configurations") in the following presentation: [NXP_RTD_AUTOSAR_S32CT_V2|https://nxp1.sharepoint.com/:p:/r/sites/Zebra/Shared%20Documents/Configuration%20(code,%20DS,%20EB,%20etc)/NXP_RTD_AUTOSAR_S32CT_V2.pptx?d=w28a51ba3c45240f5abb6a6933671dcd3&csf=1&web=1&e=r7YbFB] Make sure you have added the SYNC_VALUE and SYNC_SIZE options to each component setting that requires it (as suggested in the presentation, you can use [epdimp2ct|https://nxp1.sharepoint.com/:f:/s/Zebra/EprWldG7fTNPgdoXtWTgmIsBn1Xo56J_qJQGC37m92ax9A?e=ivi58c] to automate this task as long as you have a matching EPD for your component) Apply the changes shown in the source code references. The main points are: {noformat} [!IF "var:defined('postBuildVariant')"!]{noformat} translates to {noformat} if (useFgInfix()){noformat} The file names and configuration structures should not contain the variant infix when there's no selected post-build variant (actually, most of the changes you'll see in the references are done just to support this use-case) Sanity Check: Check that your driver can be successfully built in all three scenarios: ## ComponentGenerationMethod = EcucPostBuildVariants and VARIANT_NO = 0 ## ComponentGenerationMethod = EcucPostBuildVariants and VARIANT_NO > 1 (VARIANT_NO == 1 is the base case from which you started) ## ComponentGenerationMethod = FunctionalGroups (with at least 2 FGs configured in the project) Extensive Testing: By default, EB Tresos cannot generate variant aware EPC files without throwing a null pointer exception. To get around this limitation, the dreisoft.tresos.autosar2 plugin must be patched. To do this, download one of the two attached archives, depending on your EBT version, and extract it in <ebt_root_dir>/plugins. # Go to your driver's plugin, open {_}plugin.xml{_}, search for {_}id="EPCGenerator"{_}, and set the value of parameter "allVariants" to {_}"true"{_}. This will enable variant aware EPC file generation for your module. # Create a configuration with at least two post-build variants. The project will need EcuC for post-build variants to be enabled. The configuration should ideally use different values for nodes with postBuildVariantValue=TRUE and different list elements for nodes with postBuildVariantMultiplicity=TRUE. This will ensure that errors in variant handling can be easily caught later on while doing the diffs. # Generate the EPC files by right clicking on your project's configuration and select "Generate Project". If the 1st step has been carried out correctly, there will be a "PostBuildSelectableVariants.arxml" file in <project_root_dir>/output/output and your module's EPC file, lying inside the same directory, will contain lots of "VARIATION-POINT" elements. # Open S32DS and select File > Import > S32 Configuration Tools > Import ECU Configuration. Browse to the location where your EPC files are located within the EBT project and select at least your module's EPC file, EcuC's EPC file and PostBuildSelectableVariants.arxml. Check the "Import the configuration as a new one" radio button and select the processor / package / sdk version accordingly. # Go to the "Global settings" panel and make sure that ComponentGenerationMethod=EcucPostBuildVariants in the System component. # Select "Update Code" to generate your S32DS project files. Perform a comparison/diff of the generated files between S32DS and EBT. These files should be pretty much identical (sans whitespace or formatting) # Go to the "Global settings" panel again to generate the ECVD files (EcvdGenerationMethod=INDIVIDUAL, browse a location for EcvdOutputPath and click on the Generate Configuration button). Compare/diff your module's EPC file with your module's ECVD file. These files should be pretty much identical (sans whitespace or formatting) # The above steps tested the EBT->S32DS compatibility. To also test the S32DS->EBT compatibility, do the above steps in reverse. That is, start from an S32DS project with post-build variants, generate the ECVD files, import them into EBT, compare again the generated files and the configuration files.

ID	Subtype	Headline and Description
ARTD-28676	New Feature	[wdg] Add support for multiple configurations in S32CT NewWorkDescription: Previously, we limited the number of functional groups (multiple configurations) to 1. Now we want to add support for multiple configurations (in the form of post-build variants and classic functional groups) so that we can also replicate in S32CT the module configurations from EB Tresos in which there are two or more post-build variants. Requirement source: SRS_BSW_00405 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Read the newly introduced section ("13. Multiple Configurations") in the following presentation: [NXP_RTD_AUTOSAR_S32CT_V2|https://nxp1.sharepoint.com/:p:/r/sites/Zebra/Shared%20Documents/Configuration%20(code,%20DS,%20EB,%20etc)/NXP_RTD_AUTOSAR_S32CT_V2.pptx?d=w28a51ba3c45240f5abb6a6933671dcd3&csf=1&web=1&e=r7YbFB] Make sure you have added the SYNC_VALUE and SYNC_SIZE options to each component setting that requires it (as suggested in the presentation, you can use [epdimp2ct|https://nxp1.sharepoint.com/:f:/s/Zebra/EprWldG7fTNPgdoXtWTgmIsBn1Xo56J_qJQGC37m92ax9A?e=ivi58c] to automate this task as long as you have a matching EPD for your component) Apply the changes shown in the source code references. The main points are: {noformat} [!IF "var:defined('postBuildVariant')"!]{noformat} translates to {noformat} if (useFgInfix()){noformat} The file names and configuration structures should not contain the variant infix when there's no selected post-build variant (actually, most of the changes you'll see in the references are done just to support this use-case) Sanity Check: Check that your driver can be successfully built in all three scenarios: ## ComponentGenerationMethod = EcucPostBuildVariants and VARIANT_NO = 0 ## ComponentGenerationMethod = EcucPostBuildVariants and VARIANT_NO > 1 (VARIANT_NO == 1 is the base case from which you started) ## ComponentGenerationMethod = FunctionalGroups (with at least 2 FGs configured in the project) Extensive Testing: By default, EB Tresos cannot generate variant aware EPC files without throwing a null pointer exception. To get around this limitation, the dreisoft.tresos.autosar2 plugin must be patched. To do this, download one of the two attached archives, depending on your EBT version, and extract it in <ebt_root_dir>/plugins. # Go to your driver's plugin, open {_}plugin.xml{_}, search for {_}id="EPCGenerator"{_}, and set the value of parameter "allVariants" to {_}"true"{_}. This will enable variant aware EPC file generation for your module. # Create a configuration with at least two post-build variants. The project will need EcuC for post-build variants to be enabled. The configuration should ideally use different values for nodes with postBuildVariantValue=TRUE and different list elements for nodes with postBuildVariantMultiplicity=TRUE. This will ensure that errors in variant handling can be easily caught later on while doing the diffs. # Generate the EPC files by right clicking on your project's configuration and select "Generate Project". If the 1st step has been carried out correctly, there will be a "PostBuildSelectableVariants.arxml" file in <project_root_dir>/output/output and your module's EPC file, lying inside the same directory, will contain lots of "VARIATION-POINT" elements. # Open S32DS and select File > Import > S32 Configuration Tools > Import ECU Configuration. Browse to the location where your EPC files are located within the EBT project and select at least your module's EPC file, EcuC's EPC file and PostBuildSelectableVariants.arxml. Check the "Import the configuration as a new one" radio button and select the processor / package / sdk version accordingly. # Go to the "Global settings" panel and make sure that ComponentGenerationMethod=EcucPostBuildVariants in the System component. # Select "Update Code" to generate your S32DS project files. Perform a comparison/diff of the generated files between S32DS and EBT. These files should be pretty much identical (sans whitespace or formatting) # Go to the "Global settings" panel again to generate the ECVD files (EcvdGenerationMethod=INDIVIDUAL, browse a location for EcvdOutputPath and click on the Generate Configuration button). Compare/diff your module's EPC file with your module's ECVD file. These files should be pretty much identical (sans whitespace or formatting) # The above steps tested the EBT->S32DS compatibility. To also test the S32DS->EBT compatibility, do the above steps in reverse. That is, start from an S32DS project with post-build variants, generate the ECVD files, import them into EBT, compare again the generated files and the configuration files.

ID	Subtype	Headline and Description
ARTD-28787	Bug	[MCL] Multi variant on CT generate wrong name of Mcl_config with variant_no = 0 and post_build configuration Detailed description (how to reproduce it): , Try to config post_build variant and variant no = 0 on CT , Check code preview and code generation > Mcl_ConfigType Mcl_Config_BOARD_INITPERIPHERALS is wrong suffixes of name It should be generated name as precompile method. > Build failed Preconditions: , Variant_no = 0, Test Case ID (internal TC that caught the defect) optional: , Mcl_TC_VS_1301 Observed behavior: , Build failed with Mcl_Config_BOARD_INITPERIPHERALS structure Expected behavior: , Name of Mcl_Config must update to avoid error at building phase
ARTD-28839	New Feature	[RM] Move Sema4 APIs from IP to HLD NewWorkDescription: There are some APIs which is available on IP layer but not on HLD: uint8 Sema42_Ip_GetResetGateBusMaster(const uint32 u32Instance) boolean Sema42_Ip_IsResetGateStateIdle(const uint32 u32Instance) uint8 Sema42_Ip_GetResetGateIndex(const uint32 u32Instance) Since Rm does not support Ip layer anymore, those APIs should be moved to HLD. Update requirements will be done on ARTD-27917 Requirement source: (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: move APIs to HLD layer
ARTD-41707	Bug	[ETH] EthIf controller index shall be passed into EthIf callbacks in Eth driver NewWorkDescription: With current implementation, Eth controller index is passed into EthIf callbacks (e.g. EthIf_RxIndication, EthIf_TxConfirmation,...) in Eth driver. However, according to the following requirement: !image-2022-07-07-15-18-27-834.png! The EthIf controller index shall be passed into EthIf callbacks in Eth driver, instead of Eth controller index Requirement source: SWS_EthIf_00091, SWS_EthIf_00085, SWS_EthIf_00231 Proposed solution optional: Add a new field in the configuration of the Eth controller that will allow setting the ID of that specific controller in the context of EthIf. The name of the field should be EthCtrlEthIfIdx and it should be placed in the EthCtrlVendorSpecific container to have a consistent approach with PFE Use the new index when calling EthIf functions from the Eth driver context

ID	Subtype	Headline and Description
ARTD-28967	Bug	[Spi] Build faild on HLD with DS due to Spi Configuration gen wrong name Detailed description (how to reproduce it): !image-2022-07-13-16-05-11-141.png|thumbnail! Build faild on HLD with DS due to Spi Configuration gen wrong name: Spi_Config__BOARD_InitPeripherals !image-2022-07-13-16-07-04-158.png|thumbnail! !image-2022-07-13-16-06-09-481.png|thumbnail! Preconditions: NA Test Case ID (internal TC that caught the defect) optional: Spi_TS_D02 cfg set = 1 Observed behavior: NA Expected behavior: NA Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-28980	Bug	[SAF85_S32R41 0.9.0] RM:: Incorrect constraint when configuring multiple XrdcMrcInstance in DS interface Detailed description (how to reproduce it): when configuring multiple XrdcMrcInstance in DS/EB interface, maximum number of the configured MCR incorrect. !image-2022-07-14-06-24-38-129.png! Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: NA Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA

ID	Subtype	Headline and Description
ARTD-29347	Bug	[Port] Validation error due to missing RecommendedConfiguration Detailed description (how to reproduce it): There is reported the following error while running the bswmd file validations in third party Autosar configuration tool: Constr_4046-In a BswImplementation <BswImplementation_0> the reference RecommendedConfigurations containing EcucModuleConfigurationValues <>, the reference implementConfigVariant is empty or NULL.[Infos] <BswImplementation_0> : </Port_TS_T40D34M20I0R0/Implementations/BswImplementation_0>,<> : </Port/Port>, ERROR,S32K344_Integration_example,paramdef/bswmd_static/Port_Bswmd_original.arxml The error is reported because there is the following reference to recommended configuration: <RECOMMENDED-CONFIGURATION-REF DEST="ECUC-MODULE-CONFIGURATION-VALUES">/Port/Port</RECOMMENDED-CONFIGURATION-REF> But there is no recommended configuration available in RTD package in Autosar format (only in Tresos proprietary one in Port_TS_T40D34M20I0R0\config_ext\PortRecConfiguration_JtagPins.xdm). Preconditions: Using third party configuration editor (not Tresos) Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Error reported during validation of bswmd file Expected behavior: No error reported during validation of bswmd file Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Add the recommended configuration in Autosar format. For now we have resolved the issue by deleting the reference from Port bswmd file, i.e. removing this line from Port_Bswmd.arxml file: <RECOMMENDED-CONFIGURATION-REF DEST="ECUC-MODULE-CONFIGURATION-VALUES">/Port/Port</RECOMMENDED-CONFIGURATION-REF> So it looks as follows: !port_recommended_config_reference.png!
ARTD-29422	Bug	[S32K396 3.0.0 CD02] UART: Fix build warning example Detailed description (how to reproduce it): When build example with EB tresos have some warning !image-2022-07-28-13-30-46-619.png! Preconditions: Warning by Os and Base module Test Case ID (internal TC that caught the defect) optional: Uart_Example_S32K396 Observed behavior: Build with warning Expected behavior: Build with no warning Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A

ID	Subtype	Headline and Description
ARTD-30157	Bug	[Pins Tool] Missing input/output direction and initValue for GPIO signals Detailed description (how to reproduce it): [Pins Tool] Configure gpio mode, choose direction Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: 1. Missing Input/Output for GPIO signal 2. Missing initValue for both Input and Input/Output direction of GPIO signal Expected behavior: Can configure Input/Output direction for gpio signal Can configure initvalue for both Input and Input/Output direction of GPIO signal Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Correct .def file > input/output mode Correct CPU.ginc > initValue for input/output and input of gpio Correct pin_code_gen.js > generate .initValue for input direction
ARTD-32371	New Feature	[CRYPTO] Clear internal buffer in Crypto_Hse_ExportSymPrivAsymPub after usage NewWorkDescription: Finding during the security review: The internal buffer used inside Crypto_Hse_ExportSymPrivAsymPub() shall be cleared after the key data has been copied to the buffer provided by the caller. Requirement source: Security (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Clear Crypto_xContainer.aKey after usage. !image-2022-08-12-11-05-51-218.png!
ARTD-32377	New Feature	[CRYPTO] Add a recommendation in driver manuals for CryptoDevErrorDetect NewWorkDescription: Finding during security analysis: Add a warning in the user manual that turning off the parameters CryptoDevErrorDetect and HseIpDevErrorDetect Is not recommended from a security point of view. Only for CryptoDevErrorDetect a recommendation should be added as HseIpDevErrorDetect will result in an infinite loop if an error is detected and should be used only for development. Requirement source: Security (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Add a note in the driver manuals to encourage the user to leave the CryptoDevErrorDetect enabled as the security expert advised.
ARTD-32380	New Feature	[CRYPTO][UM] Fill the precondition field with information NewWorkDescription: The recommendation from the security analysis is to fill Precondition field even for no precondition required. In the function references in the user manual, put “None” in the Precondition field if there really are no preconditions. Requirement source: Security (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Analyze what is the preconditions and fill the precondition filed: !image-2022-08-12-12-06-32-011.png!

ID	Subtype	Headline and Description

ARTD-34371	Bug	[RTE] Protected areas fail to resume all interrupts
		
		Detailed description (how to reproduce it):
		[
		
		XPSR.I = 0 (global interrupts enabled)
		
		Enter_50()
		msr_ETH_EXCLUSIVE_AREA_50 = 0
		
		Interrupt !HERE! see in code excerpt below
		
		Enter_51()
		msr_ETH_EXCLUSIVE_AREA_51 = 0
		OsIf_SuspendAllInterrupts > XPSR.I = 1
		
		Enter_50()
		msr_ETH_EXCLUSIVE_AREA_50 = 1 (overwrites value above !)
		
		Exit_50
		XPSR.I not changed XPSR.I = 1
		
		Exit_51
		XPSR.I = 0
		
		continues Enter_50()
		OsIf_SuspendAllInterrupts > XPSR.I = 1 but in this state the msr_ETH_EXCLUSIVE_AREA_50 has wrong value 1
		
		Exit_50
		Sees that the interrupt was not disabled by Enter_50 so no reason to restore it and kept unintentionally disabled
		
		void SchM_Enter_Eth_43_PFE_ETH_EXCLUSIVE_AREA_50(void)
		{
		uint32 u32CoreId = (uint32)OsIf_GetCoreID(); if(0UL == reentry_guard_ETH_EXCLUSIVE_AREA_50[u32CoreId])
		{
		#if (defined MCAL_ENABLE_USER_MODE_SUPPORT)
		msr_ETH_EXCLUSIVE_AREA_50[u32CoreId] = OsIf_Trusted_Call_Return(Eth_43_PFE_schm_read_msr);
		#else
		msr_ETH_EXCLUSIVE_AREA_50[u32CoreId] = Eth_43_PFE_schm_read_msr(); /*read MSR (to store interrupts state)*/
		#endif / MCAL_ENABLE_USER_MODE_SUPPORT /
		if (ISR_ON(msr_ETH_EXCLUSIVE_AREA_50[u32CoreId])) /*if MSR[EE] = 0, skip calling Suspend/Resume AllInterrupts*/
		{
		/
		!HERE! INTERRUPT HERE CAUSES GLOBAL INTERRUPT (XPSR.I bit) TO BE DISABLED FOREVER
		/
		OsIf_SuspendAllInterrupts();
		#ifdef ARM_DS5_C_S32XX
		ASM_KEYWORD(" nop ");/ Compiler fix forces the CSPID instruction to be generated with 02, Ospace are selected*/
		#endif
		}
		}
		reentry_guard_ETH_EXCLUSIVE_AREA_50[u32CoreId]++;
		}
		]
		
		Preconditions:
		[Main thread and interrupt]
		
		Test Case ID (internal TC that caught the defect) optional:
		[]
		
		Observed behavior:
		[global interrupt disabled on ARM v7M XPSR.I > 1 after exiting from protected areas]
		
		Expected behavior:
		[global interrupt enabled on ARM v7M XPSR.I > 0 after exiting from protected areas]
		
		Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)
		
		Proposed solution optional:
		[
		
		void SchM_Enter_Eth_43_PFE_ETH_EXCLUSIVE_AREA_50(void)
		{
		uint32 u32CoreId = (uint32)OsIf_GetCoreID();
		/ new local variable to preserve XPSR /
		uint32 msr;
		
		if(0UL == reentry_guard_ETH_EXCLUSIVE_AREA_49[u32CoreId])
		{
		#if (defined MCAL_ENABLE_USER_MODE_SUPPORT)
		msr = OsIf_Trusted_Call_Return(Eth_43_PFE_schm_read_msr);
		#else
		msr = Eth_43_PFE_schm_read_msr(); /*read MSR (to store interrupts state)*/
		#endif / MCAL_ENABLE_USER_MODE_SUPPORT /
		if (ISR_ON(msr)) /*if MSR[EE] = 0, skip calling Suspend/Resume AllInterrupts*/
		{
		OsIf_SuspendAllInterrupts();
		#ifdef ARM_DS5_C_S32XX
		ASM_KEYWORD(" nop ");/ Compiler fix forces the CSPID instruction to be generated with 02, Ospace are selected*/
		#endif
		}
		/ preserved global XSPR should be updated after the global interrupt is disabled /
		msr_ETH_EXCLUSIVE_AREA_50[u32CoreId] = msr;
		}
		reentry_guard_ETH_EXCLUSIVE_AREA_50[u32CoreId]++;
		}

ID	Subtype	Headline and Description
ARTD-34417	Bug	[UART] LPUART baudrate capped @2Mbps in config, k344 capable of up to 5Mbps Customer claims the configuration component for LPUART and UART modules limits the maximum baudrate to 2Mpps. This is well below the 5Mbps that the K344 device is capable of. Please provide an intermediate workaround for this limitation until it is fixed.
ARTD-35078	Bug	[BASE] EXECUTE_WAIT macro shall not resume/suspend all interrupts Detailed description (how to reproduce it): The EXECUTE_WAIT macro is implemented with calling resume and suspend all interrupts as follows: #define EXECUTE_WAIT() \ do \ { \ ResumeAllInterrupts(); \ ASM_KEYWORD(" wfi"); \ SuspendAllInterrupts(); \ } while (0) There is no reason to resume all interrupts since on ARM M4 core the wakeup happens even if all interrupts are disabled with PRIMASK. as per wfi instruction definition: ========== 3.10.12. WFI Wait For Interrupt. Syntax WFI\{cond} where: cond Is an optional condition code, see Conditional execution. Operation WFI is a hint instruction that suspends execution until one of the following events occurs: • a non-masked interrupt occurs and is taken • an interrupt masked by PRIMASK becomes pending • a Debug Entry request. ========== Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: N/A Expected behavior: No supend/resume of interrupts shall be implemented in EXECUTE_WAIT macro Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: The EXECUTE_WAIT macro shall be implemented as follows: #define EXECUTE_WAIT() ASM_KEYWORD(" wfi") The detail analysis is made for Coretex-m0, Coretex-m0+, Coretex-m3, Coretex-m4, Coretex-m7 and PPC e200z4 e200z0 e200z7 series (see attachments) Document attachment is showing us that all affected architecture have capability of wakeup even if interrupt is pending because all interrupt is disable. Conlusion that we need to remove ResumeAllInterrupts(); and SuspendAllInterrupts(); from implementation.

ID	Subtype	Headline and Description

ARTD-35079	New Feature	[SPI]Update code the SPI driver SW32K3_RTD_4_4_1_0_0 to perform transmit no gap
		
		NewWorkDescription:
		
		The customer expects when Spi transmits 37 bytes conservative no gaps occur.
		
		But with the present Spi driver, this function didn't support the Framesize > 255 or the Framesize < 4
		To SPI transmit no gap with a frame size greater than 255 or frame size is an odd number smaller than 4, Spi driver needs to update as below:
		# File Lpspi_Ip.hChange the Lpspi_Ip_StatusType Lpspi_Ip_UpdateFrameSize(const Lpspi_Ip_ExternalDeviceType ExternalDevice, uint8 FrameSize);to Lpspi_Ip_StatusType Lpspi_Ip_UpdateFrameSize(const Lpspi_Ip_ExternalDeviceType ExternalDevice, uint16 FrameSize);
		# File Lpspi_Ip_Types.h
		Change:
		typedef struct
		{
		uint8 FrameSize; /**< Frame size configured /
		boolean Lsb; /**< Transfer LSB first or MSB first /
		uint32 DefaultData; /**< Default data to send when TxBuffer is NULL_PTR /
		#if (STD_ON == LPSPI_IP_HALF_DUPLEX_MODE_SUPPORT)
		Lpspi_Ip_HalfDuplexType TransferType; /**< TransferType /
		#endif }
		Lpspi_Ip_DeviceParamsType;
		
		To:
		typedef struct
		
		{
		*uint16 FrameSize; /**< Frame size configured /
		boolean Lsb; /**< Transfer LSB first or MSB first /
		uint32 DefaultData; /**< Default data to send when TxBuffer is NULL_PTR /
		#if (STD_ON == LPSPI_IP_HALF_DUPLEX_MODE_SUPPORT)
		Lpspi_Ip_HalfDuplexType TransferType; /**< TransferType /
		#endif
		}
		
		Lpspi_Ip_DeviceParamsType;
		
		3. File Lpspi_Ip.c
		3.1: Change Lpspi_Ip_StatusType Lpspi_Ip_UpdateFrameSize(const Lpspi_Ip_ExternalDeviceType ExternalDevice, uint8 FrameSize) to Lpspi_Ip_StatusType Lpspi_Ip_UpdateFrameSize(const Lpspi_Ip_ExternalDeviceType ExternalDevice, uint16 FrameSize).
		
		3.2: Change a code part in the static void Lpspi_TransmitTxInit(uint8 Instance, uint8 TxBuffer, uint16 NumberOfFrames) function as below:
		else if (State->ExternalDevice->DeviceParams->FrameSize < 17u)
		{
		if ((NumberOfFrames%2u) == 0)
		
		{ State->ExpectedFifoWrites = NumberOfFrames/2u; }
		
		else
		
		{ State->ExpectedFifoWrites = NumberOfFrames/2u 1u; }
		
		}
		else
		{
		if ((NumberOfFrames%4u) == 0)
		
		{ State->ExpectedFifoWrites = NumberOfFrames/4u; }
		
		else
		
		{ State->ExpectedFifoWrites = NumberOfFrames/4u 1u; }
		
		}
		
		3.3: Change a code part in the static void Lpspi_TransmitRxInit(uint8 Instance, uint8 TxBuffer, uint16 NumberOfFrames) function as below:
		else if (State->ExternalDevice->DeviceParams->FrameSize< 17u)
		{
		if ((NumberOfFrames%2u) == 0)
		
		{ State->ExpectedFifoReads = NumberOfFrames/2u; }
		
		else
		
		{ State->ExpectedFifoReads = NumberOfFrames/2u 1u; }
		
		}
		else
		{
		if ((NumberOfFrames%4u) == 0)
		
		{ State->ExpectedFifoReads = NumberOfFrames/4u; }
		
		else

ID	Subtype	Headline and Description
ARTD-37507	Bug	[CRYPTO] PBKDF2 iterations limitation Detailed description (how to reproduce it): The PBKDF2 service is using a 8 bit value for the iterations thus limiting the number of iterations as HSE provides a 32bit range. !image-2022-08-30-10-45-42-135.png! !image-2022-08-30-10-46-27-665.png! Preconditions: The number of iterations is bigger than 255. Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: The number of iterations can not be set over 255. Expected behavior: The number of iterations should be on 32bit value Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [^0001-Use-32bit-variable-to-save-iteration-count.patch]
ARTD-37573	Bug	[eth][netc] Timestamp is not working properly when interrupts are enabled Detailed description (how to reproduce it): Use timestamp with interrupts, transmitted frames will have problems at confirmation phase. Preconditions: None. Test Case ID (internal TC that caught the defect) optional: EthSwt_netc_TC_303 Observed behavior: Problems at TX confirmation of management frames. Expected behavior: TX of management frames to work properly with interrupts Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: TX requests for management (timestamping) frames are to be properly registered on PSI0 FIFO0, while keeping track of their requests on the initial FIFOs. If a message is to be sent from PSI0, low-level resources should be reserved on both the initial FIFO and on FIFO0. If the message is a normal frame, the resources of FIFO0 are freed, otherwise, the ones of the initial FIFO are freed, which can be done upon calling the IPW-level Transmit function. The transmit function can also remove requests from the initial FIFO and create them properly on FIFO0's queue when enqueueing management frames. When this is done, management frames are effectively moved from their initial FIFO to FIFO0 on all levels. The only information that needs to be maintained is their buffer IDs as the high-level application has no knowledge of this move. Ensuring the unicity of buffer IDs becomes mandatory, and it can be done by maintaining and using offsets. In order to be accessible to the high-level application, packets on FIFO0 have to keep track the buffer ID of their counterparts on their initial FIFOs. Test EthSwt_Netc_TS_302 (TC_303) uses polling. To verify the functionality when using interrupts, a new testing case has to be introduced.

ID	Subtype	Headline and Description
ARTD-38119	Bug	[GMAC][SAF85xx] Fatal Bus Error detected when receiving Eth frame at high throughput Detailed description (how to reproduce it): Ensure RFE firmware available since RFE_PLL needed then load and run provided elf file for cortex-A53. On Ubuntu machine: Open serial terminal to communicate with the board, for eg: python m serial.tools.miniterm raw <USB port> 115200 These message should display (type Enter if not): !image-2022-09-10-22-09-28-232.png|width=543,height=58! Then, type zperf udp download and Enter: !image-2022-09-10-22-10-35-289.png|width=396,height=189! Open another terminal on the machine and type: iperf c 192.0.2.3 u l 1470 b 200M Wait until this message is appeared: !image-2022-09-10-22-40-58-663.png|width=687,height=186! Checking DMA_CH0_Status register: !image-2022-09-10-22-14-13-830.png|width=638,height=137! Preconditions: Board X-STRX-DIGSKT-V1: Ensure PHY AR8033 is connected Ensure UART can be used to communicate with other devices (for e.g over microUSB port on board). Ubuntu machine: There is at least one unused ethernet port on Ubuntu machine which can be used to connect to the board. Download and install iperf 2.0.5. Download/install a software (for e.g [pyserial|https://pypi.org/project/pyserial/]) for UART communication between board and the machine Connect the ethernet port with RJ45 port on the board. - Connect microUSB port on the board to USB port on the machine Test Case ID (internal TC that caught the defect) optional: Observed behavior: When receiving throughput big enough (for eg. 200 Mbps), a fatal bus error occurs on receive path. Source code under rx callback, basically just read a eth frame, provide the new buffer for GMAC driver and move frame to higher layer on network stack: !image-2022-09-10-22-18-11-885.png|width=493,height=287! Expected behavior: The error is not happen and the throughput can be measured, for eg with 100Mbps ({*}iperf c 192.0.2.3 u l 1470 b 100M{*}): !image-2022-09-10-22-42-15-619.png|width=607,height=167! Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]

ID	Subtype	Headline and Description
ARTD-38961	Bug	Crypto: Short name field in ECPD file incorrect Detailed description (how to reproduce it): Short name field in ECPD file incorrect lead to cannot import ECVD file CT to EB Can see detail bellow attach file Test Case ID (internal TC that caught the defect) optional: Crypto_TS_COT_007, Crypto_TS_COT_008 Observed behavior: <SHORT-NAME>TS_T31D53M9I0R0</SHORT-NAME> => it should be <SHORT-NAME>Crypto_43_HSE_TS_T31D53M9I0R0</SHORT-NAME> <SHORT-NAME>Crypto_43_HSE</SHORT-NAME> => it should be <SHORT-NAME>Crypto</SHORT-NAME> Expected behavior: Can import ECVD file CT to EB without error Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-39645	Bug	[PWM][FLEXPWM] Spikes pulses occur when driver is initialized Detailed description (how to reproduce it): Following configuration for the related output: PwmChannelClass: PWM_VARIABLE_PERIOD PwmHwChannel: FLEX PWM1_X[3], PWM1_X[1], PWM1_X[0] PwmDutyCycleDefault: 0x0000 (0%) PwmSignal: FLEXPWM_IP_EDGE_ALIGNED Issue 1: In FlexPwm_Ip_Init function, after passing the FlexPwm_Ip_SetOutputEnHw function, a period is always created, then output signal returns the correct output level HIGH or LOW as desired Issue 2: When init channel or call set duty function with duty 0%, spikes pulse happen continuously Preconditions: Call Pwm_Init with: HwChannel: FlexPwm channel X DutyCycle: 0% Polarity: HIGH or LOW.(Can using config file in attach file) Test Case ID (internal TC that caught the defect) optional: Pwm_TC_FCT_0239 Observed behavior: 1 Period still generated when init with duty 0% Expected behavior: when init with duty 0% or 100%, no edge is generated Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-41737	New Feature	[IMPLEMENTATION] [ETH] Add support for internal buffers placed in cacheable memory sections NewWorkDescription: The Eth driver shall support allocating the internal buffers in cacheable memory spaces. This will mean adding invalidate and flush operations in the Eth driver to ensure correct sending and receiving data Requirement source: TCP/IP, stacks, zephyr teams (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-41528	Bug	[Crc] Crc_Ip_ProtocolType is not same with structure name in CDD_CRC_016 Detailed description (how to reproduce it): Crc_Ip_ProtocolType is used in driver code, not Crc_ProtocolType !image-2022-10-11-17-44-13-139.png|thumbnail! Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: NA Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Correct name this structure
ARTD-42429	Bug	[ETH][GMAC] - Mismatch between code and requirements Detailed description (how to reproduce it): A structure named Gmac_Ip_ConfigType shall define the GMAC module configuration structure. It shall have the following definition: typedef struct { uint8 rxRingCount; /{*}!< The number of Receive rings to be used by the driver. / uint8 txRingCount; /*!< The number of Transmit rings to be used by the driver. / uint32 interrupts; / {*}!< General interrupt sources. A logical OR of "Gmac_Ip_InterruptType". / Gmac_Ip_CallbackType callback; /*!< Callback function {*}/ uint16 maxFrameLen; /{*}!< Maximum frame length. / Gmac_Ip_MiiModeType miiMode; /*! < MII mode. / / MAC configuration {*}/ Gmac_Ip_SpeedType speed; /{*}!< Speed. / Gmac_Ip_DuplexType duplex; /*!< Duplex. {*}/ uint32 macConfig; /{*}!< Configures the operating mode of the MAC. A logical OR of "Gmac_Ip_MacConfigType". / uint32 macPktFilterConfig; /*!< Configures the MAC packet filter. A logical OR of "Gmac_Ip_PacketFiletConfigType". / } Gmac_Ip_ConfigType; GMAC_IP_010_001 A structure named Gmac_Ip_BufferConfigType shall define the GMAC buffer descriptors ring configuration structure. It shall have the following definition: typedef struct \{ uint16 ringSize; /*!< Buffer descriptors number. / Gmac_Ip_BufferDescriptorType ringDesc; /*!< Buffer descriptor ring start address. / uint32 interrupts; /*!< Channel interrupt sources. A logical OR of "Gmac_Ip_ChInterruptType". / Gmac_Ip_ChCallbackType callback; /*!< Callback function for current channel. / uint8 rxBuffer; /*!< Receive data buffers start address only used for receive channels. / } Gmac_Ip_BufferConfigType; GMAC_IP_076_001|An enumeration named Gmac_Ip_StatusType shall indicate GMAC's status. It shall have the following definition: typedef enum{ / GMAC specific error codes / GMAC_STATUS_SUCCESS = E_OK, GMAC_STATUS_ERROR = E_NOT_OK, GMAC_STATUS_BUSY, GMAC_STATUS_TIMEOUT } Gmac_Ip_StatusType; Preconditions: Test Case ID (internal TC that caught the defect) optional: Observed behavior: In code, there are some extra parameters which need to be added also in the requirement text. Expected behavior: Update requirement to match the code. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-47207	New Feature	[IMPLEMENTATION] [CPTD][ETH] Add Scatter/Gather Support for GMAC and other ETH IP NewWorkDescription: The RTD Ethernet driver shall expose a S/G API in parallel with the AUTOSAR API. Requirement source: [...]Technical community (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-43322	New Feature	[SPI] LSPI Sequences transfer improvement - implementation part 1 NewWorkDescription: See description AAI-1162 [SPI] SPI Sequences transfer improvement NXP Jira Cloned from AAI to track in ARTD Add a user manual chapter describing the feature Requirement source: AAI-1162 [SPI] SPI Sequences transfer improvement NXP Jira Proposed solution optional: [....]
ARTD-43566	New Feature	[FlexIO I2C][S32K3] Reduce the ISR tasks of FlexIO I2C DMA mode. Detailed description (how to reproduce it): Customer Xiaomi and Desay are using FlexIO I2C in their system. DMA mode of FlexIO I2C is required to reduce FlexIO I2C affecting other tasks. But even though we configure the FlexIO I2C work in DMA mode, there are still some critical ISRs to execute some jobs as follow lists: DMA ISR: {*}Flexio_I2c_Ip_MasterEndDmaTransfer{*}() FlexIO ISR: {*}Flexio_I2c_Ip_TimerEventHandler{*}() These two functions are very critical that they MUST be done very timely and CANNOT be delayed, blocked or interrupted for very long. However, customer's system is complicated and has a lot of tasks called by OS, ISR, etc. Therefore these critical jobs of FlexIO I2C are very easy to be blocked or interrupted for a long while. Because of this, the FlexIO I2C has very serious function degraded and cannot work in in their system. We suggest that these two function should be done by DMA scatter-gather mode, not by CPU in ISRs. We AE had build a temporary code by modifying FlexIO I2C driver code for customer use. You can find the Flexio_I2c_Ip_Temp.c and a example project, which shows you how to configure and use the temporary code, in the attachment. A screenshot of Flexio_I2c_Ip_Temp.c: !image-2022-10-26-15-16-44-807.png! Note: DMA ISR: {*}Flexio_I2c_Ip_MasterEndDmaTransfer{*}() was fixed by the temporary code, but FlexIO ISR: {*}Flexio_I2c_Ip_TimerEventHandler{*}() is not included in it. We suggested customer to send less than 13 bytes to avoid Flexio_I2c_Ip_TimerEventHandler() being called during transmission. But it also need to be fixed. Preconditions: See description Test Case ID (internal TC that caught the defect) optional: None Observed behavior: See description Expected behavior: See description Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: We suggest that these two function should be done by DMA scatter-gather mode, not by CPU in ISRs.
ARTD-43572	New Feature	[SPI] LSPI Sequences transfer improvement - dev tests NewWorkDescription: See description [AAI-1162] [SPI] SPI Sequences transfer improvement NXP Jira Cloned from AAI to track in ARTD Requirement source: [AAI-1162] [SPI] SPI Sequences transfer improvement NXP Jira Proposed solution optional: [....]

ID	Subtype	Headline and Description
ARTD-44020	New Feature	[mem_eep] Create Driver for the uSDHC IP NewWorkDescription: Add support for mem_eep, on the uSDHC/eMMC according to ASR 21-11 Requirement source: AUTOSAR_SWS_MemoryDriver.pdf (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Create Mem_Eep Driver
ARTD-44882	Bug	[S32M24x][i2s] I2s_AbortTransmit set all txRemainingWords and rxRemainingWords to 0 Detailed description (how to reproduce it): This issue found on FLEXIO and this is test scenario: !image-2022-11-14-14-21-29-422.png|width=822,height=312! Tester calls Abort function when byteRemainingCount is 54 (T_I2S_BUFFER_SIZE 10). Affter calling Abort function, tester calls getStatus function and driver is in ABORT_STATUS and expecting that remainingByte shoube <= 54. Actually, getStatus returns remainingByte = 0. This is incorrect. I checked data transmitted to MAF, it's extract 10 bytes. This means remainingByte must be 54. !image-2022-11-14-14-31-15-656.png|width=441,height=213! {*}[16/Dec/2022]{*}After verified on the label PVT_I2S_ARTD_45255 (provided by dev to fix bug), It still has issue as below: !image-2022-12-16-15-54-36-807.png|width=1122,height=565! Abort function is call when remainning words = 53, and status changed to ABORT, but when call GetStatus function and then in MasterGetStatus which shown in above figure. because IsChannelIde = TRUE, RemainWord still = 0 because line 1344 can not be in. This leads BytesRemaining = 0. This means all words were transmitted when call GetStatus function. Preconditions: Calling Abort in middle of transmission. Using FLEXIO. Test Case ID (internal TC that caught the defect) optional: I2s_TC_FCT_1001 Observed behavior: NA Expected behavior: NA Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Abort function is calling Flexio_I2s_Ip_MasterEndTransfer and Flexio_I2s_Ip_MasterEndTransfer sets all value to 0. This causes remaining byte is 0 after calling Abort function: !image-2022-11-14-14-34-36-812.png|width=494,height=185!
ARTD-45917	Bug	[CAN] The bswmd for CAN is generated with infix Can_43_FLEXCAN_Bswmd.arxml while the signing list file is looking for Can_Bswmd.arxml Detailed description (how to reproduce it): [The bwmd for CAN is generated with infix Can_43_FLEXCAN_Bswmd.arxml while the signing list file is looking for Can_Bswmd.arxml] Preconditions: [The bwmd is enabled in release build plan] Test Case ID (internal TC that caught the defect) optional: [ ] Observed behavior: [The bwmd for CAN is generated Can_Bswmd.arxml] Expected behavior: [The bwmd for CAN is generated with infix Can_43_FLEXCAN_Bswmd.arxml] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]

ID	Subtype	Headline and Description
ARTD-46562	Bug	[SENT][S32K3] Calibration error is raised when getting mesage in the second time of calling function Detailed description (how to reproduce it): Sent_GetFastMsgData called in the 1st time to get available message in channel 0, 1. After that, close MAF and call Sent_StopChannelReceiving to stop messgae from channel 0, 1. !image-2022-12-06-14-41-01-825.png|width=642,height=376! And then call Sent_GetFastMsgData again to get available message in channel 2, 3. In this time. In this time, Calibration error flags was raised for channel 0 and 1 as below figure: !image-2022-12-06-14-41-21-130.png|width=641,height=298! Root cause: Sent_GetFastMsgData bases on interrupt handler from flexio timer. So after calling in the first time of this function to get message from channel 0, 1 (Message transmit to channel 0, 1 only). Some frame still transmitted to mcu and raised flag in TIMSTAT for channel 0, 1(TIMSTAT=0x3). In the second time of calling Sent_GetFastMsgData for channel 2 and 3 (Message transmit to channel 2, 3 only). Because TIMSTAT has not clear, an interrupt handler happened right after calling Sent_GetFastMsgData for channel 0 and 1. This issue leads unexpected message is detected and some error was raised, in this case driver reported Calibration Pulse Error. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: Sent_TS_018 Observed behavior: NA Expected behavior: No error flag was raised. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: TIMSTAT should be clear in Sent_StartChannelReceiving/ Sent_StopChannelReceiving function. OR before of calling get message (Sent_GetSerialChannelMsgData / Sent_GetFastChannelMsgData / Sent_GetFastMsgData/ Sent_GetSerialMsgData)
ARTD-46641	Bug	[LIN] function Lin_SetClockMode should be supported infix in K3XX Detailed description (how to reproduce it): function Lin_SetClockMode should be support infix Preconditions: !image-2022-12-07-14-26-02-064.png! Test Case ID (internal TC that caught the defect) optional: Lin_TC_FCT_0101, Lin_TC_FCT_0100 Observed behavior: N/A Expected behavior: function Lin_SetClockMode should change Lin_43_LPUART_FLEXIO_SetClockMode to support infix Proposed solution optional: [....]

ID	Subtype	Headline and Description
ARTD-46739	Bug	[SPI][S32K3XX] With Flexio SpiShiftClockIdleLevel = HIGH, for SpiDataShiftEdge = LEADING, must to generate SHIFTCTLn using negedge of clock Detailed description (how to reproduce it): Spi Flexio has 4 combinations of (SpiShiftClockIdleLevel, SpiDataShiftEdge): (LOW, LEADING) is generated correctly as (TIMCFGn initial clock state is logic 0, SHIFTCTLn using posedge of clock) (LOW, TRAILING) is generated correctly as (TIMCFGn initial clock state is logic 0, SHIFTCTLn using negedge of clock) But (HIGH, LEADING) must be generated as (TIMCFGn initial clock state is logic 1, SHIFTCTLn using negedge of clock) And (HIGH, TRAILING) must be generated as (TIMCFGn initial clock state is logic 1, SHIFTCTLn using posedge of clock) Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Lpspi_Flexio_Ip_Transfer Example Observed behavior: Spi Flexio generated code for 2 cases are wrong. Expected behavior: Spi Flexio generated code are correct. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-46823	Bug	[Platform]SW32ZE_RTD_R21-11_0.9.0_P01: Issues with VERSION INFORMATION of Platform Detailed description (how to reproduce it): According to AUTOSAR_SWS_BSWGeneral.pdf, the version information is defined like <MIP>_VENDOR_ID (see attached Published_Information.png) with MIP being <Ma>[_<vi>_<ai>] (see MIP_Define.png). The problem is that the Module abbreviation "Platform" is reserved for Platform Types (see Module_List.png). The defines like PLATFORM_VENDOR_ID PLATFORM_AR_RELEASE_MAJOR_VERSION are reserved for the PlatformTypes.h file (generate file). But in the MCAL, the CDD Platform uses these macros to define its version information. This can lead to redefinitions. !image-2022-12-09-14-42-03-929.png! !image-2022-12-09-14-46-12-880.png! !image-2022-12-09-14-46-45-077.png! Preconditions: #define PLATFORM_VENDOR_ID 43 #define PLATFORM_AR_RELEASE_MAJOR_VERSION 4 #define PLATFORM_AR_RELEASE_MINOR_VERSION 7 #define PLATFORM_AR_RELEASE_REVISION_VERSION 0 #define PLATFORM_SW_MAJOR_VERSION 0 #define PLATFORM_SW_MINOR_VERSION 9 #define PLATFORM_SW_PATCH_VERSION 0 Test Case ID (internal TC that caught the defect) optional: None Observed behavior: #define PLATFORM_TYPES_VENDOR_ID 43 #define PLATFORM_TYPES_AR_RELEASE_MAJOR_VERSION 4 #define PLATFORM_TYPES_AR_RELEASE_MINOR_VERSION 7 #define PLATFORM_TYPES_AR_RELEASE_REVISION_VERSION 0 #define PLATFORM_TYPES_SW_MAJOR_VERSION 0 #define PLATFORM_TYPES_SW_MINOR_VERSION 9 #define PLATFORM_TYPES_SW_PATCH_VERSION 0 Expected behavior: as Preconditions Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: as Preconditions

ID	Subtype	Headline and Description
ARTD-46826	New Feature	[PWM][Emios_Ip] Fast PWM update API CR description: There were couple of attempts to improve execution time of existing functions [ARTD-14125, ARTD-14126, ARTD-23704, ARTD-23705]. It doesn't seem to be possible to merge fast execution and high level of abstraction and complexity in the same set of functions. I would propose to keep existing functions for users which prefer universal functions with higher level of abstraction and add new functions for users who need fast PWM update. Adding new functions for drivers (as was discussed during the meeting 28 September. Attendees Radu-Andrei Brasoveanu, Ioana-Andreea Pocea, Mihai Morarescu, Cosmin Gabriel Dinu, Tomas Fedor) : Supported emios modes OPWMB, OPWMCB, MCB Low level drivers: Emios_Pwm_Ip_SetUCRegA Emios_Pwm_Ip_SetUCRegB Emios_Mcl_Ip_ComparatorTransferEnable Emios_Mcl_Ip_ComparatorTransferDisable MCAL drivers: Pwm_SetUCRegA Pwm_SetUCRegB Pwm_ComparatorTransferEnable Pwm_ComparatorTransferDisable Example of use : ComparatorTransferDisable (Disable update of selected channels) SetUCRegA (Update new period value for channel operating in MCB (timebase)) SetUCRegA (Update new value for channel operating in OPWMB or OPWMCB) SetUCRegB (Update new value for channel operating in OPWMB) ComparatorTransferEnable (Enable update of selected channels. All new values will be applied on nearest reload) Reason for this change: Execution time of the PWM update using RTD drivers is too long for motor control use cases. Typical emios modes are MCB for Timebase and OPWMB for PWM channel. Registers to access A,B, OUDIS. Following API was used during the test (typical case for PWM update of one channel during the motor control) . Low level API: Emios_Pwm_Ip_ComparatorTransferDisable Emios_Pwm_Ip_SetPhaseShift Emios_Pwm_Ip_SetDutyCycle Emios_Pwm_Ip_ComparatorTransferEnable MCAL API: Pwm_SetDutyPhaseShift Pwm_SyncUpdate APIs are general and support multiple eMIOS modes which requires decisions inside function calling translated to "switch" statements. APIs involve hierarchy of cascade calling of multiple functions. APIs involve exclusive areas which can be disabled for entire driver only and not independently per channel. all mentioned above brings overhead in the execution time. M7 160MHz, execution from TCM, RTD 2.0.0 Low level API: Emios_Pwm_Ip_ComparatorTransferDisable 0.38125us Emios_Pwm_Ip_SetPhaseShift 0.925 us Emios_Pwm_Ip_SetDutyCycle 1.075 us Emios_Pwm_Ip_ComparatorTransferEnable 0.375 MCAL API: Pwm_SetDutyPhaseShift 3us Pwm_SyncUpdate 1.9125 If we look at one of the most complex use case, 12 phase motor control, where we need to update 12 emios channels 160MHz 120Hz (K312) Low level API 24.76us 33.01us MCAL API 37.91us 50.55us It enormous time for updating 12xA 12xB 2xOUDIS = 26 register writes. Benefit: Wider free fpace for user calculations/algorithms will put S32K3 and S32M27 into better position. LCU peripheral was modified during K3 development to cover 12 phase usecase so it shouldn't be masked by execution time. Use-case: Motor control area. HW/Application Engineer contact (as applies): Tomas Fedor tomas.fedor@nxp.com Feel free to invite me to a meeting if more clarification is needed.

ID	Subtype	Headline and Description
ARTD-46829	New Feature	[icu] s32k3 RTD EMIOS ICU with DMA The DMA is supported by RTD MCAL module ICU but it's not supported by the RTD lower-level module Emios_Icu_Ip. 1) The generated code "Emios_Icu_Ip_xxxx_PBcfg.c": eMios_Icu_Ip_ChannelConfigType structure has only "EMIOS_ICU_MODE_WITHOUT_DMA", and it's not possible to set "EMIOS_ICU_MODE_WITH_DMA" in the Emios_Icu_Ip configuration. 2) In the generated code "Emios_Icu_Ip_Defines.h" No configurtion option to set "EMIOS_ICU_IP_TIMESTAMP_USES_DMA" to be STD_ON. Is it possbile to allow the configuration tool to set the above options, so that user can use lower level API to implement Emios_Icu with DMA support? Regards, Jason Yang
ARTD-46840	Bug	[[BASE] Test ECVD fail BaseNXP not matching between EB and CT Detailed description (how to reproduce it): Step 1: clean generate Base_TS_COT_105 CFG_SETS = s32k358_mqfp172 Step 2: Compare all files in original_configuration folder with new_configuration folder Preconditions: NA Test Case ID (internal TC that caught the defect) optional: Base_TC_COT_0001 Observed behavior: BaseNxp.ecpd not matching between EB and CT !ecvd_bug1.png|thumbnail! Expected behavior: BaseNxp.ecpd match between EB and CT Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-46878	Bug	[I2c] Fix Misra violations for K3 platform Detailed description (how to reproduce it): Fix all violations for MISRA. !image-2022-12-11-13-14-43-402.png! Reference : MISRA Deviation List: [https://bitbucket.sw.nxp.com/projects/ASPA/repos/real_time_drivers/browse/Generic/SW%20Development/RTD%20MISRA%20Deviations.xlsx] [https://confluence.sw.nxp.com/pages/viewpage.action?pageId=133734230] Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Undocumented misra violations. Expected behavior: Only accepted misra deviations remain in the report Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA

ID	Subtype	Headline and Description
ARTD-47165	Bug	[MemAcc] Wrong InstanceId report in Det Detailed description (how to reproduce it): Driver is using AreaId to report errors as InstanceId in Det report. it is incorrect becasue Actually, MemAcc is only one instance. !image-2022-12-14-14-01-28-886.png|thumbnail! !image-2022-12-14-14-01-47-226.png|thumbnail! Preconditions: Enable dev error detect Test Case ID (internal TC that caught the defect) optional: MemAcc_TC_FCT_0005.c Observed behavior: N/A Expected behavior: N/A Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-47200	Bug	[LIN] - Build errors caused by Linif APIs when no slave is configured. Detailed description (how to reproduce it): As per Autosar Specification the below mentioned APIs will be enabled only if we configure Node Type as “Slave”. • LinIf_LinErrorIndication • LinIf_HeaderIndication • LinIf_RxIndication • LinIf_TxConfirmation However, with current LIN/LLCE LIN implementation, those functions are invoked without any pre-condition, and will be verified during runtime to decide whether it's a slave node or not. As a result, in an application where those functions are disabled in LinIf if there is no slave node, we are getting Compilation Error with those APIs from driver. Preconditions: Test Case ID (internal TC that caught the defect) optional: Observed behavior: Lin driver fails at build step because the Linif APIs are not defined anywhere. Expected behavior: Lin driver shall pass when no slave is configured and LINIF driver does not implement the APIs. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Create a precompile macro to be used in guarding the linif function calls in lin driver.
ARTD-47404	New Feature	[mem_eep] Add support for the Mem_HwSpecificService API NewWorkDescription: Add support for mem_eep, on the uSDHC/eMMC according to ASR 21-11 Requirement source: AUTOSAR_SWS_MemoryDriver.pdf (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Add support for the Mem_HwSpecificService API

ID	Subtype	Headline and Description
ARTD-47510	New Feature	[IMPLEMENTATION][PORT] RTD driver memory resource reduction required by Brose NewWorkDescription: Implement RTD driver memory optimizations required by Brose. Implementation of Change Request AAI-1345 Compiler used: IAR Requirement source: Customer Request Proposed solution optional: Implement proposals agreed on change request, as per conclusions provided in ppt documents attached to current ticket and AAI-1345. More details available in tickets dedicated for memory optimizations analysis, cloned for each driver from ARTD-43887. Update driver UserManual, UML design and examples accordingly. If new requirements are created, run traceability to ensure the new requirements are covered. Attach to this ticket an xlsx document with memory size before and after optimizations.
ARTD-47516	New Feature	[ICU] RTD driver memory resource reduction required by Brose NewWorkDescription: Implement RTD driver memory optimizations required by Brose. Implementation of Change Request AAI-1345 Compiler used: IAR Requirement source: Customer Request Proposed solution optional: Implement proposals agreed on change request, as per conclusions provided in ppt documents attached to current ticket and AAI-1345. More details available in tickets dedicated for memory optimizations analysis, cloned for each driver from ARTD-43887. Update driver UserManual, UML design and examples accordingly. If new requirements are created, run traceability to ensure the new requirements are covered. Attach to this ticket an xlsx document with memory size before and after optimizations.
ARTD-47522	New Feature	[IMPLEMENTATION][PWM] RTD driver memory resource reduction required by Brose NewWorkDescription: Implement RTD driver memory optimizations required by Brose. Implementation of Change Request AAI-1345 Compiler used: IAR Requirement source: Customer Request Proposed solution optional: Implement proposals agreed on change request, as per conclusions provided in ppt documents attached to current ticket and AAI-1345. More details available in tickets dedicated for memory optimizations analysis, cloned for each driver from ARTD-43887. Update driver UserManual, UML design and examples accordingly. If new requirements are created, run traceability to ensure the new requirements are covered. Attach to this ticket an xlsx document with memory size before and after optimizations.

ID	Subtype	Headline and Description
ARTD-47525	New Feature	[FLS] RTD driver memory resource reduction required by Brose NewWorkDescription: Implement RTD driver memory optimizations required by Brose. Implementation of Change Request AAI-1345 Compiler used: IAR Requirement source: Customer Request Proposed solution optional: Implement proposals agreed on change request, as per conclusions provided in ppt documents attached to current ticket and AAI-1345. More details available in tickets dedicated for memory optimizations analysis, cloned for each driver from ARTD-43887. Update driver UserManual, UML design and examples accordingly. If new requirements are created, run traceability to ensure the new requirements are covered. Attach to this ticket an xlsx document with memory size before and after optimizations.
ARTD-47547	Bug	[LINIF] Fix compiler warning example HLD K3XX Detailed description (how to reproduce it): Run example HLD module LIN Preconditions: !image-2022-12-20-13-11-58-784.png! Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: build warning example Expected behavior: build no warning Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-47709	New Feature	[BASE]OSIF_COUNTER_DUMMY need to note in the RTD_BASE_UM Detailed description (how to reproduce it): OSIF_COUNTER_DUMMY needs to describe in detail in the user manual Preconditions: OSIF_COUNTER_DUMMY needs to describe in detail in the user manual Test Case ID (internal TC that caught the defect) optional: None Observed behavior: Missing description detail of OSIF_COUNTER_DUMMY Expected behavior: as Detailed description Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: as Detailed description

ID	Subtype	Headline and Description
ARTD-47931	Bug	[Eth][EMAC][GMAC] stuck in GMAC_CommonIRQHandler() when both common and Rx interrupts are enabled Detailed description (how to reproduce it): Using Zephyr BSP for S32R41 or SAF85xx, build and run samples/net/zperf in the target board, e.g. west build p auto b s32r418aaevb_a53 .\samples\net\zperf Run UDP test with high traffic load during an extended period of time, e.g. zephyr-shell$ zperf udp download host-shell$ iperf c 192.0.2.1 i 5 t 600 l 1470 u b 500M Alternatively, the issue can be reproducing flooding the board with ping requests, e.g. host-shell$ sudo ping f i 0 192.0.2.1 Preconditions: samples/net/zperf loaded to board, zperf server started in the board with "zperf udp download" in the case of UDP test. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: After some time, the board becomes unreachable. It seems that Zephyr is stuck servicing the common interrupt over and over again: !image-2022-12-22-17-03-47-382.png! The issue doesn't reproduce if the common interrupt is disabled and only the Rx interrupt is used. Giving different priorities to the common and Rx interrupt doesn't seem to have any effect. This issue can be reproduced for both GMAC (R41/SAF85xx) and EMAC (S32K344) drivers. Expected behavior: Common and Rx interrupts can be used together, as long as is a valid use-case. RTD Ethernet driver works under high load. Proposed solution optional: N/A
ARTD-48206	New Feature	[CRYPTO] Implement 5 redirection requirements (SWS_Crypto_00134; SWS_Crypto_00135; SWS_Crypto_00136; SWS_Crypto_00203 and SWS_Crypto_00204) NewWorkDescription: There are 5 redirection requirements (SWS_Crypto_00134; SWS_Crypto_00135; SWS_Crypto_00136; SWS_Crypto_00203 and SWS_Crypto_00204) are partially implemented. To perform and fully implemented for next release. Requirement source: NA Proposed solution optional: NA
ARTD-48276	New Feature	[ADC] Add guard for DSPSS functions by a check box if no DSPSS thread is used NewWorkDescription: Add guard for DSPSS functions by a check box if no DSPSS thread is used Requirement source: N/A Proposed solution optional: Add node and macro for un-used DSPSS thread
ARTD-48688	New Feature	[S32K3 3.0.0] Driver activities for Adc Drivers/IPs list in SOW: [see SOW for details|https://nxp1.sharepoint.com/:w:/r/sites/Zebra/_layouts/15/Doc.aspx?sourcedoc=%7B8DBBE9CD-33BA-4B0E-A2CB-688684283055%7D&file=SW32K3%20RTD%20ASR%204.4%20%26%20R21-11%203.0.0%20SOW.docx&action=default&mobileredirect=true]
ARTD-49627	New Feature	[S32K3 3.0.0] Driver activities for Spi Drivers/IPs list in SOW: [see SOW for details|https://nxp1.sharepoint.com/:w:/r/sites/Zebra/_layouts/15/Doc.aspx?sourcedoc=%7B8DBBE9CD-33BA-4B0E-A2CB-688684283055%7D&file=SW32K3%20RTD%20ASR%204.4%20%26%20R21-11%203.0.0%20SOW.docx&action=default&mobileredirect=true]
ARTD-50296	New Feature	[S32K3 3.0.0] Driver activities for gdu Drivers/IPs list in SOW: [see SOW for details|https://nxp1.sharepoint.com/:w:/r/sites/Zebra/_layouts/15/Doc.aspx?sourcedoc=%7B8DBBE9CD-33BA-4B0E-A2CB-688684283055%7D&file=SW32K3%20RTD%20ASR%204.4%20%26%20R21-11%203.0.0%20SOW.docx&action=default&mobileredirect=true]

ID	Subtype	Headline and Description
ARTD-50398	New Feature	[S32K3 3.0.0] Driver activities for i2s Drivers/IPs list in SOW: [see SOW for details|https://nxp1.sharepoint.com/:w:/r/sites/Zebra/_layouts/15/Doc.aspx?sourcedoc=%7B8DBBE9CD-33BA-4B0E-A2CB-688684283055%7D&file=SW32K3%20RTD%20ASR%204.4%20%26%20R21-11%203.0.0%20SOW.docx&action=default&mobileredirect=true]
ARTD-50703	Bug	[CAN] build fail / multicore + precompile / EBT / S32K396 Detailed description (how to reproduce it): build CAN_TS_MC_155 / s32K396 with enable multicore precompile Preconditions: S32K396 project / EBT enable multicore precompile Test Case ID (internal TC that caught the defect) optional: CAN_TS_MC_155 Observed behavior: !image-2022-12-27-10-51-27-726.png|thumbnail! [...] => Can_Config_EcucPartition_0 is generated without prefix (43_FLEXCAN) Expected behavior: no build-error Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-52505	New Feature	[UART] Pointer User config structure must be in the none cache area NewWorkDescription: This ticket was raised for IAD-1484 from iMx team Pointer User config structure must be in the none cache area #define UART_START_SEC_VAR_CLEARED_UNSPECIFIED_NO_CACHEABLE #include "Uart_MemMap.h" / brief User config structure. / const Lpuart_Uart_Ip_UserConfigType Lpuart_Uart_Ip_apUserConfig[LPUART_INSTANCE_COUNT]; #define UART_STOP_SEC_VAR_CLEARED_UNSPECIFIED_NO_CACHEABLE #include "Uart_MemMap.h" Requirement source: N/A (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: N/A

ID	Subtype	Headline and Description
ARTD-52508	Bug	[UART] The number of bytes remaining and the status of the channel do not match Detailed description (how to reproduce it): This issue was raised for: IAD-1504 ticket from iMx team Issue: Use the Uart_GetStatus function to read the transmission status and the remaining bytes of the channel: !screenshot-1.png|thumbnail! Check the return status T_UartStatus is UART_STATUS_NO_ERROR !screenshot-2.png|thumbnail! But the number of remaining bytes is not 0 !screenshot-3.png|thumbnail! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: N/A Expected behavior: Lpuart_Uart_Ip_GetReceiveStatus and Lpuart_Uart_Ip_GetTransmitStatus function need to use exclusive area to protect status checking and update the remaining bytes Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Lpuart_Uart_Ip_GetReceiveStatus and Lpuart_Uart_Ip_GetTransmitStatus function need to use exclusive area
ARTD-52741	Bug	[ADC] Compiler error due to missing prototype of Adc_Ipw_Adc0DmaTransferCompleteNotification Detailed description (how to reproduce it): Customer is using complex ADC use case with DMA (BCTU control mode) in which they configure their own notification function at the end of ADC DMA transfer (plus their own customized DMA channel setup). They do not configure Adc_Ipw_Adc0DmaTransferCompleteNotification in MCL but instead their own notification function. With this configuration there is reported the following compiler error: "C:\nxp\SW32K3_RTD_4.4_2.0.0\eclipse\plugins\Adc_TS_T40D34M20I0R0\src\Adc_Ipw_Irq.c",1872 Error[Pa045]: function "Adc_Ipw_Adc0DmaTransferCompleteNotification ".mcal_text"" has no prototype Preconditions: Using compiler option –require_prototypes Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Compiler error Expected behavior: No compiler error Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Add the missing Adc_Ipw_Adc0DmaTransferCompleteNotification function prototype
ARTD-52748	Bug	[UART] Not match number of instance between .xls file and RM on S32K396 Detailed description (how to reproduce it): In RM of S32K396, UART have 5 instances !image-2023-01-12-16-13-55-403.png! But in .xls of interrupt map, UART had 6 instances !image-2023-01-12-16-15-01-997.png! Preconditions: NA Test Case ID (internal TC that caught the defect) optional: Uart_TS_4001 Observed behavior: NA Expected behavior: NA Proposed solution optional:

ID	Subtype	Headline and Description
ARTD-52989	New Feature	[IMPLEMENTATION] Crypto driver cannot handle variables in TCM - part1 CR description: [return variables from crypto driver functions need to support variables in TCM, addressable via backdoor address] Reason for this change: [compatibility to upper SW layers using variables in stack / TCM. driver executes error when return variables are placed in TCM Crypto driver cannot handle variables in TCM , as it uses default frontdoor access address. Translation to backdoor addresss needed]
ARTD-53492	Bug	[CRYPTO] KeyGenerate service for symmetric keys does not set the aesBlockMode keyInfo param to 0x0 Detailed description (how to reproduce it): The code in the function Crypto_Hse_KeyGenerateRequest() does not set the aesBlockModeMask parameter in the keyInfo.specific structure to 0x0, in order for the key to be able to be used with any AES algomode. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: CRYPTO_TC_DVT_0114 in TS_003 dev test suite Observed behavior: N/A Expected behavior: The code in the function Crypto_Hse_KeyGenerateRequest() should set the aesBlockModeMask parameter in the keyInfo.specific structure to 0x0, in order for the key to be able to be used with any AES algomode. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Add in function Crypto_Hse_KeyGenerateRequest() from Crypto_Hse.c the set of the aesBlockModeMask parameter in the keyInfo.specific structure to 0x0, in order for the key to be able to be used with any AES algomode.
ARTD-53529	New Feature	[MemAcc] Implement Mem service invocation feature NewWorkDescription: Follow requirement: ECUC_MemAcc_00026: there are 3 way to call Mem services: DIRECT_STATIC INDIRECT_DYNAMIC INDIRECT_STATIC But currently driver only support DIRECT_STATIC. so need to support remaining ways Requirement source: ECUC_MemAcc_00026, SWS_MemAcc_00121, SWS_MemAcc_00122, SWS_MemAcc_00025, SWS_MemAcc_00111, SWS_MemAcc_00084, SWS_MemAcc_00085 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Base on requirements to update code to support. Function need to update: MemAcc_Init MemAcc_DeInit MemAcc_ActivateMem MemAcc_DeactivateMem MemAcc_MainFunction

ID	Subtype	Headline and Description
ARTD-54058	New Feature	[Platform] Disable TRM retry in startup code NewWorkDescription: TCM retry is disabled and software should disable the TCM retry bit at startup by programming the relevant core's CM7_ITCMCR[RETEN] and CM7_DTCMR[RETEN] fields to disable state. In S32K3 Cortex M7, by default, those bits are not disabled: !image-2023-01-30-15-57-40-738.png! Requirement source: S32K3XX Reference Manual. Proposed solution optional: N/A
ARTD-54143	Bug	[pwm] Output signal is incorrect when setting duty 0% or 100% with OPWMC mode Detailed description (how to reproduce it): Output signal is incorrect when setting duty 0% or 100% with OPWMC mode. When call SetDutyCycle with 0%, driver will SetUCRegA = Period value(Get from Counter Bus period register value. but this mode run with MC_UP_DOWN_COUNTER. so Period register value is half Period require). So, output signal will be 50% duty. It is not correct When call SetDutyCycle with 100%, output signal is opposite to required Preconditions: Config channel with OPWMC mode. Call SetDutyCycle for this channel with 0% or 100% Test Case ID (internal TC that caught the defect) optional: Pwm_TS_102 Observed behavior: output signal is not correct Expected behavior: The output signal must match the requirements Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-54152	Bug	[CRYPTO] Signature verification return response Detailed description (how to reproduce it): In case of signature verification request with incorrect signature value, Crypto_ProcessJob() for an async job will return E_OK (job queued) and the CallbackNotification will return E_NOT_OK (signature does not match the expected value) with verifyPtr is set to CRYPTO_E_VER_NOT_OK. EBT and Continental request to change this behavior in order for the upper layer to identify if there was a communication error or a invalid signature by returning E_OK for invalid signature. Observation: This change applies to MACs and may apply to AEAD, thus the update will affect the mac and possible AEAD verification. !image-2023-01-05-13-19-32-720.png|thumbnail! Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: CallbackNotification returns E_NOT_OK (signature does not match the expected value) and verifyPtr is set to CRYPTO_E_VER_NOT_OK Expected behavior: CallbackNotification returns E_OK (signature does not match the expected value) and verifyPtr is set to CRYPTO_E_VER_NOT_OK. There is no clear requirement in Autosar for this behavior, this change is requested due to upper layer error handling. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Return E_OK and put the verification result in verifyPtr.

ID	Subtype	Headline and Description
ARTD-54161	Bug	The Unit of the Parameter "macLength" of Csm_MacVerify Mismatch with Crypto's definition Detailed description (how to reproduce it): For cmac verify we have a issue, that in csm module the cmac verify length format is in bits, but in crypto driver It's bytes. The parameter: Crypto_JobType > Crypto_JobPrimitiveInputOutputType. secondaryInputLength. This is confirmed (by EB) as a mistake in Autosar specification and EB had reported this to Autosar committee and it is fixed is fixed in higher version of Autosar. Also AUTOSAR ticket here: [https://jira.autosar.org/browse/AR-85638|https://eur01.safelinks.protection.outlook.com/?url=https%3A%2F%2Fjira.autosar.org%2Fbrowse%2FAR-85638&data=05%7C01%7Cxuewei.wang%40nxp.com%7C7967555f349745c1cb9408dadda963ca%7C686ea1d3bc2b4c6fa92cd99c5c301635%7C0%7C0%7C638066018720639957%7CUnknown%7CTWFpbGZsb3d8eyJWIjoiMC4wLjAwMDAiLCJQIjoiV2luMzIiLCJBTiI6Ik1haWwiLCJXVCI6Mn0%3D%7C3000%7C%7C%7C&sdata=hO0w156ENthz95V5vX70hPBtB2ehDIbbIGi8W%2F10CXk%3D&reserved=0] There is a similar issue for using FAST_CMAC: Now the CSM supports the FAST_CMAC primitive, that is, the user can call the FAST_CMAC algorithm from the CSM layer. But the issue is: the crypto driver function Crypto_Hse_FastCmac() expects the length of input message in bits: pFastCMACSrv->inputBitLength = pJob->jobPrimitiveInputOutput.inputLength; While the up layers (SecOC, CSM) use bytes as the unit for the length of message (plain text). We need to fix this. Preconditions: Test Case ID (internal TC that caught the defect) optional Observed behavior: HSE always response invalid parameter. Expected behavior: No error Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional
ARTD-54365	Bug	[ICU] The DMA has incorrect behavior when eMIOS is configured to IPWM/IPM Detailed description (how to reproduce it): Set a ICU channel (signal measurement or timestamp) using in eMIOS IPWM/IPM mode, and enable DMA to automatic transfer captured data. The DMA will operate totally the same as eMIOS SAIC mode. !image-2023-02-03-10-10-46-152.png! However eMIOS IPWM/IPM has different capture behavior. So the DMA should be changed to adapt eMIOS IPWM/IPM mode. For example, if eMIOS is set to IPWM, the DMA should transmit both A and B registers at the same time. Preconditions: Set a ICU channel (signal measurement or timestamp) using in eMIOS IPWM/IPM mode, and enable DMA to automatic transfer captured data. Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: The DMA will operate totally the same as eMIOS SAIC mode. Expected behavior: The DMA should be changed to adapt eMIOS IPWM/IPM mode. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]

ID	Subtype	Headline and Description
ARTD-54389	New Feature	[IMPLEMENTATION] Remove I3C Driver from RTD release CR description: Need to remove I3C driver from release , IP shall not be used. Errata: ERR051298: I3C: The I3C feature may not work reliably Description: The I3C module may not be 100% reliable to fulfill the protocol. This feature is not recommended for use. Workaround: There is no workaround for this. Reason for this change: Errata, IP unusable Benefit: Customer do not use depreciated IP Onetime CR/Strategic CR: Onetime CR Use-case: na HW documentation reference (as applies): Errata ERR051298 (see errata docuemnts) HW/Application Engineer contact (as applies):{*}{*} Luis Garabito Siordia Note: relevant documents to be attached to the ticket.
ARTD-54606	New Feature	[MemAcc] Integrate with Mem_43_Infls NewWorkDescription: integrate Mem_43_Infls for MemAcc. Create a dev test to run both Exfls and InFls Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Update code
ARTD-54812	New Feature	[BASE] Remove Cosmic reference NewWorkDescription: Remove Cosmic reference from build environment. Requirement source: Please check the email in attachement. (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Update compiler.h
ARTD-54856	New Feature	[Mem_Eep] Analyze and add ASR 21-11 Requirements in Doors NewWorkDescription: Analyze all requirements in the attached excel, according to the guide provided in the .docx file. Requirement source: ASR SWS (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Fill column from K to P

ID	Subtype	Headline and Description
ARTD-55000	Bug	[ocu][S32K3XX] Some variable in IP layer is conflicted when run multicore in parallel Detailed description (how to reproduce it): Some variables in the IP layer (Ftm, eMios, ...) is shared between two cores when run parallel, ex. _Emios_Ocu_Ip_spcxIpConfig (Emios_Ocu_Ip.c), Emios_Ocu_Ip_sGlobalDrvState (Emios_Ocu_Ip.c), ... It will cause a problem when one core changed the value of shared variable while another core needs to check that value to execute OCU driver APIs. For example, core 0 change driver state variable Emios_Ocu_Ip_sGlobalDrvState_ to EMIOS_OCU_IP_DRV_STATE_UNINIT while another core call Ocu_StartChannel API, that channel will not start as desired. !image-2023-02-07-11-16-43-345.png|width=728,height=729! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Ocu_TS_103 Observed behavior: Shared variable's value is changed while another core doesn't want to change that. Expected behavior: That variables need to be separated between used cores. Proposed solution optional: NA
ARTD-55018	New Feature	[MemAcc] Update follow the change on Mem_43_Exfls NewWorkDescription: Mem_Exfls added support infix. > Mem_43_Exfls Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Correct file name, link, ...

ID	Subtype	Headline and Description
ARTD-55022	Bug	[PWM] [EMIOS] Spike pulse ,noise and output signal is wrong when calling Pwm_Init and Pwm_SetDutyCycle Detailed description (how to reproduce it): In Pwm_Init: OPWFM mode : When calling Emios_Pwm_Ip_InitOutputIrqAndMode function, the signal is pulled up high level. When calling function Emios_Pwm_Ip_SetPrescalerEnable function, the signal is pulled down Low level. ==> 1 spike pulse still generated OPWMC mode: When calling Emios_Pwm_Ip_SetPwmMode function still noise OPWM mode : When calling Emios_Pwm_Ip_SetPwmMode function ==> 1 spike pulse still generated In Pwm_SetDutyCycle OPWM mode : When calling Pwm_SetDutyCycle, Pwm_Ipw_SetDutyCycle function still a noise OPWFM and OPWMC mode : Porality Low, Duty 100% ==> Signal level Low When calling Emios_Pwm_Ip_SetOutputToNormal function, signal output pulled up level high Preconditions: Call Pwm_Init with : HwChannel: EmiosPwm Duty Cycle : 100% Polarity : Low or High Pwm_SetDutyCycle with : HW Channel : PwmEmios Duty Cycle : 0% or 100% Test Case ID (internal TC that caught the defect) optional: Pwm_TS_106 Observed behavior: 1 spike pulse still generated when init with duty 100% 1 spike pulse still generated when call Pwm_SetDutyCycle with duty 100% Expected behavior: when init with duty 0% or 100%, no edge is generated Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A

ID	Subtype	Headline and Description
ARTD-55058	Bug	[CRYPTO] Driver does not support secondaryInputLength of GMAC, HMAC and SIPHASH MacVerify jobs being measured in bits Detailed description (how to reproduce it): Calling Crypto_ProcessJob() with a MacVerify primitive with algoMode set to GMAC, HMAC or SIPHASH and the secondaryInputLength parameter of the job measured in bits will fail. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Crypto driver does not take into account that the secondaryInputLength param of a MacVerify job with algoMode set to GMAC, HMAC or SIPHASH can be measured in bits. Expected behavior: Crypto driver should take into account that the secondaryInputLength param of a MacVerify job with algoMode set to GMAC, HMAC or SIPHASH can be measured in bits. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: On ticket ARTD-54161 support was added in Crypto driver to process the secondaryInputLength parameter of a CMAC Verify Job in bytes or bits, depending on the value of a boolean attribute in the configuration of the Crypto plugin. As per the [comment|https://bitbucket.sw.nxp.com/projects/ARTD/repos/crypto/pull-requests/724/overview?commentId=1584670]in the Pull Request of the ticket above, the value of the define 'CRYPTO$InfixValue $_SECINPUTLEN_FOR_MACVERIFY_JOBS_USES_BITS' should be used also when Crypto driver processes HMAC, GMAC or SIPHASH MacVerify jobs. Dev test case TC_0801 in test suite TS_011 should be updated to test the impacted MacVerify algos.
ARTD-55185	Bug	[PWM][Flexio] generate spike pulse Flexio mode Detailed description (how to reproduce it): when set Duty Cycle : 100% Porality : HIGH In Pwm_SetDutyCycle function and Pwm_SetDutyAndPeriod function Flexio mode, when calling Flexio_Pwm_Ip_ConfigurePinOverride still generate spike pulse Preconditions: Pwm_SetDutyCycle with : HW Channel : ChannelFlexio DutyCycle : 100% Pwm_SetDutyAndPeriod with : HW Channel : ChannelFlexio Period DutyCycle : 100% Test Case ID (internal TC that caught the defect) optional: Pwm_TS_106 CFG_SETS=6 Observed behavior: Generate spike pulse Expected behavior: when call function, no is generated spike pulse Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A

ID	Subtype	Headline and Description
ARTD-55421	Bug	[adc] [GENERAL] PLUGINS_DIR should point to RTD plugin folder instead of EB Tresos plugin folder in readme.txt Detailed description (how to reproduce it): In readme.txt file, the following sentence: PLUGINS_DIR The path to the Tresos plugins directory !john_floros_0-1653582301493.png|width=696,height=261! In fact, PLUGINS_DIR should point to RTD plugin folder instead of EB Tresos plugin folder in readme.txt Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: PLUGINS_DIR points to EB Tresos plugin folder in readme.txt, which is incorrect. Expected behavior: PLUGINS_DIR should point to RTD plugin folder instead of EB Tresos plugin folder in readme.txt. PLUGINS_DIR The path to the RTD plugins directory Ex: PLUGINS_DIR = C:/NXP/SW32_RTD/eclipse/plugins Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: PLUGINS_DIR should point to RTD plugin folder : PLUGINS_DIR The path to the RTD plugins directory Ex: PLUGINS_DIR = C:/NXP/SW32_RTD/eclipse/plugins
ARTD-55429	Bug	[CanTrcv] [GENERAL] PLUGINS_DIR should point to RTD plugin folder instead of EB Tresos plugin folder in readme.txt Detailed description (how to reproduce it): In readme.txt file, the following sentence: PLUGINS_DIR The path to the Tresos plugins directory !john_floros_0-1653582301493.png|width=696,height=261! In fact, PLUGINS_DIR should point to RTD plugin folder instead of EB Tresos plugin folder in readme.txt Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: PLUGINS_DIR points to EB Tresos plugin folder in readme.txt, which is incorrect. Expected behavior: PLUGINS_DIR should point to RTD plugin folder instead of EB Tresos plugin folder in readme.txt. PLUGINS_DIR The path to the RTD plugins directory Ex: PLUGINS_DIR = C:/NXP/SW32_RTD/eclipse/plugins Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: PLUGINS_DIR should point to RTD plugin folder : PLUGINS_DIR The path to the RTD plugins directory Ex: PLUGINS_DIR = C:/NXP/SW32_RTD/eclipse/plugins

ID	Subtype	Headline and Description
ARTD-55447	Bug	[eth] [GENERAL] PLUGINS_DIR should point to RTD plugin folder instead of EB Tresos plugin folder in readme.txt Detailed description (how to reproduce it): In readme.txt file, the following sentence: PLUGINS_DIR The path to the Tresos plugins directory !john_floros_0-1653582301493.png|width=696,height=261! In fact, PLUGINS_DIR should point to RTD plugin folder instead of EB Tresos plugin folder in readme.txt Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: PLUGINS_DIR points to EB Tresos plugin folder in readme.txt, which is incorrect. Expected behavior: PLUGINS_DIR should point to RTD plugin folder instead of EB Tresos plugin folder in readme.txt. PLUGINS_DIR The path to the RTD plugins directory Ex: PLUGINS_DIR = C:/NXP/SW32_RTD/eclipse/plugins Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: PLUGINS_DIR should point to RTD plugin folder : PLUGINS_DIR The path to the RTD plugins directory Ex: PLUGINS_DIR = C:/NXP/SW32_RTD/eclipse/plugins

ARTD-55298	Bug	[ICU]WKPU and SIUL2 interrupt flag is cleared when two channels occur simultaneously
		
		Detailed description (how to reproduce it):
		In the function interrupt of wkpu and siul2 harware, there is mistake in processing interrupt in case many channel occurs interrupt at the same time.
		The instruction clears the interrupt flag of the previous channel and also clears the interrupt flag of the next channel
		for (u8WkpuChannel = 0; u8WkpuChannel < (uint32)WKPU_IP_NUM_OF_CHANNELS_IN_ONE_REG; u8WkpuChannel++)
		{
		if (0x0U != (u32reg_WKPU_WISR & u32ChannelMask))
		{
		/ Clear pending interrupt serviced /
		Wkpu_Ip_pBase[0U]->WISR = u32reg_WKPU_WISR;
		
		Wkpu_Ip_Callback(u8WkpuChannel);
		}
		u32ChannelMask <<= (uint32)1U;
		}
		
		for (u8IrqChannel = firstHwChannel; u8IrqChannel < (firstHwChannel 8U); u8IrqChannel++)
		{
		if (0x0U != (u32RegIrqMask & u32ChannelMask))
		{
		/ Clear pending interrupt serviced /
		(Siul2_Icu_Ip_pBase[instance])->DISR0 = u32RegFlags & u32RegIrqMask;
		
		Siul2_Icu_Ip_ReportEvents(instance, u8IrqChannel);
		}
		u32ChannelMask <<= (uint32)1U;
		}
		Preconditions:
		Set interrupt flag for 2 channels at the same time
		
		Test Case ID (internal TC that caught the defect) optional:
		Icu_TC_WBT_0104(Icu_TS_083)
		
		Observed behavior:
		The instruction to clear the interrupt flag of the previous channel also clears the interrupt flag of the following channel
		Expected behavior:
		The instruction to clear the interrupt flag of the previous channel does not clear the interrupt flag of the following channel
		
		Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)
		
		Proposed solution optional:
		Need to change the statement to clear the interrupt flag so that the above error does not occur

ID	Subtype	Headline and Description
ARTD-55399	Bug	S32K3 FlexCAN driver sending error in RTD 2.0.0 Hello, RTD teams! Our customer feedback a randomly happened question that when CAN bus loading is high, some of the Tx MBs will stop sending forever. The crashed TxMB's code field is always 0b1101, which can not correspond to any status of the description in S32K3 reference manual. We consider it is caused by the OR operation in the function FlexCAN_Ip_Send-> FlexCAN_StartSendData > FlexCAN_SetTxMsgBuff: Flexcan_Mb = Flexcan_Mb_Config; We found that the only chance the last bit of CODE is "1", is the OR operation with 0b1001(Abort transfer). So we put a brake point into the function FlexCAN_Ip_AbortTransfer. But found this crash still happen and the brake point never arrived. The crashed MB's code filed is always 0b1101. After changing the OR operation to assignment value directly, just as below. Flexcan_Mb = Flexcan_Mb_Config; This question will never happen anymore. All the TxMBs will stay normal transfer. My question is: # Why the OR operation will lead to an unexpected CODE field sometimes? Did you meet this issue before? # Why there is an OR "|=" operation here to trigger the MB sending, instead of a "=”?
ARTD-55457	Bug	[gdu] [GENERAL] PLUGINS_DIR should point to RTD plugin folder instead of EB Tresos plugin folder in readme.txt Detailed description (how to reproduce it): In readme.txt file, the following sentence: PLUGINS_DIR The path to the Tresos plugins directory !john_floros_0-1653582301493.png|width=696,height=261! In fact, PLUGINS_DIR should point to RTD plugin folder instead of EB Tresos plugin folder in readme.txt Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: PLUGINS_DIR points to EB Tresos plugin folder in readme.txt, which is incorrect. Expected behavior: PLUGINS_DIR should point to RTD plugin folder instead of EB Tresos plugin folder in readme.txt. PLUGINS_DIR The path to the RTD plugins directory Ex: PLUGINS_DIR = C:/NXP/SW32_RTD/eclipse/plugins Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: PLUGINS_DIR should point to RTD plugin folder : PLUGINS_DIR The path to the RTD plugins directory Ex: PLUGINS_DIR = C:/NXP/SW32_RTD/eclipse/plugins

ID	Subtype	Headline and Description
ARTD-55461	Bug	[i2c] [GENERAL] PLUGINS_DIR should point to RTD plugin folder instead of EB Tresos plugin folder in readme.txt Detailed description (how to reproduce it): In readme.txt file, the following sentence: PLUGINS_DIR The path to the Tresos plugins directory !john_floros_0-1653582301493.png|width=696,height=261! In fact, PLUGINS_DIR should point to RTD plugin folder instead of EB Tresos plugin folder in readme.txt Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: PLUGINS_DIR points to EB Tresos plugin folder in readme.txt, which is incorrect. Expected behavior: PLUGINS_DIR should point to RTD plugin folder instead of EB Tresos plugin folder in readme.txt. PLUGINS_DIR The path to the RTD plugins directory Ex: PLUGINS_DIR = C:/NXP/SW32_RTD/eclipse/plugins Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: PLUGINS_DIR should point to RTD plugin folder : PLUGINS_DIR The path to the RTD plugins directory Ex: PLUGINS_DIR = C:/NXP/SW32_RTD/eclipse/plugins
ARTD-55465	Bug	[icu] [GENERAL] PLUGINS_DIR should point to RTD plugin folder instead of EB Tresos plugin folder in readme.txt Detailed description (how to reproduce it): In readme.txt file, the following sentence: PLUGINS_DIR The path to the Tresos plugins directory !john_floros_0-1653582301493.png|width=696,height=261! In fact, PLUGINS_DIR should point to RTD plugin folder instead of EB Tresos plugin folder in readme.txt Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: PLUGINS_DIR points to EB Tresos plugin folder in readme.txt, which is incorrect. Expected behavior: PLUGINS_DIR should point to RTD plugin folder instead of EB Tresos plugin folder in readme.txt. PLUGINS_DIR The path to the RTD plugins directory Ex: PLUGINS_DIR = C:/NXP/SW32_RTD/eclipse/plugins Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: PLUGINS_DIR should point to RTD plugin folder : PLUGINS_DIR The path to the RTD plugins directory Ex: PLUGINS_DIR = C:/NXP/SW32_RTD/eclipse/plugins

ID	Subtype	Headline and Description
ARTD-55467	Bug	[lin] [GENERAL] PLUGINS_DIR should point to RTD plugin folder instead of EB Tresos plugin folder in readme.txt Detailed description (how to reproduce it): In readme.txt file, the following sentence: PLUGINS_DIR The path to the Tresos plugins directory !john_floros_0-1653582301493.png|width=696,height=261! In fact, PLUGINS_DIR should point to RTD plugin folder instead of EB Tresos plugin folder in readme.txt Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: PLUGINS_DIR points to EB Tresos plugin folder in readme.txt, which is incorrect. Expected behavior: PLUGINS_DIR should point to RTD plugin folder instead of EB Tresos plugin folder in readme.txt. PLUGINS_DIR The path to the RTD plugins directory Ex: PLUGINS_DIR = C:/NXP/SW32_RTD/eclipse/plugins Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: PLUGINS_DIR should point to RTD plugin folder : PLUGINS_DIR The path to the RTD plugins directory Ex: PLUGINS_DIR = C:/NXP/SW32_RTD/eclipse/plugins
ARTD-55499	Bug	[pwm] [GENERAL] PLUGINS_DIR should point to RTD plugin folder instead of EB Tresos plugin folder in readme.txt Detailed description (how to reproduce it): In readme.txt file, the following sentence: PLUGINS_DIR The path to the Tresos plugins directory !john_floros_0-1653582301493.png|width=696,height=261! In fact, PLUGINS_DIR should point to RTD plugin folder instead of EB Tresos plugin folder in readme.txt Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: PLUGINS_DIR points to EB Tresos plugin folder in readme.txt, which is incorrect. Expected behavior: PLUGINS_DIR should point to RTD plugin folder instead of EB Tresos plugin folder in readme.txt. PLUGINS_DIR The path to the RTD plugins directory Ex: PLUGINS_DIR = C:/NXP/SW32_RTD/eclipse/plugins Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: PLUGINS_DIR should point to RTD plugin folder : PLUGINS_DIR The path to the RTD plugins directory Ex: PLUGINS_DIR = C:/NXP/SW32_RTD/eclipse/plugins

ID	Subtype	Headline and Description
ARTD-55517	Bug	[uart] [GENERAL] PLUGINS_DIR should point to RTD plugin folder instead of EB Tresos plugin folder in readme.txt Detailed description (how to reproduce it): In readme.txt file, the following sentence: PLUGINS_DIR The path to the Tresos plugins directory !john_floros_0-1653582301493.png|width=696,height=261! In fact, PLUGINS_DIR should point to RTD plugin folder instead of EB Tresos plugin folder in readme.txt Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: PLUGINS_DIR points to EB Tresos plugin folder in readme.txt, which is incorrect. Expected behavior: PLUGINS_DIR should point to RTD plugin folder instead of EB Tresos plugin folder in readme.txt. PLUGINS_DIR The path to the RTD plugins directory Ex: PLUGINS_DIR = C:/NXP/SW32_RTD/eclipse/plugins Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: PLUGINS_DIR should point to RTD plugin folder : PLUGINS_DIR The path to the RTD plugins directory Ex: PLUGINS_DIR = C:/NXP/SW32_RTD/eclipse/plugins
ARTD-55538	New Feature	[can] New header files need to be reviewed NewWorkDescription: Newest version of header files for K3 derivatives are available. Provided now separated header files for S32K342 and S32K341. Tag of Base: *PVT_BASE_S32K3XX_RTM_3.0.0_001. This tag is available on the manifest: BLN_RTD_4.7_S32K3XX_3.0.0.xml !image-2023-02-15-14-56-48-188.png|width=567,height=343! SOW link: [https://nxp1.sharepoint.com/:w:/r/sites/Zebra/_layouts/15/Doc.aspx?sourcedoc= %7B8DBBE9CD-33BA-4B0E-A2CB-688684283055%7D&file=SW32K3%20RTD%20ASR %204.4%20%26%20R21-11%203.0.0%20SOW.docx&action=default&mobileredirect=true] Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: 1. Review the changes from header files. For the fact that separate header files for S32K342 and S32K341 are provided all drivers need to be updated. 2. Also review the rest of header files.
ARTD-55547	New Feature	[dio] New header files need to be reviewed NewWorkDescription: Newest version of header files for K3 derivatives are available. Provided now separated header files for S32K342 and S32K341. Tag of Base: *PVT_BASE_S32K3XX_RTM_3.0.0_001. This tag is available on the manifest: BLN_RTD_4.7_S32K3XX_3.0.0.xml !image-2023-02-15-14-56-48-188.png|width=567,height=343! SOW link: [https://nxp1.sharepoint.com/:w:/r/sites/Zebra/_layouts/15/Doc.aspx?sourcedoc= %7B8DBBE9CD-33BA-4B0E-A2CB-688684283055%7D&file=SW32K3%20RTD%20ASR %204.4%20%26%20R21-11%203.0.0%20SOW.docx&action=default&mobileredirect=true] Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: 1. Review the changes from header files. For the fact that separate header files for S32K342 and S32K341 are provided all drivers need to be updated. 2. Also review the rest of header files.

ID	Subtype	Headline and Description
ARTD-55571	New Feature	[icu] New header files need to be reviewed NewWorkDescription: Newest version of header files for K3 derivatives are available. Provided now separated header files for S32K342 and S32K341. Tag of Base: *PVT_BASE_S32K3XX_RTM_3.0.0_001. This tag is available on the manifest: BLN_RTD_4.7_S32K3XX_3.0.0.xml !image-2023-02-15-14-56-48-188.png|width=567,height=343! SOW link: [https://nxp1.sharepoint.com/:w:/r/sites/Zebra/_layouts/15/Doc.aspx?sourcedoc= %7B8DBBE9CD-33BA-4B0E-A2CB-688684283055%7D&file=SW32K3%20RTD%20ASR %204.4%20%26%20R21-11%203.0.0%20SOW.docx&action=default&mobileredirect=true] Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: 1. Review the changes from header files. For the fact that separate header files for S32K342 and S32K341 are provided all drivers need to be updated. 2. Also review the rest of header files.
ARTD-55601	New Feature	[spi] New header files need to be reviewed NewWorkDescription: Newest version of header files for K3 derivatives are available. Provided now separated header files for S32K342 and S32K341. Tag of Base: *PVT_BASE_S32K3XX_RTM_3.0.0_001. This tag is available on the manifest: BLN_RTD_4.7_S32K3XX_3.0.0.xml !image-2023-02-15-14-56-48-188.png|width=567,height=343! SOW link: [https://nxp1.sharepoint.com/:w:/r/sites/Zebra/_layouts/15/Doc.aspx?sourcedoc= %7B8DBBE9CD-33BA-4B0E-A2CB-688684283055%7D&file=SW32K3%20RTD%20ASR %204.4%20%26%20R21-11%203.0.0%20SOW.docx&action=default&mobileredirect=true] Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: 1. Review the changes from header files. For the fact that separate header files for S32K342 and S32K341 are provided all drivers need to be updated. 2. Also review the rest of header files.
ARTD-55604	New Feature	[uart] New header files need to be reviewed NewWorkDescription: Newest version of header files for K3 derivatives are available. Provided now separated header files for S32K342 and S32K341. Tag of Base: *PVT_BASE_S32K3XX_RTM_3.0.0_001. This tag is available on the manifest: BLN_RTD_4.7_S32K3XX_3.0.0.xml !image-2023-02-15-14-56-48-188.png|width=567,height=343! SOW link: [https://nxp1.sharepoint.com/:w:/r/sites/Zebra/_layouts/15/Doc.aspx?sourcedoc= %7B8DBBE9CD-33BA-4B0E-A2CB-688684283055%7D&file=SW32K3%20RTD%20ASR %204.4%20%26%20R21-11%203.0.0%20SOW.docx&action=default&mobileredirect=true] Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: 1. Review the changes from header files. For the fact that separate header files for S32K342 and S32K341 are provided all drivers need to be updated. 2. Also review the rest of header files.
ARTD-55607	New Feature	[wdg] New header files need to be reviewed NewWorkDescription: Newest version of header files for K3 derivatives are available. Provided now separated header files for S32K342 and S32K341. Tag of Base: *PVT_BASE_S32K3XX_RTM_3.0.0_001. This tag is available on the manifest: BLN_RTD_4.7_S32K3XX_3.0.0.xml !image-2023-02-15-14-56-48-188.png|width=567,height=343! SOW link: [https://nxp1.sharepoint.com/:w:/r/sites/Zebra/_layouts/15/Doc.aspx?sourcedoc= %7B8DBBE9CD-33BA-4B0E-A2CB-688684283055%7D&file=SW32K3%20RTD%20ASR %204.4%20%26%20R21-11%203.0.0%20SOW.docx&action=default&mobileredirect=true] Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: 1. Review the changes from header files. For the fact that separate header files for S32K342 and S32K341 are provided all drivers need to be updated. 2. Also review the rest of header files.

ID	Subtype	Headline and Description
ARTD-55693	Bug	[PWM] Can not configure 100% duy cycle for Emios IPL Detailed description (how to reproduce it): Can not configure 100% duy cycle for Emios IPL. when configure duty cycle[ticks] value same with Period[ticks] value, it will be raise an error " Period value is smaller than dutyCycle". In Emios_Pwm.component, EmiosChPeriod node check: <constraint cond_expr="$parent.EmiosChDutyCycle.getValue() < $this.getValue()" !image-2023-02-20-15-22-18-158.png! Preconditions: Configure duty cycle value same with period value Test Case ID (internal TC that caught the defect) optional: Ip_Emios_TS_001 Observed behavior: An error will be raised when configure duty value = period value Expected behavior: No error will be raised when configure duty value = period value Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update the condition of the node *Period ticks* in Emios_Pwm.component file to allow configure case period equal to duty value with CT tools
ARTD-55706	Bug	[Platform]S32K3_RTD_2_0_1, The size of ICTM and DCTM in the linker_flash_s32k314.ld file overcome the actual size. Detailed description (how to reproduce it): The size of ICTM and DCTM in the linker_flash_s32k314.ld file is not correct. !image-2023-02-20-16-35-17-227.png! !image-2023-02-20-16-36-41-199.png! Preconditions: The size of ICTM and DCTM in the linker_flash_s32k314.ld file doesn't overcome the actual size. Test Case ID (internal TC that caught the defect) optional: None Observed behavior: The size of ICTM and DCTM in the linker_flash_s32k314.ld file overcome the actual size. Expected behavior: as Preconditions Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: !image-2023-02-20-16-40-50-562.png!

ID	Subtype	Headline and Description
ARTD-55757	Bug	[MCL] Exclusive areas are not generated accordingly in bswmd file Detailed description (how to reproduce it): In MCL Module, the following exclusive areas are not getting generated in RTE integrator from customers. SchM_Enter_Mcl_MCL_EXCLUSIVE_AREA_13 SchM_Enter_Mcl_MCL_EXCLUSIVE_AREA_14 SchM_Enter_Mcl_MCL_EXCLUSIVE_AREA_15 SchM_Enter_Mcl_MCL_EXCLUSIVE_AREA_16 SchM_Enter_Mcl_MCL_EXCLUSIVE_AREA_17 SchM_Enter_Mcl_MCL_EXCLUSIVE_AREA_18 The Mcl_Bswmd.arxml file need to be updated (see attachment) Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Exclusive areas are not getting generated in customers RTE integrator Expected behavior: Exclusive areas shall be generated in customers RTE integrator Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: See attachment
ARTD-55855	New Feature	[pwm] Implement CPR_RTD_00664 requirement for S32K3xx RTM 300 release NewWorkDescription: In RTD S32XX RTM 4.0.0, we implemented the change of below requirement. However, we only updated for IPV ({*}FTM{*}) of the S32XX derivatives, so in this release (S32K3xx 3.0.0) we have to review and update remaining IPs (IPvs of S32K3xx derivatives Emios, FlexIO, ...). Old requirements: ID|Req ID|cPRT|Functionality / Item|Req Type|Platform|IP|Req State|Verification Criteria 28|CPR_RTD_00028|ISR shall check whether its respective interrupt status flag and interrupt enable flag are set; i.e. whether the interrupt is not spurious. If at least one flag is not set, then the interrupt is spurious and the ISR shall only clear the interrupt status flag and return immediately.|ALL_DRV_WITH_INTERRUPTS|Functional|ALL|ALL|Approved|Test Case |||||||| After change: CPR_RTD_00028 is replaced by CPR_RTD_00664 ID|Req ID|cPRT|Functionality / Item|Req Type|Platform|IP|Req State|Verification Criteria |||||||| 670|CPR_RTD_00664|ISR shall check whether its respective interrupt status flag and interrupt enable flag are set; i.e. whether the interrupt is not spurious. If at least one of the flags is not set, then the interrupt is spurious and the ISR shall not treat the event (return immediately). Rationale: A spurious interrupt is considered when there is a glitch in the hardware mechanisms that trigger the CPU exception. Drivers must ensure only relevant events are treated and spurious ones are discarded|ALL_DRV_WITH_INTERRUPTS|Functional|ALL|ALL|Approved|Test Case Proposed solution : For development: Implement CPR_RTD_00664 in driver Update FMEA report on dedicated ticket and link this driver ticket to FMEA ticket. Apply a new driver requirement baseline on DOOR and update in FMEA report. In the FMEA, list also the ID of the driver’s ticket along the Req ID in the sections that refer to mechanism to avoid spurious interrupts and infinite loops Update UML design to ensure traceability In the Traceability Warnings sheet, put the ID of the driver’s ticket on the column that signals a warning because a test case will exist for something that does not appear to be a requirement in the module. For testing: Create test case to verify those requirements

ID	Subtype	Headline and Description
ARTD-56509	New Feature	[I2S] Add phantom derivative resource files for S32K3XX NewWorkDescription: There are some new phantom derivatives of S32K3 were added in this release, details below: s32k310_lqfp48 \ s32k310_mqfp100 \ s32m274_lqfp64 \ s32k394_mapbga289 Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Create new resource files for those derivatives
ARTD-56989	Bug	[LinIf] Fix build failed by incorrect condition Detailed description (how to reproduce it): The #if condition is incorrect. Need to fix the condition as below: #if define() #endif Preconditions: Using Linif Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Incorrect condition Expected behavior: Correct condition Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-58440	New Feature	[MemAcc] Integrate with Mem_43_Eep NewWorkDescription: integrate Mem_43_Infls for MemAcc. Create a dev test to run both Exfls and InFls Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Update code
ARTD-58508	Bug	[Gdu] Synchronization enable and HD high voltage detect not propagated to the generated files Detailed description (how to reproduce it): Settings of Synchronization enable and HD high voltage detect are not propagated to the generated files. !GDU1.PNG! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: The settings in the picture above are not propagated to the generated structure. The highlighted parameters in the picture below remain at zero value regardless of the settings in the graphical tool. !GDU2.PNG! Expected behavior: To get propagated to the generated structure Proposed solution optional: N/A

ID	Subtype	Headline and Description
ARTD-58791	Bug	[CAN] Update the driver according with SWS_Can_00441 and SWS_Can_00442 Detailed description (how to reproduce it): The CAN driver MainFunctions names shall be according with SWS_Can_00441 and [SWS_Can_00442] correct. Now we have a deviation mentioned in manual and this will lead to BSWMD error [SWS_Can_00441] ⌈ If more than one main function period is configured by CanMainFunctionRWPeriods (see ECUC_Can_00437), the name of the Can_MainFunction_Write() functions shall be # Can_MainFunction_Write_<CanMainFunctionRWPeriods.ShortName>() for each CanMainFunctionRWPeriods that is referenced by at least one TRANSMIT CanHardwareObject (see ECUC_Can_00438). [SWS_Can_00442] ⌈ If more than one main function period is configured by CanMainFunctionRWPeriods (see ECUC_Can_00437), the name of the Can_MainFunction_Read() functions shall be # Can_MainFunction_Read_<CanMainFunctionRWPeriods.ShortName>() for each CanMainFunctionRWPeriods that is referenced by at least one RECEIVE CanHardwareObject (see ECUC_Can_00438) Don't forgot if an update is taken then to update the documentation too by remove the deviation and check if the driver is still complaint with the VSMD report. Preconditions: Use Polling mode with mainfunctions read\write Test Case ID (internal TC that caught the defect) optional: n/A Observed behavior: We kept ASR 4.3 older requirement. Expected behavior: Comply with standard requirements SWS_Can_00441 and SWS_Can_00442 Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-58832	Bug	[S32K3XX] [Platform] IAR linker ram does not have some symbols used for Fls driver Detailed description (how to reproduce it): Fls test build failed because following symbols do not exist in iar linker ram Fls_ACWriteSize Fls_ACEraseSize Fls_ACWriteRomStart Fls_ACEraseRomStart Preconditions: iar compiler Test Case ID (internal TC that caught the defect) optional: Fls_TS_020 Observed behavior: Error[Li005]: no definition for "Fls_ACWriteSize" [referenced from d:\Zebra\SASW\JSW_MCAL\XPC56xx\output \S32K3XX_S32K344_iar\fls\Fls_TS_020_cfg1_CORE0\out\Fls_c.o] Error[Li005]: no definition for "Fls_ACEraseSize" [referenced from d:\Zebra\SASW\JSW_MCAL\XPC56xx\output \S32K3XX_S32K344_iar\fls\Fls_TS_020_cfg1_CORE0\out\Fls_c.o] Error[Li005]: no definition for "Fls_ACWriteRomStart" [referenced from d:\Zebra\SASW\JSW_MCAL\XPC56xx\output \S32K3XX_S32K344_iar\fls\Fls_TS_020_cfg1_CORE0\out\Fls_c.o] Error[Li005]: no definition for "Fls_ACEraseRomStart" [referenced from d:\Zebra\SASW\JSW_MCAL\XPC56xx\output \S32K3XX_S32K344_iar\fls\Fls_TS_020_cfg1_CORE0\out\Fls_c.o] Expected behavior: build successfully Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A

ID	Subtype	Headline and Description
ARTD-58945	Bug	[GDU] Do not write b3 in the Interrupt Flag (INTF) Detailed description (how to reproduce it): Trigger the GDU_INT interrupt line. Preconditions: Aec_Ip_SpiRead gives an erroneous read value with bit 3 (reserved to 0) set . Test Case ID (internal TC that caught the defect) optional: Observed behavior: Bit 3 in INTF will have a W1C operation applied to it. Expected behavior: Bit 3 in INTF does not support writing to it. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Mask out the reserved bit before clearing the interrupt flags.

ARTD-58888	Bug	[PWM] FlexPWM interrupt flag is cleared when two channels occur simultaneously
		
		Detailed description (how to reproduce it):
		
		In the function interrupt of FlexPWM harware at the compare interrupt, there is mistake in processing interrupt in case many channel occurs interrupt at the same time.
		The instruction clears the interrupt flag of the previous channel and also clears the interrupt flag of the next channel.
		
		static inline void FlexPwm_Ip_ClearInterruptCmpFlagHw(FlexPwm_Ip_HwAddrType const Base, uint8 SubModule, uint8 IntFlag)
		{
		#ifdef FLEXPWM_AE_IP_HW
		Base->SUB[SubModule].STS = FLEXPWM_STS_CMPF(IntFlag);
		#else
		Base->SM[SubModule].SMSTS = FLEXPWM_SMSTS_CMPF(IntFlag);
		#endif
		}
		
		Preconditions:
		Set interrupt flag for 2 channels at the same time in the compare interrupt.
		
		Test Case ID (internal TC that caught the defect) optional:
		PWM_TS_013
		
		Observed behavior:
		The instruction to clear the interrupt flag of the previous channel also clears the interrupt flag of the following channel
		
		Expected behavior:
		The instruction to clear the interrupt flag of the previous channel does not clear the interrupt flag of the following channel
		
		Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)
		
		Proposed solution optional:
		[....]

ARTD-58973	Bug	[PORT] Precompile value should not different between each variant configuration in S32DS for S32K3 Detailed description (how to reproduce it): Open S32DS, config 3 VS, VS_0 and VS_1 config variant = VariantPostBuild, VS_2 = VariantPreCompile Preconditions: config 3 VS, build in S32DS 3.4, tag PVT_ARTD_PORT_V100 Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: not have any warning or error==> incorrect concept about config multivariant VS_0 and VS_1: !image-2021-04-07-13-32-27-058.png! VS_2: !image-2021-04-07-13-33-10-512.png! Expected behavior: config in 1 VS, but need affect to 3 VS following concept multivariant configuration Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA

ID	Subtype	Headline and Description
ARTD-58981	Bug	[UART] The number of bytes remaining and the status of the channel do not match belong Flexio Ip and Linflexd Ip Detailed description (how to reproduce it): This issue was raised for: IAD-1504 ticket from iMx team Issue: Use the Uart_GetStatus function to read the transmission status and the remaining bytes of the channel: !screenshot-1.png|thumbnail! Check the return status T_UartStatus is UART_STATUS_NO_ERROR !screenshot-2.png|thumbnail! But the number of remaining bytes is not 0 !screenshot-3.png|thumbnail! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: N/A Expected behavior: Flexio_Uart_Ip_GetStatus function needs to use an exclusive area to protect status checking and update the remaining bytes Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Flexio_Uart_Ip_GetStatus functions need to use an exclusive area
ARTD-58991	Bug	[CRYPTO] The IP files miss Autosar version check Detailed description (how to reproduce it): The IP files now missing the check for Autotar version. More detail at https://bitbucket.sw.nxp.com/projects/ARTD/repos/crypto/pull-requests/746/overview?commentId=1633774 Preconditions: Crypto is cloned Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: The IP files now missing the check for Autotar version Expected behavior: The IP files have the check for Autotar version. Proposed solution optional: Add Autosar version check for IP files
ARTD-59009	Bug	[LINIF] Define macro error Detailed description (how to reproduce it): One macro is define wrong Preconditions: Test Case ID (internal TC that caught the defect) optional: Observed behavior: Expected behavior: !image-2023-03-03-17-18-35-549.png|thumbnail! Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]

ID	Subtype	Headline and Description
ARTD-59012	Bug	[S32K3XX] [DIO] Code generated is inconsistent between EB tresos and S32DS when test the MultiCore Detailed description (how to reproduce it): Create config for dio in EB tresos Create config for dio in S32DS Enable Multicore, add channel group Generate code Preconditions: Enable Multicore, add channel group Test Case ID (internal TC that caught the defect) optional: Dio_TS_203 Observed behavior: Data generated in Dio_Cfg.h and Dio_Cfg.c : Code generated is inconsistent between EB tresos and S32DS Dio_Cfg.h !image-2023-03-03-17-23-06-511.png|thumbnail! Dio_Cfg.c !image-2023-03-03-17-22-39-265.png|thumbnail! Expected behavior: code generate between EB tresos and S32DS is consistent Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Added Dio_ConfigName variable such that all DioConfig variables in C code contain the name of DioConfig field in S32DS, the same as in Tresos generated code.
ARTD-59247	Bug	[CANIF] Fix compiler warning/errors Detailed description (how to reproduce it): There are some warnings in generated code for CanIf module. Please check the attached file. Preconditions: Compile the tests for Can driver. Test Case ID (internal TC that caught the defect) optional: CAN_TS_COT_056 Observed behavior: There are some warnings. Expected behavior: No warnings Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-59304	Bug	[S32K3 3.0.0] Crypto: Generate fail when config key material on S32DS Detailed description (how to reproduce it): When config on S32DS tool a keyelement with keyelement ID=1 and disabled both of EncryptedKeyExport and AuthenticatedKeyExport, the driver still requires KeyelementID=99 and error "HSE Key Export is enabled requiring CryptoKeyElement with CryptoKeyElementId = 99 (CRYPTO_KE_EXPORT_AUTHENTICATION)" will appear Preconditions: config a key material and disabled EncryptedKeyExport and AuthenticatedKeyExport Test Case ID (internal TC that caught the defect) optional: All of test suite Observed behavior: error "HSE Key Export is enabled requiring CryptoKeyElement with CryptoKeyElementId = 99 (CRYPTO_KE_EXPORT_AUTHENTICATION)" will appears whenever you config key material on DS Expected behavior: User can config keymaterial disabled EncryptedKeyExport and AuthenticatedKeyExport without any error Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]

ID	Subtype	Headline and Description
ARTD-59314	Bug	[pwm] Emios_Pwm_Ip_SetPhaseShift prevent 100% dutycycle Detailed description (how to reproduce it): Phase shift doesn't allow to ser reg A to zero which prevents 100% duty cycle (considering polarity edpol =1). see attached slides for more details. Preconditions: see emios and clock settings in attached configuration (same is possible to achieve with low level drivers and config tools) . EMIOS_PWMA for example. Observed behavior: 1 tic k is missing if duty cycle Expected behavior: It should be possible to set full range of dutycycle <0,100%> with full range of phaseshift <0,100%>. I recommend at least to test 0%, 50%, 100% and transitions between each other. Proposed solution optional: CounterStart in Emios_Pwm_Ip_SetPhaseShift should be 0._ corner case "0 tic phaseshif and 0 tic dutycicle" should be analyzed too as described in slides 7-10.
ARTD-59342	Bug	[ICU] Icu_SetInitialCounterValue and Icu_SetMaxCounterValue functions are not working correctly Detailed description (how to reproduce it): After calling Icu_ResetEdgeCount function, I use Icu_SetInitialCounterValue function the counter value does not change and is equal to =0 even though I have passed a non-zero value to the function then I call the function Icu_SetMaxCounterValue the value of register A is also unchanged even though the value is passed to the function Preconditions: use the function Icu_SetInitialCounterValue and Icu_SetMaxCounterValue Test Case ID (internal TC that caught the defect) optional: Icu_TC_FCT_0232(Icu_TS_115) Observed behavior: The counter value and the A register of the EMIOS channel do not change even though the values have been passed to the Icu_SetInitialCounterValue and Icu_SetMaxCounterValue functions. Expected behavior: EMIOS channel A register and counter value will change for correct operation Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: To change the value of counter and register A need to change the operation mode to GPIO when using these 2 functions.
ARTD-59357	Bug	[S32K3 3.0.0] [Mem_Eep] On EB tresos, SD clock must be less than uSDHC clock Detailed description (how to reproduce it): On EB tresos, Mem_Eep allow to configure SD clock must be higher than uSDHC clock. SD clock > uSDHC clock make mem driver caculate wrong base clock value. So we should use contrain(SD clock < uSDHC) on EB tresos to cover. Preconditions: SD clock must be less than uSDHC clock Test Case ID (internal TC that caught the defect) optional: Mem_Eep_TS_001 Observed behavior: SD clock > uSDHC clock make mem driver caculate wrong base clock value Expected behavior: SD clock must be less than uSDHC clock Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: n/A

ID	Subtype	Headline and Description
ARTD-59396	Bug	[I2S] Generate fail ecpd file on Flexio_I2s_Ip Detailed description (how to reproduce it): Can not generate ecpd file with component Flexio_I2s_Ip Preconditions: Flexio_I2s_Ip Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Can not generate ecpd file with component Flexio_I2s_Ip Log : SEVERE: [SDK/Data] Code generation failed for Peripherals: Script finished with exception: Value of: $parent.FlexioClocks not found. Script's directory: C:\NXP\S32DS.3.5\eclipse\mcu_data\components\PlatformSDK_S32K3_3_0_0\system Mar 07, 2023 2:07:32 PM com.nxp.swtools.common.utils.runtime.ExecutableExtensionProvider getExtensionsMap Expected behavior: Generate successfully ECPD File Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-59462	Bug	[ADC] Error AutoSar Version Numbers of SDADC_Ip.h and SDADC_Ip_Cfg.h are different Detailed description (how to reproduce it): AutoSar Version Numbers of SDADC_Ip.h and SDADC_Ip_Cfg.h are different !image-2023-03-08-08-56-22-798.png! ADC_SAR_IP_VENDOR_ID_CFG > SDADC_IP_VENDOR_ID_CFG !image-2023-03-08-08-57-08-812.png! Error has no right operand !image-2023-03-08-09-00-38-007.png! Preconditions: Test Case ID (internal TC that caught the defect) optional: ADC_TS_001 Observed behavior: Test generate failed Expected behavior: Test generate pass Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]

ARTD-59640	Bug	[ICU]Emios overflow interrupt flag in EDGE COUNTER mode incorrect
		
		Detailed description (how to reproduce it):
		in driver code interrupt flag of edge count mode is OVFL:
		if((EMIOS_ICU_MODE_NO_MEASUREMENT != eMios_Icu_Ip_ChState[eMios_Icu_Ip_IndexInChState[instance][channel]].channelMode) && bEnableInter)
		{
		#if (EMIOS_ICU_IP_OVERFLOW_NOTIFICATION_API == STD_OFF)
		bOverflow = ((eMIOS_S_OVFL_MASK == (u32RegCSR & eMIOS_S_OVFL_MASK)) ? TRUE : FALSE);
		#endif
		
		During debugmode, the interrupt flag for this mode is FLAG, not OVFL
		The driver code is using the wrong interrupt flag in edge counting mode
		Preconditions:
		using ICU's edge counting mode
		
		Test Case ID (internal TC that caught the defect) optional:
		Icu_TC_WBT_8094(Icu_TS_CC42)
		
		Observed behavior:
		interrupt flag in edge count mode incorrect in driver code
		
		Expected behavior:
		correct edge count mode interrupt flag in driver code
		
		Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)
		
		Proposed solution optional:
		interrupt flag in edge counting mode must be FLAG

ID	Subtype	Headline and Description
ARTD-59655	Bug	[Spi] halfduplex 8bit transmit and receive fail Detailed description (how to reproduce it): halfduplex receive fail when config frame size equal to number of bit mode (2bits, 4bits. 8bits) Minimum framzeSize should be 16bits for 8bits parallel mode, 8bits the others, refer to attachment Preconditions: NA Test Case ID (internal TC that caught the defect) optional: Spi_TS_120 cfg set 6, 7 Observed behavior: NA Expected behavior: NA Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Minimum framzeSize should be 16bits for 8bits parallel mode, 8bits the others Add constraint to Ebt and DS interface to guide user to configure
ARTD-59685	New Feature	[MemAcc] Integration with Mem_43_Infls need to be updated NewWorkDescription: Following by this PR of mem_infls: [https://bitbucket.sw.nxp.com/projects/ARTD/repos/mem_infls/pull-requests/4/ commits/03ec58cf045805a177a8182cac57cdca9dc467da#generic/config/EBT/Mem_InFls.xdm] The schema cfg of memacc need to update ASPathDataOfSchema from mem into Mem_43_InFls (see the attach photo 1) Also, dev test also need to update mem_43_infls.xdm and memacc.xdm(see the attach photos 2, 3) Fix gen fail on DS. Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Update code follow update on Mem Infls Update DS part fix generate fail build fail
ARTD-59852	Bug	[S32K3XX 300][port] Fix file version checking Detailed description (how to reproduce it): Fix all violation version checking Link station: [baltic.ea.freescale.net/0/project/download/ ZTpcbG9jYWxfMDFcb3V0cHV0XGFydGlmYWN0c1xjdXN0b21fZmlsZV92ZXJjaGVja2luZ1wyMDIzMDMxMDA1MDgwODUzNDAwMFxkb3dubG9hZHN http://baltic.ea.freescale.net/0/project/download/ ZTpcbG9jYWxfMDFcb3V0cHV0XGFydGlmYWN0c1xjdXN0b21fZmlsZV92ZXJjaGVja2luZ1wyMDIzMDMxMDA1MDgwODUzNDAwMFxkb3dubG9hZHN Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: reference link: [http://baltic.ea.freescale.net/0/project/custom_file_verchecking/details] !image-2023-03-10-14-04-06-996.png! Expected behavior: No file version checking errors. Please ensure all violations fix for your driver Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A

ID	Subtype	Headline and Description
ARTD-59937	Bug	[PORT] Missing .mux field in Siul2_Port_Ip_Cfg.c and several observations when using Pins tool Detailed description (how to reproduce it): Issue #1{color}: When using the Pins tool, it was noticed that there's an issue on generation files because of missing .mux field. This issue's happening on IP layer. {*}Issue #2{*}: Missing default pin(s) on Pins tool when creating new project. It causes the failing at build step on wizard data checking/testing. Issue #3: Unsupported target processor: S32K312 MQFP 172: !image-2023-03-12-20-59-48-906.png|width=574,height=317! Issue #4: Failling on generate step for S32K312 MQFP 100: !image-2023-03-12-21-01-44-595.png|width=587,height=290! Preconditions: With issue #1: S32K312/S32K322/S32K342/S32K341 derivatives, IP layer using Pins tool. With issue #2: S32K310/S32K394/S32M274 derivatives, IP layer using Pins tool. With issue #3, #4: S32K312 MQFP 172 and S32K312 MQFP 100: derivatives, IP layer using Pins tool. Test Case ID (internal TC that caught the defect) optional: All tests which is using Pins tool from IP layer Observed behavior: 4 kinds of issue founded. Expected behavior: No issues would be detected when delivering the packages. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-59948	Bug	[PWM] Driver compiler warning Detailed description (how to reproduce it): Have compiler warning for some compilers, see detail in attachment file. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Have drive warning Expected behavior: Build without compiler warning Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-59954	Bug	[ICU] Fix some warning errors Detailed description (how to reproduce it): In the drive code, there are still some warnings in the file described below Preconditions: run test Test Case ID (internal TC that caught the defect) optional: Icu_TS_082,Icu_TS_100,Icu_TS_102,Icu_TS_105,Icu_TS_107,Icu_TS_111,Icu_TS_112 Observed behavior: some warning errors exist in the description file below Expected behavior: no longer exist warning error exists in below description file Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: see some errors in the description file and fix these errors

ID	Subtype	Headline and Description
ARTD-60094	Bug	[CRYPTO] [S32K3XX] Some field's name in ECVD file is changed when import config from EB to CT Detailed description (how to reproduce it): Tag: PVT_CRYPTO_S32K3XX_300_V02 Testing site have a scenario to test ECVD : create project S32DS > export ra file ECVD > Import original EVCD file to EB> export EPC from EB> Import EPC to S32DS> Export new ECVD and compare folder generate of new ECVD with folder generate original ECVD. If the both folder generate ECVD similar , test pass. But when i run test check EVCD, i see some different when compare folder generate new ECVD and folder generate original ECVD. This error occurs at both of layer (HL and IPL). You can see detail at picture attach Diffrence index key element between EB and CT in Crypto_Cfg.c Test Case ID (internal TC that caught the defect) optional: Crypto_TS_COT_007 Observed behavior: Run test follow scenario to check ECVD and see some different between original ECVD and new ECVD Diffrence index key element between EB and CT: !image-2023-03-15-12-31-59-123.png! Expected behavior: Run pass test with no different between original ECVD and new ECVD No diffrence index key element between EB and CT in Crypto_Cfg.c Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-60085	Bug	[S32K3 3.0.0] Crypto: The oder of NVM and Ram key catalog are changed when import epc file to S32DS Detailed description (how to reproduce it): when user import epc file to S32DS the order of NVM and RAM keytalog are changed and it can lead to fail some test. You can try with config on attach file Preconditions: import epc file to s32ds Test Case ID (internal TC that caught the defect) optional: Crypto_TS_027, Crypto_TS_005 Observed behavior: the order of NVM and RAM keytalog are changed in S32DS Expected behavior: when import epc file to S32DS the order of the order of NVM and RAM keytalog aren't changed Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-60242	Bug	[LIN] Lin.h includes LinIf.h Detailed description (how to reproduce it): Lin in RTD 1.0 (S32K1xx): lin.h includes linif.h which causes circular inclusion error when using Vector stack. This was not included in MCAL 4.2 and 4.3 Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: lin.h includes linif.h which causes circular inclusion error when using Vector stack. Expected behavior: Error should not raise Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Analyze to remove include LinIf.h in Lin.h

ID	Subtype	Headline and Description
ARTD-60252	Bug	[Spi] Flexio have Rx overflow in slave mode - removal of feature Detailed description (how to reproduce it): Flexio spi had Rx overflow in slave mode if configuration cpha is TRAILING Preconditions: configuration cpha is TRAILING Test Case ID (internal TC that caught the defect) optional: Spi_TS_105 config FLEXIO_CPOL_CPHA_2, FLEXIO_CPOL_CPHA_4 Observed behavior: Transmit end with Rx overflow Expected behavior: Transmit end with Rx no overflow Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-60282	Bug	[LIN] Remove LPUART_MSC instance on K39x Detailed description (how to reproduce it): LPUART_MSC is a special resource and it only support the Receive Interrupt, not Transmit Interrupt. So this instance can't apply for Lin driver because Lin driver need both Receive and Transmit Interrupt. Preconditions: Config LPUART_MSC Test Case ID (internal TC that caught the defect) optional: None Observed behavior: LPUART_MSC is not working on Lin driver Expected behavior: Remove LPUART_MSC from resource of Lin driver Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Remove LPUART_MSC from resource of Lin driver and update some config file which generate.
ARTD-60348	Bug	[S32K3 3.0.0][MemAcc] error while writing data to address of second SubAddressArea Detailed description (how to reproduce it): MemAcc_GetSubAddressArea return wrong value of subarea Step 1: call MemAcc_Init Step 2: call MemAcc_Write with address in second SubAddressAres Step 3: Call MemAcc_Compare to compare data written Preconditions: Test Case ID (internal TC that caught the defect) optional: MemAcc_TC_FCT_0202 Observed behavior: data not written correctly in second SubAddressArea !screenshot-1.png|thumbnail! Expected behavior: data written correctly in second SubAddressArea Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA

ID	Subtype	Headline and Description
ARTD-60435	New Feature	[MCU] Remove I3C Driver from RTD release CR description: Need to remove I3C driver from release , IP shall not be used. Errata: ERR051298: I3C: The I3C feature may not work reliably Description: The I3C module may not be 100% reliable to fulfill the protocol. This feature is not recommended for use. Workaround: There is no workaround for this. Reason for this change: Errata, IP unusable Benefit: Customer do not use depreciated IP Onetime CR/Strategic CR: Onetime CR Use-case: na HW documentation reference (as applies): Errata ERR051298 (see errata docuemnts) HW/Application Engineer contact (as applies):{*}{*} Luis Garabito Siordia Note: relevant documents to be attached to the ticket.
ARTD-60738	Bug	[PWM] Unresolved symbol Pwm_Ipw_ValidateModuleId and Pwm_ValidateModuleId function when using FastUpdate Detailed description (how to reproduce it): Unresolved symbol Pwm_Ipw_ValidateModuleId and Pwm_ValidateModuleId functions when using FastUpdate and enable DEV_ERROR_DETECT If sync update is not enable > Pwm_Ipw_ValidateModuleId function is not defined. but in fast update still using it. so it cause fail error Preconditions: enable FastUpdate Enable dev error detect Test Case ID (internal TC that caught the defect) optional: Pwm_TS_015 Observed behavior: build error Expected behavior: no build error Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]

4.3 Change List for 2.0.3

ID	Subtype	Headline and Description

4.4 Change List for 2.0.1

ID	Subtype	Headline and Description
ARTD-24427	Bug	[CRYPTO] Error VKMS_ERR_SMALL_BUFFER should be stored on pResult[CRYPTO_CUSTOM_RESP_STATUS_OFFSET_U32] Detailed description (how to reproduce it): Error code VKMS_ERR_SMALL_BUFFER is be stored on pResultLength[CRYPTO_CUSTOM_RESP_STATUS_OFFSET_U32] , but it have to stored in pResult[CRYPTO_CUSTOM_RESP_STATUS_OFFSET_U32] Preconditions: Call function with length of data is set to 1 Test Case ID (internal TC that caught the defect) optional: Crypto_TC_FCT_VKMS_0003 Observed behavior: Error code VKMS_ERR_SMALL_BUFFER is be stored on pResultLength[CRYPTO_CUSTOM_RESP_STATUS_OFFSET_U32] Expected behavior: Error VKMS_ERR_SMALL_BUFFER should be stored on pResult[CRYPTO_CUSTOM_RESP_STATUS_OFFSET_U32] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-26550	Bug	[CRYPTO] Analyze the case to avoid Dir. 4.7 even false positives Detailed description (how to reproduce it): MISRA reports false positive Dir. 4.7, for more details see ARTD-26511 Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: There is no Dir. 4.7 reported in the MISRA report Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Analyse all the cases of Dir. 4.7 and design a solution(if possible) that does not duplicate the checks.

ARTD-27732	New Feature	[CRYPTO][S32K344][STD] Update the corresponding resource files with HSE_S32K3XX_0.2.1.0_RC1 interface
		
		NewWorkDescription:
		Update resource files:
		# Crypto.HseSptHmac.<HSE FW TYPE> : Support for HMAC_SHA2_(224, 256) as defined in FIPS PUB 198-1 and SP 800-107.
		To =>> # Crypto.HseSptHmac.<HSE FW TYPE> : Support for HMAC_SHA2_(224, 256, 384, 512*) as defined in FIPS PUB 198-1 and SP 800-107.
		Added:
		# Crypto.HseAesBlockModeMask.<HSE FW TYPE> : Support for Cipher modes flags for AES keys.
		# Crypto.HseEccKeyFormat.<HSE FW TYPE> : Support for HSE ECC key format.
		
		Requirement source:
		[...]
		(e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...)
		
		Proposed solution optional:
		[....]

ID	Subtype	Headline and Description
ARTD-27890	Bug	[CRYPTO] Fix Key Generate and Key Derive functions when functionality is disabled from resource Detailed description (how to reproduce it): Run TS 001 when key generation and derivation are disabled from resource Preconditions: GM driver flavour Test Case ID (internal TC that caught the defect) optional: TS 001 Observed behavior: Functions returns E_OK instead of E_NOT_OK Expected behavior: Function returns NOT_SUPPORTED. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: !image-2022-06-17-18-54-14-290.png|thumbnail!
ARTD-28139	New Feature	[CRYPTO][S32K344][STD] Add interface HSE_S32K3XX_0.2.1.0_RC2 NewWorkDescription: Integrate new HSE_S32K3XX_0.2.1.0_RC2 interface. Requirement source: HSE (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Create an excel with the comparison of the new interface with old interface Add the new headers in the crypto repo Add the fw image in the crypto repo Update resource files if there is any changes
ARTD-28183	Bug	[CRYPTO] Function Hse_Ip_GeneralPurposeIrqHandler in Hse_Ip does not follow reqs CPR_RTD_00011 and CPR_RTD_00664 Detailed description (how to reproduce it): Function Hse_Ip_GeneralPurposeIrqHandler() tries to process information even when the driver is not initialized. Preconditions: Driver is not initialized Test Case ID (internal TC that caught the defect) optional: FMEA Analysis Observed behavior: Function executes it's body even when driver is not initialized Expected behavior: Function executes it's body when driver is initialized. Please see reqs CPR_RTD_00011 and CPR_RTD_00664 Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Execute function's code when driver is intialized.
ARTD-28586	Bug	[CRYPTO] Fix Misra violations for S32K344 201 Detailed description (how to reproduce it): There is one Misra violation in the Crypto driver: 22222925 MISRA C-2012 Rule 8.13 The pointer variable "base" points to a non-constant type but does not modify the object it points to. Consider adding const qualifier to the points-to type. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: There is one Misra violation: MISRA C-2012 Rule 8.13. Expected behavior: There is no Misra violation in the Crypto driver Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]

4.5 2.0.0

ID	Subtype	Headline and Description
ARTD-6142	New Feature	[PORT] S32K3 ADC channels mux select<*> There are some ADC channels that can be routed to more than one PAD. Such as ADC1_S14, it can be mapped to PTC5 or PTB0. These settings are included in the register DCMRWF4. Is it possible to include this feature in s32ds CT pin config or in PORT module?
ARTD-9555	New Feature	[mcu] Padkeeping auto enabled leading to siul stuck after standby wakeup<*> Pad keeping is enabled by default[0-enable;1-disable]. If user do not set it. After wakeup from standby, without disabling it, the siul module can't be set again. So User need to be notified in S32CT[power module] whether need to enable pad keeping function. Attached is the test code on S32DS3.4+RTD 0.9.0 beta.
ARTD-9729	New Feature	[ICU][CMP] Output Int. Trigger<*> There's no way to select the "INTTRIG_NONE" option in the graphical config. Tool. Therefore, it's not possible to only enable the Round-Robin interrupt.* Which is sometimes required for STANDBY wake-up operation.
ARTD-10734	Bug	[PWM] Redundant parameter configuration on both Higl level and IP level<*> Detailed description (how to reproduce it): Period, (initial) duty cycle, notification and polarity need to be configured in several places while there is a cross check between these parameters, the issue creates a major inconvenience for platform where it is expected to have a large number of PWM channels (like K3). For instance: To set up Period the user must write a value in: Pwm/PwmChanel/PwmPeriodDefault Pwm/PwmEmiosChannel/EmiosChPeriod and when master bus is used: Mcl/EmiosCommon/EmiosMclMasterBus/EmiosMclDefaultPeriod In case of MasterBus configuration this issue become serious since the user configures a period inside the channel but that period value is ignored and the PWM output will be different from the one expected by usr. Preconditions: master bus is configured in MCL and OPWMT mode is selected for PWM channel. Test Case ID (internal TC that caught the defect) optional: none Observed behavior: PWM period is not the one user configured in PWM. Expected behavior: Parameters should be configured only once (see proposed solution) Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: In most cases the input parameter should be at high level (Pwm channel) definition. There is no need for a period, duty, polarity or notification parameters at IP, in configuration. For eMIOS channels that use Master bus, the period should be written only in MCL and PWM DefaultPeriod parameter should be ReadOnly with its value automatically calculated based on the MCU frequency and the period value from Mcl/EmiosCommon/EmiosMclMasterBus/EmiosMclDefaultPeriod.
ARTD-11235	New Feature	[PWM] Timer drivers should have reference to MCL and MCU common configurations<*> _*Detailed description (how to reproduce it): When drivers use common resources from other drivers, these resources should be accessed via references to those drivers. For instance in case OCU, PWM and ICU when configured to use eMIOS IP, they might use a common bus configured in MCL. The configuration of each drivers should reference the bus configuration to access certain parameters that may be needed in their internal logic (number of configured counter ticks, dividers etc). Using a reference might also insure that invalid configuration of the bus are not exported to driver. Internal references which are NOT configured by the user SHOULD not be used since they might mask problems. PWM, OCU and GPT drivers should always use references to MCU driver even in cases where AUTOSAR does not require it since a reference to MCU clock will make much easier to determine the frequency of the given channel... For ICU this is not needed since in all cases the result of the ICU measurement is in ticks. Preconditions: [none] Test Case ID (internal TC that caught the defect) optional: [none] Observed behavior: [see description] Expected behavior: [see description] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:

ID	Subtype	Headline and Description
ARTD-12331	New Feature	[BUILD_ENV] Update Ecuc.xdm in project template to match newly added container<*> NewWorkDescription: EcucPduCollection is de-populated after the tresosproject.pl script is run at generation. This causes drivers dependend on that container (i.e Fr) to fail at generation. Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Add EcucPduCollection in the new template.
ARTD-14050	New Feature	[I3C] Add support for In-band interrupt (IBI)<*> NewWorkDescription: In-band interrupt (IBI) Please refer to initial analysis done in https://nxp1.sharepoint.com/:x:/r/sites/Zebra/Shared%20Documents/Group%204/I3C/I3C_Analysis.xlsx?d=w15656ae7d09a4b49939fa7d8e84207c3&csf=1&web=1&e=RiyG9f Check if requirement available or need any updates Create/update dev test Add section/update UM Update UML if required If examples already available, update examples with any eventual new nodes Requirement source: RM.pdf Proposed solution optional: brief Perform a Slave Request on the I3C bus. details This function is used to request an In-Band Interrupt, Hot-Join, or Master Request IbiData and ExtData parameters are used only ive the Event is an In-Band Interrupt. If the Event is not an In-Band Interrupt, these parameters are ignored in the API's implementation. IbiData and ExtData are ignored if the In-Band Interrupt has no mandatory byte. If the In-Band Interrupt has only one mandatory byte, ExtData is ignored. param[in] Event Type of the event: IBI, HJ, MR param[in] IbiData If IBI, the mandatory byte param[in] ExtData If IBI and more than one madatory byte, pointer to the extra bytes / I3c_Ip_StatusType I3c_SlaveRequestEvent(const I3c_SlaveRequestType Event, const uint8 IbiData, uint8 ExtData);
ARTD-14051	New Feature	[I3C] Add support for Hot-join<*> NewWorkDescription: Hot-join Please refer to initial analysis done in https://nxp1.sharepoint.com/:x:/s/Zebra/EedqZRWa0ElLk5-n2OhCB8MByBV0CEBRFInle2wexrt_0g?e=TP6TXV Check if requirement available or need any updates Create/update dev test Add section/update UM Update UML if required If examples already available, update examples with any eventual new nodes Requirement source: RM.pdf Proposed solution optional: [...]
ARTD-14054	New Feature	[I3C] Add exclusive areas support<*> Implement exclusive areas https://nxp1.sharepoint.com/:p:/s/Zebra/EehFcYqIlpVJkmyNp8pcae4BNyizwm47eVxbN_s7u30Tzg?e=gTPmi7 Analyze and try to move in IPL, to have exclusive areas as small as possible. See details in presentation and recording Take into account also BSWMD guideline: https://confluence.sw.nxp.com/display/AUTORD/BSWMD
ARTD-14839	Bug	[RM] Incorrect DERR used for XRDC_1<*> Detailed description (how to reproduce it): In _Xrdc_Ip_GetDomainIDErrorStatus_ function, the Xrdc_DomainErrorWord array, which contains the DERR word index positions, are both used two instance, which is not matched with XRDC_1. Also the loop checks through XRDC_NUMOF_DOMAIN_ERROR_WORD indexes, which is 17, however in XRDC_1 there are only 7 indexes. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: In _Xrdc_Ip_GetDomainIDErrorStatus_ function, the _Xrdc_DomainErrorWord array and XRDC_NUMOF_DOMAIN_ERROR_WORD are used for both of these two XRDC instances, which is not correct Expected behavior: Correct values are used for XRDC_1 in _Xrdc_Ip_GetDomainIDErrorStatus_ function Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-15328	New Feature	[LIN] Implement CPR_RTD_00543.lin (MR-200)<*> NewWorkDescription: Driver should implement req as below: Req ID||Object Text||Verification Criteria CPR_RTD_00543.lin|The driver shall prevent configuration of the same hardware instance between HL configuration and standalone IP configuration.|Test Case Requirement source: CPR_RTD_00543.lin (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Implement CPR_RTD_00543.lin
ARTD-15535	New Feature	[SPI] Implement new requirement: CPR_RTD_00543.spi<*> NewWorkDescription: Implement new requirements: CPR_RTD_00543.spi and CPR_RTD_00544.spi Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Follow guiding: https://nxp1.sharepoint.com/:p:/r/sites/Zebra/_layouts/15/Doc.aspx?sourcedoc=%7B28A51BA3-C452-40F5-ABB6-A6933671DCD3%7D&file=NXP_RTD_AUTOSAR_S32CT_V2.pptx&action=edit&mobileredirect=true
ARTD-15574	New Feature	[ADC] Parameter for Adc_CtuEnableHwTrigger() should be defined as symbolic values or enums<*> Detailed description (how to reproduce it): In order to enable HW triggering via BCTU mode the user must call Adc_CtuEnableHwTrigger() with the correct trigger source. This trigger source is configurable and enabled in /Adc/AdcConfigSet/BctuHwUnit//BctuInternalTrigger via BctuTriggerSource parameter. However that value is NOT generated anywhere, and the user is unaware what is the correct value for which the Adc_CtuEnableHwTrigger(_Adc_CtuTrigSrcType Trigger_) will work. The documentation does not provide a table o value and Adc_CtuTrigSrcType is defined as integer. Preconditions: BCTU mode configure. Test Case ID (internal TC that caught the defect) optional: note Observed behavior: Function fails at compile time which may happen if the application references the /Adc/AdcConfigSet/BctuHwUnit//BctuInternalTrigger container and expects that a define value is generated in ADC from BctuTriggerSource. Function fails at run time if application does not call Adc_CtuEnableHwTrigger() with the correct index in the list of triggers described in the Reference Manual (chapter 55.1.2) and there is not direct correlation between the table in the RM and the enum used for defining BctuTriggerSource in Adc.xdm. So finding the correct value become a matter of try and error. Expected behavior: [...] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Define Adc_CtuTrigSrcType as enum containing the list of triggers expected by Adc_CtuEnableHwTrigger(). The labels of this enum should be identical with the labels used for BctuTriggerSource.

ID	Subtype	Headline and Description
ARTD-15901	New Feature	[I3C] Implement I3c_SetBaudRate and I3c_GetBaudRate<*> NewWorkDescription: There are some remaining features need to be implemented: / brief Set the baud rate for all subsequent I3C communications. details This function is used to set the baud rate for all subsequent I3C communications. param[in] Instance I3C instance param[in] I2cBaud I2c baud param[in] OpenDrainBaud Open Drain baud param[in] PushPullBaud Push pull baud / Std_ReturnType I3c_SetBaudRate(const uint32 Instance, const uint8 I2cBaud, const uint8 OpenDrainBaud, const uint8 PushPullBaud); / brief Get the baud rate of the I3C module. details This function is used to get the baud rate of the I3C module. param[in] Instance I3C instance param[in] I2cBaud I2c baud param[in] OpenDrainBaud Open Drain baud param[in] PushPullBaud Push pull baud / Std_ReturnType I3c_GetBaudRate(const uint32 Instance, uint8 I2cBaud, uint8 OpenDrainBaud, uint8 PushPullBaud); Requirement source: RM (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]
ARTD-16302	Bug	[ADC] AdcPreSamplingOnce has no effect on generated code<*> Detailed description (how to reproduce it): AdcPreSamplingOnce has no effect on codegen of EB/CT UI, should be not editable with default value as "enabled" base on current driver implementation Preconditions: AdcPreSamplingOnce must be fully supported with ON/OFF feature Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: AdcPreSamplingOnce has no effect on generated code. Expected behavior: All nodes should have effect on generated code/be used by the driver. AdcPreSamplingOnce is fully supported Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Add support AdcPreSamplingOnce
ARTD-17307	Bug	[S32DS] There are many Semantic errors message raised by S32DS but they are already defined in the project<*> Detailed description (how to reproduce it): There are many Semantic errors message raised by S32DS but they are already defined in the project and the project still build successful. This kind of error will be only appeared in almost of files after open them. They are not raised if the source files are not opened. This problem is appeared on all RTD releases, can check this problem on Examples project. !image-2021-09-27-14-22-49-376.png! Preconditions: The problem can be also reproduced on S32K3: Install the packages: S32 Design Studio 3.4 Service pack 2 with S32K3xx development package build 210923 [LINK|https://nxp1.sharepoint.com/sites/freeshareprivate/S32DSproject/Lists/Builds/DispForm.aspx?ID=1744] RTD S32K3XX RTM100 update side Open example: Can_example_S32K344 Generate code by press "Update code" button on GUI of peripheral tool Build project Open some source files in "RTD" and "board" folders in the project on S32DS GUI Test Case ID (internal TC that caught the defect) optional: Examples project Observed behavior: Semantic errors appears but they are already defined in other files and the project still build successfully Expected behavior: There is no Semantic errors Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA

ID	Subtype	Headline and Description
ARTD-17156	New Feature	[SENT] Improve Received Message Diagnostics for sent driver<*> NewWorkDescription: Implements for each channel all receiver diagnostics as specified by the SAE Specifications. 1. Calibration pulse length < 56 clock ticks – 25% or > 56 clock ticks 25%. *2.* *Not the expected number of falling edges between calibration pulses. (Message length is pre-defined by each sensor device). 3. Checksum error. 4. Any nibble data values measured as < 0 or > 15. *5. Successive Calibration Pulses. Sent driver need to improve to implement #2 and #5*. Requirement source: SAE Specifications Proposed solution optional: NA
ARTD-17198	Bug	[SPI] SPI_EXCLUSIVE_AREA_02 is missing in bswmd file<*> Detailed description (how to reproduce it): SPI_EXCLUSIVE_AREA_02 is not assigned to any function in bswmd file. This results in compiler error as this exclusive area is not generated by Autosar RTE. Preconditions: Spi driver used with Autosar RTE Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Exclusive areas 02 is not generated by Autosar RTE Expected behavior: Exclusive areas 02 is generated by Autosar RTE Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update the exclusive_areas_to_be_defined_in_bsw_scheduler.dox to map the exclusive areas to a function which is generated into bswmd file.
ARTD-17241	New Feature	[I3C] Input parameter "Instance" should be uint8 ,,"Input parameter ""Instance"" should be uint8 instead of uint32.
ARTD-17268	Bug	[ADC] Unused ADC_MAX_HARDWARE_TRIGGERS define when CTU hardware trigger API is disabled<*> Detailed description (how to reproduce it): ADC_MAX_HARDWARE_TRIGGERS is unused if ADC_ENABLE_CTUTRIG_NONAUTO_API is STD_OFF. Preconditions: EB or CT config with CTU trigger mode disabled. Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: ADC_MAX_HARDWARE_TRIGGERS is generated when CTU trigger mode is not enabled. Expected behavior: ADC_MAX_HARDWARE_TRIGGERS should only be generated when CTU trigger mode is enabled. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-17358	Bug	[I3C] Arrays are generated from CT even if they contain no elements<*> Detailed description (how to reproduce it): [...] Build plugin and import example in S32DS. Configure IBI Address Registry and Dynamic Address List arrays with no elements and generate. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] !image-2021-09-30-15-25-55-475.png! !image-2021-09-30-15-26-17-595.png! Expected behavior: [...] These arrays should not be generated in PBcfg.c if they contain no elements. In master config structure they should be generated with NULL_PTR, in this case. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-17424	Bug	[gpt] Array indices are not correctly generated in DS when multicore support is enabled<*> Detailed description (how to reproduce it): Array index is wrong when the structures are generated per partition, as you can see in attached pictures. !image-2021-10-01-15-17-19-822.png! !image-2021-10-01-15-17-36-860.png! Preconditions: to use Design Studio as config tool to use at least one partition Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: the index is equal with the array size Expected behavior: the index should be the correct one Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: to update the templates to generate the correct index
ARTD-17496	Bug	[ICU] check DMA notification function name 'dmaLogicChannel_InterruptCallback' is wrong<*> Detailed description (how to reproduce it): when configuring more than 1 Mcl DMA channel, if configuring the name of the first channel as 'dmaLogicChannel_Type_1' and the name of the next channel as 'dmaLogicChannel_Type_13' and only one Icu channel configured as a DMA link is used to 'dmaLogicChannel_Type_13'. The node 'dmaLogicChannel_InterruptCallback' in Mcl will be wrong. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-17507	Bug	[ADC] Missing exclusive areas in bswmd file<*> Detailed description (how to reproduce it): The folowing excusive areas is not getting generated in rte.c: ADC_EXCLUSIVE_AREA_17 ADC_EXCLUSIVE_AREA_23 ADC_EXCLUSIVE_AREA_24 ADC_EXCLUSIVE_AREA_26 ADC_EXCLUSIVE_AREA_27 ADC_EXCLUSIVE_AREA_39 ADC_EXCLUSIVE_AREA_40 ADC_EXCLUSIVE_AREA_69 ADC_EXCLUSIVE_AREA_70 They are not generated because these exclusive areas are missing or not assigned to a function in bswmd file. Preconditions: Adc driver used with Autosar RTE Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Exclusive areas not generated by RTE Expected behavior: Exclusive areas are generated by RTE Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Add exclusive areas into bswmd file. Internally update the exclusive_areas_to_be_defined_in_bsw_scheduler.dox file to map the exclusive areas to functions and then also add the IP functions into NonASR_ServiceID.xml file.
ARTD-17527	New Feature	[S32K3xx] Only files .c and .h should be showed on Code preview of Peripheral tool<*> Step: 1.Create project S32K3xx attach sdk RTD 1.0.0 with gcc10.2/ghs/iar toolchain 2. Open Peripheral tool, then check Code Preview 3. Add any sdk component then check Code Preview Observed behavior: 2,3: Many files .ecpd (about 70-90 files) are showed Expected behavior: 2,3: Only necessary files .c and .h should be showed

ID	Subtype	Headline and Description
ARTD-17564	Bug	[ADC] Open findings from code review checklist<*> Detailed description (how to reproduce it): Fix remaining findings that were postponed on ARTD-15668. #|Source Code file|Issue |Proposed Correction|Status|Comment 1|All EB and CT generate files using AdcEnableDmaTrasferMode and CtuEnableDmaTrasferMode nodes|Rule 3|AdcEnableDmaTransferMode, CtuEnableDmaTransferMode|Postponed|Postponed due to affect test code 5|All files using source file version information of IPW, some header wrappers in IPL.|Rule 19,25: some defines don't have appropriate prefix equivalent to layer (HLD/IPW/IPL)|Add prefix ADC_IPW, ADC_SAR_IP, BCTU_IP to defines|Postponed|Postponed due to affect test code 6|Adc_Sar_Ip_Types.h|Rule 20,25: RESOLUTION_x of Adc_Sar_Ip_Resolution doesn't have prefix|Add prefix ADC_SAR_IP to defines and update generation code|Postponed|Postponed due to affect test code 7|Adc_Ipw_Types.h|Rule 22: Some typedef missing Ipw prefix|Add prefix Ipw to typedefs|Postponed|Postponed due to affect test code 9|Adc.c, Adc_Ipw.c, Adc_Ip.c, Ctu_Ip.c, Bctu_Ip.c|Rule 28|Correct prefix of global variables|Postponed|Postponed due to affect test code Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: NA Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-17575	New Feature	[BUILD_ENV] Update compiler options<*> NewWorkDescription: There are some points conflict and needs to update after review and compare compiler option between SOW with S32DS in the ticket _**_ ARTD-16608 # For GHS: !image-2021-10-06-18-58-23-983.png! Option “-nostartfiles” is an linker option. It also mentioned in GHS document: !image-2021-10-06-18-44-13-702.png! So, this option should be moved from Compiler section to Linker section in excel file [LINK|https://nxp1.sharepoint.com/:x:/r/sites/Zebra/Shared%20Documents/Tools%20(build,%20misra,%20vsmd,%20etc)/Compilers/RTD_Compiler_Options.xlsx?d=wc54fdf4ed62b4036b28bba16838efb73&csf=1&web=1&e=qdKltI] 2. For IAR: !image-2021-10-06-18-57-39-415.png! The define "-DEU_DISABLE_ANSILIB_CALLS" is only used in EUnit.c for testing and not used in our driver code. So it should be removed from our compiler option and move to EUnit. Option “-c” is described in excel file but it is not exist on IAR compiler. So, this option should be removed. !image-2021-10-06-18-56-53-569.png! For more detail please check in email attached. Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: NA
ARTD-17576	Bug	[PWM] Debug and correct nightly build<*> Detailed description (how to reproduce it): Investigate, debug and correct test case that runs nighly on the board. Driver bamboo is failing with inconsistent data on runtime for PWM see log. !image-2021-10-06-15-49-24-543.png|width=843,height=224! [https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?FolderCTID=0x012000D681AD520E486343AF1E2AF7AEE3B740&id=%2Fsites%2FZebra%2FShared%20Documents%2FNightly%2FEmailMessages%5F10%5F2021%2FreportBLNRTD44S32K3XX10058%5F1776126004%2Ehtml&parent=%2Fsites%2FZebra%2FShared%20Documents%2FNightly%2FEmailMessages%5F10%5F2021] Preconditions: NA Test Case ID (internal TC that caught the defect) optional: Nightly Observed behavior: test case failing on run Expected behavior: test pass Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA

ID	Subtype	Headline and Description
ARTD-17579	Bug	[ICU] Debug and correct nightly build<*> Detailed description (how to reproduce it): Investigate, debug and correct test case that runs nighly on the board. Driver bamboo is failing with test execution fails : see in build [artifact|https://bamboo3.sw.nxp.com/artifact/ARTD-CIICU/BRT/build-46/Dev-Tests-Artifacts/dev_tests_reports/S32K3XX_4.4/gcc] !image-2021-10-06-15-49-24-543.png|width=843,height=224! [https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?FolderCTID=0x012000D681AD520E486343AF1E2AF7AEE3B740&id=%2Fsites%2FZebra%2FShared%20Documents%2FNightly%2FEmailMessages%5F10%5F2021%2FreportBLNRTD44S32K3XX10058%5F1776126004%2Ehtml&parent=%2Fsites%2FZebra%2FShared%20Documents%2FNightly%2FEmailMessages%5F10%5F2021] Preconditions: NA Test Case ID (internal TC that caught the defect) optional: Nightly Observed behavior: test case failing on run Expected behavior: test pass Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-17583	New Feature	[RM] XRDC shall allow locking the XRDC registers<*> NewWorkDescription: A safety requirement (ARSW-46) requires that XRDC configuration to be lock-able, to prevent other master changing it. Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Support locking the XRDC configured registers, as a configuration option. Could be done by having some extra masks or in a separate step at the end of init.

ARTD-17736	Bug	[FLS] Qspi_Ip_Read function checks error callout for NULL_PTR instead of ECC callout<*>
		
		Detailed description (how to reproduce it):
		Source code : Qspi_Ip.c
		Function : Qspi_Ip_Read
		There is a process to call eccCheckCallout on line 1168, but line 1166 checks whether errorCheckCallout is NULL_PTR. We believe that it is necessary to check eccCheckCallout.
		/ Call user callout, if available, to check ecc status /
		if ((STATUS_QSPI_IP_SUCCESS == status) && (NULL_PTR != state->configuration->errorCheckCallout))
		{
		status = state->configuration->eccCheckCallout(instance, crtAddress, chunkSize);
		}
		Preconditions:
		N/A
		Test Case ID (internal TC that caught the defect) optional:
		N/A
		Observed behavior:
		errorCheckCallout is checked if it is NULL_PTR
		Expected behavior:
		eccCheckCallout shall be checked if it is NULL_PTR
		Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)
		Proposed solution optional:
		Replace the check for NULL_PTR as follows (errorCheckCallout modified to eccCheckCallout):
		/ Call user callout, if available, to check ecc status /
		if ((STATUS_QSPI_IP_SUCCESS == status) && (NULL_PTR != state->configuration->eccCheckCallout))
		{
		status = state->configuration->eccCheckCallout(instance, crtAddress, chunkSize);
		}

ARTD-17766	New Feature	[Wdg] Replace Swt_Ip_FeatureDefine.h with resource symbols and generate in CfgDefines.h<*> NewWorkDescription: [Wdg] Replace Swt_Ip_FeatureDefine.h with resource symbols and generate in CfgDefines.h Requirement source: Internal refactoring Proposed solution optional: [Wdg] Replace Swt_Ip_FeatureDefine.h with resource symbols and generate in CfgDefines.h
ARTD-17794	Bug	[ADC] WDG and EOC might be stuck in Handler with spurious interrupt<*> WDG and EOC function are still available in IPL after disable them from configurator. Only ISR for them are disabled, that can lead to stuck in handler infinite since cannt clear its flag The proposal is to disable all functions related to these feature if disabled on UI and need to handle spurious interrupt for this case

ID	Subtype	Headline and Description
ARTD-17796	Bug	[CRYPTO] Fix compiler warnings reported in S32K3XX 1.0.0 P01 for GM releases<*> Detailed description (how to reproduce it): There are 3 compiler warnings that are listed in the attached Compiler Warnings report. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: Crypto_TS_DefineCompile_cfg1_CORE0 Crypto_TS_DefineCompile_cfg2_CORE0 Observed behavior: [...] Expected behavior: No compiler warnings present Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:
ARTD-17800	New Feature	[RM] Improve code for XRDC, common for all platforms ,,"Detailed description (how to reproduce it): Currently, some PID APIs support only 1 instance. But with new platform which may have more than one instance. So those APIs should be update to support. Preconditions: on platform which is support PID feature Test Case ID (internal TC that caught the defect) optional: Dev test 001 Observed behavior: NA Expected behavior: NA Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update to support multi instances
ARTD-17802	Bug	[S32K3xx] Board and RTD folder should be excluded after detach SDK<*> Preconditions: Install *S32DS 3.5 B211006* RTD package for S32K3xx: B211007 (S32K3XX_RTD_4_4_RTM_1_0_0_DS_updatesite_2110.zip) Test Case: # Create project enable SDK S32CT for any processors (ex: S32K344) # Right-click on project → SDKs → Detach SDK # Check board and RTD folder Observed behavior: RTD and board folder are still *included Expected behavior: RTD and board folder should be excluded Note: This issue is also happened in S32DS 3.4 Update 3 with this RTD package. And It *is not happended in S32DS 3.4 Service pack 2 release _RTD package for S32K3xx: B211007 (*S32K3XX_RTD_4_4_RTM_1_0_0_DS_updatesite_2110.zip)
ARTD-17812	Bug	[Adc] MISRA Rule 8.5 Symbol "Adc_Sar_x_Isr" is declared more than once. ,,"Detailed description (how to reproduce it): Symbol ""Adc_Sar_x_Isr"" is declared more than once. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Symbol ""Adc_Sar_x_Isr"" is declared more than once. Expected behavior: Violation is fixed Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:
ARTD-17847	Bug	[S32K3] RTD 1.0.0 code generation fails in S32 Design Studio<*> Installed the SW32K3_RTD_4.4_1.0.0_DS_updatesite_D2110.zip inside the S32 Design Studio IDE v3.4 Service Pack 2, following the instructions from the Release Notes (...it must be installed by opening Help > S32 Design Studio Extensions and Updates > Add Update Sites and selecting the archive file containing the S32 RTD software and then check the S32 RTD software package to be installed and continue the installation process.) Imported Uart_Example_S32K344, then pressed the Update Code button the following error is generated (please see attached error.png) Same behavior is reproductible for other examples as well (e.g. Pwm_Example_S32K344)

ID	Subtype	Headline and Description
ARTD-17865	New Feature	[I3c] Integrate DAA in Init function<*> NewWorkDescription: Integrate DAA in Init function Array is already generated by configurator. Need to call API in init with generated array Also add a configurator checkbox & define to allow users to enable/disable this functionality Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]
ARTD-17849	New Feature	[I3c] Validate support for Dynamic Address Assignment<*> NewWorkDescription: Please refer to initial analysis done in [https://nxp1.sharepoint.com/:x:/s/Zebra/EedqZRWa0ElLk5-n2OhCB8MByBV0CEBRFInle2wexrt_0g?e=TP6TXV] Check if requirement available or need any updates Create dev test with Dynamic Addressing use 2 boards with I3C Fix findings. Requirement source: RM.pdf Proposed solution optional: [...]
ARTD-17867	New Feature	[I3c] Implement methods to set the slave status activities<*> NewWorkDescription: Implement methods to set the slave activities which are returned by GETSTATUS command. Check if all bitfields should be set by the user. Check if requirement available or need any updates. Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]
ARTD-17898	Bug	[RM] Update the MRC granularity constraints<*> Detailed description (how to reproduce it): The XRDC MRC granularity and alignment restrictions have been increased from 32 bytes to 4KB in newer RM versions. This needs to be updated in the Tresos and CT field checks, to enforce the new values. more details in the attached email thread. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Review the RMs for the Notes mentioning this details, update the CT and EBT schema validations to enforce this new values. [...]
ARTD-17931	Bug	[Wdg] When WdgDevErrorDetect disabled, some generated defines are not used ,,"Detailed description (how to reproduce it): When WdgDevErrorDetect disabled, some generated defines are not used MISRA C-2012 Rule 2.5 1164 Advisory Low Quality Macro ""WDG_TIMEOUT_VALUE_ARRAY"" is defined but never used. /ARTD-CIW55-9/sources/SJA11XX_4.4/output/SJA11XX_SJA1110/wdg/Wdg_TS_Shared_000_cfgPB_CORE0/generate_tresos/include/Wdg_Cfg_Defines.h 228 Intentional Dismissed This violation requires information for indirect service mode MISRA C-2012 Rule 2.5 1164 Advisory Low Quality Macro ""SWT_TIMEOUT_VALUE_ARRAY"" is defined but never used. /ARTD-CIW55-9/sources/SJA11XX_4.4/output/SJA11XX_SJA1110/wdg/Wdg_TS_Shared_000_cfgPB_CORE0/generate_tresos/include/Swt_Ip_Cfg_Defines.h 100 Intentional Dismissed This violation requires information for indirect service mode MISRA C-2012 Rule 2.5 1164 Advisory Low Quality Macro ""WDG_IPW_TIMEOUT_VALUE_ARRAY"" is defined but never used. /ARTD-CIW55-9/sources/SJA11XX_4.4/output/SJA11XX_SJA1110/wdg/Wdg_TS_Shared_000_cfgPB_CORE0/generate_tresos/include/Wdg_Ipw_Cfg_Defines.h Preconditions: Direct service mode disabled Test Case ID (internal TC that caught the defect) optional: N.A. Observed behavior: See description Expected behavior: Defines are not generated if not used Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Only generate when WdgDevErrorDetect enabled in both S32CT and EBT

ID	Subtype	Headline and Description
ARTD-17933	Bug	[I2c] Cannot migrate EB tresos configuration to CT configuration because note slave address<*> Detailed description (how to reproduce it): [...] I converted example from EB to CT. I import i2c.epc file to CT. Open peripheral tool in S32DS. Have error CDD_i2c component. I saw that the node error belong to Ip layer. It should not add in HLD CDD_i2c component. !image-2021-10-18-16-59-18-790.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...] Remove node slave address on CT configuration
ARTD-17951	Bug	[ADC] Unused ISR code when interrupts are disabled in HLD configurator AdcInterrupt tab<*> Detailed description (how to reproduce it): At IPL for all IPs, ISRs are not removed at precompiled, even if interrupts are not being configured. Preconditions: None. Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: ISR code is always compiled. Expected behavior: ISR code not present when corresponding interrupts are not configured. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ARTD-17979	Bug	[Emios Ip] All emios IP functions have the input parameter not follow the Pascal rule<*>
		
		Detailed description (how to reproduce it):
		[Emios Ip] All Emios IP functions have the input parameter not follow the Pascal rule
		Example:
		void Emios_Mcl_Ip_ComparatorTransferDisable(uint8 instance, uint32 channelMask);
		Emios_Ip_CommonStatusType Emios_Mcl_Ip_Deinit(uint8 instance);
		void Emios_Mcl_Ip_SetReloadInterval(uint8 hwInstance, uint8 hwChannel, uint8 interval);
		Rule 27: Local variables, function parameters and struct members shall use only PascalCase naming, without any special prefix (e.g. Hungarian notation or <Msn>, <Ip> etc.)
		<VarName>
		Example: Channel, State, Index, Config, etc.
		Preconditions:
		NA
		Test Case ID (internal TC that caught the defect) optional:
		NA
		Observed behavior:
		NA
		Expected behavior:
		NA
		Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)
		Proposed solution optional:
		NA

ARTD-17988	New Feature	[BASE] Use linkerFile tag instead of resourceFile tag in itm file for IAR profile<*> NewWorkDescription: IAR profile setting in itm file should update according to the advice from S32DS team mentioned in the ticket S32DS-24032. For option 'incPaths' tag, 'configId' attribute should be removed. For linker file configuration, linkerFile tag should be used instead of resourceFile tag. So, for Debug_RAM profile, no need to duplicate the options 'incPaths' and 'icfFile'. Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: NA

ID	Subtype	Headline and Description
ARTD-18037	New Feature	[gpt] Create new APIs for STM and FTM Ips<*> NewWorkDescription: This ticket is cloned because bamboo build is failing for S32XX and S32K3XX platforms because some drivers are not updated for these releases. For this ticket the only thing which is needed is to re-run bamboo plan with these 2 platforms. We received a request for stm and ftm ips from Zephyr team; they need in their application an API which will provide a match with an absolute value as timeout/compare value(refer to the attached picture). Our proposal is to create an API <IpName>_Ip_StartCountingAbsolute(uint8 instance, uint8 channel uint32 timevalue), timevalue_ represents the absolute value of counter register Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]

ARTD-18747	Bug	[Wdg] Wdg_ChannelInit fails if SWT is already init out of reset by the IVT config<*>
		
		In S32K3, there is an option to enable the SWT (Watchdog) by the Bootheader, so the watchdog is enable out of reset.
		If this is the case the function Wdg_ChannelInit fails to initialize/configure the SWT long as there is a part of the driver that corroborate if the module is already active or not.
		.....
		if ((Swt_Ip_IsEnable(base)) ((boolean)(Swt_Ip_Unlock(base) == SWT_IP_STATUS_ERROR)))
		{
		ret = SWT_IP_STATUS_ERROR;
		.....
		
		In our Startup code there is a part where the SWT are disabled as there is an Autosar Guideline which mentions:
		/ Autosar Guidance 5 The start-up code shall ensure that the MCU internal watchdog shall not be serviced until the watchdog is initialized from the MCAL watchdog driver. This can be done for example by increasing the watchdog service time. /
		
		But as long as this is no a "MUST", customer mentioned that there is not need to disabled the Watchdog and that the driver should be able to propertly configure the Watchdog even if it is already enable by the bootheader.
		
		They also mentioned that if they try to reconfigure the SWT to extent the period of time to service the watchdog, the init function is still failing.
		
		So, in conclusion, Wdg_ChannelInit should be able to verify if the SWT is already enabled by the bootheader, and if so, reconfigure it with the application configuration.

ARTD-18759	Bug	[CAN] Timestamp name does not match R41's RM<*> Detailed description (how to reproduce it): Create S32R41 project for CAN testing: Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: !image-2021-10-26-15-39-45-435.png! Expected behavior: Timestamp name should be re-checked for PFE !image-2021-10-26-15-39-19-914.png! Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-18762	Bug	[Base] Driver and requirement are inconsistent<*> Detailed description (how to reproduce it): There are 3 requirements that are inconsistent between Requirements and Driver code !image-2021-10-26-16-17-07-413.png|thumbnail! Preconditions: Requirement baseline: 26.3 INTREQ_BASE_RTD_4.4_SJA11XX_0.9.0_I03 Base tag: BASE_258 Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: See detail description Expected behavior: The requirement and driver should be consistent Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Create ITWG ticket to update internal requirements

ID	Subtype	Headline and Description
ARTD-18833	New Feature	[BASE] Split ASM_KEYWORD into volatile and non-volatile<*> NewWorkDescription: Split ASM_KEYWORD into volatile and non-volatile in order to avoid compiler warnings related to volatile asm statements used out of functions. Requirement source: N/A (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Split ASM_KEYWORD into volatile and non-volatile.
ARTD-18840	New Feature	[adc] [S32 3.0.0] Create driver for S32G3<*> Support derivative S32G3: S32G378A_BGA525 S32G379A_BGA525 S32G398A_BGA525 S32G399A_BGA525 S32G338M_BGA525 S32G339M_BGA525 S32G358A_BGA525 S32G359A_BGA525 With similar support as for S32G2. S32G3 Examples will be developed and tested on EVB Board. For detailed scope of the release see SOW: [S32 RTD for S32 3.0.0 SOW.docx (sharepoint.com)|https://nxp1.sharepoint.com/:w:/r/sites/Zebra/_layouts/15/Doc.aspx?sourcedoc=%7BD4BB6374-2FF8-4854-98BF-B8C762052305%7D&file=S32%20RTD%20for%20S32%203.0.0%20SOW.docx&action=default&mobileredirect=true]
ARTD-18887	New Feature	[platform] [S32K3 2.0.0 CD01] Create driver for S32K342<*> Support derivative S32K342: S32K342_100MQFP S32K342_172MQFP With: Tresos & S32CT support Create Tresos and CT examples for driver and execute examples Run development tests For detailed scope of the release see SOW: [S32K3 RTD ASR 4.4 2.0.0 SOW.docx (sharepoint.com)|https://nxp1.sharepoint.com/:w:/r/sites/Zebra/_layouts/15/Doc.aspx?sourcedoc=%7B3C101971-D503-429C-B4CF-779627CDE942%7D&file=S32K3%20RTD%20ASR%204.4%202.0.0%20SOW.docx&action=default&mobileredirect=true]
ARTD-18894	New Feature	[uart] [S32K3 2.0.0 CD01] Create driver for S32K342<*> Support derivative S32K342: S32K342_100MQFP S32K342_172MQFP With: Tresos & S32CT support Create Tresos and CT examples for driver and execute examples Run development tests For detailed scope of the release see SOW: [S32K3 RTD ASR 4.4 2.0.0 SOW.docx (sharepoint.com)|https://nxp1.sharepoint.com/:w:/r/sites/Zebra/_layouts/15/Doc.aspx?sourcedoc=%7B3C101971-D503-429C-B4CF-779627CDE942%7D&file=S32K3%20RTD%20ASR%204.4%202.0.0%20SOW.docx&action=default&mobileredirect=true]

ID	Subtype	Headline and Description
ARTD-18949	Bug	[SPI] Function parameter of Spi_SetupEB was not following the requirement and autosar specs<*> Detailed description (how to reproduce it): The function declaring of Spi_SetupEB was not following the requirement and autosar specs Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Std_ReturnType Spi_SetupEB (Spi_ChannelType Channel, Spi_DataBufferType SrcDataBufferPtr, Spi_DataBufferType DesDataBufferPtr, Spi_NumberOfDataType Length) Expected behavior: Std_ReturnType Spi_SetupEB (Spi_ChannelType Channel, const Spi_DataBufferType SrcDataBufferPtr, Spi_DataBufferType DesDataBufferPtr, Spi_NumberOfDataType Length) Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Change Spi_SetupEB to follow requirement and autosar specs
ARTD-18951	New Feature	[ADC] Remove unnecessary checking by FEATURE_ADC_BAD_ACCESS_PROT_CHANNEL<*> For Adc_sar IP driver, FEATURE_ADC_BAD_ACCESS_PROT_CHANNEL is used to not access to unavailable register that can lead to hardfault or unexpected behavior Using this marco requires a lot of checking when accessing many register that takes time and might cause overhead. Proposal to not use it and find the better way to improve driver regarding this Proposal is to improve/remove unnecessary checking by this define
ARTD-18969	Bug	[ARTD][Eth][S32K344] Wrongly truncated buffer on Gmac_Ip_ReadFrame function<*> Detailed description (how to reproduce it): The S32K3 TCPIP stack is ported over Gmac_Ip driver. On Gmac_Ip_ReadFrame function, there is a condition that truncates the receive buffer length: /* *According to requirement CPR_RTD_00284.eth* */ *if (Buff->Length > (uint16)(Bd->Info1 & GMAC_INFO1_LENGTH_MASK)) *{ *Buff->Length = (uint16)(Bd->Info1 & GMAC_INFO1_LENGTH_MASK); *} For some reason, this buffer length is set to 0 when this condition is executed. I assume this happens because Bd->Info1 is already 0 (so it sets the Buff->Length also to 0). (Picture attached) This issue was noticed during TCPIP testing over Gmac_Ip driver. After the board acquired Ipv4 address, we sent pings to it. After several pings, the issue occured. (Picture attached). Notes: If this condition is commented/removed, the TCPIP stack is working well. This condition was not available on RTD S32K3 BETA 0.9.2 Preconditions: S32DS 3.4 with S32K3XX_RTD_4_4_RTM_1_0_0_DS_updatesite_2110 installed. S32DS project with Gmac_Ip component configured. Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: The Gmac_Ip_ReadFrame function sets Rx buffer length to 0 on certain condition is met, making the driver not working correctly anymore. Expected behavior: The buffer length should not be set to 0 in this case. It should be set to its correct value. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-18975	New Feature	[ETH][GMAC] Improve zero-copy operating mode<*> NewWorkDescription: Improve zero-copy operating mode Requirement source: Internal driver requirements (GMAC_IP_001) (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Add compiler-time switches EthCtrlAllocateTxDataBuffers and EthCtrlAllocateRxDataBuffers to avoid extraneous memory consumption when the application provides its own buffers. Add examples of usage in the documentation.
ARTD-18978	Bug	[ADC] BCTU and CTU Ip includes Det.h<*> Detailed description (how to reproduce it): BCTU and CTU Ip includes Det.h in Bctu_Ip_PBcfg.c and Ctu_Ip_PBcfg.c generated from EBT or S32CT Adc_Ipw_Irq.c included Det.h to checking spurious interrupt. But there is no Det need to be reported here because of Rationale: The DEM or DET callback is long in its full implementation, delaying the ISR. Currently, Adc report all DET error at HLD layer Preconditions: N.A. Observed behavior: BCTU and CTU Ip includes Det.h in Bctu_Ip_PBcfg.c and Ctu_Ip_PBcfg.c generated from EBT or S32CT Expected behavior: BCTU and CTU Ip must not have dependency on Det.h Consider remove Det.h also in Adc_Ipw_Irq.c Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N.A.
ARTD-18991	Bug	[CRYPTO] Functions should be return error CRYPTO_E_BUSY when channel busy<*> Detailed description (how to reproduce it): Some function not return error CRYPTO_E_BUSY when channel busy (u8MuChannel = HSE_IP_INVALID_MU_CHANNEL_U8) Preconditions: Call several ProcessJob on async mode to make channel busy Test Case ID (internal TC that caught the defect) optional: Crypto_TC_FCT_0047 Observed behavior: Some function return error E_NOT_OK when channel busy Expected behavior: All function will return error CRYPTO_E_BUSY when channel busy Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-19000	Bug	[Gpt] GPT_CONFIG_VS_0_PB macro is generated when VariantPreCompile is used<*> Detailed description (how to reproduce it): When I run the test with test code covarage, I get a build failed error like the image described below This error is caused by the GPT_CONFIG_VS_0_PB macro that does not contain data in the Gpt_n_PBcfg.h file: #define GPT_CONFIG_VS_0_PB \ Preconditions: Configuration in local file CCOV_ENABLE := ON LDRA_DIR := C:/LDRA_Toolsuite ALLOW_MULTIPLE_INSTANCES:=ON Test Case ID (internal TC that caught the defect) optional: Gpt_TC_FCT_0203(Gpt_TS_C07) Observed behavior: Build failed when running test code coverage Expected behavior: Build is successful when running test code coverage Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: in case of precompile variant this macro shouldn't be generated
ARTD-19050	Bug	[ADC] Disable Aux Trigger from driver and configurator<*> Aux external trigger is not supported on S32G2 and S32R45, S32R41 so it should be disabled from driver and configurator and driver code This is document issue as confirmed by HW team. For more details, refer to attachment

ID	Subtype	Headline and Description
ARTD-19081	Bug	[ETH] The start of index for each fifo read incorrectly<*> Detailed description (how to reproduce it): follow code driver: !image-2021-11-05-19-22-32-604.png|thumbnail! The start of index of each fifo equal the start of index of previous fifo number of buffers configured for fifo which was calculating. This is incorrectly. It should be he start of index number of buffers configured of previous fifo. Preconditions: Number of fifo > 1 Number of buffers configured in each fifo is different Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: The start of fifo's index is incorrectly. Expected behavior: The start of fifo's index need to calculate correctly. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Code should be changed to !image-2021-11-05-19-29-41-691.png|thumbnail!
ARTD-19261	New Feature	[BASE][STUBS][S32CT] Add support for postBuildVariants<*> NewWorkDescription: Add support for postBuildVariants Requirement source: N/A (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Update the generic "system" component to provide mechanisms that can enable the creation and usage of postBuildVariants
ARTD-19267	Bug	[LIN] LinNodeType has been generated incorrectly with multi channels setup<*> Detailed description (how to reproduce it): Configuration lin driver with multi channels: Channel 0: Lin node type is Slave. Channel 1: Lin node type is Master. ..... Observed behavior: All LinNodeTypes have been generated to LIN_SLAVE_NODE Expected behavior: LinNodeType of channel 0 is LIN_SLAVE_NODE. LinNodeType of channel 1 is LIN_MASTER_NODE. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-19288	Bug	Flexio Sent Ip use float64 variables<*> Detailed description (how to reproduce it): Flexio_Sent_Ip.c The function "static Flexio_Sent_Ip_StatusType Flexio_Sent_Ip_StartTransfer" uses float64 type variable. Line 814 "if(((float64)PulseWidthTick >= SYNC_CAL_TICK_MIN) && ((float64)PulseWidthTick <= SYNC_CAL_TICK_MAX))" Since S32K3 does not support this float type by hardware, it will call div64 library and takes much more execution time. Is it possible to change the float64 to uint32? Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-19312	Bug	[GPT] Do not jump into the Pit_Ip_ProcessCommonInterrupt function when using PIT_0_CH_6 channel<*> Detailed description (how to reproduce it): When using interrupt for PIT_0_CH_6 channel, after entering PIT_0_ISR function, we can't jump to Pit_Ip_ProcessCommonInterrupt function again because the loop is incorrect. The reason is that the S32R41 platform does not support PIT_RTI Preconditions: Use interrupt of PIT_0_CH_6 channel Test Case ID (internal TC that caught the defect) optional: Gpt_TC_FCT_0007(Gpt_TS_001) Observed behavior: Do not jump into the Pit_Ip_ProcessCommonInterrupt function Expected behavior: interrupt works correctly when jumping into Pit_Ip_ProcessCommonInterrupt function Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: For S32R41 platform we should change the loop for accuracy
ARTD-19320	Bug	[ETH] Dependency on DEM is still expected when ETH_DEM_EVENT_DETECT = STD_OFF<*> Detailed description (how to reproduce it): Not all inclusions of Dem.h are guarded by macro ETH_DEM_EVENT_DETECT Preconditions: Set EthDisableDemEventDetect = TRUE in configuration Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Build fails if DEM isn't included in the build even though the configuration tells the driver to disable DEM. Expected behavior: Build is passing even if DEM isn't included in the build when configuration tells the driver to disable DEM. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Guard the #include "Dem.h" directives with ETH_DEM_EVENT_DETECT in files Eth.c and Eth_Ipw_Irq.c (their corresponding file version checks)
ARTD-19321	Bug	[S32K3][SENT] A error will be generated when Pause Pulse is enabled.<*> Detailed description (how to reproduce it): In SENT driver, the API Flexio_Sent_Ip_StartTransfer*() is used to measure the PulseWidth of the signal. However, when Pause Pulse is enabled, SUCCESS status will be returned in STATUS_SENT_FAST_SYNC_CALIB phase, not STATUS_SENT_FAST_PAUSE_PULSE phase. Because of that, the Pause Pulse nibble will lead to a error at next STATUS_SENT_FAST_IDLE phase. Customer cannot accept this error. When Pause Pulse is enabled, SUCCESS status should be returned in STATUS_SENT_FAST_PAUSE_PULSE phase. See attached for more information. Preconditions: The Pause Pulse of SENT is enabled Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: When Pause Pulse is enabled, SUCCESS status should be returned in STATUS_SENT_FAST_PAUSE_PULSE phase. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-19326	Bug	[ADC] S32ConfigurationTool: Configuration error when selecting DMA channel for BCTU/CTU FIFO<*> Detailed description (how to reproduce it): [Configuration error when selecting DMA channel for BCTU FIFO, and this problem does not exist in BLN_RTD_4.4_S32K3XX_0.9.0] Preconditions: [Configuration: Tick the "Watermark DMA enable" option, and configure the "Select Dma Channel for Fifo" option] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [Generate error: Value is not available] Expected behavior: [Generate pass] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-19351	Bug	[Adc] S32CT config generate incorrect data of aHwLogicalId<*> Detailed description (how to reproduce it): Code generation for Adc Ipw when configuring only Adc 1 is wrong. Consequently, when using Adc_1, we cannot have result buffer update. Steps: Configure only one Hw unit Adc 1 Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: Adc_Ipw_PbCfg.c { ADC_IPW_INVALID_LOGICAL_UNIT_ID , ADC_IPW_INVALID_LOGICAL_UNIT_ID , ADC_IPW_INVALID_LOGICAL_UNIT_ID }, / aHwLogicalId / Expected behavior: Adc_Ipw_PbCfg.c { ADC_IPW_INVALID_LOGICAL_UNIT_ID , 1U, ADC_IPW_INVALID_LOGICAL_UNIT_ID }, / aHwLogicalId / Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-19431	New Feature	[RM] XRDC shall allow locking the XRDC registers (implemented on CT)<*> NewWorkDescription: A safety requirement (ARSW-46) requires that XRDC configuration to be lock-able, to prevent other master changing it. Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Support locking the XRDC configured registers, as a configuration option. Could be done by having some extra masks or in a separate step at the end of init.
ARTD-19435	Bug	[LIN] Function Lpuart_Lin_Ip_AutoBaudCapture can't detect wakeup signal<*> Detailed description (how to reproduce it): After Init driver call function Lpuart_Lin_Ip_GoToSleepMode and waiting master node send wakeup signal. But driver can't wakeup when autobaudrate feature enable. Preconditions: In func Lpuart_Lin_Ip_AutoBaudCapture, driver only handle case wakeup signal if func Lpuart_Lin_Ip_AutoBaudCapture called at least 3 times. But in this case after Init, driver go into SLEEP mode and Lpuart_Lin_Ip_AutoBaudCapture never called before. So when received wakeup signal driver only call Lpuart_Lin_Ip_AutoBaudCapture 2 time and ignore wakeup signal. !image-2021-11-15-10-59-35-409.png|width=906,height=387! Test Case ID (internal TC that caught the defect) optional: Ip_Lpuart_Lin_TC_FCT_0021 Observed behavior: Can't wakeup Expected behavior: Can wakeup Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-19452	Bug	[CRYPTO] HIS_CCM over 20 for two Crypto functions<*> Detailed description (how to reproduce it): Run a bamboo build for S32K3XX 1.0.0 P02 with Coverity enabled, look in Coverity or in the generated HIS report. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: Development test case that is run by the bamboo build: Crypto_TS_SharedCfg Observed behavior: Two functions have the CCM above 20: 11250967|HIS_CCM|None|None|Low| Quality|Measured value of CCM metric 21.00 is higher than maximum value 10.00 allowed by the HIS metrics policy.|/ARTD-CIC89-2/sources/S32K3XX_4.4/output/eclipse/plugins/Crypto_TS_T40D34M10I0R0/src/Crypto.c|Crypto_KeyElementGet|2808|Intentional|Dismissed|The function will not be split any further in this release to ensure logical consistency. 11485591|HIS_CCM|None|None|Low| Quality|Measured value of CCM metric 21.00 is higher than maximum value 10.00 allowed by the HIS metrics policy.|/ARTD-CIC89-2/sources/S32K3XX_4.4/output/eclipse/plugins/Crypto_TS_T40D34M10I0R0/src/Crypto_Hse.c|Crypto_Hse_ExportSymPrivAsymPub|2773|Intentional|Dismissed|The function will not be split any further in this release to ensure logical consistency. Expected behavior: CCM level for all the functions should be below 20. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Rework the functions to have a lower CCM than 20.

ID	Subtype	Headline and Description
ARTD-19455	New Feature	[ICU] fix nightly build for module<*> NewWorkDescription: Nightly build fail because it cannot generate and validate the bswmd file. Fix bug to generate bswmd file. Requirement source: (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Check Wkpu_Ip_PBcfg.c and remove unneeded code. !image-2021-11-18-10-47-34-262.png|width=820,height=412!
ARTD-19487	Bug	[FLS][S32K3XX] C40 FLS_DATA_BLOCK_END_ADDR<*> FLS_DATA_BLOCK_END_ADDR defined as 0x1003FFFFU (256KB) in C40_Ip_CFG.h. However, all the S32K3 parts have 128KB DFlash.
ARTD-19486	New Feature	[BASE][S32CT] Add support to filter generated artifacts and components<*> NewWorkDescription: Add support to filter generated artifacts and components: Invoking the S32DS CLI generator with option "-ExportArgs" will let the user filter the generated artifacts (e.g. "-ExportArgs ecpd" means that only ECPDs will be generated; "-ExportArgs c h" means that only .c and .h files will be generated) Invoking the S32DS CLI generator with option "-ExportComponentIds" will let the user filter the generated components (e.g. "-ExportComponentIds Eth_43_GMAC" means that only the generator for Eth_43_GMAC will be invoked) Note: The arguments to both options are case-insensitive (e.g. "eCpD" and "ecpd" are equivalent; "eTh_43_gMac" and "Eth_43_GMAC" are equivalent). The options themselves are optional. If "-ExportArgs" is omitted, no filtering on artifacts is performed. If "-ExportComponentIds" is omitted, no filtering on components is performed. Requirement source: N/A (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Update System files to support filtering generated artifacts and components.
ARTD-19519	Bug	[S32K3XX][PORT] Pad selection of ADC mux-mode channels does not take effect<*> Detailed description (how to reproduce it): [Pad selection of ADC mux-mode channels does not take effect. For example, no matter in EB or CT configuration interface, when you select PAD46 for ADC0_S9 channel which is driven by PAD1(default) and PAD46, this configuration does not take effect. The reason caused this problem is that the RTD driver won't configure corresponding DCM register bits (DCM.DCMRWF4[2] for ADC0_S9 channel) to select the correct PAD, and this work should be automatically done by the RTD driver instead of manually configuring the register bits by the user.] Preconditions: [Select PAD46 for ADC0_S9 channel which is driven by PAD1(default) and PAD46.] Test Case ID (internal TC that caught the defect) optional: [NA] Observed behavior: [Pad selection of ADC mux-mode channels does not take effect.] Expected behavior: [RTD driver can automatically configure corresponding DCM register bits according to the Pad selection of ADC mux-mode channels.] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [NA]
ARTD-19575	Bug	[PORT] Port driver have to add some Det_reportError function following requirement<*> Detailed description (how to reproduce it): If Det is enabled, some function shall report specify error and return without any other action. Detail: CPR_RTD_00423.port: The function Port_ResetPinMode shall report PORT_E_MODE_UNCHANGEABLE error and return without any other action, if the parameter PortPinModeChangeable is set to FALSE. CPR_RTD_00426.port*: The function Port_SetAsUnusedPin shall report PORT_E_MODE_UNCHANGEABLE error and return without any other action, if the parameter PortPinModeChangeable is set to FALSE. CPR_RTD_00428.port*: The function Port_SetAsUsedPin shall report PORT_E_MODE_UNCHANGEABLE error and return without any other action, if the parameter PortPinModeChangeable is set to FALSE. SWS_Port_00223: The function Port_SetPinMode shall reportPORT_E_MODE_UNCHANGEABLE error and return without any other action, if the parameter PortPinModeChangeable is set to FALSE. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Port driver should add some Det_reportError function with specify error following the requirement in Detailed Description.

ID	Subtype	Headline and Description
ARTD-19581	Bug	[SPI][LPSPI] Cannot move received data to Rx buffer if previous channel has RX buffer is NULL in DMA mode<*> Detailed description (how to reproduce it): Cannot move received data to Rx buffer if previous channel has RX buffer is NULL in DMA mode. See attachment email for details. Preconditions: Previous channel using RX buffer is NULL in DMA mode Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Cannot move received data to Rx buffer Expected behavior: Receive data successful Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update driver to update DMA_IP_CH_SET_DESTINATION_SIGNED_OFFSET if previous channel has RX buffer is NULL. Check for TX also in case that previous channel has TX is NULL (transmit default data)
ARTD-19580	Bug	[ICU][S32R41] Don't have Siul2_Icu component in S32DS<*> Detailed description (how to reproduce it): Don't have Siul2_Icu component in S32DS !image-2021-11-18-11-14-07-132.png! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Ip_Siul2_TS_160 Observed behavior: [...] Expected behavior: [...] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-19662	New Feature	[PORT] Allow to configure IMCR with pin as GPIO mode during Port_Init() for S32K3, S32R41, S32ZSE, SJA11XX, SAF85XX ,,"NewWorkDescription: In S32G's BootROM, PF_04 was configured as QSPI_INTA_b, and IMCR[37] was set to 0x2. After that the code jumped to the application where called Port_Init(), with PF_04 was configured as GPIO, and customer expected IMCR[37] would be cleared to 0x0. However, with current implementation of Port driver, Port_Init() doesn't touch IMCR registers with pins configured as GPIO mode. As a result, IMCR[37] was still 0x2, and PF_04 couldn't be used as GPIO mode Requirement source: N/A (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: CE's comment: Since there was a UntouchedIMCR list where user can add pins that they don't want IMCR to be re-configured, my proposal is with the pins configured as GPIO mode in PortContainer, IMCR shall be reset as 0x0. It's better to have an option for user to choose either IMCR would be disabled low or disabled high.

ID	Subtype	Headline and Description
ARTD-19738	Bug	[i2c] Update missing exclusive areas in BSWMD<*> Detailed description (how to reproduce it): Do a repo sync on bswmd_creator to sync with the manifest (make sure that you've checked out BLN_BSWMD_CREATOR_04.08.03) Compile the plugin passing parameter GENERATE_BSWMD_FILE=ON to the make command (`p s1 b` in ZTH) If the plugin was compiled successfully and there are no errors from bswmd_creator regarding missing or unmapped exclusive areas, then you can close your clone with "Fixed No Action Taken". Otherwise, proceed with the solutions given in the "Proposed solution" section. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Missing exclusive areas in <Module>_Bswmd.arxml Expected behavior: All exclusive areas are included in <Module>_Bswmd.arxml Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Potential Issue #1 Missing exclusive areas for ISRs Solution #1 The bswmd_creator script will automatically fetch ISRs from the source code as long as they're defined with ISR(...). Every ISR mentioned in the "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" files shall also be wrapped in ISR(...). For example: ADC_EXCLUSIVE_AREA_70 is used in function ISR(Ctu_Error_Isr) to protect the updates for CTU_IFR register Potential Issue #2 Missing exclusive areas for IPL functions which are not called by any HLD function Solution #2 # Have the EA mentioned in "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" only as used by the IPL function. For example: ADC_EXCLUSIVE_AREA_17 is used in function Adc_Sar_Ip_AbortConversion to protect the updates for ADC_MCR register # Add the IPL function in NonASR_ServiceID.xml Note: Do not use other workarounds like artificially mentioning in .dox that the IPL function is called by an HLD function which is included in NonASR_ServiceID.xml (even though, in reality, it's not)
ARTD-19741	Bug	[lin] Update missing exclusive areas in BSWMD<*> Detailed description (how to reproduce it): Do a repo sync on bswmd_creator to sync with the manifest (make sure that you've checked out BLN_BSWMD_CREATOR_04.08.03) Compile the plugin passing parameter GENERATE_BSWMD_FILE=ON to the make command (`p s1 b` in ZTH) If the plugin was compiled successfully and there are no errors from bswmd_creator regarding missing or unmapped exclusive areas, then you can close your clone with "Fixed No Action Taken". Otherwise, proceed with the solutions given in the "Proposed solution" section. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Missing exclusive areas in <Module>_Bswmd.arxml Expected behavior: All exclusive areas are included in <Module>_Bswmd.arxml Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Potential Issue #1 Missing exclusive areas for ISRs Solution #1 The bswmd_creator script will automatically fetch ISRs from the source code as long as they're defined with ISR(...). Every ISR mentioned in the "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" files shall also be wrapped in ISR(...). For example: ADC_EXCLUSIVE_AREA_70 is used in function ISR(Ctu_Error_Isr) to protect the updates for CTU_IFR register Potential Issue #2 Missing exclusive areas for IPL functions which are not called by any HLD function Solution #2 # Have the EA mentioned in "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" only as used by the IPL function. For example: ADC_EXCLUSIVE_AREA_17 is used in function Adc_Sar_Ip_AbortConversion to protect the updates for ADC_MCR register # Add the IPL function in NonASR_ServiceID.xml Note: Do not use other workarounds like artificially mentioning in .dox that the IPL function is called by an HLD function which is included in NonASR_ServiceID.xml (even though, in reality, it's not)

ID	Subtype	Headline and Description
ARTD-19742	Bug	[mcl] Update missing exclusive areas in BSWMD<*> Detailed description (how to reproduce it): Do a repo sync on bswmd_creator to sync with the manifest (make sure that you've checked out BLN_BSWMD_CREATOR_04.08.03) Compile the plugin passing parameter GENERATE_BSWMD_FILE=ON to the make command (`p s1 b` in ZTH) If the plugin was compiled successfully and there are no errors from bswmd_creator regarding missing or unmapped exclusive areas, then you can close your clone with "Fixed No Action Taken". Otherwise, proceed with the solutions given in the "Proposed solution" section. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Missing exclusive areas in <Module>_Bswmd.arxml Expected behavior: All exclusive areas are included in <Module>_Bswmd.arxml Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Potential Issue #1 Missing exclusive areas for ISRs Solution #1 The bswmd_creator script will automatically fetch ISRs from the source code as long as they're defined with ISR(...). Every ISR mentioned in the "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" files shall also be wrapped in ISR(...). For example: ADC_EXCLUSIVE_AREA_70 is used in function ISR(Ctu_Error_Isr) to protect the updates for CTU_IFR register Potential Issue #2 Missing exclusive areas for IPL functions which are not called by any HLD function Solution #2 # Have the EA mentioned in "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" only as used by the IPL function. For example: ADC_EXCLUSIVE_AREA_17 is used in function Adc_Sar_Ip_AbortConversion to protect the updates for ADC_MCR register # Add the IPL function in NonASR_ServiceID.xml Note: Do not use other workarounds like artificially mentioning in .dox that the IPL function is called by an HLD function which is included in NonASR_ServiceID.xml (even though, in reality, it's not)
ARTD-19750	Bug	[pwm] Update missing exclusive areas in BSWMD<*> Detailed description (how to reproduce it): Do a repo sync on bswmd_creator to sync with the manifest (make sure that you've checked out BLN_BSWMD_CREATOR_04.08.03) Compile the plugin passing parameter GENERATE_BSWMD_FILE=ON to the make command (`p s1 b` in ZTH) If the plugin was compiled successfully and there are no errors from bswmd_creator regarding missing or unmapped exclusive areas, then you can close your clone with "Fixed No Action Taken". Otherwise, proceed with the solutions given in the "Proposed solution" section. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Missing exclusive areas in <Module>_Bswmd.arxml Expected behavior: All exclusive areas are included in <Module>_Bswmd.arxml Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Potential Issue #1 Missing exclusive areas for ISRs Solution #1 The bswmd_creator script will automatically fetch ISRs from the source code as long as they're defined with ISR(...). Every ISR mentioned in the "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" files shall also be wrapped in ISR(...). For example: ADC_EXCLUSIVE_AREA_70 is used in function ISR(Ctu_Error_Isr) to protect the updates for CTU_IFR register Potential Issue #2 Missing exclusive areas for IPL functions which are not called by any HLD function Solution #2 # Have the EA mentioned in "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" only as used by the IPL function. For example: ADC_EXCLUSIVE_AREA_17 is used in function Adc_Sar_Ip_AbortConversion to protect the updates for ADC_MCR register # Add the IPL function in NonASR_ServiceID.xml Note: Do not use other workarounds like artificially mentioning in .dox that the IPL function is called by an HLD function which is included in NonASR_ServiceID.xml (even though, in reality, it's not)

ID	Subtype	Headline and Description
ARTD-19756	Bug	[spi] Update missing exclusive areas in BSWMD<*> Detailed description (how to reproduce it): Do a repo sync on bswmd_creator to sync with the manifest (make sure that you've checked out BLN_BSWMD_CREATOR_04.08.03) Compile the plugin passing parameter GENERATE_BSWMD_FILE=ON to the make command (`p s1 b` in ZTH) If the plugin was compiled successfully and there are no errors from bswmd_creator regarding missing or unmapped exclusive areas, then you can close your clone with "Fixed No Action Taken". Otherwise, proceed with the solutions given in the "Proposed solution" section. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Missing exclusive areas in <Module>_Bswmd.arxml Expected behavior: All exclusive areas are included in <Module>_Bswmd.arxml Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Potential Issue #1 Missing exclusive areas for ISRs Solution #1 The bswmd_creator script will automatically fetch ISRs from the source code as long as they're defined with ISR(...). Every ISR mentioned in the "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" files shall also be wrapped in ISR(...). For example: ADC_EXCLUSIVE_AREA_70 is used in function ISR(Ctu_Error_Isr) to protect the updates for CTU_IFR register Potential Issue #2 Missing exclusive areas for IPL functions which are not called by any HLD function Solution #2 # Have the EA mentioned in "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" only as used by the IPL function. For example: ADC_EXCLUSIVE_AREA_17 is used in function Adc_Sar_Ip_AbortConversion to protect the updates for ADC_MCR register # Add the IPL function in NonASR_ServiceID.xml Note: Do not use other workarounds like artificially mentioning in .dox that the IPL function is called by an HLD function which is included in NonASR_ServiceID.xml (even though, in reality, it's not)

ARTD-19927	Bug	S32K3 SIUL2 ICU code generation issue<*>
		
		Detailed description (how to reproduce it):
		Add an Siul2_Icu component into an S32DS project in the configuration tool and click generate code.
		In the generated file: "Power_Ip_BOARD_InitPeripherals_PBcfg.c"
		const Siul2_Icu_Ip_ChannelConfigType Siul2_Icu_Ip_0_ChannelConfig_PB_BOARD_InitPeripherals[1U] =
		{
		/ brief IcuSiul2Channel_0 /
		{
		/ brief Siul2 HW Module and Channel used by the Icu channel /
		0U,
		/ brief Siul2 Digital Filter enable /
		TRUE,
		/ brief Siul2 Digital Filter value /
		1U,
		/ brief Siul2 request type*/
		SIUL2_ICU_IRQ,
		/ brief Siul2 Edge type*/
		SIUL2_ICU_RISING_EDGE,
		/ brief Callback Pointer /
		NULL_PTR,
		/ brief Notification function /
		&NULL_PTR,
		/ brief Callback Param1*/
		0U
		}
		};
		In this generated structure, the line of "&NULL_PTR" will bring compiling error.
		Preconditions:
		[...]
		Test Case ID (internal TC that caught the defect) optional:
		[...]
		Observed behavior:
		[...]
		Expected behavior:
		[...]
		Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)
		Proposed solution optional:
		Change the "&NULL_PTR" to be "NULL_PTR"

ID	Subtype	Headline and Description
ARTD-19950	Bug	[adc] Update missing exclusive areas in BSWMD<*> Detailed description (how to reproduce it): Do a repo sync on bswmd_creator to sync with the manifest (make sure that you've checked out BLN_BSWMD_CREATOR_04.08.03) Compile the plugin passing parameter GENERATE_BSWMD_FILE=ON to the make command (`p s1 b` in ZTH) If the plugin was compiled successfully and there are no errors from bswmd_creator regarding missing or unmapped exclusive areas, then you can close your clone with "Fixed No Action Taken". Otherwise, proceed with the solutions given in the "Proposed solution" section. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Missing exclusive areas in <Module>_Bswmd.arxml Expected behavior: All exclusive areas are included in <Module>_Bswmd.arxml Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Potential Issue #1 Missing exclusive areas for ISRs Solution #1 The bswmd_creator script will automatically fetch ISRs from the source code as long as they're defined with ISR(...). Every ISR mentioned in the "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" files shall also be wrapped in ISR(...). For example: ADC_EXCLUSIVE_AREA_70 is used in function ISR(Ctu_Error_Isr) to protect the updates for CTU_IFR register Potential Issue #2 Missing exclusive areas for IPL functions which are not called by any HLD function Solution #2 # Have the EA mentioned in "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" only as used by the IPL function. For example: ADC_EXCLUSIVE_AREA_17 is used in function Adc_Sar_Ip_AbortConversion to protect the updates for ADC_MCR register # Add the IPL function in NonASR_ServiceID.xml Note: Do not use other workarounds like artificially mentioning in .dox that the IPL function is called by an HLD function which is included in NonASR_ServiceID.xml (even though, in reality, it's not)
ARTD-19991	Bug	[SENT] Sent example should use mcu instead of sys_init and some example descriptions are not correct<*> Detailed description (how to reproduce it): EBT sent example is using sys_init to initial clocking, it should using mcu driver incorrect pin connection for S32K312 and S32K342 example in description Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: EBT sent example is using sys_init to initial clocking incorrect pin connection for S32K312 and S32K342 example in description Expected behavior: Using mcu driver for all example to initial clocking J459 instead of J458 is used to be pin connection Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Using mcu driver for all example to initial clocking J459 instead of J458 is used to be pin connection
ARTD-20018	Bug	[S32K3xx] Version 2.0.0 should be updated to some file .c and .h<*> Step: 1.Create project S32K3xx and attach sdk RTD 2.0.0 2. Open S32CT tool > Update code 3. Open all .c, .h then check Observed behavior: 3. Version 2.0.0 isn't updated to some file as below main.c Siul2_Port_Ip_Cfg.c Siul2_Port_Ip_Cfg.h Expected behavior: 3. Version 2.0.0 is updated

ID	Subtype	Headline and Description
ARTD-20029	Bug	[CAN][HLD-S32CT] This warning 'Issue: CanController_0 should be referred by CanIfCtrlCanCtrlRef' appears even if the controller is referred by CanIf<*> Detailed description (how to reproduce it): Project is created by EBT >import epc files from EBT to S32CT. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: Can_TS__CT_115 Observed behavior: !image-2021-11-30-11-48-36-294.png! Expected behavior: No warning appears. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA

ID	Subtype	Headline and Description

ARTD-20042	Bug	[S32K3XX] Imprecise bus fault exception in sys_m7_cache_clean() function<*>
		
		Detailed description (how to reproduce it):
		Customer has an issue with system.c from Platform driver on S32K312. The software jumps in an undefined handler (escalated hard fault from bus fault, imprecise) when executing the function sys_m7_cache_clean() at the end of sys_m7_cache_init():
		static void sys_m7_cache_clean(void)
		{
		uint32 ccsidr = 0U;
		uint32 sets = 0U;
		uint32 ways = 0U;
		S32_SCB->CSSELR = 0U; / select Level 1 data cache /
		ASM_KEYWORD("dsb");
		ccsidr = S32_SCB->CCSIDR;
		sets = (uint32)(CCSIDR_SETS(ccsidr));
		do {
		ways = (uint32)(CCSIDR_WAYS(ccsidr));
		do {
		S32_SCB->DCCISW = (((sets << 5) & (uint32)0x3FE0U)
		((ways << 30) & (uint32)0xC0000000U));
		ASM_KEYWORD("dsb");
		} while (ways != 0U); / within this do while loop imprecise bus fault happens /
		} while(sets != 0U);
		S32_SCB->CSSELR = (uint32)((S32_SCB->CSSELR) 1U);
		S32_SCB->ICIALLU = 0UL;
		ASM_KEYWORD("dsb");
		}
		!image-2021-11-30-12-57-41-450.png!
		!image-2021-11-30-12-57-51-884.png!
		Preconditions:
		N/A
		Test Case ID (internal TC that caught the defect) optional:
		N/A
		Observed behavior:
		Undefined handler (imprecise bus fault) called while executing startup
		Expected behavior:
		No undefined handler (imprecise bus fault) called while executing startup
		Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)
		Proposed solution optional:
		Remove the call to sys_m7_cache_clean() from the end of sys_m7_cache_init*() function as follows:
		static void sys_m7_cache_init(void)
		{
		#ifdef D_CACHE_ENABLE
		uint32 ccsidr = 0U;
		uint32 sets = 0U;
		uint32 ways = 0U;
		/*init Data caches*/
		S32_SCB->CSSELR = 0U; / select Level 1 data cache /
		ASM_KEYWORD("dsb");
		ccsidr = S32_SCB->CCSIDR;
		sets = (uint32)(CCSIDR_SETS(ccsidr));
		do {
		ways = (uint32)(CCSIDR_WAYS(ccsidr));
		do {
		S32_SCB->DCISW = (((sets << SCB_DCISW_SET_Pos) & SCB_DCISW_SET_Msk)
		((ways << SCB_DCISW_WAY_Pos) & SCB_DCISW_WAY_Msk));
		ASM_KEYWORD("dsb");
		} while (ways != 0U);
		} while(sets != 0U);
		ASM_KEYWORD("dsb");
		S32_SCB->CCR = (uint32)SCB_CCR_DC_Msk; / enable D-Cache /
		ASM_KEYWORD("dsb");
		ASM_KEYWORD("isb");
		#endif
		#ifdef I_CACHE_ENABLE
		/*init Code caches*/
		ASM_KEYWORD("dsb");
		ASM_KEYWORD("isb");
		S32_SCB->ICIALLU = 0UL; / invalidate I-Cache /
		ASM_KEYWORD("dsb");
		ASM_KEYWORD("isb");
		S32_SCB->CCR = (uint32)SCB_CCR_IC_Msk; / enable I-Cache /
		ASM_KEYWORD("dsb");
		ASM_KEYWORD("isb");
		#endif
		/*sys_m7_cache_clean();*/ / !!! commented out to solve the issue !!! /
		}
		After commenting out the call of sys_m7_cache_clean() the issue does not happen anymore. Also calling the sys_m7_cache_clean() is very strange as both data and instruction caches are already invalidated and enabled just before that (so there is no need to do it again inside sys_m7_cache_clean()).

ID	Subtype	Headline and Description
ARTD-20043	Bug	[MCL] Compiler error due to missing #ifdef __cplusplus<*> Detailed description (how to reproduce it): There is generated a compiler error due to missing #ifdef cplusplus } #endif at the end of the following files: Dma_Ip_Cfg_Defines.h Dma_Ip_Cfg_DeviceRegistersV3.h Trgmux_Ip_Cfg_Defines.h Also this code is wrongly placed in Lcu_Ip_DevAssert.h. Preconditions: Using C compiler Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Compiler error due to missing #ifdef cplusplus Expected behavior: No compiler error Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Add the missing code #ifdef cplusplus } #endif at the end of the following files: Dma_Ip_Cfg_Defines.h Dma_Ip_Cfg_DeviceRegistersV3.h Trgmux_Ip_Cfg_Defines.h Plus also fix the end of Lcu_Ip_DevAssert.h file to be as follows (#ifdef cplusplus moved just before last #endif): #endif / #if (STD_ON == LCU_IP_IS_AVAILABLE) / #ifdef cplusplus } #endif #endif / #ifndef LCU_IP_DEVASSERT_H / Also check all other files whether extern “C” is properly opened and closed.
ARTD-20066	Bug	[ADC] Group sw single continuous without interrupt can not transfer to buffer continuously<*> Detailed description (how to reproduce it): Group sw single continuous without interrupt can not transfer to buffer continuously Preconditions: Group sw single continuous without interrupt DMA transfer Test Case ID (internal TC that caught the defect) optional: Adc_TC_FCT_1408 Adc_TS_013 cfg BetweenDMA Observed behavior: Start group sw single continuous without interrupt Set AN_2 with 5V as out range voltage 0.5 1.5V Read group till E_OK expected time out Set AN_2 with 1V as in range voltage 0.5 1.5V Read group till E_OK expected not time out Real status: buffer is always 0xFFF and not updating Read group till E_OK and timeout occured Expected behavior: Read group till E_OK expected not time out Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-20075	Bug	[RM] XRDC can not rearm PDAC Error Capture register<*> Detailed description (how to reproduce it): Xrdc_Ip_GetDomainIDErrorStatus_Privileged can not rearm PDAC Error Capture register Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Error operate on RECR in DERR_W3_0, DERR_W3_1,DERR_W3_2 Expected behavior: Resets the error capture registers (DERR_W0_d, DERR_W1_d) after rearms instance error capture Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: XRDC_REG_WRITE32(XRDC_DERR_W_ADDR32(u32Instance,XRDC_WORD3,(uint32)u8counter), XRDC_ERROR_RECR_U32); => XRDC_REG_WRITE32(XRDC_DERR_W_ADDR32(u32Instance,XRDC_WORD3,(uint32)(u8counter 16U)), XRDC_ERROR_RECR_U32);

ID	Subtype	Headline and Description
ARTD-20161	Bug	[Clocks Diagram][HSE_CLK]HSE clock need to be limited between 24MHz and 120MHz<*> Detailed description (how to reproduce it): The HSE Firmware is operational when HSE_CLK is between 24MHz and 120MHz, but in the config tools HSE_CLK can be configured to 160Mhz. !image-2021-12-03-14-33-14-203.png|width=554,height=217! !image-2021-12-03-14-37-55-331.png! Observed behavior: The observed behavior is currently uncertain, found two cases: 1. The customer project uses config tools and RTD to set HSE_CLK to 160Mhz, causing the program to fail to run, the chip is temporarily secured. 2. The customer configured the HSE clock to 160Mhz through the bare-metal driver written by himself, trig MC_ME "HSE_SWT_RST" flag, even after the configuration is correct, HSE still cannot work ， it seems HSE firmware damage. Expected behavior: [...] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Check the HSE_CLK after configured
ARTD-20170	New Feature	[RM] Showcase the XRDC and Sema4 locking in examples<*> NewWorkDescription: The XRDC is a complex module and one of the most important ones on the platforms where isolation and virtualization play an important role. Given the difficulty of correctly configuring this module, the XRDC examples (part of RM module) should showcase the XRDC integration with the semaphore module. Requirement source: FAE community, for showcasing a complex topic involved in isolation. Proposed solution optional: Create a new example(preferable) in which you showcase only the XRDC and sema4 integration. lock a region, showcase that you still have read access even without sema4 taken take the sema4, show that you have write now that region the region can be memory (peripheral also if you find any benefit) show that if you do not have the sema4, an error will be reported recover from the error in the same context now force clear the sema4 to highlight this feature also, as it may be needed if the other user is non responsive
ARTD-20214	Bug	[ADC] Build faild when configuring ctu control mode<*> Detailed description (how to reproduce it): Build faild when configuring ctu control mode Preconditions: Configure ctu tab for eq class test AdcEnableCtuControlModeApi is enable Test Case ID (internal TC that caught the defect) optional: Adc_TS_COT_011 cfg 46 Observed behavior: Build fail error log: 1. CtuTriggerIndex is 3 but only1 element in CtuHwUnit tab: TARGET:Ctu_Ip_VS_0_PBcfg_c.o STDERR:"e:/S32K1XX/output/S32XX_S32G2XX/adc/Adc_TS_COT_011_cfg46_CORE4/generate_tresos/src/Ctu_Ip_VS_0_PBcfg.c", line 105: error #1981-D: STDERR: empty initializer is non-standard STDERR: }; 2. CtuFifoDmaEn is disable, but CtuDmaFifo0 still in struct Ctu_Ip_FifoConfigType CtuIpResultFifos_VS_0[]: STDERR:"e:/S32K1XX/output/S32XX_S32G2XX/adc/Adc_TS_COT_011_cfg46_CORE4/generate_tresos/src/Ctu_Ip_VS_0_PBcfg.c", line 136: error #20: STDERR: identifier "CtuDmaFifo0" is undefined STDERR: CtuDmaFifo0, / pUserFifoBuffer / STDERR: STDERR: STDERR:"e:/S32K1XX/output/S32XX_S32G2XX/adc/Adc_TS_COT_011_cfg46_CORE4/generate_tresos/src/Ctu_Ip_VS_0_PBcfg.c", line 192: error #28: STDERR: expression must have a constant value STDERR: CtuIpResultFifos_VS_0 / pFifoConfigs / STDERR: Expected behavior: Build done Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A

ID	Subtype	Headline and Description
ARTD-20327	Bug	[CRC] The data in ECVD file different from interface<*> Detailed description (how to reproduce it): N/A Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: When user add CRC64 custom with polynomial value on S32CT is 0x42F0E1EBA9EA3693, but polynomial value in ECVD file is 0x42F0E1EBA9EA37D8 Expected behavior: Update crc to polynomial value in ECVD file is the same interface Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-20324	Bug	[ADC] Mismatch prototype between driver code and requirements for 3 non-autosar extension APIs<*> Detailed description (how to reproduce it): Mismatch function prototype between driver code and requirements Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Mismatch function prototype between driver code and requirements, see detail in attachment (excel file) Expected behavior: No mismatching Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-20328	Bug	[CAN][S32CT/IPL] Build failed when tranfer type is set to USING DMA but LegacyFIFO is disabled<*> Detailed description (how to reproduce it): Transfer type is set to using_dma but legacy fifo feature is disabled. !image-2021-12-07-19-04-56-139.png! Preconditions: NA Test Case ID (internal TC that caught the defect) optional: lp_FlexCAN_TS_TRUST_001 Observed behavior: !image-2021-12-07-19-06-47-800.png! Expected behavior: No error at building Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-22018	Bug	[S32K3XX] Implement the WFI errata for CM7 hang<*> Detailed description (how to reproduce it): The CM7 can hang in certain corner-cases upon using WFI instruction (see attached file for more details) Preconditions: see attached file for more details Test Case ID (internal TC that caught the defect) optional: NA {_}*Observed behavior:*{_}unable to wakeup/reattach to M7 core {_}*Expected behavior:*{_}WFI functioning correctly, able to wakeup and re-attach to core anytime there is an interrupt or debug event. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: see attached file for more details implement the proposed workaround in startup file. document this errata in a highly visible place (RTD_S32K3XX_IM and release notes).

ID	Subtype	Headline and Description
ARTD-22027	Bug	[ADC] Incorrect command position in CTU optimization<*> Detailed description (how to reproduce it): When AdcCtuHardwareTriggerOptimization is enabled, the command position in configuration is incorrect in HW groups For example: the Group0 has 3 channel, Group1 has 2 channel, Group0 has 1 channel Then the starting position for G0 pos=0, G1 pos=3, G2 pos=4 But in codegen, the position for G0 pos=0, G1 pos=2, G2 pos=3 Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: incorrect CTU/BCTU command position Expected behavior: correct CTU/BCTU command position Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-21725	New Feature	[S32K3 2.0.0] Driver activities for UART<*> Drivers/IPs list in SOW: [see SOW for details|https://nxp1.sharepoint.com/:w:/r/sites/Zebra/_layouts/15/Doc.aspx?sourced oc=%7BD1DC93AE-F154-48B3-8D46-A8F7B0725503%7D&file=S32K3%20RTD%20ASR%204.4%202.0.0%20S OW.docx&action=default&mobileredirect=true]
ARTD-21882	New Feature	[S32K3 2.0.0] Driver activities for Resource<*> Drivers/IPs list in SOW: [see SOW for details|https://nxp1.sharepoint.com/:w:/r/sites/Zebra/_layouts/15/Doc.aspx?sourced oc=%7BD1DC93AE-F154-48B3-8D46-A8F7B0725503%7D&file=S32K3%20RTD%20ASR%204.4%202.0.0%20S OW.docx&action=default&mobileredirect=true]
ARTD-22269	Bug	[ADC] Remove unused ADC_USER_MODE_REG_PROT_ENABLED and port compiler warning fix<*> Detailed description (how to reproduce it): ADC_USER_MODE_REG_PROT_ENABLED is unused now and need to be removed from codegen Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: ADC_USER_MODE_REG_PROT_ENABLED is unused Expected behavior: not gen ADC_USER_MODE_REG_PROT_ENABLED Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-22288	New Feature	[ETH]Add infix support in the Eth driver<*> NewWorkDescription: Add infix support in the Eth driver Requirement source: Planned activity (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: For having separate and independent namespaces, drivers with the defined multiplicity greater than 1 need to have their name extended with an infix. Steps: Outside of the driver: Add in Base a new MemMap Eth_43_NETC_MemMap.h generated for the new naming Add in Rte new SchM files Schm_Eth_43_NETC,c and Schm_Eth_43_NETC.h generated for the new naming In the driver: Add in the HLD and IPW M4 tags that will be replaced with the infix The files need to be renamed, the types, the functions, etc. Do not rename the types and defines that are specified in Eth_GeneralTypes. Those need to keep their name, as they will be used as defined by all Eth drivers (if more drivers are present in a project) Update the xdm file to change the package name and use the short_name of the driver instead of MODULE_NAME where needed Update the mak file of the driver to rename all files and to propagate the m4_infix_value in all needed files In the tests: Change the xdm configuration for the tests to use the new format Change the mak file of the tests to compile the correct plugin folder Create a wrapper file Eth.h which includes Eth_43_NETC.h and redefines all needed macros, typedefs and functions to point to the newly named entities

ID	Subtype	Headline and Description
ARTD-22309	Bug	[ADC] Adc_Ipw_EndHardwareConv and Adc_Ipw_EndSoftwareConv not used in corner case configuration<*> Detailed description (how to reproduce it): With DMA disabled, SW normal groups with interrupt (no HW normal groups), EOC enabled, Adc Use Hardware Normal Groups disabled: Adc_Ipw_EndHardwareConv not used. Workaround is to enabled AdcUseHardwareNormalGroups, with minor impact on code size. With DMA disabled, HW triggered injected groups (no SW injected groups), EOC enabled, Adc Use Software Injected Group disabled: Adc_Ipw_EndSoftwareConv not used. Workaround is to enable Adc Use Software Injected Group, with minor impact on code size. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Observed behavior: See description Expected behavior: No warning Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Propose for this release:
ARTD-22352	Bug	S32DS3.4 Pin Tool Configuration for S32K3xx doesn't show 3 external signals per ADC<*> The problem occurs when trying to configure external channels for ADC using a multiplexer. We have 3 output signals per ADC module, in case of ADC0 they are ADC0_MA[0], ADC0_MA[1] and ADC0_MA[2]. The tool however only allows to select mux_output and hence when we attempt to configure the 3 signals, they show an error which tells that there is a conflict. Please see the attached picture.
ARTD-22397	New Feature	[RM] Implement XRDC Gui Mock up for Domain master assignment in the RM Driver<*> The XRDC GUI configurators (Tresos and CT) need to be reviewed to incorporate the feedback from [~nxa14515] and [~nxa21761]. Update domain configuration follow slide 2&3
ARTD-22454	Bug	[platform] Analysis the consistent between functionalities requirement and driver implementation<*> Situation: During the last minutes of S32K3 1.0.0, we used an owner tool to check the consistent between requirement and source code implementation and found some drivers that have the inconsistent between the functions' requirements and drivers implementation. Something is really to fix in the below scenarios: Miss or redundant parameters. Platform is declared mark for this situation Wrong function name Functions are not expose to Users (in header files) We already fixed in Platform, LIN, MCL, MCU, LIN, SENT, FLS, ADC, SAI drivers. The rests should be analysis and dig into the inconsistent if it is wrong or not. The following 3 categories were found : The functions are declared in "*.h" files of driver code (exported to user) but not included in "ReqExport.txt" file (no requirement are found in Doors > no traceability > no test) The functions are found in "ReqExport.txt" (requirement exists) but the functions are not declared in "*.h" files of driver code (are not present for user) The function name is found in both "ReqExport.txt" and in "*.h" file but there is at least one mismatch on data type, variable name, ... Proposal: With the remaining findings, please to: This ticket should perform after requirement analyis ticket Export all requirement and take a review to conclude the consistent between requirement and implementation. Please take a review on Crucible, the checklist at attachment. In the case there is the needed to update driver or to update requirement, please create a ticket to implement and link to this ticket For each driver, analysis and resolution should be completed with relevant information Reference: Findings from S32K3 1.0.0 release (attachment), as optional Contact SW Testers to provide the latest results for each drivers (it's mandatory input)
ARTD-22537	New Feature	[BASE] Remove release note link in rtd.collateral.release_id.xml file<*> NewWorkDescription: The release notes document link (from Flexera) will be available on RTD Updatesite description !image-2021-12-20-14-48-58-473.png! The release note document file inside Updatesite is no longer exist. So, the old link to release note pushed in itm.<PlatformName>.rtd.collateral.release_id.xml should be removed. Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: NA

ID	Subtype	Headline and Description
ARTD-22859	New Feature	Implement XRDC Gui Mock up for Memory region(part 2) in the RM Driver<*> The XRDC GUI configurators (Tresos and CT) need to be reviewed to incorporate the feedback from [~nxa14515] and [~nxa21761]. Add validate check for overlap regions (Start address, end address). 2 regions same memory controller should not overlap address. If yes, raise a warning. using <a:da name="WARNING" type="XPath">
ARTD-22898	New Feature	Implement XRDC Gui Mock up for Memory region(part 3) in the RM Driver<*> The XRDC GUI configurators (Tresos and CT) need to be reviewed to incorporate the feedback from [~nxa14515] and [~nxa21761]. Remove Mrc descriptor field and generate it automatically. Check if configured Mrc is over its number of descriptors.
ARTD-22910	New Feature	[RM] Configure XRDC Sema42 with logical channel instead of hardware sema42 in HLD<*> NewWorkDescription: Feature Xrdc sema42 is using Sema42 hardware to configure in HLD. But Seme42 supports logic channels to configure. Need an update to Xrdc sema42 used logic channels to config !image-2021-12-29-14-04-41-484.png|width=616,height=261! Also, need remove u32XrdcLock}} in define stuct Xrdc_Ip_MemConfigType}} because it's not used Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Update interface and codegen for XRDC
ARTD-22902	Bug	[CAN] Can_SetBaudrate still change internal state in case of failure/timeout<*> Detailed description (how to reproduce it): !image-2021-12-29-10-27-41-462.png! Can_au16BaudrateIDConfig[Controller]* is being changed unconditionally (without checking eRetVal status => this will cause related api (Can_SetControllerMode will work on unexpected previous config state of {_}*Can_au16BaudrateIDConfig*{_}{_}){_} Please also re-check other similar API Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: CAN_TC_FCT_1666 Observed behavior: Expected behavior: status of setting api should be checked to make sure not to save non-working configuration, for example, as below expected handler: !image-2021-12-29-10-26-33-630.png! Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-22933	Bug	[CAN] CAN_BUSOFF_POLLING_SUPPORT is generated differently between S32CT and EB<*> Detailed description (how to reproduce it): Create s32ct / s32k148 project: config CanController_0/ bus-off processing type as POLL config CanController_1/ bus-off processing type as INTERRUPT Make the same settings on EB, then comparing two generated code Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: !image-2021-12-31-15-28-51-444.png! Expected behavior: Two generators should generate similar code Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A

ID	Subtype	Headline and Description
ARTD-22976	New Feature	[CAN] implement new timestamp requirements CPR_RTD_00581.can, CPR_RTD_00582.can, CPR_RTD_00583.can, CPR_RTD_00584.can, CPR_RTD_00585.can Part 2 ,,"NewWorkDescription: new requirements need to be implemented: CPR_RTD_00581.can:Service name: Can_GetCurrentTime Syntax: Std_ReturnType Can_GetCurrentTime(uint8 ControllerId, Can_TimeStampType timeStampPtr) Service ID[hex]: 0x13 Sync/Async: Synchronous Reentrancy: Non Reentrant Parameters (in): ControllerId Index of the addresses CAN controller. Parameters (out): timeStampPtr current time stamp Return value: Std_ReturnType E_OK: successful E_NOT_OK: failed Description: Shall return current timestamp for the CAN controller CPR_RTD_00582.can:Service name: Can_EnableEgressTimeStamp Syntax: void Can_EnableEgressTimeStamp (Can_HwHandleType Hth) Service ID[hex]: 0x14 Sync/Async: Synchronous Reentrancy: Non Reentrant Parameters (in): Hth HW-transmit handle used for enabling the time stamp. Description: Shall activate egress time stamping on a dedicated HTH. CPR_RTD_00583.can:Service name: Can_GetEgressTimeStamp Syntax: Std_ReturnType Can_GetEgressTimeStamp (PduIdType TxPduId, Can_HwHandleType Hth, Can_TimeStampType timeStampPtr) Service ID[hex]: 0x15 Sync/Async: Synchronous Reentrancy: Non Reentrant for the same TxPduId. Parameters (in): TxPduId L-PDU handle of CAN L-PDU for returned timestamp Hth HW-transmit handle for the retrieved egress timestamp Parameters (out): timeStampPtr current timestamp Return value: Std_ReturnType E_OK: success E_NOT_OK: failed to read timestamp. Description: Shall read back the egress timestamp on a dedicated message object. This function has to be called within the TxConfirmation() function. CPR_RTD_00584.can:Service name: Can_GetIngressTimeStamp Syntax: Std_ReturnType Can_GetIngressTimeStamp (Can_HwHandleType Hrh, Can_TimeStampType timeStampPtr) Service ID[hex]: 0x16 Sync/Async: Synchronous Reentrancy: Non Reentrant for the same Hrh, Reentrant for different Hrh Parameters (in): Hrh HW-receive handle for the retrieved ingress timestamp Parameters (out): timeStampPtr current time stamp Return value: Std_ReturnType E_OK: success E_NOT_OK: failed to read time stamp. Description: Shall read back the ingress timestamp on a dedicated message object and needs to be called within the RxIndication() function. CPR_RTD_00585.can:Name: CanGlobalTimeSupport Parent Container CanGeneral Description Shall enable/disable the Global Time APIs used when hardware timestamping is supported by CAN controller. Multiplicity 1 Type EcucBooleanParamDef Default value – Post-Build Variant Value false Value Configuration Class Pre-compile time X All Variants Link time – Post-build time – Scope / Dependency scope: local Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-22979	Bug	[PORT]Port.h: MemMap include missing<*> Detailed description (how to reproduce it): In the file Port.h a memory section is defined in the lines 317 and 321 by PORT_START_SEC_CONFIG_DATA_UNSPECIFIED and PORT_STOP_SEC_CONFIG_DATA_UNSPECIFIED. But in both cases, the include of the Port_MemMap.h is missing. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: In customer's integrator environment, their MemMap is checking the correctness of the memory sections which leads to compiling errors in this case. Expected behavior: Adding the include of the Port_MemMap.h within corresponding section, in order to fix the compiling errors in customer's integrator environment. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-23025	Bug	[port] Update missing exclusive areas in BSWMD for S32K3, S32ZSE, SJA11XX ,,"Detailed description (how to reproduce it): Do a repo sync on bswmd_creator to sync with the manifest (make sure that you've checked out BLN_BSWMD_CREATOR_04.08.03) Compile the plugin passing parameter GENERATE_BSWMD_FILE=ON to the make command (`p s1 b` in ZTH) If the plugin was compiled successfully and there are no errors from bswmd_creator regarding missing or unmapped exclusive areas, then you can close your clone with ""Fixed No Action Taken"". Otherwise, proceed with the solutions given in the ""Proposed solution"" section. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Missing exclusive areas in <Module>_Bswmd.arxml Expected behavior: All exclusive areas are included in <Module>_Bswmd.arxml Note: in the ""Expected behavior"" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Potential Issue #1 Missing exclusive areas for ISRs Solution #1 The bswmd_creator script will automatically fetch ISRs from the source code as long as they're defined with ISR(...). Every ISR mentioned in the ""exclusive_areas_to_be_defined_in_bsw_scheduler.dox"" files shall also be wrapped in ISR(...). For example: ADC_EXCLUSIVE_AREA_70 is used in function ISR(Ctu_Error_Isr) to protect the updates for CTU_IFR register Potential Issue #2 Missing exclusive areas for IPL functions which are not called by any HLD function Solution #2 # Have the EA mentioned in ""exclusive_areas_to_be_defined_in_bsw_scheduler.dox"" only as used by the IPL function. For example: ADC_EXCLUSIVE_AREA_17 is used in function Adc_Sar_Ip_AbortConversion to protect the updates for ADC_MCR register # Add the IPL function in NonASR_ServiceID.xml Note: Do not use other workarounds like artificially mentioning in .dox that the IPL function is called by an HLD function which is included in NonASR_ServiceID.xml (even though, in reality, it's not)
ARTD-23038	Bug	[RM] Missing some peripherals definition when using multi variant<*> Detailed description (how to reproduce it): With Multivariant, when config 2 Variant with different Configurations, Code Build Fail Preconditions: Enable multi variant configuration, at least 2 variant: VS0 and VS1 Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Some definition of peripherals is missing when using multi variant configuration because some peripherals are configuration in VS0 but not in VS0 Expected behavior: Definition of peripherals are generated for all variant Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Generate all definition of all peripherals from resource instead of configuration

ID	Subtype	Headline and Description
ARTD-23039	Bug	[dio] Update missing exclusive areas in BSWMD for SJA1XX, S32K3XX and STRXOneChip ,,"Detailed description (how to reproduce it): Do a repo sync on bswmd_creator to sync with the manifest (make sure that you've checked out BLN_BSWMD_CREATOR_04.08.03) Compile the plugin passing parameter GENERATE_BSWMD_FILE=ON to the make command (`p s1 b` in ZTH) If the plugin was compiled successfully and there are no errors from bswmd_creator regarding missing or unmapped exclusive areas, then you can close your clone with ""Fixed No Action Taken"". Otherwise, proceed with the solutions given in the ""Proposed solution"" section. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Missing exclusive areas in <Module>_Bswmd.arxml Expected behavior: All exclusive areas are included in <Module>_Bswmd.arxml Note: in the ""Expected behavior"" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Potential Issue #1 Missing exclusive areas for ISRs Solution #1 The bswmd_creator script will automatically fetch ISRs from the source code as long as they're defined with ISR(...). Every ISR mentioned in the ""exclusive_areas_to_be_defined_in_bsw_scheduler.dox"" files shall also be wrapped in ISR(...). For example: ADC_EXCLUSIVE_AREA_70 is used in function ISR(Ctu_Error_Isr) to protect the updates for CTU_IFR register Potential Issue #2 Missing exclusive areas for IPL functions which are not called by any HLD function Solution #2 # Have the EA mentioned in ""exclusive_areas_to_be_defined_in_bsw_scheduler.dox"" only as used by the IPL function. For example: ADC_EXCLUSIVE_AREA_17 is used in function Adc_Sar_Ip_AbortConversion to protect the updates for ADC_MCR register # Add the IPL function in NonASR_ServiceID.xml Note: Do not use other workarounds like artificially mentioning in .dox that the IPL function is called by an HLD function which is included in NonASR_ServiceID.xml (even though, in reality, it's not)
ARTD-23045	Bug	[I2c] Fix different short name node in ecvd file<*> Detailed description (how to reproduce it): [...] Fix different in ecvd file on LPi2c DS !image-2022-01-07-16-18-09-660.png! On HLD DS !image-2022-01-10-10-25-24-930.png!!image-2022-01-10-10-26-05-981.png!!image-2022-01-10-10-29-51-225.png!! image-2022-01-10-10-30-45-638.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-23087	New Feature	[FLS] Make the CRC check optional<*> NewWorkDescription: The CRC config check happening at Fls_Init takes 6ms, which is not needed as the image has been anyway authenticated. Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Make the CRC check optional, with default to OFF, disabled. Document this behavior in the manual, the reason for this change and when this check is needed.

ID	Subtype	Headline and Description
ARTD-23102	Bug	[LIN] Function interface don't matching with function API in driver<*> Detailed description (how to reproduce it): Function interface don't matching with function API in driver Preconditions: !image-2022-01-11-14-58-20-399.png! Test Case ID (internal TC that caught the defect) optional: !image-2022-01-11-14-58-25-115.png! Observed behavior: NA Expected behavior: NA Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-23108	Bug	[I2s] Flexio supports only 1 Master or Slave channel<*> On K1, Flexio has 4 shifters/timers. So it can support max 2 masters or 1 slave per derivatives. For K3 it will be higher since it has 8 shifters/timers But configurator support max 1 master or 1 slave for K1. This requires some changes in codegen Fix Master and Slave cannt work if the first resource index number is odd Add devtest to verify the new feature with multiple flexio configuration on K3 Remove I2sNumLogicChn node from configurator
ARTD-23127	Bug	[ADC] Build fail: "unresolved symbols: EndConversionNotification" when configuring transfer types are different between multi VS ,,"Detailed description (how to reproduce it): Build fail: ""unresolved symbols: EndConversionNotification"" when configuring transfer types are different between multi VS Preconditions: VS_0: ADC0: AdcTransferType: ADC_INTERRUPT ADC1: AdcTransferType: ADC_DMA VS_1: ADC0: AdcTransferType: ADC_DMA ADC1: AdcTransferType: ADC_INTERRUPT Test Case ID (internal TC that caught the defect) optional: Adc_TC_FCT_1601 Adc_TS_023 cfg 3VS_PC_DMA Observed behavior: Build fail log: [elxr] (error #412) unresolved symbols: 2 Adc_Ipw_Adc1EndConversionNotification from Adc_Ip_VS_1_PBcfg_c.o Adc_Ipw_Adc0DmaTransferCompleteNotification from Dma_Ip_VS_1_PBcfg_c.o Only ADC_UNIT_1_DMA_TRANSFER_USED and ADC_UNIT_0_END_CONVERSION_NOTIF_USED define in ADC_CfgDefines.h Expected behavior: Build done Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-23161	Bug	[SPI] Spi_SyncTransmit with length is 0 not Timeout erorr<*> Detailed description (how to reproduce it): Sync Transmit 1 job / 1 channel with 0 lengh EB. Lpspi_Ip_SyncTransmit: State->RxIndex = State->ExpectedFifoReads =0 not into while loop so not check timeout and return LPSPI_IP_IDLE !image-2022-01-14-16-12-26-000.png|thumbnail! Preconditions: Sync Transmit 1 job / 1 channel with 0 lengh EB: Spi_SetupEB(SpiConf_SpiChannel_007, Spi_TestDataTx[0], Spi_TestDataRx[0], 0) !image-2022-01-14-16-17-47-639.png|thumbnail! Test Case ID (internal TC that caught the defect) optional: Spi_TC_PER_1000 Observed behavior: Lpspi_Ip_SyncTransmit return LPSPI_IP_IDLE Spi_SyncTransmit return E_OK Expected behavior: Lpspi_Ip_SyncTransmit return LPSPI_IP_TIMEOUT Spi_SyncTransmit return E_NOT_OK Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA

ID	Subtype	Headline and Description
ARTD-23199	Bug	[BASE][S32CT] ECVD files containing INDEX elements don't pass the XSD validation<*> Detailed description (how to reproduce it): Generate the ECVD file of a component containing a setting that defines a "requiresIndex" option. Validate the generated ECVD file against the XSD. Preconditions: ECVD file containing an INDEX element Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: ECVD files containing INDEX elements don't pass the validation check of the schema definition (AUTOSAR_00046.xsd) Expected behavior: ECVD files containing INDEX elements pass the validation check of the schema definition (AUTOSAR_00046.xsd) Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: INDEX elements should not be generated in the middle of another group's sequence. In particular, for ECUC-CONTAINER-VALUE, the INDEX element shall be placed between SHORT-NAME and DEFINITION-REF elements.
ARTD-23261	Bug	[ADC] Import ECVD with errors from S32ConfigurationTool to Tresos configurator<*> Detailed description (how to reproduce it): [ADC] Import ECVD with errors from S32CT to EBT Steps: # Create new project wizard on S32DS and add component Adc # Generate ECVD for Adc component # Create new project wizard on EBT and add component Adc # Import ECVD and enable auto mapping # Run importer # VERIFICATION_POINT: Run importer without error, no error on EBT project => FAIL !image-2022-01-18-14-50-14-333.png! Workaround: replace AdcUserCfg to Adc in ecvd file !image-2022-01-18-14-54-12-843.png! Preconditions: Test Case ID (internal TC that caught the defect) optional: Adc_TS_COT_003 Observed behavior: Expected behavior: Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-23275	Bug	[UART] - Build fail on CT IP driver when adding a callback parameter<*> Detailed description (how to reproduce it): Import any IP uart driver CT component in S32DS. Configure a callback parameter. Generate the configuration files. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: There is a build fail on this configuration Expected behavior: Analyze the Uart Callback Parameter usage. Define a way to define/declare the callback in parameter. Fix build error. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-23291	Bug	[WDG] Generate fail ECVD for Wdg_43_Instance1 on S32DS<*> Detailed description (how to reproduce it): Step 1: Custom tool [^validate_ip_ecpd.pl] Step 2: Update file [^plugin.xml] Step 3: Update [^Wdg_TS_COT_005.mak] file Step 4: clean generate Wdg_TS_COT_005 CFG_SETS = s32k148_lqfp176 Step 5: Compare all files in original_configuration folder with new_configuration folder Step 6: Import Wdg_43_Instance1.epc at path: " ...\output\S32K1XX_S32K148\wdg \Wdg_TS_COT_005_cfgs32k148_lqfp176\generate_s32ct\output " into S32DS Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: Wdg_43_Instance1.ecpd not matching between EB and CT !image-2022-01-19-16-12-00-689.png|width=1042,height=151! Unable to generate .c and .h files related to Wdg_43_instance1 for EB !image-2022-01-19-16-14-39-466.png|width=972,height=221! Error when importing epc file into S32DS !image-2022-01-19-16-13-37-326.png|width=644,height=370! Expected behavior: Generate ecvd successfully for Wdg_43_Instance1 Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-23295	Bug	[ICU][S32K3XX] when configuring eMios channel using masterbus, error in DS IPL ,,"Detailed description (how to reproduce it): When configuring eMios channel using CounterBus in ICU there is an error in DS IPL: In Peripheral Emios_Mcl_Ip -At General Configuration Tab, put the check to “Enable Emios Common Support” At Emios Common Tab, Select MCB_UP_COUNTER to “Master Bus Mode Type” and Set 65535 to “Default Period” and . In Peripheral Emios_Icu At IcuHwInterruptConfigList tab of IcuConfigSet Tab, Enable EMIOS_0_CH_0 At IcueMios Tab of IcuConfigSet Tab, select EMIOS_ICU_BUS_DIVERSE to “IcuEmiosBusSelect” and Select following to “IcuEmiosBusRef”. /Emios_Mcl_Ip_1/EmiosMcl/EmiosCommon_0/EMIOS_0_MasteBus0 pls see attached files Preconditions: use ICU component with configuration for Emios channels that need Couter Bus. Prepare the MCL side settings and try to generate code. Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Error issued on generation Expected behavior: No error on generation Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: please see analysis tab
ARTD-23328	Bug	[PORT] Disable the configuration of CommonPublishedInformation container in S32DS<*> Detailed description (how to reproduce it): In S32CT, Port driver still allows user to config all the parameters in CommonPublishedInformation container. It will violate the Autosar expectation. Please refer General Specification of Basic Software Modules AUTOSAR CP Release 4.4.0 documentaion chapter 10.3Published Information Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Expected behavior: Port driver disables the configuration of that container in S32DS Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA

ID	Subtype	Headline and Description
ARTD-23329	Bug	[DIO] Disable the configuration of CommonPublishedInformation container in S32DS<*> Detailed description (how to reproduce it): In S32CT, Port driver still allows user to config all the parameters in CommonPublishedInformation container. It will violate the Autosar expectation. Please refer General Specification of Basic Software Modules AUTOSAR CP Release 4.4.0 documentaion chapter 10.3Published Information Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Expected behavior: Port driver disables the configuration of that container in S32DS Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-23332	Bug	[CAN] redundant check pState->mbs[u32MbIdx].isPolling inside FlexCAN_IRQHandlerTxMB<*> Detailed description (how to reproduce it): [...] Preconditions: analysis ccov report (MCDC tab) !image-2022-01-21-14-05-50-639.png|thumbnail! Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: redundant check causes uncovered code in MCDC report !image-2022-01-21-14-12-20-287.png|thumbnail! Expected behavior: analysis redundant code Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-23347	Bug	[CAN] Driver is not compiling when using INFIX<*> Detailed description (how to reproduce it): Driver is not compiling when using INFIX. There are multiple variables that are infixed in some of the places, not in all places. There are 2 methods of adding infix using M4, it is almost impossible to keep track of the infix method based on the file. There is no INFIX in the IP DRIVER. Flex LLCE will use the IP driver data structures in the interface, so it can't compile along FlexLLCE driver on the host side. Preconditions: Generate the driver using infix Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Not compiling {_}*Expected behavior:*{_}To compile Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Fix Compile error. Stick to only one way of adding infix. Add INFIX to IP driver.

ID	Subtype	Headline and Description
ARTD-23359	Bug	[I2C] Wrong variable of I2c_ErrorCallback<*> Detailed description (how to reproduce it): Project: C:\NXP\SW32_RTD_4.4_3.0.0\eclipse\plugins\I2c_TS_T40D11M30I0R0\examples\EBT \I2c_HLD_Transfer_S32G274A_M7 EB treos: DMA was in disable state. Disable I2c_Callback, Enable I2c_ErrorCallback. !image-2022-01-24-11-15-02-761.png|width=515,height=330! I2c_Ipw.c : !image-2022-01-24-11-16-52-969.png|width=878,height=103! I2C_EVENT_DMA_TRANSFER_ERROR_MASTER could not be found in I2c_Ipw.c* file result to building failed. But I found I2C_MASTER_EVENT_DMA_TRANSFER_ERROR in I2c_Ip_Callbacks.h. I2c_Ip_Callbacks.h : !image-2022-01-24-11-42-53-783.png|width=510,height=131! So, I doubt it should be "I2C_MASTER_EVENT_DMA_TRANSFER_ERROR" instead of "I2C_EVENT_DMA_TRANSFER_ERROR_MASTER" in I2c_Ipw.c. Please help to check it. Thanks. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: N/A Expected behavior: N/A Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-23375	Bug	[LIN] The driver doesn't report error if PID is set incorrectly by user<*> Detailed description (how to reproduce it): A LIN frame was configured with an incorrect PID value, e.g. PID=0x10. However, the driver doesn't report any error in Lin_SendFrame() function, although the frame couldn't be sent at all. Preconditions: A LIN frame was configured with an incorrect PID value. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: The LIN driver doesn't report any error in Lin_SendFrame() function Expected behavior: The LIN driver shall report error in Lin_SendFrame() function in case PID was incorrect set by user. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: CE's comment: When going down the Lin_SendFrame() path it was seen that the parity was set incorrectly, so Lin_Ipw_CheckFrameInfo() was returning E_NOT_OK. However, TempReturn does not change from initialization in Lin_Ipw_SendFrame(), so eventually Lin_SendFrame() will return E_OK. It was a typical issue of missing “else” condition in the implementation. A possible workaround would be adding the missing “else” condition in the “if” statement. Something like: !image-2022-01-25-14-07-05-171.png!
ARTD-23384	Bug	[WDG]There are some data types mismatch between EBT and CT<*> There are some value mismatches between EBT and CT. Please see for example the attached file. [VALIDATION] Mismatch between the types of EPD:WdgClockValue (ECUC-INTEGER-PARAM-DEF) and CT:WdgClockValue (info) [VALIDATION] EPD:WdgEcucPartitionRef has multiplicity, but CT:WdgEcucPartitionRef is not an array [VALIDATION] EPD:WdgExternalConfiguration has multiplicity, but CT:WdgExternalConfiguration is not an array [VALIDATION] EPD:WdgExternalContainerRef has multiplicity, but CT:WdgExternalContainerRef is not an array Verify EPD/EPC support for HLD and IPLD. Please refer to [this post on Teams https://teams .microsoft.com/l/message/19:e451c595d3ba410c8f9c1f5efc19a8a3@thread.tacv2/1606904026692? tenantId=686ea1d3-bc2b-4c6f-a92c-d99c5c301635&groupId=f9decd68-7b74-4101-a4d2- ad54e86f727f&parentMessageId=1606904026692&teamName=Zebra&channelName=Configuration%20(code%2C%20DS%2C %20EB%2C%20etc)&createdTime=1606904026692] for additional details. From the presentation, the main focus should be on the following sections: Mapping XDM to Component EPD Importer EPD Generation EPC Importer EPC Generation

ID	Subtype	Headline and Description
ARTD-23401	Bug	[Gpt] Emios ChannelTickFrequency need update formula<*> Detailed description (how to reproduce it): there are two UC, with different Pre-scaler (16 vs 1). Based on this, the corresponding Gpt channel for EmiosChannel_1 should be 16 times the corresponding GPT channel for EmiosChannel_0. However, both of these GPT channels are having equal clock frequency, after automatically calculated by EB GUI. please see the picture for more details Preconditions: configuration gptEmios same instance have channel with different prescaler. Test Case ID (internal TC that caught the defect) optional: Gpt_TS_001 Observed behavior: Prescaler of emios channels are different but having same clock frequency, after automatically calculated by EB GUI. Check also s32 DesignStudio. Expected behavior: Correct Calculate tick frequency Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: correct Calculate tick frequency
ARTD-23414	Bug	[dio] [S32CT] Incorrect enable attributes for ConfigTimeSupport fields<*> Detailed description (how to reproduce it): Manually check the ConfigTimeSupport fields of the S32CT component / template Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: POST_BUILD_VARIANT_USED has enable="false" IMPLEMENTATION_CONFIG_VARIANT has enable="false" Expected behavior: POST_BUILD_VARIANT_USED has enable="false" if and only if postBuildVariantSupport="false" in the config set's options_expr. IMPLEMENTATION_CONFIG_VARIANT has enable="true" or no enable attribute (which is equivalent to enable="true"). Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: POST_BUILD_VARIANT_USED has enable="false" if and only if postBuildVariantSupport="false" in the config set's options_expr. IMPLEMENTATION_CONFIG_VARIANT has enable="true" or no enable attribute (which is equivalent to enable="true").
ARTD-23417	Bug	[fee] [S32CT] Incorrect enable attributes for ConfigTimeSupport fields<*> Detailed description (how to reproduce it): Manually check the ConfigTimeSupport fields of the S32CT component / template Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: POST_BUILD_VARIANT_USED has enable="false" IMPLEMENTATION_CONFIG_VARIANT has enable="false" Expected behavior: POST_BUILD_VARIANT_USED has enable="false" if and only if postBuildVariantSupport="false" in the config set's options_expr. IMPLEMENTATION_CONFIG_VARIANT has enable="true" or no enable attribute (which is equivalent to enable="true"). Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: POST_BUILD_VARIANT_USED has enable="false" if and only if postBuildVariantSupport="false" in the config set's options_expr. IMPLEMENTATION_CONFIG_VARIANT has enable="true" or no enable attribute (which is equivalent to enable="true").
ARTD-23425	Bug	[lin] [S32CT] Incorrect enable attributes for ConfigTimeSupport fields<*> Detailed description (how to reproduce it): Manually check the ConfigTimeSupport fields of the S32CT component / template Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: POST_BUILD_VARIANT_USED has enable="false" IMPLEMENTATION_CONFIG_VARIANT has enable="false" Expected behavior: POST_BUILD_VARIANT_USED has enable="false" if and only if postBuildVariantSupport="false" in the config set's options_expr. IMPLEMENTATION_CONFIG_VARIANT has enable="true" or no enable attribute (which is equivalent to enable="true"). Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: POST_BUILD_VARIANT_USED has enable="false" if and only if postBuildVariantSupport="false" in the config set's options_expr. IMPLEMENTATION_CONFIG_VARIANT has enable="true" or no enable attribute (which is equivalent to enable="true").

ID	Subtype	Headline and Description
ARTD-23433	Bug	[port] [S32CT] Incorrect enable attributes for ConfigTimeSupport fields<*> Detailed description (how to reproduce it): Manually check the ConfigTimeSupport fields of the S32CT component / template Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: POST_BUILD_VARIANT_USED has enable="false" IMPLEMENTATION_CONFIG_VARIANT has enable="false" Expected behavior: POST_BUILD_VARIANT_USED has enable="false" if and only if postBuildVariantSupport="false" in the config set's options_expr. IMPLEMENTATION_CONFIG_VARIANT has enable="true" or no enable attribute (which is equivalent to enable="true"). Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: POST_BUILD_VARIANT_USED has enable="false" if and only if postBuildVariantSupport="false" in the config set's options_expr. IMPLEMENTATION_CONFIG_VARIANT has enable="true" or no enable attribute (which is equivalent to enable="true").
ARTD-23438	Bug	[sent] [S32CT] Incorrect enable attributes for ConfigTimeSupport fields<*> Detailed description (how to reproduce it): Manually check the ConfigTimeSupport fields of the S32CT component / template Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: POST_BUILD_VARIANT_USED has enable="false" IMPLEMENTATION_CONFIG_VARIANT has enable="false" Expected behavior: POST_BUILD_VARIANT_USED has enable="false" if and only if postBuildVariantSupport="false" in the config set's options_expr. IMPLEMENTATION_CONFIG_VARIANT has enable="true" or no enable attribute (which is equivalent to enable="true"). Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: POST_BUILD_VARIANT_USED has enable="false" if and only if postBuildVariantSupport="false" in the config set's options_expr. IMPLEMENTATION_CONFIG_VARIANT has enable="true" or no enable attribute (which is equivalent to enable="true").
ARTD-23442	Bug	[uart] [S32CT] Incorrect enable attributes for ConfigTimeSupport fields<*> Detailed description (how to reproduce it): Manually check the ConfigTimeSupport fields of the S32CT component / template Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: POST_BUILD_VARIANT_USED has enable="false" IMPLEMENTATION_CONFIG_VARIANT has enable="false" Expected behavior: POST_BUILD_VARIANT_USED has enable="false" if and only if postBuildVariantSupport="false" in the config set's options_expr. IMPLEMENTATION_CONFIG_VARIANT has enable="true" or no enable attribute (which is equivalent to enable="true"). Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: POST_BUILD_VARIANT_USED has enable="false" if and only if postBuildVariantSupport="false" in the config set's options_expr. IMPLEMENTATION_CONFIG_VARIANT has enable="true" or no enable attribute (which is equivalent to enable="true").

ID	Subtype	Headline and Description
ARTD-23452	Bug	[S32K3][SENT] There are some issues related to Polling mode of SENT<*> Detailed description (how to reproduce it): {*}Issues 1{*}: Serials (Slow) Message cannot be received normally in in case of multi-channel receiving. {*}Issues 2{*}: The Error Notification of different channels seems to be called incorrectly by each other occasionally. {*}Issues 3{*}: When there are multiple channels and Sent_GetSerialMsgData(), which will open interrupt of SENT, is used, if the other edge of a channel comes during the ISR of SENT, the second flag bit triggered by the latter edge may be cleared, resulting in missing an edge. {*}Issues 4{*}: In Sent_GetSerialMsgData(), it is not feasible to process multi-channel data serially, because the buffer of the latter channels are prone to overflow. {*}Issues 5{*}: When reprocessing data, there is a problem with the buffer index continuation. I found some workarounds which is uploaded within the attached Email. I modified some source code of SENT low level driver which can preliminarily solve these issues I mentioned above as I tested, and {+}*just for your reference*{+}. Preconditions: Set SENT work at {+}*Polling mode*{+}, and use Sent_GetFastChannelMsgData(), Sent_GetSerialChannelMsgData(), Sent_GetFastMsgData() and Sent_GetSerialMsgData() to receive multi-sent signals (in my testing it's two SENT channels), respectively. The error notifications of fast and slow message also should be enabled. Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-23453	New Feature	[S32K3][SENT] Expand the range of Sent Tick Length to less than 3 us.<*> NewWorkDescription: From customer NASN, the Sent Tick Length of their sensor is about 1.65 us that is less than smallest standard tick length 3 us. But obviously the FlexIO module can realize such a Tick Length, so it is better to expand the feature of SENT to cover more situation. Requirement source: Customer Request (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]
ARTD-23495	Bug	[CAN] s32k342 only support 4 controllers<*> Detailed description (how to reproduce it): s32ct for K342 show more than 4 controllers !image-2022-01-28-11-06-18-789.png|thumbnail! it may come from base component Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: problem in registers.xml file of base module Expected behavior: s32k342 only support 4 controllers Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-23518	New Feature	[ETH] Add support for 200Mbps MII on K3<*> NewWorkDescription: According to the latest S32K3 RM & DS, EMAC can work with an overclocked MII at 50 MHz TX/RX_CLK and 200Mbps data rate. Requirement source: S32K3 Reference Manual Rev4 Draft A & Data Sheet Rev 3 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Update EthCtrlMacLayerSpeed and the constraints of EthCtrlConfigShaper to handle 200M in MII.

ID	Subtype	Headline and Description
ARTD-23559	Bug	[ITG] [Uart] HLD Transmit and Receive functions need to check both receive and transmit status for reporting det error<*> Detailed description (how to reproduce it): This ticket has been cloned from https://jira.sw.nxp.com/browse/ARTD-17018. In the https://jira.sw.nxp.com/browse/ARTD-19289 the checking on both transmission and reception on HLD for busy channel has been removed because it is not the correct approach on the loopback mode. Due to missing information on the ARTD-17018, we cannot figure out if the both operations checkins are necessary. What we need to do in this ticket bug is analyze if the updates are impacted the other functionality. If the impact exists, update the code in the way that driver works correctly both on internal loopback and normal mode. Another analysis required is that: is the last bug impacting all the platforms? If yes, then let's update the bug according If no, then let's update the code accordingly (maybe an update on the generic file is not correct). Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: NA Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-23581	Bug	[S32K1XX] [Crypto] Missing field CommonPublishedInformation in ECVD file of HLD<*> Detailed description (how to reproduce it): When config HL layer on S32DS , ECVD file missing fied " CommonPublishedInformation" Test Case ID (internal TC that caught the defect) optional: Crypto_TS_COT_007 Observed behavior: When config HL layer on S32DS , ECVD file missing field " CommonPublishedInformation", see detail at attachments site Expected behavior: When config HL layer on S32DS, ECVD file have all field Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-23609	Bug	[Uart] ECPD: Difference EPC from EBT to CT<*> Detailed description (how to reproduce it): [ECVD files which are generated by EBT and CT have difference as picture !image-2022-02-09-14-41-52-843.png|thumbnail! !image-2022-02-09-14-42-19-290.png|thumbnail!] Preconditions: NA Test Case ID (internal TC that caught the defect) optional: Uart_TS_ECPD_01 Observed behavior: NA Expected behavior: ECVD between EBT and CT must be same Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-23612	Bug	[MCL] DMA Enable Start option removed for DMA Transfer configuration<*> Changing Enable Start in the configuration tool does not change the generated structure !image-2022-02-09-10-02-10-091.png|thumbnail! !image-2022-02-09-10-02-45-778.png|thumbnail!

ID	Subtype	Headline and Description
ARTD-23625	Bug	[CAN] out-of-range access when CAN_MAX_PARTITIONS < coreid value / multicore platforms<*> Detailed description (how to reproduce it): Create s32k324 project Enable multicore Configure only 1 partition (EcucPartition_0), and mapping it to core value 6 (or > 1) => review the value of CAN_MAX_PARTITIONS Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: review Observed behavior: detail in attachment Expected behavior: out-of-range access should be eliminated Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-23630	Bug	[CAN] Driver is not compiling when using INFIX check on S32CT<*> Detailed description (how to reproduce it): Driver is not compiling when using INFIX. There are multiple variables that are infixed in some of the places, not in all places. There are 2 methods of adding infix using M4, it is almost impossible to keep track of the infix method based on the file. There is no INFIX in the IP DRIVER. Flex LLCE will use the IP driver data structures in the interface, so it can't compile along FlexLLCE driver on the host side. Preconditions: Generate the driver using infix Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Not compiling {_}*Expected behavior:*{_}To compile Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Fix Compile error. Stick to only one way of adding infix. Add INFIX to IP driver.
ARTD-23643	Bug	[PORT] Inconsistent file name and component references<*> Detailed description (how to reproduce it): Inconsistent casing between the driver file names and the references from CT components. This makes the build/generate stage fail on Linux environments which are case sensitive. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Check and ensure all file names and the places where they are referenced, will use the exact same case. See the attached email for more details.
ARTD-23682	New Feature	[PORT] Change the define names to not contain derivatives name<*> NewWorkDescription: [https://bitbucket.sw.nxp.com/projects/ARTD/repos/port/pull-requests/410/overview?commentId=1104467] [Radu-Andrei Brasoveanu|https://bitbucket.sw.nxp.com/users/nxa19269] i would advise in creating a follow up ticket for entire code and changing the define names to not contain derivatives name. more suitable will be to use something like: FEATURE_PORT_CI_PORT_IP_PCR_MUXING}} Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Change the define names to not contain derivatives name.

ID	Subtype	Headline and Description
ARTD-23704	Bug	[PWM] Long execution time of mc related api<*> Detailed description (how to reproduce it): 4 Motor control(MC)examples were created to test RTD deployment in the most common mc use cases : All examples were created using Low level API: MCSPTE1AK344_BLDC_6Step_hall_ll MCSPTE1AK344_BLDC_6Step_sensorless_ll MCSPTE1AK344_PMSM_FOC_1Sh_ll MCSPTE1AK344_PMSM_FOC_3Sh_ll as well as Autosar API: MCSPTE1AK344_BLDC_6step_hall_as_tr MCSPTE1AK344_BLDC_6Step_sensorless_as_tr MCSPTE1AK344_PMSM_FOC_1Sh_as_tr MCSPTE1AK344_PMSM_FOC_3Sh_as_tr Examples with Autosar API were tested with RTD Beta release (they are being ported to RTM release) Examples with Low Level API has been tested with RTD RTM release. Examples based on Beta release can be found here : [https://nxp1.sharepoint.com/teams/8_8/Shared%20Documents/Forms/AllItems.aspx?RootFolder=%2Fteams%2F8%5F8%2FShared%20Documents%2FGPIS%2F2%29%20GPIS%20Solutions%2F1%29%2E%20Motor%20Control%2FS32K3%2FSW%20example%20%2D%20RTD&FolderCTID=0x012000AA56F78ADAFAF34494EE7E329455794F&View=%7B2A8302C6%2DEA4B%2D4B43%2DA84E%2D646706AB5F7D%7D] Examples based on RTM release can be sent on demand. Note: TCM was not used for RTD functions, Caches were enabled. Execution time of RTD functions was measured using systic timer when motor was spinning at 1000 rpm. Worst-case was captured during 5 minutes window. In case of any question about methodology, project settings or if any additional information is needed please do not hesitate to contact me: tomas.fedor@nxp.com Observed behavior: All details about collaboration with RTD team can be found here: [https://nxp1-my.sharepoint.com/:f:/g/personal/tomas_fedor_nxp_com/EhB3sgULJt5Ij0YHzEFJN-sBr3dEPgPsgKASAD8qM-N4zA?e=7Js0Xu] Execution time of following API was too long: Emios_Pwm, Emios_Mcl, Adc_Sar_Ip, Bctu_Ip, Lcu_Ip, Emios_Gpt Adc, Pwm, Mcl, Gpt Location: Collaboration with RTD team\jira_ticket_execution_time\api_testing.xlsx Following scenarios within tested examples were identified as the most critical (items are ordered according the priority) 1) PWM and Trigger update in PMSM singleshunt application (Highest priority) MCSPTE1AK344_PMSM_FOC_1Sh_ll & MCSPTE1AK344_PMSM_FOC_1Sh_as_tr In this scenario we have to update 9 channels (if we considered frequency wobbling we would have to update also 2 time base channels). The worst measured execution time of this action was Non Autosar: Measured in application: 31.275 us Calculated from worst-cases of particular functions: 52.23375 us Autosar : Calculated from worst-cases of particular functions: 74.45 us Location: Collaboration with RTD team\jira_ticket_execution_time\api_testing.xlsx: tab PWM and Trigger update in PMSM 2) ADC reading and list configuration. There are various caseses across the examples: Execution tine was 2.1375us 4.275us Changing list of conversions 1.84375us Location: Collaboration with RTD team\jira_ticket_execution_time\api_testing.xlsx: tab ADC reading and list config 3)LCU: Lcu_Ip_SetSyncOutputEnable 2.8us Mcl_SetLcuSyncOutputEnable 3.1125us Location: Collaboration with RTD team\jira_ticket_execution_time\api_testing.xlsx 4)Timer: Emios_Gpt_Ip_StopTimer 1.15625 us Emios_Gpt_Ip_StartTimer 2.85625 us Location: Collaboration with RTD team\jira_ticket_execution_time\api_testing.xlsx Expected behavior: All details about collaboration with RTD team can be found here: [https://nxp1-my.sharepoint.com/:f:/g/personal/tomas_fedor_nxp_com/EhB3sgULJt5Ij0YHzEFJN-sBr3dEPgPsgKASAD8qM-N4zA?e=7Js0Xu] Location: Collaboration with RTD team\Motor_control_req_test.xlsx list of all discussed requirements Location: Collaboration with RTD team\jira_ticket_execution_time\MC_REQ_0039.pptx defined requirement Location: Collaboration with RTDteam\jira_ticket_execution_time\MC_REQ_0039_testing_RTM.pptx tested requirement 1) PWM and Trigger update in PMSM singleshunt application (Highest priority) The same action using bare metal approach takes less than 2us{color}. We should get to this number as much as possible. 2) ADC reading and list configuration. The same action using bare metal approach takes less than 1us{color}.We should get to this number as much as possible. 3) LCU: The same action using bare metal approach takes less than 1us{color}.We should get to this number as much as possible. It is important when we want to dimension ... 4) Timer: ADC reading and list configuration. The same action using bare metal approach takes less than 1us{color}.We should get to this number as much as possible. StopTimer/StartTimer functionality is a push button action. Proposed solution optional: Any solution addressing this issue is welcomed. Just it is necessary to cover Non-Autosar as well as Autosar part. I would follow this principle:

ID	Subtype	Headline and Description
ARTD-23706	Bug	[GPT] Long execution time of mc related api<*> Detailed description (how to reproduce it): 4 Motor control(MC)examples were created to test RTD deployment in the most common mc use cases : All examples were created using Low level API: MCSPTE1AK344_BLDC_6Step_hall_ll MCSPTE1AK344_BLDC_6Step_sensorless_ll MCSPTE1AK344_PMSM_FOC_1Sh_ll MCSPTE1AK344_PMSM_FOC_3Sh_ll as well as Autosar API: MCSPTE1AK344_BLDC_6step_hall_as_tr MCSPTE1AK344_BLDC_6Step_sensorless_as_tr MCSPTE1AK344_PMSM_FOC_1Sh_as_tr MCSPTE1AK344_PMSM_FOC_3Sh_as_tr Examples with Autosar API were tested with RTD Beta release (they are being ported to RTM release) Examples with Low Level API has been tested with RTD RTM release. Examples based on Beta release can be found here : [https://nxp1.sharepoint.com/teams/8_8/Shared%20Documents/Forms/AllItems.aspx?RootFolder=%2Fteams%2F8%5F8%2FShared%20Documents%2FGPIS%2F2%29%20GPIS%20Solutions%2F1%29%2E%20Motor%20Control%2FS32K3%2FSW%20example%20%2D%20RTD&FolderCTID=0x012000AA56F78ADAFAF34494EE7E329455794F&View=%7B2A8302C6%2DEA4B%2D4B43%2DA84E%2D646706AB5F7D%7D] Examples based on RTM release can be sent on demand. Note: TCM was not used for RTD functions, Caches were enabled. Execution time of RTD functions was measured using systic timer when motor was spinning at 1000 rpm. Worst-case was captured during 5 minutes window. In case of any question about methodology, project settings or if any additional information is needed please do not hesitate to contact me: tomas.fedor@nxp.com Observed behavior: All details about collaboration with RTD team can be found here: [https://nxp1-my.sharepoint.com/:f:/g/personal/tomas_fedor_nxp_com/EhB3sgULJt5lj0YHzEFJN-sBr3dEPgPsgKASAD8qM-N4zA?e=7Js0Xu] Execution time of following API was too long: Emios_Pwm, Emios_Mcl, Adc_Sar_Ip, Bctu_Ip, Lcu_Ip, Emios_Gpt Adc, Pwm, Mcl, Gpt Location: Collaboration with RTD team\jira_ticket_execution_time\api_testing.xlsx Following scenarios within tested examples were identified as the most critical (items are ordered according the priority) 1) PWM and Trigger update in PMSM singleshunt application (Highest priority) MCSPTE1AK344_PMSM_FOC_1Sh_ll & MCSPTE1AK344_PMSM_FOC_1Sh_as_tr In this scenario we have to update 9 channels (if we considered frequency wobbling we would have to update also 2 time base channels). The worst measured execution time of this action was Non Autosar: Measured in application: 31.275 us Calculated from worst-cases of particular functions: 52.23375 us Autosar : Calculated from worst-cases of particular functions: 74.45 us Location: Collaboration with RTD team\jira_ticket_execution_time\api_testing.xlsx: tab PWM and Trigger update in PMSM 2) ADC reading and list configuration. There are various caseses across the examples: Execution tine was 2.1375us 4.275us Changing list of conversions 1.84375us Location: Collaboration with RTD team\jira_ticket_execution_time\api_testing.xlsx: tab ADC reading and list config 3)LCU: Lcu_Ip_SetSyncOutputEnable 2.8us Mcl_SetLcuSyncOutputEnable 3.1125us Location: Collaboration with RTD team\jira_ticket_execution_time\api_testing.xlsx 4)Timer: Emios_Gpt_Ip_StopTimer 1.15625 us Emios_Gpt_Ip_StartTimer 2.85625 us Location: Collaboration with RTD team\jira_ticket_execution_time\api_testing.xlsx Expected behavior: All details about collaboration with RTD team can be found here: [https://nxp1-my.sharepoint.com/:f:/g/personal/tomas_fedor_nxp_com/EhB3sgULJt5lj0YHzEFJN-sBr3dEPgPsgKASAD8qM-N4zA?e=7Js0Xu] Location: Collaboration with RTD team\Motor_control_req_test.xlsx list of all discussed requirements Location: Collaboration with RTD team\jira_ticket_execution_time\MC_REQ_0039.pptx defined requirement Location: Collaboration with RTDteam\jira_ticket_execution_time\MC_REQ_0039_testing_RTM.pptx tested requirement 1) PWM and Trigger update in PMSM singleshunt application (Highest priority) The same action using bare metal approach takes less than 2us{color}. We should get to this number as much as possible. 2) ADC reading and list configuration. The same action using bare metal approach takes less than 1us{color}.We should get to this number as much as possible. 3) LCU: The same action using bare metal approach takes less than 1us{color}.We should get to this number as much as possible. It is important when we want to dimm the light. 4) Timer: ADC reading and list configuration. The same action using bare metal approach takes less than 1us{color}.We should get to this number as much as possible. StopTimer/StartTimer functionality is a push button action. Proposed solution optional: Any solution addressing this issue is welcomed. Just it is necessary to cover Non-Autosar as well as Autosar part. I would follow this principle:

ID	Subtype	Headline and Description
ARTD-23729	Bug	[Port] Hard Fault at port initiation (Port_Init)<*> Detailed description (how to reproduce it): Use PORT_143 for the Plugins Create a random configuration and use Port_Init to initiate that. Test Case ID (internal TC that caught the defect) optional: Port_TC_WBT_0015 Observed behavior: The program runs into an infinity loop of Hard Fault at the clearing IMCR step (after the for loop at line 480 of Port_Ipw.c) !image-2022-02-17-15-30-09-316.png! !image-2022-02-17-15-30-22-735.png! The macro must be re-corrected according to the header files of the newest base's tag (PVT_BASE_S32K3XX_RTM_200_001). It should be IP_SIUL2_BASE Expected behavior: Port_Init must not run into Hard Fault loop when running through the IMCR clearing step
ARTD-23772	Bug	[I3c] ReadTerminate and Transfer Size seem redundant in transfer structure<*> Detailed description (how to reproduce it): generate and build any test suite (for ex. TS_005 and TS_006) Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: ReadTerminate and TransferSize seem redundant in transfer options structure. For use case master reads from slave, if SlaveTransferSize > MasterTransferSize Complete flag is not set when MasterBufferSize = 0, which leads to STOP not emitted. There are 2 possible scenarios: if ReadTerminate is set to the transfer size, STOP is emitted after ReadTerminate bytes and TERM warning/error is set in Slave error register; however, master receives a number of ReadTerminate bytes, with no error set in master erro register if ReadTerminate is not set, an SDA remains unchanged in a certain frame and Timeout error is set in Master error register Expected behavior: [...] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: remove ReadTerminate from transfer options structure and set it to the transfer size within driver logic when emitting START request when write, do remove operation to set the ReadTerminate
ARTD-23776	New Feature	[ETH]Update driver follow to RM Rev3 updated<*> NewWorkDescription: RM Rev.3 updated. Driver need to update accordingly. Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: RM Rev.3 updated. Driver need to update accordingly.
ARTD-23792	Bug	[S32K3 2.0.0][SENT] Wrong behavior when use SentFastFrame in Flexio_Sent_Ip_StartTransfer<*> Detailed description (how to reproduce it): In the function behavior Flexio_Sent_Ip_StartTransfer, it uses SentFastFrame* to get ChannelID and Instance. This is a wrong behavior. Flexio_Sent_Ip_StartTransfer is call from others function: Flexio_Sent_Ip_GetFastChannelMsgData, Flexio_Sent_Ip_GetFastMsgData, Flexio_Sent_Ip_GetSerialChannelMsgData, Flexio_Sent_Ip_GetSerialMsgData. In these functions, SentFastFrame is declared with no specific value so it can be used liked parameter-in in function Flexio_Sent_Ip_StartTransfer: !image-2022-02-22-15-31-04-999.png|width=618,height=99! !image-2022-02-22-15-32-05-202.png|width=913,height=56! Preconditions: Enable SentFastErrorNotif in configuration Test Case ID (internal TC that caught the defect) optional: Sent_TS_14 Observed behavior: NA Expected behavior: NA Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-23822	New Feature	[I3c] Add support to get master and slave status flags<*> NewWorkDescription: Add APIs to get master and slave status flags (MSTATUS and SSTATUS). Requirement source: RM.pdf Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-23825	Bug	[S32K3 2.0.0][SENT] Data[FLEXIO_INSTANCE_NO][ChannelId] always be reset in Flexio_Sent_Ip_GetSerialMsgData function<*> Detailed description (how to reproduce it): In function Flexio_Sent_Ip_GetSerialMsgData, there are some issues: # Data array always be reset before processing fast msg and serial msg. So it never jumps to serial msg processing segment. !image-2022-02-23-17-50-26-323.png|width=848,height=84! # Data's elements (.SerialState and FastMsgCount) must be reset only when a serial msg is captured. If not, it always detect another serial msg after the first serial msg. It should be like this: !image-2022-02-23-17-57-50-239.png|width=605,height=84! 3. Because the change of GetSerialMsgData function, it captures a present serial msg at right after calling this function so there is some variables are unnecessary in Flexio_Sent_Ip_GetSerialMsgData: FastMsgCount[FLEXIO_INSTANCE_NO][ChannelId] can be replaced by Data[FLEXIO_INSTANCE_NO][ChannelId].FastMsgCount. Flexio_Sent_Ip_axFastData[FLEXIO_INSTANCE_NO][ChannelId].TimerbufferIndx should not be used to allocate TimerbufferIndx. 4. Timeout max is currently 65535, This duration is too small to detect a serial msg. So it should equals to 2^16. For more details, please check the attached files. I update some line of code to capture a serial msg. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: Sent_TS_14 Observed behavior: NA Expected behavior: NA Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Check attached file.
ARTD-23826	Bug	[ICU][S32K3XX RTM 2.0.0] [S32DS]The build error with DMA function<*> Detailed description (how to reproduce it): When using channel with DM for signal measurement or timestamp mode, In the file Icu_DmaNotification generated in output, the function DMA does not have the name as following: !image-2022-02-23-17-09-18-405.png! !image-2022-02-23-19-07-48-711.png! Preconditions: Channel is enabled with DMA for signal measurement mode. Test Case ID (internal TC that caught the defect) optional: Icu_TC_FCT_0226 (Icu_TS_110), Icu_TC_WBT_0302 (Icu_TS_031) Observed behavior: [...] Expected behavior: [...] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: The DMA callback function is generated.
ARTD-23864	Bug	[BASE][S32CT] Code generation failed during RTD - LLCE integration<*> Detailed description (how to reproduce it): While creating a project with multiple drivers, including LLCE modules and Dio, the code generation was failed. Preconditions: Integrating Dio from RTD_3.0.0 and LLCE modules from LLCE_1.0.3 Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: The following error was shown: !image-2022-02-25-09-39-48-908.png! Expected behavior: The project can be generated without any error. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: A temporary solution is to add a requireScript in dio_codegenerator.js file. It is needed because "index" was somewhere initiated, and requireScript reimport index function to make sure that Dio can get the correct "index" !image-2022-02-25-09-42-58-349.png!

ID	Subtype	Headline and Description
ARTD-23868	Bug	[gpt] Update missing exclusive areas in BSWMD<*> Detailed description (how to reproduce it): Do a repo sync on bswmd_creator to sync with the manifest (make sure that you've checked out BLN_BSWMD_CREATOR_04.08.03) Compile the plugin passing parameter GENERATE_BSWMD_FILE=ON to the make command (`p s1 b` in ZTH) If the plugin was compiled successfully and there are no errors from bswmd_creator regarding missing or unmapped exclusive areas, then you can close your clone with "Fixed No Action Taken". Otherwise, proceed with the solutions given in the "Proposed solution" section. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Missing exclusive areas in <Module>_Bswmd.arxml Expected behavior: All exclusive areas are included in <Module>_Bswmd.arxml Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Potential Issue #1 Missing exclusive areas for ISRs Solution #1 The bswmd_creator script will automatically fetch ISRs from the source code as long as they're defined with ISR(...). Every ISR mentioned in the "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" files shall also be wrapped in ISR(...). For example: ADC_EXCLUSIVE_AREA_70 is used in function ISR(Ctu_Error_Isr) to protect the updates for CTU_IFR register Potential Issue #2 Missing exclusive areas for IPL functions which are not called by any HLD function Solution #2 # Have the EA mentioned in "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" only as used by the IPL function. For example: ADC_EXCLUSIVE_AREA_17 is used in function Adc_Sar_Ip_AbortConversion to protect the updates for ADC_MCR register # Add the IPL function in NonASR_ServiceID.xml Note: Do not use other workarounds like artificially mentioning in .dox that the IPL function is called by an HLD function which is included in NonASR_ServiceID.xml (even though, in reality, it's not)
ARTD-23884	Bug	[ETH] GMAC driver sets wrong value for Tx Queue Size<*> Detailed description (how to reproduce it): For example, configure egress FIFO with buffer size 512 and buffer count 16. This should give an MTL queue size of 16*512/256=32. The MTL_TxQn_Operation_Mode.TQS should be programmed to 31 (0x1F). Observed behavior: MTL_TxQn_Operation_Mode.TQS is programmed to 0 if queue size is 32. Additionally, when using above configuration and TQS=0, GMAC produces an underflow error for frames > 230 bytes. Expected behavior: MTL_TxQn_Operation_Mode.TQS is programmed to (queue size 1).
ARTD-23889	Bug	[S32K3][Crypto] ECVD file miss some field when it is generated from mex file<*> Detailed description (how to reproduce it): When generate file ECVD from mex file of HLD in tag CRYPTO_121, it will be missing field CryptoKeyElementRef in CryptoKeytypes due to gen fail when import ECVD file to EB Test Case ID (internal TC that caught the defect) optional: Crypto_TS_COT_007 Observed behavior: When import ECVD to EB , it report gen fail due to missing CryptoKeyElementRef Expected behavior: EVCD file have mapping with mex file when it gen from S32DS Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-23903	New Feature	[PORT] Redo the implementations for Virtual Wrapper for S32K3XX RTM 2.0.0<*> NewWorkDescription: There are 3 new requirements for Virtual Wrapper's implementations: CPR_RTD_00442.port: For each PortPin, the configured PDAC slot for its registers shall be specified using a configuration parameter named VirtWrapper PDAC implemented in the PortPin container. The default value of VirtWrapper PDAC shall be PDAC0 CPR_RTD_00657.port: The configured PDAC slot for Dio and Port registers shall be selectable per pin basis in the configurator if Virt Wrapper support is enabled. Rationale: Port and Dio mirrors should be configured even if RM is not available in project. Base address registers for Port and Dio registers depend on the previously configured virtual wrapper assignment. CPR_RTD_00658.port: The configured PDAC slot for Dio and Port registers shall be interrogated from the RM component per pin basis if Virt Wrapper support is enabled and if the RM component is available in the project. Requirement source: CPR_RTD_00442, CPR_RTD_00657, CPR_RTD_00658 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: First of all, create a new parameter in configurator as mentioned in CPR_RTD_00442 Then following the CPR_RTD_00657 and CPR_RTD_00658, the PDACs slot will not be gotten from partitions (multicore) Dio and Port will implement the Virtual Wrapper even if RM is available in the project or not.
ARTD-23904	New Feature	[DIO] Redo the implementations for Virtual Wrapper for S32K3XX RTM 2.0.0<*> NewWorkDescription: There are 3 new requirements for Virtual Wrapper's implementations: CPR_RTD_00442.port: For each PortPin, the configured PDAC slot for its registers shall be specified using a configuration parameter named VirtWrapper PDAC implemented in the PortPin container. The default value of VirtWrapper PDAC shall be PDAC0 CPR_RTD_00657.port: The configured PDAC slot for Dio and Port registers shall be selectable per pin basis in the configurator if Virt Wrapper support is enabled. Rationale: Port and Dio mirrors should be configured even if RM is not available in project. Base address registers for Port and Dio registers depend on the previously configured virtual wrapper assignment. CPR_RTD_00658.port: The configured PDAC slot for Dio and Port registers shall be interrogated from the RM component per pin basis if Virt Wrapper support is enabled and if the RM component is available in the project. Requirement source: CPR_RTD_00442, CPR_RTD_00657, CPR_RTD_00658 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: First of all, create a new parameter in configurator as mentioned in CPR_RTD_00442 Then following the CPR_RTD_00657 and CPR_RTD_00658, the PDACs slot will not be gotten from partitions (multicore) Dio and Port will implement the Virtual Wrapper even if RM is available in the project or not.
ARTD-23906	Bug	[WDG] Generated code by 3rd party tool is incorrect when /ActiveEcuC/Wdg is defined<*> Detailed description (how to reproduce it): Generated code by 3rd party tool is incorrect when /ActiveEcuC/Wdg is defined in the configuration file instead of /Wdg/Wdg. Preconditions: Generated code by 3rd party tool, /ActiveEcuC/Wdg is defined in the configuration file Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Generated code by 3rd party tool is incorrect when /ActiveEcuC/Wdg is defined in the configuration file instead of /Wdg/Wdg. Expected behavior: Generated code should be correct regardless the node definitions. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: There was a known issue from MCAL (e.g. MCAL-2875 in which: The autosar path Mod/ELEMENTS/Mod (where Mod is module name, for example Adc, Mcu, Resource etc.) must not be used in code generation templates (Mod_PBcfg.c, Mod_Cfg.c) to reference other nodes. The reason is that this path does not exist if there is used third party configuration tool. This leads to generation errors as node is not found. The solution would be replace the ./../../../Wdg/ELEMENTS/Wdg by: node:refs('ASPathDataOfSchema:/AUTOSAR/Wdg')

ID	Subtype	Headline and Description
ARTD-23911	Bug	[ICU][S32K3] CT reports an error when select a global bus as time base in ICU module<*> Detailed description (how to reproduce it): When the ICU channel selects a global bus as time base, there will be a error in CT. However, the Emios_Mcl_Ip driver was added and configured. Moreover, the configuration code can be generated normally. It was firstly reported in ARTD-12355, but it was closed and this issue has not been solved in RTD 1.0.0. Customer GLB recently reported it to AE. !image-2022-02-28-15-45-53-992.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-23915	New Feature	[adc] Adjust range of integer node in EB due to limitation of java<*> NewWorkDescription: Previously, we implement integer node has maximum range from [TPS_GST_00008]: 9223372036854775808 .. 18446744073709551615 but in latest release node of EB28, it state that: Deviating from the AUTOSAR traceable [TPS_GST_00008], the formula language in terpreter of EB tresos Studio supports only the signed 64-bit range for integer values, i. e. from 0x8000000000000000 (-9223372036854775808) to 0x7fffffffffffffff (9223372036854775807). The formula language parser of EB tresos Studio is implemented in Java. It uses the long primitive type for integer values and therefore can only support the restricted range. Requirement source: Please try to generate vsmd report using EB 28.2 if you got no error, please ignore this ticket. If you got some errors, you might see this warning in log prompt from EB on terminal (eg: ADC): This is a restriction of tresos Studio. The value is automatically restricted to 9223372036854775807. WARNING 22-03-08,11:28:58 (23016) The MAX attribute (describing the maximum allowed value for the parameter AdcPowerState with current value 18446744073709551615 defined in file D:\Git_rtd\tools\tresos_plugin_builder\make\..\..\..\output\eclipse\plugins\Adc_TS_T31D53M8I0R0\autosar\Adc_s32e27x_bga975.epd at line 4981) is greater than 64 bit signed integer. This is a restriction of tresos Studio. The value is automatically restricted to 9223372036854775807. {_}*Error EcucSws_1007: For Integer and Float Parameters the MIN values must be >= and the MAX values <= as in the StMD. (see example in VSMD report of ADC in attachment*{_}{*}{{*}} Proposed solution optional: To elimilate warning and error on vsmd report, we need to implement a fix to change the range of integer node adapt with EB example: Before* <v:var name="AdcChannelConvTime" type="INTEGER"> <a:da name="INVALID" type="Range"> <a:tst expr="<=18446744073709551615"/> <a:tst expr=">=0"/> </a:da> </v:var> Example: After fixed <v:var name="AdcChannelConvTime" type="INTEGER"> <a:da name="INVALID" type="Range"> <a:tst expr="<=9223372036854775807"/> <a:tst expr=">=0"/> </a:da> </v:var> The range of all integer nodes should be limit from 0x8000000000000000 (-9223372036854775808) to 0x7fffffffffffffff (9223372036854775807).

ID	Subtype	Headline and Description
ARTD-23927	New Feature	[i2c] Adjust range of integer node in EB due to limitation of java<*> NewWorkDescription: Previously, we implement integer node has maximum range from [TPS_GST_00008]: 9223372036854775808 .. 18446744073709551615 but in latest release node of EB28, it state that: Deviating from the AUTOSAR traceable [TPS_GST_00008], the formula language in terpreter of EB tresos Studio supports only the signed 64-bit range for integer values, i. e. from 0x8000000000000000 (-9223372036854775808) to 0x7fffffffffffffff (9223372036854775807). The formula language parser of EB tresos Studio is implemented in Java. It uses the long primitive type for integer values and therefore can only support the restricted range. Requirement source: Please try to generate vsmd report using EB 28.2 if you got no error, please ignore this ticket. If you got some errors, you might see this warning in log prompt from EB on terminal (eg: ADC): This is a restriction of tresos Studio. The value is automatically restricted to 9223372036854775807. WARNING 22-03-08,11:28:58 (23016) The MAX attribute (describing the maximum allowed value for the parameter AdcPowerState with current value 18446744073709551615 defined in file D:\Git_rtd\tools\tresos_plugin_builder\make\..\..\..\output \eclipse\plugins\Adc_TS_T31D53M8I0R0\autosar\Adc_s32e27x_bga975.epd at line 4981) is greater than 64 bit signed integer. This is a restriction of tresos Studio. The value is automatically restricted to 9223372036854775807. {_}*Error EcucSws_1007: For Integer and Float Parameters the MIN values must be >= and the MAX values <= as in the StMD. (see example in VSMD report of ADC in attachment*{_}{*}{{*}} Proposed solution optional: To elimilate warning and error on vsmd report, we need to implement a fix to change the range of integer node adapt with EB example: Before* <v:var name="AdcChannelConvTime" type="INTEGER"> <a:da name="INVALID" type="Range"> <a:tst expr="<=18446744073709551615"/> <a:tst expr=">=0"/> </a:da> </v:var> Example: After fixed <v:var name="AdcChannelConvTime" type="INTEGER"> <a:da name="INVALID" type="Range"> <a:tst expr="<=9223372036854775807"/> <a:tst expr=">=0"/> </a:da> </v:var> The range of all integer nodes should be limit from 0x8000000000000000 (-9223372036854775808) to 0x7fffffffffffffff (9223372036854775807).

ID	Subtype	Headline and Description
ARTD-23930	New Feature	[icu] Adjust range of integer node in EB due to limitation of java<*> NewWorkDescription: Previously, we implement integer node has maximum range from [TPS_GST_00008]: 9223372036854775808 .. 18446744073709551615 but in latest release node of EB28, it state that: Deviating from the AUTOSAR traceable [TPS_GST_00008], the formula language in terpreter of EB tresos Studio supports only the signed 64-bit range for integer values, i. e. from 0x8000000000000000 (-9223372036854775808) to 0x7fffffffffffffff (9223372036854775807). The formula language parser of EB tresos Studio is implemented in Java. It uses the long primitive type for integer values and therefore can only support the restricted range. Requirement source: Please try to generate vsmd report using EB 28.2 if you got no error, please ignore this ticket. If you got some errors, you might see this warning in log prompt from EB on terminal (eg: ADC): This is a restriction of tresos Studio. The value is automatically restricted to 9223372036854775807. WARNING 22-03-08,11:28:58 (23016) The MAX attribute (describing the maximum allowed value for the parameter AdcPowerState with current value 18446744073709551615 defined in file D:\Git_rtd\tools\tresos_plugin_builder\make\..\..\..\output \eclipse\plugins\Adc_TS_T31D53M8I0R0\autosar\Adc_s32e27x_bga975.epd at line 4981) is greater than 64 bit signed integer. This is a restriction of tresos Studio. The value is automatically restricted to 9223372036854775807. {_}*Error EcucSws_1007: For Integer and Float Parameters the MIN values must be >= and the MAX values <= as in the StMD. (see example in VSMD report of ADC in attachment*{_}{*}{{*}} Proposed solution optional: To elimilate warning and error on vsmd report, we need to implement a fix to change the range of integer node adapt with EB example: Before* <v:var name="AdcChannelConvTime" type="INTEGER"> <a:da name="INVALID" type="Range"> <a:tst expr="<=18446744073709551615"/> <a:tst expr=">=0"/> </a:da> </v:var> Example: After fixed <v:var name="AdcChannelConvTime" type="INTEGER"> <a:da name="INVALID" type="Range"> <a:tst expr="<=9223372036854775807"/> <a:tst expr=">=0"/> </a:da> </v:var> The range of all integer nodes should be limit from 0x8000000000000000 (-9223372036854775808) to 0x7fffffffffffffff (9223372036854775807).

ID	Subtype	Headline and Description
ARTD-23937	New Feature	[platform] Adjust range of integer node in EB due to limitation of java<*> NewWorkDescription: Previously, we implement integer node has maximum range from [TPS_GST_00008]: 9223372036854775808 .. 18446744073709551615 but in latest release node of EB28, it state that: Deviating from the AUTOSAR traceable [TPS_GST_00008], the formula language in terpreter of EB tresos Studio supports only the signed 64-bit range for integer values, i. e. from 0x8000000000000000 (-9223372036854775808) to 0x7fffffffffffffff (9223372036854775807). The formula language parser of EB tresos Studio is implemented in Java. It uses the long primitive type for integer values and therefore can only support the restricted range. Requirement source: Please try to generate vsmd report using EB 28.2 if you got no error, please ignore this ticket. If you got some errors, you might see this warning in log prompt from EB on terminal (eg: ADC): This is a restriction of tresos Studio. The value is automatically restricted to 9223372036854775807. WARNING 22-03-08,11:28:58 (23016) The MAX attribute (describing the maximum allowed value for the parameter AdcPowerState with current value 18446744073709551615 defined in file D:\Git_rtd\tools\tresos_plugin_builder\make\..\..\..\output \eclipse\plugins\Adc_TS_T31D53M8I0R0\autosar\Adc_s32e27x_bga975.epd at line 4981) is greater than 64 bit signed integer. This is a restriction of tresos Studio. The value is automatically restricted to 9223372036854775807. {_}*Error EcucSws_1007: For Integer and Float Parameters the MIN values must be >= and the MAX values <= as in the StMD. (see example in VSMD report of ADC in attachment*{_}{*}{{*}} Proposed solution optional: To elimilate warning and error on vsmd report, we need to implement a fix to change the range of integer node adapt with EB example: Before* <v:var name="AdcChannelConvTime" type="INTEGER"> <a:da name="INVALID" type="Range"> <a:tst expr="<=18446744073709551615"/> <a:tst expr=">=0"/> </a:da> </v:var> Example: After fixed <v:var name="AdcChannelConvTime" type="INTEGER"> <a:da name="INVALID" type="Range"> <a:tst expr="<=9223372036854775807"/> <a:tst expr=">=0"/> </a:da> </v:var> The range of all integer nodes should be limit from 0x8000000000000000 (-9223372036854775808) to 0x7fffffffffffffff (9223372036854775807).

ID	Subtype	Headline and Description
ARTD-23940	New Feature	[pwm] Adjust range of integer node in EB due to limitation of java<*> NewWorkDescription: Previously, we implement integer node has maximum range from [TPS_GST_00008]: 9223372036854775808 .. 18446744073709551615 but in latest release node of EB28, it state that: Deviating from the AUTOSAR traceable [TPS_GST_00008], the formula language in terpreter of EB tresos Studio supports only the signed 64-bit range for integer values, i. e. from 0x8000000000000000 (-9223372036854775808) to 0x7fffffffffffffff (9223372036854775807). The formula language parser of EB tresos Studio is implemented in Java. It uses the long primitive type for integer values and therefore can only support the restricted range. Requirement source: Please try to generate vsmd report using EB 28.2 if you got no error, please ignore this ticket. If you got some errors, you might see this warning in log prompt from EB on terminal (eg: ADC): This is a restriction of tresos Studio. The value is automatically restricted to 9223372036854775807. WARNING 22-03-08,11:28:58 (23016) The MAX attribute (describing the maximum allowed value for the parameter AdcPowerState with current value 18446744073709551615 defined in file D:\Git_rtd\tools\tresos_plugin_builder\make\..\..\..\output \eclipse\plugins\Adc_TS_T31D53M8I0R0\autosar\Adc_s32e27x_bga975.epd at line 4981) is greater than 64 bit signed integer. This is a restriction of tresos Studio. The value is automatically restricted to 9223372036854775807. {_}*Error EcucSws_1007: For Integer and Float Parameters the MIN values must be >= and the MAX values <= as in the StMD. (see example in VSMD report of ADC in attachment*{_}{*}{{*}} Proposed solution optional: To elimilate warning and error on vsmd report, we need to implement a fix to change the range of integer node adapt with EB example: Before* <v:var name="AdcChannelConvTime" type="INTEGER"> <a:da name="INVALID" type="Range"> <a:tst expr="<=18446744073709551615"/> <a:tst expr=">=0"/> </a:da> </v:var> Example: After fixed <v:var name="AdcChannelConvTime" type="INTEGER"> <a:da name="INVALID" type="Range"> <a:tst expr="<=9223372036854775807"/> <a:tst expr=">=0"/> </a:da> </v:var> The range of all integer nodes should be limit from 0x8000000000000000 (-9223372036854775808) to 0x7fffffffffffffff (9223372036854775807).

ID	Subtype	Headline and Description
ARTD-23948	New Feature	[uart] Adjust range of integer node in EB due to limitation of java<*> NewWorkDescription: Previously, we implement integer node has maximum range from [TPS_GST_00008]: 9223372036854775808 .. 18446744073709551615 but in latest release node of EB28, it state that: Deviating from the AUTOSAR traceable [TPS_GST_00008], the formula language in terpreter of EB tresos Studio supports only the signed 64-bit range for integer values, i. e. from 0x8000000000000000 (-9223372036854775808) to 0x7fffffffffffffff (9223372036854775807). The formula language parser of EB tresos Studio is implemented in Java. It uses the long primitive type for integer values and therefore can only support the restricted range. Requirement source: Please try to generate vsmd report using EB 28.2 if you got no error, please ignore this ticket. If you got some errors, you might see this warning in log prompt from EB on terminal (eg: ADC): This is a restriction of tresos Studio. The value is automatically restricted to 9223372036854775807. WARNING 22-03-08,11:28:58 (23016) The MAX attribute (describing the maximum allowed value for the parameter AdcPowerState with current value 18446744073709551615 defined in file D:\Git_rtd\tools\tresos_plugin_builder\make\..\..\..\output\eclipse\plugins\Adc_TS_T31D53M8I0R0\autosar\Adc_s32e27x_bga975.epd at line 4981) is greater than 64 bit signed integer. This is a restriction of tresos Studio. The value is automatically restricted to 9223372036854775807. {_}*Error EcucSws_1007: For Integer and Float Parameters the MIN values must be >= and the MAX values <= as in the StMD. (see example in VSMD report of ADC in attachment*{_}{*}{{*}} Proposed solution optional: To elimilate warning and error on vsmd report, we need to implement a fix to change the range of integer node adapt with EB example: Before* <v:var name="AdcChannelConvTime" type="INTEGER"> <a:da name="INVALID" type="Range"> <a:tst expr="<=18446744073709551615"/> <a:tst expr=">=0"/> </a:da> </v:var> Example: After fixed <v:var name="AdcChannelConvTime" type="INTEGER"> <a:da name="INVALID" type="Range"> <a:tst expr="<=9223372036854775807"/> <a:tst expr=">=0"/> </a:da> </v:var> The range of all integer nodes should be limit from 0x8000000000000000 (-9223372036854775808) to 0x7fffffffffffffff (9223372036854775807).
ARTD-23956	Bug	[ICU] The function description did not map with autosar spec<*> Detailed description (how to reproduce it): [The Icu_GetTimestampIndex function description did not map with ICU autosar spec. !image-2022-03-01-09-28-19-598.png|thumbnail! Autosar Spec: !image-2022-03-01-09-38-07-824.png|thumbnail! The description is cloned from Icu_GetTimeElapsed. Unfortunately, my application did not work when I used and read the Icu_GetTimestampIndex API. !image-2022-03-01-09-39-00-397.png|thumbnail! Please double-check with other functions. Second Issue: I configure the emios channel. When I select the global bus, the EB require to link EmiosBus reference from MCL module. However, the description did not mention anything for customer by setting emios bus in MCL. That's an issue. !screenshot-1.png|thumbnail!] Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [Wrong function description] Expected behavior: [Correct the description] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-23962	Bug	[ICU][S32K3XX RTM 2.0.0] The build fail error with ip Emios file in S32DS<*> Detailed description (how to reproduce it): The file Emios_Icu_Ip_SA_VS_0_PBcfg.c generated in S32DS is empty: !image-2022-03-01-15-11-38-159.png! !image-2022-03-01-16-22-36-039.png! Please check above code section in file Emios config to find the issue. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: N/A Expected behavior: N/A Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-23975	New Feature	[adc] [S32CT] Update code generation to work in JS strict mode<*> NewWorkDescription: Note: Only Peripherals Tool's components are affected{color}*. There has been an update to the System module: System scripts now run in strict mode and contain include guards to protect against multiple inclusion System utilities / functions have been made read-only Code templates are now evaluated in strict mode so that developers can be aware of overwriting existing variables or using undeclared variables*. Requirement source: Consequence of https://jira.sw.nxp.com/browse/ARTD-23864 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: What you have to do: ## Open S32DS's logging file (swtools.log) or launch the program with console logging activated (e.g. run ".\s32ds.exe consoleLog in CMD/PowerShell) ## Create a new project and instantiate your high-level / low-level component. ## Fix the encountered errors related to your component. Most of them will be along the lines of "ReferenceError: <variable_name> is not defined" or "TypeError: <variable_name> is not a writable property of [object global]"_. Both can be resolved by simply defining the offending variable using "var". ## Remove inclusions of "refsSolver.js" in your code templates or code generator scripts. If there's an API you need from that file which is not provided in codegeneratorUtils.js, please let me know.
ARTD-23977	New Feature	[can] [S32CT] Update code generation to work in JS strict mode<*> NewWorkDescription: Note: Only Peripherals Tool's components are affected{color}*. There has been an update to the System module: System scripts now run in strict mode and contain include guards to protect against multiple inclusion System utilities / functions have been made read-only Code templates are now evaluated in strict mode so that developers can be aware of overwriting existing variables or using undeclared variables*. Requirement source: Consequence of https://jira.sw.nxp.com/browse/ARTD-23864 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: What you have to do: ## Open S32DS's logging file (swtools.log) or launch the program with console logging activated (e.g. run ".\s32ds.exe consoleLog in CMD/PowerShell) ## Create a new project and instantiate your high-level / low-level component. ## Fix the encountered errors related to your component. Most of them will be along the lines of "ReferenceError: <variable_name> is not defined" or "TypeError: <variable_name> is not a writable property of [object global]"_. Both can be resolved by simply defining the offending variable using "var". ## Remove inclusions of "refsSolver.js" in your code templates or code generator scripts. If there's an API you need from that file which is not provided in codegeneratorUtils.js, please let me know.

ID	Subtype	Headline and Description
ARTD-23983	New Feature	[dio] [S32CT] Update code generation to work in JS strict mode<*> NewWorkDescription: Note: Only Peripherals Tool's components are affected{color}*. There has been an update to the System module: System scripts now run in strict mode and contain include guards to protect against multiple inclusion System utilities / functions have been made read-only Code templates are now evaluated in strict mode so that developers can be aware of overwriting existing variables or using undeclared variables*. Requirement source: Consequence of https://jira.sw.nxp.com/browse/ARTD-23864 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: What you have to do: ## Open S32DS's logging file (swtools.log) or launch the program with console logging activated (e.g. run ".\s32ds.exe consoleLog in CMD/PowerShell) ## Create a new project and instantiate your high-level / low-level component. ## Fix the encountered errors related to your component. Most of them will be along the lines of "ReferenceError: <variable_name> is not defined" or "TypeError: <variable_name> is not a writable property of [object global]"_. Both can be resolved by simply defining the offending variable using "var". ## Remove inclusions of "refsSolver.js" in your code templates or code generator scripts. If there's an API you need from that file which is not provided in codegeneratorUtils.js, please let me know.
ARTD-23994	New Feature	[i2c] [S32CT] Update code generation to work in JS strict mode<*> NewWorkDescription: Note: Only Peripherals Tool's components are affected{color}*. There has been an update to the System module: System scripts now run in strict mode and contain include guards to protect against multiple inclusion System utilities / functions have been made read-only Code templates are now evaluated in strict mode so that developers can be aware of overwriting existing variables or using undeclared variables*. Requirement source: Consequence of https://jira.sw.nxp.com/browse/ARTD-23864 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: What you have to do: ## Open S32DS's logging file (swtools.log) or launch the program with console logging activated (e.g. run ".\s32ds.exe consoleLog in CMD/PowerShell) ## Create a new project and instantiate your high-level / low-level component. ## Fix the encountered errors related to your component. Most of them will be along the lines of "ReferenceError: <variable_name> is not defined" or "TypeError: <variable_name> is not a writable property of [object global]"_. Both can be resolved by simply defining the offending variable using "var". ## Remove inclusions of "refsSolver.js" in your code templates or code generator scripts. If there's an API you need from that file which is not provided in codegeneratorUtils.js, please let me know.
ARTD-24003	New Feature	[platform] [S32CT] Update code generation to work in JS strict mode<*> NewWorkDescription: Note: Only Peripherals Tool's components are affected{color}*. There has been an update to the System module: System scripts now run in strict mode and contain include guards to protect against multiple inclusion System utilities / functions have been made read-only Code templates are now evaluated in strict mode so that developers can be aware of overwriting existing variables or using undeclared variables*. Requirement source: Consequence of https://jira.sw.nxp.com/browse/ARTD-23864 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: What you have to do: ## Open S32DS's logging file (swtools.log) or launch the program with console logging activated (e.g. run ".\s32ds.exe consoleLog in CMD/PowerShell) ## Create a new project and instantiate your high-level / low-level component. ## Fix the encountered errors related to your component. Most of them will be along the lines of "ReferenceError: <variable_name> is not defined" or "TypeError: <variable_name> is not a writable property of [object global]"_. Both can be resolved by simply defining the offending variable using "var". ## Remove inclusions of "refsSolver.js" in your code templates or code generator scripts. If there's an API you need from that file which is not provided in codegeneratorUtils.js, please let me know.

ID	Subtype	Headline and Description
ARTD-24005	New Feature	[port] [S32CT] Update code generation to work in JS strict mode<*> NewWorkDescription: Note: Only Peripherals Tool's components are affected{color}*. There has been an update to the System module: System scripts now run in strict mode and contain include guards to protect against multiple inclusion System utilities / functions have been made read-only Code templates are now evaluated in strict mode so that developers can be aware of overwriting existing variables or using undeclared variables*. Requirement source: Consequence of https://jira.sw.nxp.com/browse/ARTD-23864 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: What you have to do: ## Open S32DS's logging file (swtools.log) or launch the program with console logging activated (e.g. run ".\s32ds.exe consoleLog in CMD/PowerShell) ## Create a new project and instantiate your high-level / low-level component. ## Fix the encountered errors related to your component. Most of them will be along the lines of "ReferenceError: <variable_name> is not defined" or "TypeError: <variable_name> is not a writable property of [object global]"_. Both can be resolved by simply defining the offending variable using "var". ## Remove inclusions of "refsSolver.js" in your code templates or code generator scripts. If there's an API you need from that file which is not provided in codegeneratorUtils.js, please let me know.
ARTD-24006	New Feature	[pwm] [S32CT] Update code generation to work in JS strict mode<*> NewWorkDescription: Note: Only Peripherals Tool's components are affected{color}*. There has been an update to the System module: System scripts now run in strict mode and contain include guards to protect against multiple inclusion System utilities / functions have been made read-only Code templates are now evaluated in strict mode so that developers can be aware of overwriting existing variables or using undeclared variables*. Requirement source: Consequence of https://jira.sw.nxp.com/browse/ARTD-23864 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: What you have to do: ## Open S32DS's logging file (swtools.log) or launch the program with console logging activated (e.g. run ".\s32ds.exe consoleLog in CMD/PowerShell) ## Create a new project and instantiate your high-level / low-level component. ## Fix the encountered errors related to your component. Most of them will be along the lines of "ReferenceError: <variable_name> is not defined" or "TypeError: <variable_name> is not a writable property of [object global]"_. Both can be resolved by simply defining the offending variable using "var". ## Remove inclusions of "refsSolver.js" in your code templates or code generator scripts. If there's an API you need from that file which is not provided in codegeneratorUtils.js, please let me know.
ARTD-24008	New Feature	[rm] [S32CT] Update code generation to work in JS strict mode<*> NewWorkDescription: Note: Only Peripherals Tool's components are affected{color}*. There has been an update to the System module: System scripts now run in strict mode and contain include guards to protect against multiple inclusion System utilities / functions have been made read-only Code templates are now evaluated in strict mode so that developers can be aware of overwriting existing variables or using undeclared variables*. Requirement source: Consequence of https://jira.sw.nxp.com/browse/ARTD-23864 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: What you have to do: ## Open S32DS's logging file (swtools.log) or launch the program with console logging activated (e.g. run ".\s32ds.exe consoleLog in CMD/PowerShell) ## Create a new project and instantiate your high-level / low-level component. ## Fix the encountered errors related to your component. Most of them will be along the lines of "ReferenceError: <variable_name> is not defined" or "TypeError: <variable_name> is not a writable property of [object global]"_. Both can be resolved by simply defining the offending variable using "var". ## Remove inclusions of "refsSolver.js" in your code templates or code generator scripts. If there's an API you need from that file which is not provided in codegeneratorUtils.js, please let me know.

ID	Subtype	Headline and Description
ARTD-24012	New Feature	[spi] [S32CT] Update code generation to work in JS strict mode<*> NewWorkDescription: Note: Only Peripherals Tool's components are affected{color}*. There has been an update to the System module: System scripts now run in strict mode and contain include guards to protect against multiple inclusion System utilities / functions have been made read-only Code templates are now evaluated in strict mode so that developers can be aware of overwriting existing variables or using undeclared variables*. Requirement source: Consequence of https://jira.sw.nxp.com/browse/ARTD-23864 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: What you have to do: ## Open S32DS's logging file (swtools.log) or launch the program with console logging activated (e.g. run ".\s32ds.exe consoleLog in CMD/PowerShell) ## Create a new project and instantiate your high-level / low-level component. ## Fix the encountered errors related to your component. Most of them will be along the lines of "ReferenceError: <variable_name> is not defined" or "TypeError: <variable_name> is not a writable property of [object global]"_. Both can be resolved by simply defining the offending variable using "var". ## Remove inclusions of "refsSolver.js" in your code templates or code generator scripts. If there's an API you need from that file which is not provided in codegeneratorUtils.js, please let me know.
ARTD-24014	New Feature	[uart] [S32CT] Update code generation to work in JS strict mode<*> NewWorkDescription: Note: Only Peripherals Tool's components are affected{color}*. There has been an update to the System module: System scripts now run in strict mode and contain include guards to protect against multiple inclusion System utilities / functions have been made read-only Code templates are now evaluated in strict mode so that developers can be aware of overwriting existing variables or using undeclared variables*. Requirement source: Consequence of https://jira.sw.nxp.com/browse/ARTD-23864 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: What you have to do: ## Open S32DS's logging file (swtools.log) or launch the program with console logging activated (e.g. run ".\s32ds.exe consoleLog in CMD/PowerShell) ## Create a new project and instantiate your high-level / low-level component. ## Fix the encountered errors related to your component. Most of them will be along the lines of "ReferenceError: <variable_name> is not defined" or "TypeError: <variable_name> is not a writable property of [object global]"_. Both can be resolved by simply defining the offending variable using "var". ## Remove inclusions of "refsSolver.js" in your code templates or code generator scripts. If there's an API you need from that file which is not provided in codegeneratorUtils.js, please let me know.
ARTD-24015	New Feature	[wdg] [S32CT] Update code generation to work in JS strict mode<*> NewWorkDescription: Note: Only Peripherals Tool's components are affected{color}*. There has been an update to the System module: System scripts now run in strict mode and contain include guards to protect against multiple inclusion System utilities / functions have been made read-only Code templates are now evaluated in strict mode so that developers can be aware of overwriting existing variables or using undeclared variables*. Requirement source: Consequence of https://jira.sw.nxp.com/browse/ARTD-23864 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: What you have to do: ## Open S32DS's logging file (swtools.log) or launch the program with console logging activated (e.g. run ".\s32ds.exe consoleLog in CMD/PowerShell) ## Create a new project and instantiate your high-level / low-level component. ## Fix the encountered errors related to your component. Most of them will be along the lines of "ReferenceError: <variable_name> is not defined" or "TypeError: <variable_name> is not a writable property of [object global]"_. Both can be resolved by simply defining the offending variable using "var". ## Remove inclusions of "refsSolver.js" in your code templates or code generator scripts. If there's an API you need from that file which is not provided in codegeneratorUtils.js, please let me know.
ARTD-24018	New Feature	[DIO] Change the define names to not contain derivatives name<*> NewWorkDescription: [https://bitbucket.sw.nxp.com/projects/ARTD/repos/port/pull-requests/410/overview?commentId=1104467] [Radu-Andrei Brasoveanu|https://bitbucket.sw.nxp.com/users/nxa19269] i would advise in creating a follow up ticket for entire code and changing the define names to not contain derivatives name. more suitable will be to use something like: FEATURE_PORT_CI_PORT_IP_PCR_MUXING}} Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Change the define names to not contain derivatives name.

ID	Subtype	Headline and Description
ARTD-24022	Bug	[S32K3 2.0.0] Crypto: Include incorrect file "S32K342_MUB.h" on the file Hse_Ip_Cfg.h ,,"Detailed description (how to reproduce it): Build fail test with derivative S32K342 because on the Base header file don't have contain S32K342_MUB.h, it name correct is S32K342_MU.h Preconditions: Build fail test with derivative S32K342 Test Case ID (internal TC that caught the defect) optional: All test build fail Observed behavior: all test build fail with error cannot open source file ""S32K342_MUB.h"" Expected behavior: All test can build success with derivative S32K342 Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Change include ""S32K342_MUB.h"" to ""S32K342_MU.h""
ARTD-24024	Bug	[S32K3 2.0.0][SENT] FXIO_ISR_PROCESS_TIMER_CTRLx shoud be defined in case SentFastNotification<*> Detailed description (how to reproduce it): Since function Flexio_Sent_Ip_GetFastMsgData used interrupt to collect timer value, function Flexio_Sent_Ip_IRQTimerHandler need to declared. So FXIO_ISR_PROCESS_TIMER_CTRL need to define to declare Flexio_Sent_Ip_IRQTimerHandler Preconditions: Using Flexio_Sent_Ip_GetFastMsgData Test Case ID (internal TC that caught the defect) optional: TS_10 Observed behavior: NA Expected behavior: NA Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: update Flexio_Sent_Ip_Cfg.h [!IF "SentProcessing = 'POLLING'"!] [!LOOP "SentChannelConfig/*"!] [!IF "((node:exists(SentFastNotification) and (SentFastNotification != 'NULL_PTR')) or (node:exists(SentSlowNotification) and (SentSlowNotification != 'NULL_PTR')))"!] [!VAR "ChnlPollingFlag" = "'true'"!] [!BREAK!] [!ENDIF!] [!ENDLOOP!] [!IF "$ChnlPollingFlag = 'true'"!] [!CODE!]#define FXIO_ISR_PROCESS_TIMER_CTRL[!"text:split((node:ref(SentHwControllerRef)/FlexioMclInstances),'_')[2]"!][!CR!][!ENDCODE!] [!ENDIF!] [!ENDIF!]
ARTD-24031	Bug	[MCU] 'STANDBY' can not let S32K3 MCU really enter standby mode<*> Detailed description (how to reproduce it): If we select STANDBY in MCU power component, MCU can not enter standby mode after calling MCU_Set_Mode(STANDBY). If we select SOC_STANDBY in MCU power component, MCU can enter standby mode after calling MCU_Set_Mode(SOC_STANDBY). Many customers have met the issue and I have tested it. If we select STANDBY in MCU power component, MCU can not really enter standby mode after calling MCU_Set_Mode(STANDBY). However, customers hope we can provide MCAL level code to config fast standby exit address. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-24053	New Feature	[icu][S32CT] Update code generation to work in JS strict mode<*> NewWorkDescription: Note: Only Peripherals Tool's components are affected{color}*. There has been an update to the System module: System scripts now run in strict mode and contain include guards to protect against multiple inclusion System utilities / functions have been made read-only Code templates are now evaluated in strict mode so that developers can be aware of overwriting existing variables or using undeclared variables*. Requirement source: Consequence of https://jira.sw.nxp.com/browse/ARTD-23864 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: What you have to do: ## Open S32DS's logging file (swtools.log) or launch the program with console logging activated (e.g. run ".\s32ds.exe consoleLog in CMD/PowerShell) ## Create a new project and instantiate your high-level / low-level component. ## Fix the encountered errors related to your component. Most of them will be along the lines of "ReferenceError: <variable_name> is not defined" or "TypeError: <variable_name> is not a writable property of [object global]"_. Both can be resolved by simply defining the offending variable using "var". ## Remove inclusions of "refsSolver.js" in your code templates or code generator scripts. If there's an API you need from that file which is not provided in codegeneratorUtils.js, please let me know.
ARTD-24054	Bug	[ICU] There are some errors in S32DS with HLD and IP layer<*> Detailed description (how to reproduce it): The file Icu_Cfg.h is generated is empty for high layer : !image-2022-03-03-08-45-26-442.png! In S32DS for IP layer, this error log appears: !image-2022-03-03-09-09-15-466.png! In the file Siul2_Icu_Ip_Cfg.h and Wkpu_Ip_Defines.h, the code is empty, please check the file Siul2_Icu_Ip.mex and Wkpu_Ip.mex attached : !image-2022-03-04-08-47-40-530.png! !image-2022-03-04-08-53-12-651.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: Icu_TC_FCT_0211 Observed behavior: N/A Expected behavior: N/A Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-24080	Bug	[CRYPTO] No mechanism is present to clear the receive register when request timeout occurs<*> Detailed description (how to reproduce it): Set a low request timeout value, smaller than the time it takes HSE FW to process the request, and send the request. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: The analysis on the driver code revealed that if the timeout is reached the channel will be released from the Crypto driver (IP) point of view but the from the hardware point of view the channel is not fully free until the RR register is read. The RR register can be read after the HSE firmware has finished the service and provided an response in RR. The channel on which the timeout has occurred can not be allocated again even if the firmware has finalized the request. Expected behavior: The channel is freed after the firmware has finished the processing so during the channel allocation request it can be allocated for requests. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: To avoid this situation the RR register can be read during the channel allocation in order to unblock the channels that satisfy the following points: # The Crypto driver has the channel marked as free # FSR bit for the channel is clear # TSR is set
ARTD-24105	New Feature	[CRYPTO] Fix compiler warnings<*> NewWorkDescription: Fix the compiler warnings present in the attached excels. ITG generated(for K3):[^RTD_CRYPTO_Compiler_Warnings (11) (1).xlsx] Develop generated(for G2):[^AUTOSAR_MCAL_CRYPTO_Compiler_Warnings.xlsx] Requirement source: Release Criteria (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Analyze and fix the issues found.

ID	Subtype	Headline and Description
ARTD-24092	Bug	[S32K3XX][s32k3_300] Project can't generate config on S32CT<*> Detailed description (how to reproduce it): Creating new project with platform component on s32ds, Add some config and update code. The project can't generate config Preconditions: PVT_S32K3XX_ARTD_22061_003, Test Case ID (internal TC that caught the defect) optional: Platform_TS_CT_001 Observed behavior: !image-2022-03-04-11-55-59-838.png! Expected behavior: Project generate success. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: add var before the variable !image-2022-03-04-12-01-01-620.png!
ARTD-24095	Bug	[PWM] Short-name of some nodes in ECVD file on S32DS are blank<*> Detailed description (how to reproduce it): IPL: Difference when generating between mex file and ecvd file. Some of the container's short names are not generated when generating with mex file but it is generated when generating with ecvd file: <SHORT-NAME>EmiosChIrqCallback</SHORT-NAME> <SHORT-NAME>PwmGeneral</SHORT-NAME> HLD: In the evcd file there is no node PwmChannel Class. When generating the source file, it will take the default value of the node PwmChannelClass. it causes a difference between the source file generate. Please compare folder new_configuration and original_configuration in attach file. Preconditions: Compare output when generating with mex file and ecvd file Test Case ID (internal TC that caught the defect) optional: Ip_Emios_TS_ECPD_001 Observed behavior: N/A Expected behavior: The output generated must be the same Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-24117	Bug	[S32K3 2.0.0] Crypto:Fix compiler warnings<*> Detailed description (how to reproduce it): There are some compiler warnings existed in the report on attached file below. Preconditions: Build test with TEST_PARAMS=@LoadTo=flash Tag test":PVT_TEST_CRYPTO_S32K3_RTM_200_V18 Tag Dev VT_CRYPTO_K3_200_HF_V01 Test Case ID (internal TC that caught the defect) optional: Crypto_TS_005 Observed behavior: There are some compiler warning in the report. Expected behavior: There is no compiler warning in the report. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-24118	Bug	[S32K3 2.0.0] FLS: fix version checking<*> Detailed description (how to reproduce it): FLS have some file version checking incorrect Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: check report in [http://kara.ea.freescale.net/0/project/custom_file_verchecking/details] need fix all validation Expected behavior: FLS version checking correct Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-24135	Bug	[CRYPTO] Crypto_CancelJob can never report timeout runtime error<*> Detailed description (how to reproduce it): Try to make timeout runtime error for Crypto_CancelJob and Crypto_MainFunction. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: Crypto_CancelJob and Crypto_MainFunction can never report timeout runtime error. Expected behavior: Crypto_CancelJob and Crypto_MainFunction can report timeout runtime error. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update the low level code to report timeout error to HLD layer (detail on the attached email)
ARTD-24152	Bug	[S32K3][Platform] Update linkers to ensure that .acfls_code_ram section is aligned with cache line<*> Detailed description (how to reproduce it): .acfls_code_ram is not allocated to cacheline-aligned address, so Fls driver cannot work properly Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Fls_TC_FCT_4001 Observed behavior: .acfls_code_ram section is not fully synchronized with cache after calling Fls_LoadAc and Cache_Ip_CleanByAddr Expected behavior: that section must be fully synchronized Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) please see below figures Proposed solution optional: .acfls_code_ram must be aligned with cache line
ARTD-24176	Bug	[I3c] Async transfer method doesn't wait for MCTRLDONE after Stop is emitted<*> Detailed description (how to reproduce it): Build any dev tests with Async transfers. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: Ascyn transfer method doesn't wait for MCTRLDONE after STOP or Force Exit is emitted. Expected behavior: Ascyn transfer method waits for MCTRLDONE after STOP or Force Exit is emitted. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: wait for MCTRLDONE using Control Done interrupt for I2c legacy transfers, remove delay added in Complete/End Transfer handlers for I2c Bus type, when STOP is emitted, MCONFIG[ODSTOP] must be 1.
ARTD-24262	Bug	[platform][s32k3_200] compiler warning<*> Detailed description (how to reproduce it): Compiler warning detect with K3xx derivative. Preconditions: PVT_S32K3XX_ARTD_22061_004 Test Case ID (internal TC that caught the defect) optional: Platform_TS_001 Observed behavior: Excel attachments. Expected behavior: Driver no warning, error Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-24263	New Feature	[S32K3 2.0.0] FLS: improve calculate value for "Fls Access Code" ,,"NewWorkDescription: updated calucate value for ""Fls Access Code"" update M4 macro for Fls Access Code less flexible so that sould get FlsAcErase, FlsAcWrite value from Resource Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-24283	New Feature	[BASE] Add support for S32K322 and S32K341 derivative<*> NewWorkDescription: Add support for S32K322 and S32K341 derivative Requirement source: RM rev 3 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional:
ARTD-24297	Bug	[I3C] Dma master/slave node is not disabled corresponding to I3cMasterSlaveMode<*> Detailed description (how to reproduce it): [I3C] Dma master/slave node is not disabled corresponding to I3cMasterSlaveMode I3cDmaFeature= true I3cMasterSlaveMode=Slave I3cMasterTransferType=DMA I3cMasterDmaTxChannel and I3cMasterDmaRxChannel are editable Same issue when I3cMasterSlaveMode=Master for I3cSlaveDmaTxChannel and I3cSlaveDmaRxChannel !image-2022-03-09-17-54-38-372.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: I3c_TC_FCT_1000 Observed behavior: [...] Expected behavior: The I3cMasterDmaTxChannel and I3cMasterDmaRxChannel should be editable if I3cMasterSlaveMode != 'SLAVE' and {color} {color:#ce9178}node:value(../I3cMasterTransferType) = 'DMA' Similar for I3cSlaveDmaTxChannel and I3cSlaveDmaRxChannel nodes Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-24300	Bug	“Input Inversion Select” in pin config tool<*> “Input Inversion Select” item in routing details in pin config tool should be changed to “Output Inversion Select”. I confirmed this on my board. INV bit in MCSR register does not affect the input. Regardless of INV bit, input register GPDI always shows the same logic level as connected to a pin. If a pin is configured as output, level of a pin can be inverted by INV. But also in this case, GPDI still shows the real level of a pin. !invert.jpg!
ARTD-24303	Bug	[icu] [S32K3XX 2.0.0] Fix all violations (HIS + MISRA + VSMD reports)<*> Detailed description (how to reproduce it): Create HIS MISRA VSMD reports Fix all violations for HIS MISRA VSMD reports Please see the attached file to know more details https://bamboo3.sw.nxp.com/artifact/ARTD-CIICU/BUILDCOV/build-480/MISRA_HIS-XLSX-Reports,-Compiler-Warnings,-Code-Exposure-and-Violations-logs/coverity_artifacts/S32K3XX_4.4_BLN_RTD_4.4_S32K3XX_2.0.0/ *Reference: SOW: https://nxp1.sharepoint.com/sites/Zebra/_layouts/15/Doc.aspx?sourcedoc= %7BD1DC93AE-F154-48B3-8D46-A8F7B0725503%7D&file=S32K3%20RTD%20ASR%204 .4%202.0.0%20SOW.docx&action=default&mobileredirect=true&cid=e08b347a-ad8c-495e-bed0-64fb8c121547 MISRA Deviation List: [https://bitbucket.sw.nxp.com/projects/ASPA/repos/real_time_drivers/browse/Generic/SW%20Development/RTD%20MISRA%20Deviations.xlsx] [https://confluence.sw.nxp.com/pages/viewpage.action?pageId=133734230] RTD Quality Criteria: [https://bitbucket.sw.nxp.com/projects/ASPA/repos/real_time_drivers/browse/Generic/Quality%20Assurance/RTD%20AASWS%20Gate%20and%20Release%20Criteria.xlsx] VSMD report: 0 warning, 0 error for RTM release MISRA report: 0 unjustified MISRA violations HIS report: !image-2021-08-30-12-26-52-249.png! Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: NA All violations fix and follow RTD Quality Criteria Proposed solution optional: Fix all MISRA, HIS, VSMD violations

ID	Subtype	Headline and Description
ARTD-24321	New Feature	[S32K3XX] Add support for S32K322 and S32K341<*> NewWorkDescription: Add support for S32K322 and S32K341 Requirement source: RM rev 3 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]
ARTD-24371	New Feature	[spi] [K3 2.0.0] Support new derivatives<*> [K3 2.0.0] Support new derivatives: S32K341: S32K341_100MQFP, S32K341_172MQFP S32K322: S32K322_100MQFP, S32K322_172MQFP Reference docs: Reference Manual |S32K3xx Reference Manual, Rev. 3, 10/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3Z4S2lrZDFFbTJnQWI0QlctTnpZTkdCNW9sQ3A2UF9aOUdKYnc%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FArchive%2FS32K3xx%5FRM%5FRev3%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FArchive] Datasheet |S32K3xx Data Sheet, Rev. 3 — 10/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3Z4S2lrZDFFbTJnQWI0QlctTnpZTkdCNW9sQ3A2UF9aOUdKYnc%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FArchive%2FS32K3xx%5FDS%5FRev3%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FArchive]
ARTD-24372	New Feature	[sent] [K3 2.0.0] Support new derivatives<*> [K3 2.0.0] Support new derivatives: S32K341: S32K341_100MQFP, S32K341_172MQFP S32K322: S32K322_100MQFP, S32K322_172MQFP Reference docs: Reference Manual |S32K3xx Reference Manual, Rev. 3, 10/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3Z4S2lrZDFFbTJnQWI0QlctTnpZTkdCNW9sQ3A2UF9aOUdKYnc%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FArchive%2FS32K3xx%5FRM%5FRev3%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FArchive] Datasheet |S32K3xx Data Sheet, Rev. 3 — 10/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3Z4S2lrZDFFbTJnQWI0QlctTnpZTkdCNW9sQ3A2UF9aOUdKYnc%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FArchive%2FS32K3xx%5FDS%5FRev3%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FArchive]
ARTD-24374	New Feature	[uart] [K3 2.0.0] Support new derivatives<*> [K3 2.0.0] Support new derivatives: S32K341: S32K341_100MQFP, S32K341_172MQFP S32K322: S32K322_100MQFP, S32K322_172MQFP Reference docs: Reference Manual |S32K3xx Reference Manual, Rev. 3, 10/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3Z4S2lrZDFFbTJnQWI0QlctTnpZTkdCNW9sQ3A2UF9aOUdKYnc%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FArchive%2FS32K3xx%5FRM%5FRev3%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FArchive] Datasheet |S32K3xx Data Sheet, Rev. 3 — 10/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3Z4S2lrZDFFbTJnQWI0QlctTnpZTkdCNW9sQ3A2UF9aOUdKYnc%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FArchive%2FS32K3xx%5FDS%5FRev3%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FArchive]

ID	Subtype	Headline and Description
ARTD-24378	New Feature	[adc] [K3 2.0.0] Support new derivatives<*> [K3 2.0.0] Support new derivatives: S32K341: S32K341_100MQFP, S32K341_172MQFP S32K322: S32K322_100MQFP, S32K322_172MQFP Reference docs: Reference Manual |S32K3xx Reference Manual, Rev. 3, 10/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3Z4S2lrZDFFbTJnQWI0QlctTnpZTkdCNW9sQ3A2UF9aOUdKYnc%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FArchive%2FS32K3xx%5FRM%5FRev3%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FArchive] Datasheet |S32K3xx Data Sheet, Rev. 3 — 10/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3Z4S2lrZDFFbTJnQWI0QlctTnpZTkdCNW9sQ3A2UF9aOUdKYnc%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FFDS%2FArchive%2FS32K3xx%5FDS%5FRev3%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FFDS%2FArchive]
ARTD-24382	New Feature	[wdg] [K3 2.0.0] Support new derivatives<*> [K3 2.0.0] Support new derivatives: S32K341: S32K341_100MQFP, S32K341_172MQFP S32K322: S32K322_100MQFP, S32K322_172MQFP Reference docs: Reference Manual |S32K3xx Reference Manual, Rev. 3, 10/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3Z4S2lrZDFFbTJnQWI0QlctTnpZTkdCNW9sQ3A2UF9aOUdKYnc%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FArchive%2FS32K3xx%5FRM%5FRev3%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FArchive] Datasheet |S32K3xx Data Sheet, Rev. 3 — 10/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3Z4S2lrZDFFbTJnQWI0QlctTnpZTkdCNW9sQ3A2UF9aOUdKYnc%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FFDS%2FArchive%2FS32K3xx%5FDS%5FRev3%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FFDS%2FArchive]
ARTD-24383	New Feature	[crypto] [K3 2.0.0] Support new derivatives<*> [K3 2.0.0] Support new derivatives: S32K341: S32K341_100MQFP, S32K341_172MQFP S32K322: S32K322_100MQFP, S32K322_172MQFP Reference docs: Reference Manual |S32K3xx Reference Manual, Rev. 3, 10/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3Z4S2lrZDFFbTJnQWI0QlctTnpZTkdCNW9sQ3A2UF9aOUdKYnc%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FArchive%2FS32K3xx%5FRM%5FRev3%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FArchive] Datasheet |S32K3xx Data Sheet, Rev. 3 — 10/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3Z4S2lrZDFFbTJnQWI0QlctTnpZTkdCNW9sQ3A2UF9aOUdKYnc%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FFDS%2FArchive%2FS32K3xx%5FDS%5FRev3%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FFDS%2FArchive]
ARTD-24384	New Feature	[dio] [K3 2.0.0] Support new derivatives<*> [K3 2.0.0] Support new derivatives: S32K341: S32K341_100MQFP, S32K341_172MQFP S32K322: S32K322_100MQFP, S32K322_172MQFP Reference docs: Reference Manual |S32K3xx Reference Manual, Rev. 3, 10/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3Z4S2lrZDFFbTJnQWI0QlctTnpZTkdCNW9sQ3A2UF9aOUdKYnc%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FArchive%2FS32K3xx%5FRM%5FRev3%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FArchive] Datasheet |S32K3xx Data Sheet, Rev. 3 — 10/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3Z4S2lrZDFFbTJnQWI0QlctTnpZTkdCNW9sQ3A2UF9aOUdKYnc%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FFDS%2FArchive%2FS32K3xx%5FDS%5FRev3%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FFDS%2FArchive]

ID	Subtype	Headline and Description
ARTD-24385	New Feature	[port] [K3 2.0.0] Support new derivatives<*> [K3 2.0.0] Support new derivatives: S32K341: S32K341_100MQFP, S32K341_172MQFP S32K322: S32K322_100MQFP, S32K322_172MQFP Reference docs: Reference Manual |S32K3xx Reference Manual, Rev. 3, 10/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3Z4S2lrZDFFbTJnQWI0QlctTnpZTkdCNW9sQ3A2UF9aOUdKYnc%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FArchive%2FS32K3xx%5FRM%5FRev3%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FArchive] Datasheet |S32K3xx Data Sheet, Rev. 3 — 10/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3Z4S2lrZDFFbTJnQWI0QlctTnpZTkdCNW9sQ3A2UF9aOUdKYnc%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FArchive%2FS32K3xx%5FDS%5FRev3%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FArchive]
ARTD-24387	New Feature	[icu] [K3 2.0.0] Support new derivatives<*> [K3 2.0.0] Support new derivatives: S32K341: S32K341_100MQFP, S32K341_172MQFP S32K322: S32K322_100MQFP, S32K322_172MQFP Reference docs: Reference Manual |S32K3xx Reference Manual, Rev. 3, 10/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3Z4S2lrZDFFbTJnQWI0QlctTnpZTkdCNW9sQ3A2UF9aOUdKYnc%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FArchive%2FS32K3xx%5FRM%5FRev3%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FArchive] Datasheet |S32K3xx Data Sheet, Rev. 3 — 10/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3Z4S2lrZDFFbTJnQWI0QlctTnpZTkdCNW9sQ3A2UF9aOUdKYnc%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FArchive%2FS32K3xx%5FDS%5FRev3%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FArchive]
ARTD-24389	New Feature	[pwm] [K3 2.0.0] Support new derivatives<*> [K3 2.0.0] Support new derivatives: S32K341: S32K341_100MQFP, S32K341_172MQFP S32K322: S32K322_100MQFP, S32K322_172MQFP Reference docs: Reference Manual |S32K3xx Reference Manual, Rev. 3, 10/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3Z4S2lrZDFFbTJnQWI0QlctTnpZTkdCNW9sQ3A2UF9aOUdKYnc%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FArchive%2FS32K3xx%5FRM%5FRev3%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FArchive] Datasheet |S32K3xx Data Sheet, Rev. 3 — 10/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3Z4S2lrZDFFbTJnQWI0QlctTnpZTkdCNW9sQ3A2UF9aOUdKYnc%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FArchive%2FS32K3xx%5FDS%5FRev3%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FArchive]
ARTD-24338	Bug	[UART][S32K3_200] Fix MISRA violation<*> Detailed description (how to reproduce it): Lpuart violate MISRA rule 10.3 Symbol "Lpuart_Uart_Ip_apStateStructure" is declared more than once and with types that are not identical. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: UART_TC_0001 Observed behavior: This is the struct that is extern to use in the configuration file. Expected behavior: Fix MISRA rule 8.3 Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA

ID	Subtype	Headline and Description
ARTD-24362	Bug	[I3C] ISR doesn't clear interrupt status flag if the driver is not initialized<*> Detailed description (how to reproduce it): Req ID: CPR_RTD_00011.i3c ISR shall check whether its respective driver is initialized. If the driver is not initialized, the ISR shall only clear interrupt status flag and return immediately. I3C ISR doesn't clear interrupts status flag if driver is not initialized !image-2022-03-13-23-09-28-929.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: I3c_TC_FCT_0004 Observed behavior: [...] Expected behavior: [...] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Refer SAI0_IRQHandler in [Source of Sai_Ip.c i2s NXP Bitbucket|https://bitbucket.sw.nxp.com/projects/ARTD/repos/i2s/browse/ip/IP_SAI/src/Sai_Ip.c]
ARTD-24391	Bug	[S32K3XX][PORT] Init value was incorrect when config Analog Input Mode<*> Detailed description (how to reproduce it): Pin PA9 was config ADC0_ADC0_P7 with level: high/low/not change, check initValue Preconditions: use tag PVT_PORT_S32K3XX_2.0.0_V07 Test Case ID (internal TC that caught the defect) optional: Port_TC_FCT_0005 Observed behavior: !image-2022-03-14-11-12-29-810.png! Expected behavior: InitValue = 0/1/2 corresponding config level low/high/notchange Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-24392	Bug	[S32K3 2.0.0][SENT] Receiver->TransferErrorDetect is not reset after De-Initialization<*> Detailed description (how to reproduce it): Receiver->TransferErrorDetect[SentFastFrame->ChannelId] = TRUE when driver detects a Calibration Pulse error. But this variable can not be reset when driver De-Initialize. It makes the issue: when initialize driver again, it can not detect error relate to Calibration Pulse. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: TS_19 Observed behavior: NA Expected behavior: NA Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-24419	Bug	[Spi] "OsAppEcucPartitionRefList" is not defined on ds s32k324 ,,"Detailed description (how to reproduce it): ""OsAppEcucPartitionRefList"" is not defined Preconditions: enable multicore with s32k324 on ds Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: NA Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA

ID	Subtype	Headline and Description
ARTD-24433	New Feature	[cryif] [K3 2.0.0] Support new derivatives<*> [K3 2.0.0] Support new derivatives: S32K341: S32K341_100MQFP, S32K341_172MQFP S32K322: S32K322_100MQFP, S32K322_172MQFP Reference docs: Reference Manual |S32K3xx Reference Manual, Rev. 3, 10/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3Z4S2lrZDFFbTJnQWI0QlctTnpZTkdCNW9sQ3A2UF9aOUdKYnc%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FArchive%2FS32K3xx%5FRM%5FRev3%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FArchive] Datasheet |S32K3xx Data Sheet, Rev. 3 — 10/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3Z4S2lrZDFFbTJnQWI0QlctTnpZTkdCNW9sQ3A2UF9aOUdKYnc%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FArchive%2FS32K3xx%5FDS%5FRev3%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FArchive]
ARTD-24435	New Feature	[csm] [K3 2.0.0] Support new derivatives<*> [K3 2.0.0] Support new derivatives: S32K341: S32K341_100MQFP, S32K341_172MQFP S32K322: S32K322_100MQFP, S32K322_172MQFP Reference docs: Reference Manual |S32K3xx Reference Manual, Rev. 3, 10/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3Z4S2lrZDFFbTJnQWI0QlctTnpZTkdCNW9sQ3A2UF9aOUdKYnc%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FArchive%2FS32K3xx%5FRM%5FRev3%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FArchive] Datasheet |S32K3xx Data Sheet, Rev. 3 — 10/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3Z4S2lrZDFFbTJnQWI0QlctTnpZTkdCNW9sQ3A2UF9aOUdKYnc%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FArchive%2FS32K3xx%5FDS%5FRev3%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FArchive]
ARTD-24436	Bug	[CAN] analysis global variable access in multithreads/multicores scenario<*> Detailed description (how to reproduce it): Case A: !image-2022-03-15-14-32-03-471.png|thumbnail! [...] static ReceivedDataBuffer variable could be accessed simultaneously as below supposed scenario: multithreads: Can_MainFunction_Read_0 is executed on thread_0, Can_MainFunction_Read_1 is executed on thread_1 multicores: core0 and core1 execute on Can_MainFunction_Read(); Case B: !image-2022-03-15-14-39-03-414.png|thumbnail! Can_Ipw_au16TxPduId could be changed during it is being passed to CanIf_TxConfirmation. This case can only happen in multithreads scenario: Can_MainFunction_Write is executed on thread_0, Can_Write is executed on thread_1. !image-2022-03-15-14-48-40-278.png|thumbnail! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: review Observed behavior: some shared global variable access is not safe Expected behavior: global variables should be analysed Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A

ID	Subtype	Headline and Description

ARTD-24455	Bug	hard fault during flash reading<*>
		
		Detailed description (how to reproduce it):
		I can share the project if it is needed.
		Observed behavior:
		During our MC development we experienced very latent Hard fault.
		I think it might happen due to speculative fetches.
		Expected behavior:
		Fault occurred in Clock_Ip_Init(&Mcu_aClockConfigPB[0]); when optimization was set to O3 (if you set O1 or if you set a break point there on that instruction Hardfault will not occur)
		40563e: f8df 8138 ldr.w r8, [pc, #312] ; 405778 <Clock_Ip_InitClock+0x5cc> caused hard fault
		!image-2022-03-16-09-58-56-799.png|thumbnail!
		Proposed solution optional:
		we discussed this topic with BACH NGUYEN <B.Nguyen@nxp.com>.
		conclusion is that in system.c MPU settings should be changed.
		instead of
		/*Program flash which would extract from linker symbol*/
		rbar[2]=(uint32)__ROM_CODE_START;
		rasr[2]=0x060{color:red}B{color}002BUL;
		There should be(Memory type: Device):
		/*Program flash which would extract from linker symbol*/
		rbar[2]=(uint32)__ROM_CODE_START;
		rasr[2]=0x060{color:red}1{color}002BUL;

ARTD-24498	Bug	[S32K3 2.0.0][SENT] Slow/FastNotification can not be imported from epc to S32DS<*> Detailed description (how to reproduce it): When import epc file fto S32DS, some notification nodes do not appear on S32DS !image-2022-03-17-14-40-04-930.png! Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: NA Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-24511	Bug	[S32DS][SAF85xx] Build fail with new project on S32DS after updating code<*> Detailed description (how to reproduce it): 1. Install S32DS3.4 with devpackage: com.nxp.s32ds.saf85.update_3.4.4.20220310181914.zip and update_site: S32R_RTD_4_4_EAR_0_8_0_DS_updatesite_2203_signed.zip Wed Mar 16 20:27:12 2022 2. Integrate GHS 202114 and DIAB 7.0.3.0 into S32DS 3. Create new project following steps: Step1: In S32DS choose File > New > S32DS Application project Step2: Fulfil project name and Choose Family/SAF8544 (M7/A53) > Next> Next Step3: Select required tool chain plugin from toolchain tab x number of tools chains Step4: Type a project name(e.g NewProject). Step5: Select SDK version Step6: Click Finish Step7: Build project with RAM and FLASH Step8: Click on Update code Step9: Build project with RAM and FLASH Preconditions: Test Case ID (internal TC that caught the defect) optional: INTEGRATION_TC_017 INTEGRATION_TC_037 INTEGRATION_TC_077 Observed behavior: Build fails after updating code both cores M7 and A53 on all compilers !image-2022-03-17-17-30-18-091.png|width=1003,height=218! Expected behavior: Have no warnings, errors when building new project on all compilers Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:

ID	Subtype	Headline and Description
ARTD-24529	Bug	[S32K3 2.0.0] [OCU] Incorrect autosar minor version in file Ocu.template<*> Detailed description (how to reproduce it): In file Ocu.template using wrong M4 define (M4_XDM_AR_SPEC_VERSION_PATCH) for autosar minor version. Correct M4 is M4_XDM_AR_SPEC_VERSION_MINOR Preconditions: Build test ecpd high layer Test Case ID (internal TC that caught the defect) optional: Ocu_TS_ECPD_001.c Observed behavior: Test Ocu_TS_ECPD_001 not pass, there is a different of ArReleaseMinorVersion between new configuration and original configuration (0 and 4) Expected behavior: ArReleaseMinorVersion in new configuation change to 4, test passed Proposed solution optional: NA
ARTD-24548	New Feature	s32k324 dual core template in a single project<*> NewWorkDescription: Include attached project in Platform examples Requirement source: Customer request Proposed solution optional: Include project in platform
ARTD-24575	Bug	[S32K3XX] I3c_Init() jumps to hardfault with update from Platform<*> Detailed description (how to reproduce it): I3c_Init() jumps to hardfault with update from Platform !image-2022-03-21-15-43-19-116.png! Change compare PVT_S32K3XX_ARTD_22061_020 vs PVT_S32K3XX_ARTD_22061_016 !image-2022-03-21-15-43-36-430.png! Preconditions: Use Platform with tag PVT_S32K3XX_ARTD_22061_020 Test Case ID (internal TC that caught the defect) optional: I3c_TS_WIR_100 Observed behavior: Program jumps to hardfault Expected behavior: No error when executing test Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-24644	Bug	[WDG] Missing Wdg_Instance1 for S32K322 derivative from S32ConfigurationTool<*> Detailed description (how to reproduce it): Step 1: Create new project Step 2: Add Wdg and dependencies to new project Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Missing Wdg_Instance1 for S32K322 derivative !image-2022-03-21-18-11-04-571.png|width=956,height=538! Expected behavior: Add Wdg_Instance1 for K322 derivative Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]

ID	Subtype	Headline and Description
ARTD-25248	Bug	[Port][S32K342] Incorrect PORT_MAX_UNUSED_PADS_U16 macro value generated from S32CT<*> Detailed description (how to reproduce it): Use tag PVT_PORT_S32K3XX_2.0.0_V15 for the Port plugins Open S32DS and configurate S32K342 with S32K342_100MQFP package. Add random pins to the CTHL and open Port_VS_0_PBcfg.c and Port_Cfg.h One examples .mex was attached for reviewing. Preconditions: PVT_PORT_S32K3XX_2.0.0_V15 Test Case ID (internal TC that caught the defect) optional: Port_TC_COT_0001 Observed behavior: the array Port_aUnusedPads_VS_0 has more elements than the number of elements generated ({*}PORT_MAX_UNUSED_PADS_U16{*}) With the attached .mex, the number of elements is 126 but the macro PORT_MAX_UNUSED_PADS_U16 is 124 Expected behavior: The number of PORT_MAX_UNUSED_PADS_U16 is correct corresponding to the number of the elements of Port_aUnusedPads_VS_0 Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: It seems like the resource.txt for S32K342_100MQFP is wrong with the Port.{*}Siul2Instance0NotImplementedMscrs{*}, please re-check.
ARTD-25261	Bug	[Port][S32K3xx] Untouch IMCR feature doesn't work as expected<*> Detailed description (how to reproduce it): Use tag PVT_PORT_S32K3XX_2.0.0_V15 for the plugins. Create some random configuration with IMCR 188 set in the UntouchedIMCR tab Preconditions: PVT_PORT_S32K3XX_2.0.0_V15 Test Case ID (internal TC that caught the defect) optional: Port_TC_WBT_0009 Observed behavior: At the clearing IMCR step in Port_lpw.c, the driver keeps clearing IMCR 188 even it is set in the UntouchedIMCR tab. !image-2022-03-22-19-30-14-965.png! Expected behavior: No Imcr set in UntouchedIMCR tab are cleared during Port_Init Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-25266	Bug	[I3C] MISRA violations of Rule 2.3<*> Detailed description (how to reproduce it): !https://bitbucket.sw.nxp.com/rest/api/1.0/projects/ARTD/repos/i3c/attachments/12639! Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Undocumented misra violations Expected behavior: Only accepted misra deviations remain in the report Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-25282	Bug	[UART] Wrong lowerMultiplicity attribute on ecpd<*> Detailed description (how to reproduce it): lowerMultiplicity of UartEcucPartitionRef is wrong, must be 0 Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Have unexpected error Expected behavior: No error Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Fix lowerMultiplicity value of UartEcucPartitionRef to 0

ID	Subtype	Headline and Description
ARTD-25285	Bug	[S32K3XX RTM 2.0.0] Fix warning of example<*> Detailed description (how to reproduce it): In the example IP LAYER{color}, the build warning appear because of Port warning: !image-2022-03-23-14-46-54-680.png! In the example{color:#de350b} Icu_BlinkLed_ASR_Emios_S32K344 and Icu_BlinkLed_ASR_Emios_S32K342{color}, the warning of Mcu apppear: !image-2022-03-23-14-49-19-116.png! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: N/A Expected behavior: N/A Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-25301	Bug	[S32K3 2.0.0][RM] Compiler Warning on IAR<*> Detailed description (how to reproduce it): Compiler warnings on IAR: static const uint8 Xrdc_Master[XRDC_COUNT] = XRDC_MASTER_INSTANCE; "d:\ARTD\S32K3XX\output\eclipse\plugins\Rm_TS_T40D34M20I0R0\src\Xrdc_Ip.c",148 Warning[Be006]: possible conflict for segment/section ".mcal_const": variable "Xrdc_Master ".mcal_const"" (declared at line 148 of "d:/ARTD/S32K3XX/output/S32K3XX_S32K344_iar/rm/../../eclipse/plugins/Rm_TS_T40D34M20I0R0/src/Xrdc_Ip.c") is an initialized variable (2 more variables like this) variable "Xrdc_Ip_InstanceAddress ".mcal_const"" (declared at line 136 of "d:/ARTD/S32K3XX/output/S32K3XX_S32K344_iar/rm/../../eclipse/plugins/Rm_TS_T40D34M20I0R0/src/Xrdc_Ip.c") is a constant (4 more variables like this) const Xrdc_Ip_InstanceConfigType aXrdc_Config_Array[1] = \{&Xrdc_Config_XRDC_INSTANCE0}; "d:\ARTD\S32K3XX\output\S32K3XX_S32K344\rm\Rm_TS_001_cfg1_CORE0\generate_tresos\src\Xrdc_Ip_PBcfg.c",538 Warning[Be006]: possible conflict for segment/section ".mcal_const_cfg": variable "aXrdc_Config_Array ".mcal_const_cfg"" (declared at line 538 of "d:/ARTD/S32K3XX/output/S32K3XX_S32K344/rm/Rm_TS_001_cfg1_CORE0/generate_tresos/src/Xrdc_Ip_PBcfg.c") is an initialized variable variable "Xrdc_Instances_InUsed ".mcal_const_cfg"" (declared at line 150 of "d:/ARTD/S32K3XX/output/S32K3XX_S32K344/rm/Rm_TS_001_cfg1_CORE0/generate_tresos/src/Xrdc_Ip_PBcfg.c") is a constant (5 more variables like this) Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Compiler warning on IAR Expected behavior: No Compiler warning Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-25452	Bug	[I3c] Init functions do not reset state structure to default values<*> Detailed description (how to reproduce it): Preconditions: Test Case ID (internal TC that caught the defect) optional: Observed behavior: I3c_Ip_MasterInit and I3c_Ip_SlaveInit functions do not reset state structures to default values. Also I3c_Ip_MasterDeInit and I3c_Ip_SlaveDeInit should reset registers to their default values. Expected behavior: I3c_Ip_MasterInit and I3c_Ip_SlaveInit functions reset state structures to default values. I3c_Ip_MasterDeInit and I3c_Ip_SlaveDeInit reset registers to their default values. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:

ID	Subtype	Headline and Description
ARTD-25453	Bug	[WDG] The macro SWT_IP_MAP has Multiple Definition<*> Detailed description (how to reproduce it): SWT_IP_MAP has Multiple Definition Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Expected behavior: SWT_IP_MAP define in Swt_Ip_Cfg_Defines.h Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: SWT_IP_MAP delete define in Swt_Ip.c
ARTD-25457	Bug	[FLS][C40][S32K3 2.0.0] Hardfault exception occurs when accessing unaligned address<*> Detailed description (how to reproduce it): Due to the compiler optimized code, some lines of C code that handle the unalignment were cut out. When reading data from unaligned buffer address, instead of read one byte one of unaligned address, it read 4-byte into DataTemp32 due to compiler optimization then Hardfault will occur. (see attached figure for details) Preconditions: NA Test Case ID (internal TC that caught the defect) optional: Fls_TS_051 Observed behavior: Read from unaligned address cause hardfault Expected behavior: Avoid compiler from optimizing Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Add the volatile key word for variable uint32 DataTemp32; to prevent optimization
ARTD-25464	New Feature	[Gpt]Update some data test<*> NewWorkDescription: Update test data ecpd due to some module changes for new derivative S32K322, S32K341 Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Update test data with some test
ARTD-25488	Bug	[S32K3XX 2.0.0][PORT] Fix warning at build for S32K3 example<*> Detailed description (how to reproduce it): There are warnings related to Siul2_Port driver when build examples for S32K3 platform. Only occurred at IP layer. !image-2022-03-25-14-04-19-748.png|width=660,height=182! Preconditions: Build examples for modules that use Siul2_port driver (ex. Ocu, Icu,...) Test Case ID (internal TC that caught the defect) optional: Emios_Ocu_Example, Emios_Icu_Example, ... Observed behavior: The warnings related to Siul2_port driver appear Expected behavior: No warnings appear Proposed solution optional: NA
ARTD-25494	Bug	[Platform][s3k3xx_200] update linker file<*> Detailed description (how to reproduce it): Linker 344 Preconditions: PVT_S32K3XX_ARTD_22061_033 Test Case ID (internal TC that caught the defect) optional: Platform_TS_001 Observed behavior: Linker Expected behavior: Running project multicore on k324 Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: update sizes of ITCM and DTCM are 32K and 64k

ID	Subtype	Headline and Description
ARTD-25529	Bug	[PORT] [S32K3XX_2.0.0] Duplicate the define SIUL2_MAX_NUM_OF_IMCR_REG in Siul2_Port_Ip.h<*> Detailed description (how to reproduce it): There is a duplicate define about SIUL2_MAX_NUM_OF_IMCR_REG in Siul2_Port_Ip.h Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: There is a duplicate define about SIUL2_MAX_NUM_OF_IMCR_REG in Siul2_Port_Ip.h Expected behavior: There is no duplication for the defines. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Remove one redundant define of SIUL2_MAX_NUM_OF_IMCR_REG in Siul2_Port_Ip.h
ARTD-25606	Bug	[UART] Getting an error when enabling multicore node on S32CT<*> Detailed description (how to reproduce it): N/A Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Getting an error when enabling multicore node on S32CT !screenshot-1.png|thumbnail! Expected behavior: Update uart component on S32CT Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:

4.6 1.0.0

ID	Subtype	Headline and Description
ARTD-3065	New	New Feature [S32K3] Add support for SIUL2 External Interrupts with Config Tools for RTD ,,"There is no SIUL2 External Interrupts Config Tool component. Please add a Config Tool Component that sets, for each external interrupt channel, the action on which each interrupts is triggered (rising edge, falling edge or both edges). An approach is to provide callbacks for each channel. (There are 4 interrupts vectors, e.g. IRQ_07_00, each handling 8 input channels. The RTD should implement the interrupts and trigger a callback for each pin state change.) Detailed explanation in the context of MBDT code generation:* The tool allows the user to select the eirq pins for the SIUL2 peripheral. However, I was not able to find structures that allow the user to select which action is going to trigger that interrupt (rising, falling, either edge). More than that, the interrupt block is going to implement and install the interrupt handler assigned to the required pins group (there are 32 external interrupts pins muxed 8 by 8 in 4 handlers) but since there is no interrupt configuration as mentioned above, which block is going to configure that, the interrupt block or is going to be another block for that? Also, we need other blocks that will return the IREER, IFEER registers values, in order to identify which pin and state triggered the interrupts. Test case: S32K / MPC approach: # Single block that performs the following actions: Initialize pin Configure interrupt action (Rising Edge ...) Installs interrupt Handles the interrupt (decides which pin triggered the ISR) Clears the pins interrupt S32K3 Initialize pin (Pins Tool) Configure interrupt action (Rising Edge ...) (*RTD CONFIG TOOL ISR PERIPH* ???) For the Periph tool, we have two requirements: 1. Provide a dedicated tab/setting for each enabled PIN allowing users to set the action that will trigger the interrupt like Rising edge. 2. A tab/setting in which the user must specify the handler name and priority for each interrupt group *IRQ**_07_00* Installs interrupt (Interrupt block) Handles the interrupt (decides which pin triggered the ISR) (Interrupt block) (RTD Function to return *DISR0* register) Clears the pins interrupt (Interrupt block) (RTD Function to reset the interrupt status in DISR0 defined in Siul2_Icu_Ip_Irq.c) We found that there is an implementation in the *Siul2_Icu_Ip_Irq.c* *that access the status* ** *flags* ** but the config tool is not copying the files in the project and no configuration structure for the IFEER/IREER found. "

ID	Subtype	Headline and Description
ARTD-3069	New	New Feature [S32K3] Enhance the EMIOS driver features ,,"In case of EMIOS only the PWM feature is available in the S32DS Config Tools. Please add components for other functionalities like Input capture, Counter bus, etc. Also, please add a way of configuring the eMIOS Global Prescaler. Regarding the PWM, from the current CT initialization, even if you can configure a channel to be driven by a Global counter bus, for example, the Global counter bus A, I was not able to find an option that can configure the Global Counter bus A to count up. "
ARTD-3072	New	New Feature [S32K3] Add RTD example for EMIOS ,,"Since the EMIOS is a complex peripheral which is critical for Motor Control applications, please consider adding RTD examples to demonstrate how to use the driver in various scenarios like: PWM generations: asymmetric/symmetric/edge/center align Input Capture"
ARTD-3491	New	New Feature [RM] Support PID LOCK For XRDC ,," Mpu_M7_Ip_EnableRegion_Privileged is Reentrant, should be marked as NonReentrant per channel, and no EA needed; update also associated req, as the HLD one is Non_Reentrant. Mpu_M7_Ip_SetAccessRight_Privileged is Reentrant, should be marked as NonReentrant per channel, and no EA needed; update also associated req, as the HLD one is Non_Reentrant. Add support for non-supported field LK2 TSM LNUM"
ARTD-3773	New	New Feature [ADC] Check and update DMA support for S32ConfigurationTool High Level Driver ,,DMA for SW triggered groups and Triggered Mode
ARTD-4422	New	New Feature [FEE] Add support for bad Sector Management and Sector Retirement (part 1) ,,"NewWorkDescription: Add support for bad Sector Management and Sector Retirement (CPR_RTD_00505.fee). This involves removing Sectors from configuration when they become unusable. Rationale: some flash memory specs have low endurance/write cycles availability, which needs to be improved by the ability to retire bad sectors or locations affected by permanent ECC, at the expense of allocated flash size the endurance being a ppm specification."" Requirement source: cPRD (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Add support to use un-consecutive logical sector addresses."

ID	Subtype	Headline and Description
ARTD-5105	New	New Feature [sai] [S32CT] Implement EPD/EPC support for HLD and IPLD ,,"Implement EPD/EPC support for HLD and IPLD. Please refer to [this post on Teams https://teams.microsoft.com/l/ message/19:e451c595d3ba410c8f9c1f5efc19a8a3@thread.tacv2/1606904026692? tenantId=686ea1d3-bc2b-4c6f-a92c-d99c5c301635&groupId=f9decd68-7b74-4101- a4d2- ad54e86f727f&parentMessageId=1606904026692&teamName=Zebra&channelName=Configuration %20(code%2C%20DS%2C%20EB%2C%20etc)&createdTime=1606904026692] for additional details. From the presentation, the main focus should be on the following sections: Mapping XDM to Component EPD Importer EPD Generation EPC Importer EPC Generation "
ARTD-5234	New	New Feature [ADC] Use HW logical for calling all extension APIs, instead of directly physical id" ,,"Use HW logical for calling all extension APIs, instead of directly physical id Make sure order of generation in the config struct for multiple instances& different logical IDs, is correct also in S32CT
ARTD-6079	Bug	[Port] Pins tool still config MSCR[SRC] bit when driver not support by hardware<*> Detailed description (how to reproduce it): Configuration some pins by pins tool in S32DS. Slew Rate is Slowest setting. Calling Siul2_Port_Ip_Init function with config pins has _Slew Rate is Slowest setting,_ bit MSCR[SRC] not set to 1 (Slowest setting). Test Case ID (internal TC that caught the defect) optional: IP_Port_Siul2_TC_0005 Observed behavior: Some pins has bit MSCR[SRC] default by hardware.

ID	Subtype	Headline and Description
ARTD-6095	Bug	[S32K3XX][RM] XRDC does not trigger exception, cannot configure PIDM when using PID feature ,,"There is no exception when violate accessing memory with config enable PE bits follow 2 fomula below 10b The process identifier is included in the domain hit evaluation as defined by the following expression: partial_domain_hit = (PE == 10b) && ((PID & PIDM) == (PIDn[PID] & PIDM)) 11b The process identifier is included in the domain hit evaluation as defined by the following expression: partial_domain_hit = (PE == 11b) && ((PID & PIDM) == (PIDn[PID] & PIDM)) PIDM can not configure in EB interface Expect behavior: XRDC should trigger exception on wrong PID set up of domain when accessing memory. PIDM is configurable
ARTD-6219	Bug	[MCU] Some nodes are not active in S32 Configuration Tool<*> The following nodes are not active in S32 Configuration Tool: McuNoPLL; McuFxoscUnderMcuControl; McuFircUnderMcuControl; McuPll0UnderMcuControl; McuSxoscUnderMcuControl; McuSircUnderMcuControl. Please see attached file.

ID	Subtype	Headline and Description
ARTD-6298	Bug	[SAI] Wrong transmit data after aborting/timeout transfer<*> Detailed description (how to reproduce it): Wrong transmit data after aborting/timeout transfer. Please refer the MAF log and the logic analyzer Sai_Abort_Sending.logicdata: the first transmission is abort at middle, then try to send again !image-2021-01-14-11-07-28-788.png! Initialize SAI driver as master mode, master sends data with I2S protocol Initialize MAF I2S interface: slave mode, receiver and 8-bit word size SAI driver starts an asynchronous transaction on the SAI bus Wait until the SAI transmission status is not SAI_STATUS_BUSY Abort on going transfer Verification Point: The SAI transmission status is SAI_STATUS_ABORTED MAF waits until the transmitting transaction finishes Verify: the MAF return status is E_MAF_OK MAF test the received frames, compare with the passed data array with data in the MAF RX buffer Verification Point: + the MAF return status is E_MAF_OK + The callback counter for SAI_IP_RUN_ERROR event equals 1 SAI driver starts an asynchronous transaction on the SAI bus Wait until the SAI transmission status is not SAI_STATUS_BUSY Verification Point: The SAI transmission status is SAI_STATUS_COMPLETED MAF test the received frames, compare with the passed data array with data in the MAF RX buffer Verification Point: + the MAF return status is E_MAF_OK => Failed at this verification point + The callback counter for SAI_IP_RUN_ERROR event equals 0 DeInitializes the SAI module Preconditions: [...] Observed behavior: Wrong transmit data after aborting/timeout event Expected behavior: Correct transmit data after aborting/timeout event Proposed solution optional:
ARTD-6477	Bug	[SAI] File version check missing for SchM_Sai header in Sai_Ip.c<*> File version checks

ID	Subtype	Headline and Description
ARTD-6677	New	New Feature [ADC] Add Memory Mapping ,,"Add memory map according to following guidelines: According Autosar memmap standard (AUTOSAR_SWS_MemoryMapping.pdf) The shortcut \{INIT_POLICY} means the initialization policy of variables. Possible INIT_POLICY postfixes are: NO_INIT*, used for variables that are never cleared and never initialized. CLEARED, used for variables that are cleared to zero after every reset. POWER_ON_CLEARED, used for variables that are cleared to zero only after power on reset. INIT*, used for variables that are initialized with values after every reset. POWER_ON_INIT, used for variables that are initialized with values only after power on reset. All global elements (variable, array, struct) that are initialized with 0 value (NULL,NULL_PTR) should be put in __INIT memory section. For example, following declaration is wrong*: #define PORT_START_SEC_VAR**_NO_INIT_**UNSPECIFIED_NO_CACHEABLE #include ""Port_MemMap.h"" static const Port_ConfigType Port_pConfig = NULL_PTR; #define PORT_STOP_SEC_VAR**_NO_INIT_**UNSPECIFIED_NO_CACHEABLE #include ""Port_MemMap.h"" Should be corrected : #define PORT_START_SEC_VAR**_INIT_**UNSPECIFIED_NO_CACHEABLE #include ""Port_MemMap.h"" static const Port_ConfigType Port_pConfig = NULL_PTR; #define PORT_STOP_SEC_VAR**_INIT_**UNSPECIFIED_NO_CACHEABLE #include ""Port_MemMap.h"" Build environment need to update compiler option not to implicitly move zero-initialized elements to BSS-like memory section. Note: in GHS and GCC, bss-zero optimization is applied not in all cases, do not only check map file to find wrong memory mapping placement "
ARTD-7670	Bug	[S32DS] Functional groups are not working correctly<*> 1. Create project enable RTD for S32G274_Rev2 2. Open Peripherals tool-> Add more functions using function group item on toolbar. 3. Add some components for each function 4. Export html report > each function contains their components information correctly in the content of HTML report. 5. Check source code generated. > There is no function from step 2 added into source code generated for all components. If the function group feature has not been supported yet, it should be disabled or removed from toolbar.
ARTD-7686	New	New Feature [ADC] Extend HLD examples with DMA usecase ,,"the Adc DMA is a common application for customer, suggest to add a Adc DMA case Extend HLD EBT and S32CT examples with DMA usecase"

ID	Subtype	Headline and Description
ARTD-7928	New	New Feature [SAI] Optimize interrupt loops ,,"Optimize interrupt loops: Move switch outside while/for loops to avoid checking condition for each data written in FIFO"
ARTD-7938	New	New Feature [ICU] Improve validation regarding input signals used on LPCMP ,,Analise and add validation based on available input channels used by CMP
ARTD-7964	New	New Feature [ADC] Avoid sorting HW triggered channels when enabling hw triggered groups ,,"Avoid sorting HW triggered channels when enabling hw triggered groups Sorting is only required for DMA, because BCTU does not support issuing DMA request when conversion list is completed only interrupt. So this is required to trigger DMA only after the last adc channel finishes conversion (the largest physical channel id) Ideas to optimize: reorder channels only for DMA but make sure order is same in result for DMA and interrupt, and Autosar requirement generate an array already sorted tbd how affects set channel feature others TBD"
ARTD-8151	New	New Feature [gpt] Review changes according to Reference Manual (Rev2DraftB) ,,"Review changes according to Reference Manual (Rev2DraftB). [Link|https://nxp1.sharepoint.com/:b:/t/25_43/k344/EcYwLySwZpJNkMY2fbsfreMBsrEqt6vbefT0AM-VaRzIbw?e=UNoWjF] "IP_" prefix was added to all defines from the "Peripheral instance base addresses" section. Please update driver code with the new prefix."
ARTD-8152	New	New Feature [pwm] Review changes according to Reference Manual (Rev2DraftB) ,,"Review changes according to Reference Manual (Rev2DraftB). [Link|https://nxp1.sharepoint.com/:b:/t/25_43/k344/EcYwLySwZpJNkMY2fbsfreMBsrEqt6vbefT0AM-VaRzIbw?e=UNoWjF] "IP_" prefix was added to all defines from the "Peripheral instance base addresses" section. Please update driver code with the new prefix."
ARTD-8155	New	New Feature [spi] Review changes according to Reference Manual (Rev2DraftB) ,,"Review changes according to Reference Manual (Rev2DraftB). [Link|https://nxp1.sharepoint.com/:b:/t/25_43/k344/EcYwLySwZpJNkMY2fbsfreMBsrEqt6vbefT0AM-VaRzIbw?e=UNoWjF] "IP_" prefix was added to all defines from the "Peripheral instance base addresses" section. Please update driver code with the new prefix."

ID	Subtype	Headline and Description
ARTD-8091	New	New Feature [ADC] Add support for enable high speed conversion ,,"ADC_SAR on K3 supports high speed conversion. It is enabled by HSEN field found in AMSIO register. Enabling this allows ADC conversions to use a higher clock speed when doing conversions or calibrations."
ARTD-8098	New	New Feature [S32K3XX][BASE] Update Header File to RM Rev.2. Draft B ,,Update Header File to latest RM revision: S32K3xx RM Rev.2. Draft B
ARTD-8225	Bug	[S32K3][MCU] SWT1_RST is not supported in S32K314, S32K344, K312, K311 ,,"According Table 163. Register fields and applicability in S32K3XXRM Reference Manual Rev.2 Draft B, 02/2021. SWT1_RST dose not exist in S32K344 and S32K314 !image-2021-03-05-16-01-07-325.png! But in driver code supported SWT1_RST, it should be removed. and some macro must be remove SWT1_RST in S32K314 and S32K344 MC_RGM_FES_RWBITS_MASK32 include SWT1 MC_RGM_FES_IRQ_BITS_MASK include SWT1 MC_RGM_FERD_RWBITS_MASK include SWT1
ARTD-8230	Bug	[PWM] Fix Typos in FlexIO API requirements<*> {code:c} Requirement FLEXIO_PWM_IP_005_001: Service name: Flexio_Pwm_Ip_UpdatePeriodDuty Syntax: Flexio_Pwm_Ip_StatusType Flexio_Pwm_Ip_UpdatePeriodDuty(uint8 instance, uint8 channel, uint ... OK Requirement FLEXIO_PWM_IP_006_001: Service name: Flexio_Pwm_Ip_GetOutputState Syntax: boolean Flexio_Pwm_Ip_GetOutputState(uint8 instanceId, uint8 channel) Sync/Async: Sync Reent ... should use one naming parameter (instance or instanceId) for all of apis to synchronize between the driver code and the requirement The Flexio source code has all APIs defeined with instanceId. FlexIO requirements should be updated to reflect this.
ARTD-8238	New	New Feature [ICU][CMP] Create example for CMP and RTC-API ,,"Add example for using RTC-API and CMP as depicted in Reference Manual. The example should be as close as possible for manual/user verification (not automated) and included in plugin examples if possible. !image-2021-03-05-14-02-13-002.png|width=415,height=283!"

ID	Subtype	Headline and Description
ARTD-8318	Bug	[S32CT][LIN] Should not allow to select the same Flexio channel for Lin TX and Lin RX<*> On S32CT, at IPL, the LIN Flexio Rx Channel and LIN Flexio Tx Channel should not be assigned to the same MCL Flexio channel. There should be a error in the Problems view. Please check the attached file.
ARTD-8360	New	New Feature [ADC] Refactor implementation of DMA stream optimization feature ,,"Refactor implementation of DMA stream optimization feature: implement similarly with DMA streaming without interrupt even if requires to have result reorder enabled. this would avoid the need to have channels consecutive in the group which is more restrictive than result reorder. Also need to remove checks from configurators remove DmaMuxSource and workaround to enable/disable in Adc_Ipw_StartDmaOperation"
ARTD-8365	New	New Feature [ADC] S32CT IPL standalone mode must generate defines for IP instances used ,,"[ADC] S32CT IPL standalone mode must generate defines for IP instances used !image-2021-03-09-17-20-28-153.png|thumbnail! Update also example"
ARTD-8373	Bug	[Adc] Mismatching information between Tresos and S32ConfigurationTool configurators when comparing layout<*> Detailed description (how to reproduce it): Step 1: Repo sync Adc module and dependent module Step 2: compile plugin and generate layout for S32DS Step 3: Config S32CT same with EB Step 4: Compare layout of S32CT with EB Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: There is some information that does not match EB and S32CT when comparing layout CT: missing node *AdcClockSource* EB : redundant AdcHwTrigTimer node ** Some name of nodes different between EB with CT. Detail in *share point link*: https://nxp1.sharepoint.com/:x:/r/sites/Zebra/_layouts/15/Doc.aspx?sourcedoc=%7BD9A67063-B22E-47AE-A2C0-5D798377D1D2%7D&file=ADC_Compare_Node.xlsx&action=default&mobileredirect=true Expected behavior: All nodes on EB and CT should be the same

ID	Subtype	Headline and Description
ARTD-8377	Bug	[Platform][S32K3] Code generate between EB and CT is not equivalent when disable interrupt monitoring<*> Detailed description* (how to reproduce it): # On EB and S32DS config Platform component with unchecked "Interrupt Monitoring Enabled" # Compare "Platform_CfgDefines.h" file !image-2021-03-10-14-50-15-113.png! Test Case ID (internal TC that caught the defect):* N/A Observed behavior:*_ The file "Platform_CfgDefines.h" between EB and S32DS is not equivalent Expected behavior: The file "Platform_CfgDefines.h" between EB and S32DS is equivalent
ARTD-8384	Bug	[LIN] Lin driver can't report timeout error caused by hardware error<*> In case run out of timeout, driver can't report timeout the error as requested in the requirements SWS_Lin_00097, SWS_Lin_00218
ARTD-8407	Bug	[S32K3][Mcu-clock] Wrong clocks frequency when disabling clock gating by calling Clock_Ip_DisableModuleClock()<*> Test procedure: Step1: Disables clock gating by calling Clock_Ip_DisableModuleClock() Step2: Check frequency values Expected result: The returned frequency is 0 !image-2021-03-11-14-07-07-392.png|width=757,height=315!
ARTD-8409	New	New Feature [FLEXIO-LIN] - Add protocol timeout ,,Add protocol timeout on reception and transmission
ARTD-8420	Bug	[GPT] Cannot start Pit with countValue set to maximum<*> Call of Gpt_StartTimer with Pit channel and argument value set to MAX value, it fails in function Pit_Ip_StartChannel on check: DevAssert(PIT_MAX_VALUE > countValue);}} It should be possible to use MAX value. The check should be updated to:}} DevAssert(PIT_MAX_VALUE >= countValue);}}{{}} Same check is used also in Stm_Ip_StartCounting and Ftm_Gpt_Ip_StartCounting. It should be fixed also there, if the hardware supports using maximal value.}}

ID	Subtype	Headline and Description
ARTD-8427	Bug	[SENT] Follow up - fix HIS and MISRA warnings<*> Detailed description (how to reproduce it): Fix HIS and MISRA warnings Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-8429	Bug	[RM] Add Ip level parameter input checks<*> Detailed description (how to reproduce it): Do not check input parameters of functions yet Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Do not check input parameters of functions yet Expected behavior: Check input parameters of functions Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Check input parameters of functions

ID	Subtype	Headline and Description
ARTD-8453	Bug	[GPT] Case sensitive include file should be fixed<*> Detailed description (how to reproduce it): On Pit_Ip_Cfg.h , there is #include "Pit_Ip_BOARD_INITPERIPHERALS_PBcfg.h" instead of #include "Pit_Ip_BOARD_InitPeripherals_PBcfg.h" (notice case sensitive) This should be fixed at it will not compile on Linux env. Picture attached Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-8455	New	New Feature [RM][S32K3XX] Fix and comment static analysis violations (MISRA + HIS + CERT-C) ,,"All static analysis need to be fixed for the BETA release. Everything needs to be fixed in the code or commented in Coverity if it cannot be fixed. The following wiki is work in progress, but it will be updated with all needed information: [https://confluence.sw.nxp.com/pages/viewpage.action?pageId=133734230] "
ARTD-8461	Bug	no pinmux configuration for CLKOUT in S32_CT<*> Detailed description (how to reproduce it): [...] Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...] - There is no pinmux configuration for CLKOUT in Pins of S32_CT

ID	Subtype	Headline and Description
ARTD-8466	Bug	[LIN] - Driver can't change status to LIN_TX_BUSY after Lin_SendFrame function called<*> Detailed description (how to reproduce it): Driver can't change status to LIN_TX_BUSY after Lin_SendFrame and Lin_GetStatus function called. Preconditions: In Lin_SendFrame driver set Lin_Ipw_au8LinChFrameStatus[u8Channel] = LIN_CH_READY_STATE; but if Lin_Ipw_au8LinChFrameStatus[u8Channel] = LIN_CH_READY_STATE then when function Lin_GetStatus called, it will return LIN_OPERATION status. It must return LIN_TX_BUSY status. Test Case ID (internal TC that caught the defect) optional: Lin_TC_FCT_1007 Observed behavior: Lin_GetStatus will return LIN_OPERATION status Expected behavior: Lin_GetStatus will return LIN_TX_BUSY status Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-8467	Bug	[LIN] The length of wake-up pulse generated by Flexio IP longer than standard<*> Detailed description (how to reproduce it): The length of wake-up pulse generated by Flexio IP is 23.53ms over LIN standard from 250 Amicros to 5ms Preconditions: NA Test Case ID (internal TC that caught the defect) optional: Lin_TS_021 Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-8478	Bug	[LIN] Driver's autobaud rate feature fail<*> Detailed description (how to reproduce it): Driver's autobaud rate feature fail. Preconditions: Driver use Osif timer to check baudrate but It don't enable bit interrupt enable. So, driver can't goto interrupt handler function. Test Case ID (internal TC that caught the defect) optional: Ip_Lpuart_TC_FCT_0002 Observed behavior: Baudrate calculator incorrect Expected behavior: Baudrate calculator correct Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-8495	Bug	[PWM]: Correct and update Pwm driver for S32K1XX<*> Update Pwm driver for S32K1XX IPV FTM : Update the dithering is unavailable on the instance 0 in S32K1XX Flexio: Add Flexio_Pwm_Ip_GetPeriod() api Update the features are not supported for S32K1XX IPW Integrate Flexio in IPW S32K1XX Update the validation functions in IPW HLD Add the validation api to check the SetOutputToIdle is not supported in FLEXIO channel in S32K1XX Correct Pwm driver for S32K1XX Correct the resource for S32K1XX Correct the CT to align with EBT
ARTD-8546	Bug	[SPI][FLEXIO] flexio driver cannot work when using flexio_logic_channel 3 4 5 6<*> Detailed description (how to reproduce it): the flexio driver cannot work when using flexio_logic_channel 3 4 5 6 for spi, but it can work when using flexio_logic_channel 0 1 2 3. !image-2021-03-16-14-48-01-287.png! Preconditions: flexio is enabled. Test Case ID (internal TC that caught the defect) optional: Int_TC_FCT_0301 Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-8551	Bug	[RM] Should not be select Physical core when disable multicore on S32CT and EBT<*> Detailed description (how to reproduce it): 1. Should not be select Physical core when disable multicore on S32CT and EBT. Please check the attached file. 2. The Region number on S32CT should be configurable. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: Rm_TC_COT_0001 Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-8571	Bug	[MCU] Difference LABEL of nodes between S32CT and EB<*> Detailed description (how to reproduce it): Add MCU component on S32CT and EB Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: The description between S32CT and EB is the difference(see attached file) Expected behavior: Synchronize description between S32CT and EB Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A

ID	Subtype	Headline and Description
ARTD-8579	Bug	[MCL-LCU][Tresos] Should check lcuLogicInput_UsingSwOverride before generate SwSynMode, SwValue ,,"Detailed description (how to reproduce it): [Tresos] Should check lcuLogicInput_UsingSwOverride before generate SwSynMode, SwValue Observed behavior: When lcuLogicInput_UsingSwOverride = false*, SwSynMode, SwValue still generated the value which is configured by user. Expected behavior: When lcuLogicInput_UsingSwOverride = false*, SwSynMode, SwValue should be generated the default value: <code> / boolean SwSynMode / LCU_IP_SW_SYNC_IMMEDIATE,\n</code> <code> / uint8 SwValue / LCU_IP_SW_OVERRIDE_LOGIC_LOW,\n</code> Only When lcuLogicInput_UsingSwOverride = true*, SwSynMode, SwValue generate the value which is configured by user. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-8586	Bug	[ICU][S32K3XX] The ICU_GET_INPUT_LEVEL_API macro does not change according to the state of the button on the DS<*> Detailed description (how to reproduce it): The ICU_GET_INPUT_LEVEL_API macro does not change according to the state of the button on the DS. pls see attach file. Preconditions: Use DS3.4 project. Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: The ICU_GET_INPUT_LEVEL_API macro does not change according to the state of the button on the DS. pls see attach file. Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:

ID	Subtype	Headline and Description
ARTD-8590	Bug	[CAN] #include <stdint.h> in FlexCAN_Ip_HwAccess.h when CCOPT+=-DNO_STDINT_H<*> Detailed description (how to reproduce it): Build CAN_TS_WIR_100 with CCOPT+=-D*NO_STDINT_H* on ghs compiler Preconditions: ghs compiler Test Case ID (internal TC that caught the defect) optional: CAN_TS_WIR_100 with CCOPT+=-D*NO_STDINT_H is added to makefile Observed behavior: A build fail error: !image-2021-03-17-16-30-32-132.png! NOTE_*_: Inclusion should be investigated and being fixed if if is implemented in wrong way !image-2021-03-17-16-30-01-692.png! Proposed solution optional: [...]
ARTD-8591	Bug	[ICU][S32K3XX] Value 'true' is generated in DS project configuration<*> Detailed description (how to reproduce it): Still has the value 'true' in the generation file in DS. pls see attach file Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-8614	Bug	Lpi2c CT generated code error<*> Detailed description (how to reproduce it): in s32ds 3.4, configuration tool, add lpi2c module into the new project, update code. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: There are only two header files included in the generated file "Lpi2c_Ip_Cfg.h" #include "Mcal.h" #include "OsIf.h" Expected behavior: #include "Mcal.h" #include "OsIf.h" #include "Lpi2c_Ip_BOARD_InitPeripherals_PBcfg.h" Note:*_ Proposed solution optional: Add the line into "Lpi2c_Ip_Cfg.h" #include "Lpi2c_Ip_BOARD_InitPeripherals_PBcfg.h"
ARTD-8617	Bug	[GPT] Pit_Ip_StartChannel reading CVAL value while timer is disabled doesn't follow Reference Manual<*> Detailed description (how to reproduce it): In S32K3 RTD 0.8.1 GPT driver, these below piece of code in Pit_Ip_StartChannel: !image-2021-04-02-15-45-01-973.png! After writing to RTI_LDVAL, driver will wait for PIT to copy value configured in RTI_LDVAL to RTI_CVAL by polling RTI_CVAL in Pit_Ip_GetCounterValue(). However, in previous state, (Gpt_Init()), timer was disabled, and reading RTI_CVAL is not recommended due to the fact that RTI_CVAL will not return a correct value, as shown in S32K3 reference manual. Preconditions: Gpt_StartTimer() is called, channel PIT is used Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Driver is reading RTI_CVAL while timer is disabled, which is not recommended by RM. Expected behavior: Implementation follows with RM Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A

ID	Subtype	Headline and Description
ARTD-8625	New	New Feature [ADC] Extend resolution to allow reading 15b register value for similar format as DMA transferred data ,,"NewWorkDescription: Implement method for the user to get raw register value, instead of value calculated based on the resolution set in the configurator. This is necessary since DMA will bypass any resolution conversions that are done in the driver and the module will always write 15-bits to the data register. Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]"
ARTD-8636	Bug	[S32K3xx][RM] Cortex- M7_1 only supports on S32K32x<*> Detailed description (how to reproduce it): N/A Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: RM_TC_0010 Observed behavior: Cortex M7_1 only supports on S32K32x, so resource of S32K33x and S32K31x need to remove Cortex M7_1 Expected behavior: N/A Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A

ID	Subtype	Headline and Description
ARTD-8652	Bug	[S32G2XX][S32K344][S32K1XX][Example] OCU: Duplicate number of paragraphs in 'description.txt' file of some example project<*> Precondition:* Open S32SD3.4 update1 which installed package SW32_RTD_4.4_1.0.0_HF01_D2102_DS_Updatesite.zip! Step: 1.Import all example project for S32G: 2. Open description.txt then check content Observed behavior: Duplicate number of catalogue " 3.2 Compiling the application" and " 3.2 Running the application on the board" Wdg_Example_IPL_DS Wdg_Example_HLD_DS Uart_HLD_S32G_DS_Example Linflexd_Uart_Ip_S32G_DS Spi_IP_example_CT_S32G Spi_HLD_example_CT_S32G Qdec_Ip_example_DS Qdec_example_DS Port_example_DS Ocu_Ftm_example_DS Ocu_example_DS Ocotp_IP_Example Ocotp_AUTOSAR_Example Lin_example_IPV Lin_example_HLD Icu_Siul2_Wkpu_example Icu_Ftm_example Icu_ASR_example I2c_S32G274A_IP_DS I2c_S32G274A_HLD_DS Example_S32G2XX_DS_Qspi_Ip Example_S32G2XX_DS_Fls Fee_Example_S32G2 Eth_Example_DS_002 Eth_Example_DS_001 Example_S32G2XX_DS_Eep Dio_example_DS_S32G Hse_Ip_Read_Hse_Attr Hse_Ip_Aes_Enc_Async_Irq Crypto_Hash Crypto_Cmac_Gen_Ver Crypto_Aes_Enc_Dec FlexCAN_example_CT CAN_example_CT Adc_example_DS_IP Adc_example_DS Expected behavior: Number of catalogue is updated correctly

ID	Subtype	Headline and Description
ARTD-8648	Bug	[ADC] ADC_ReadGroup when called for group with DMA does not return result masked according to resolution<*> Detailed description (how to reproduce it): ADC_ReadGroup when called for group with DMA, does not return result masked according to resolution Instead returns result on 15bits Observed behavior: Result is returned on 15bits Expected behavior: Result is returned masked according to selected resolution Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update Adc_Ipw_MaskConvResult
ARTD-8646	Bug	[ADC] Fix VSMD error EcucSws_1008 for AdcChannelId node and update Adc channel names stated by RM or IOMUX<*> Detailed description (how to reproduce it): Add AdcChannelName which is an ENUMURATION node having value is channel name stated in RM or IOMUX sheet. Fix VSMD error EcucSws_1008 by changing the attribute of AdcChannelId node from ENUMURATION to INTEGER. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-8661	Bug	[ETH][S32CT] The value for .enableCtrl (in generated code) should be upper case<*> Detailed description (how to reproduce it): When CCOPT+=-DNO_STDINT_H is enabled, the tests failed due to .enableCtrl value (in Gmac_Ip_BOARD_InitPeripherals_PBcfg.c file) is lower case (false/true). Please check the attached file. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: Eth_TS_COT_001 Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-8680	Bug	[ADC] Build failed with ADC group software trigger, when no HW triggers configured ,,"Detailed description (how to reproduce it): Build failed with ADC group software trigger In EB tresos, create new project and add ADC module Configure a simple group with trigger source is software(please refer the xdm file in the attachment) Generate code Build project with GHS compiler => Error: S32K3XX/eclipse/plugins/Adc_TS_T40D34M9I0R0/include/Adc_Ipw_Types.h"", line 395: error #94: the size of an array must be greater than zero const uint8 au8HwTriggIndex[ADC_MAX_HARDWARE_TRIGGERS]; /**< Hardware trigger sources in configuration array / make: [Makefile:325: Adc.o] Error 1 Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: Build error with GHS compiler with ADC group software trigger Expected behavior: No error when compiling with ADC group software trigger Note: in the ""Expected behavior"" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-8710	Bug	[ICU] Align HLD and IPL for Signal Measurement and Timestamp<*> Detailed description (how to reproduce it): Align HLD and IPL for Signal Measurement and Timestamp. Allow HLD DMA only in HLD side to be configured and serviced. IPL DMA should be only on IPL side to be handled by user notification. Processing of Signal Measurement and Timestamp should be done on IPL level and use pointers to variables to get the results on HLD. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-8726	Bug	[LIN] a redundant pulse sent before sending break<*> Detailed description (how to reproduce it): A redundant pulse is sent before break field when using IPV FlexIO as the image attached Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-8749	Bug	[ICU] DMA notification handlers function is not generated in DS<*> Detailed description (how to reproduce it): DMA notification handlers function (IcuChannel_0_MclDmaTransferCompletionNotif) is not generated in DS. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-8841	New	New Feature [can] Remove TypeReferenceDef in .component ,,"All uses of TypeReferenceDef (i.e. element <reference></reference>) shall be removed in favor of the structure described in [this presentation| https://nxp1.sharepoint.com/sites/Zebra/_layouts/15/Doc.aspx? OR=teams&action=edit&sourcedoc=%7B28A51BA3-C452-40F5-ABB6- A6933671DCD3%7D]. In a nutshell, each TypeReferenceDef element shall be replaced with the referenced type."

ID	Subtype	Headline and Description
ARTD-8780	New	New Feature [BUILD_ENV] Update compiler options to enable hardware FPU, remove short-enums, optimize zero initializers" ,,"We need to update the list of compiler options and memmap implementation following the compiler options alignment accross sw products: use hard fp remove short-enums remove no_discard_zero_init Changes should be applied for all compilers Source: https://nxp1.sharepoint.com/:x:/s/Zebra/EU7fT8Ur1jZAsou6FoOO-3MBrWTd1WdnvcVdNuqwLzncxg?e=LvE8aL
ARTD-8795	Bug	[LIN][FLEXIO] - Lin bus is not idle after the transfer has completed successfully.<*> Detailed description (how to reproduce it): After the transfer is completed successfully the node state is not IDLE Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Flexio_Lin_Ip_GotoIdleState must be called after reporting via the callback that the transfer is completed without errors.
ARTD-8799	New	New Feature [SPI][FLEXIO] Improve configuration of hardware resources follow new mcl update. ,,"NewWorkDescription: Mcl will update to add one more pin selection in each flexio channel because SPI want to select PINs for both Shifter and Timer registers which were lock per Flexio channel. Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Mcl will update to add one more pin selection in each flexio channel because SPI want to select PINs for both Shifter and Timer registers which were lock per Flexio channel."

ID	Subtype	Headline and Description
ARTD-8801	Bug	[ADC] Adc_ValidateQueueNotFull is redundant with HW trigger groups<*> Detailed description (how to reproduce it): Hw queue is removed completely in ARTD-2316 then no need to check queue full for HW trigger groups. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Remove ADC_E_QUEUE_FULL_LIST input param when calling Adc_ValidateExtraParams in Adc_EnableHardwareTrigger and Adc_DisableHardwareTrigger
ARTD-8809	New	New Feature [MCL] TRGMUX multicore support ,,"NewWorkDescription: Add multicore support for TRGMUX IP. Requirement source: (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Add multicore support for TRGMUX IP in driver code EBT S32CT."
ARTD-8823	Bug	[S32K3][LIN-FLEXIO] Work only with channel 0 configured for Rx<*> Detailed description (how to reproduce it): When configured Rx channel different 0, LIN driver can not work Preconditions: configured Rx channel different 0 Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-8874	Bug	[S32XX][DIO] Not run test when write to Port K on S32R45<*> Detailed description (how to reproduce it): Execute(generate, build, run) Dio_TS_701 from repo test_dio When invoke Dio_MaskedWritePort() or Dio_WriteChannelGroup() with PortId=9 (port K) =>stop by hard fault When write value to Port 9 by MAF, Dio_ReadPort() is working incorrect: these two lines need to swap in Dio_ReadPort() PortLevel = (Dio_PortLevelType)(PortLevel & Dio_aAvailablePinsForRead[PortId]); PortLevel = (Dio_PortLevelType)(PortLevel & Dio_Ipw_ReverseBits(Dio_aAvailablePinsForRead[PortId])); Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: TS: Dio_TS_701 TC: Dio_TC_FCT_0214 Dio_TC_FCT_0205 Observed behavior: Test not run when write to Port K: Dio_TC_FCT_0214: line 181, using Dio_MaskedWritePort() with PortId=9 (port K) Dio_TC_FCT_0205: line 134, using Dio_WriteChannelGroup() with ChannelGroupIdPtr.port=9 (port K) Expected behavior: Write successfully, no error
ARTD-8890	Bug	[FLEXIO_Sent][CT] Wrong component name and duplicate component in Manager SDK Components tab<*> Detailed description (how to reproduce it): Step 1: Create new project. Step 2: Select project > right click > S32 Configuration tool > Manage SDK components Step 3: Check all components that there are no duplicate component name Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: Wrong component name and duplicate component in Manager SDK Components tab. Detail was attached. Expected behavior: Remove an instance and update the component's name from Flexio to Flexio_Sent*

ID	Subtype	Headline and Description
ARTD-8960	Bug	[MCU] FXOSC not stable when set GM_SEL = 0000b<*> Detailed description (how to reproduce it): The description of field GM_SEL have note: - In Crystal mode FXOSC will not function with zero transconductance (GM_SEL = 0000b). - For details on how to set this field, see Initializing FXOSC. But in configuration user can configure GM_SEL = 0000b in Crystal mode. that is root cause FXOSC not stable Preconditions: Crystal overdrive protection = 0 Test Case ID (internal TC that caught the defect) optional: 1001 Observed behavior: FXOSC not stable Expected behavior: FXOSC stable Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: In Crystal mode make an invalid in configuration when user configure Crystal overdrive protection (GM_SEL) = 0000b In Single-Input Bypass mode write 0000b to Crystal overdrive protection (GM_SEL)
ARTD-8963	Bug	[LIN] The requirement CPR_RTD_00311.lin is not covered<*> Detailed description (how to reproduce it): The requirement CPR_RTD_00311.lin is not covered by driver. "In order to provide support for importing configuration information from different formats (i.e. DBC, LDF, FIBEX, AUTOSAR system description ARXML), the so-called ComImporter shall be registered in the CAN/LIN/FlexRay/Eth driver module's plugin.xml file." Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: ComImporter is not registered in plugin.xml Expected behavior: ComImporter is registered in plugin.xml Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: PLG_USE_COMIMPORTER is set to true in Lin.mak

ID	Subtype	Headline and Description
ARTD-8961	Bug	[CAN][S32XX] Wrong HwObjectID in CanTxTimestampNotification() when using interrupt mode<*> Detailed description (how to reproduce it): Configure CAN as below: The first hw object is HRH, the second Hw object is HTH In case of Tx processing is set to Interrupt mode, the driver code always uses _Can_pHwObjectConfig_ ptr (this specifies the first HRH) to notify timestamp for the current transmission , so the timestamp notification is wrong for the hw transmit object. !image-2021-03-30-10-47-11-829.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-8964	Bug	[SENT] Checking invalid channel of sent HLD layer is incorrect<*> Detailed description (how to reproduce it): Using channelId is equal with number of sent channel as parameter of Sent_GetFastChannelMsgData and Sent_GetSerialChannelMsgData, driver should report DET error of invalid channel id but actually not. Preconditions: Using channelId is equal with number of sent channel as parameter of Sent_GetFastChannelMsgData and Sent_GetSerialChannelMsgData Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: Driver should report DET error of invalid channel Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Change this condition (u8ChannelId > SENT_NUMBER_CONFIGURED_CHANNELS) to (u8ChannelId >= SENT_NUMBER_CONFIGURED_CHANNELS) Tester should create a new testcase to cover this case

ID	Subtype	Headline and Description
ARTD-9016	New	New Feature [MCU] Support configuration for CMU on S32CT ,,"In the generated clock settings file ""Clock_Ip_PBcfg.c"", there is a huge structure ""Clock_Ip_ClockConfigType Mcu_aClockConfigPB[1]"". In this structure, there is one sub-structure called ""Clock_Ip_CmuConfigType"". There are 3 elements in this structure definition but there are 6 data provided in the generated code. So there is compiler warning ""../board/Clock_Ip_PBcfg.c:1568:21: warning: excess elements in struct initializer"" Can we fix this? And I didn't see any CMU related settings in the clock diagram view in S32DS CT. Is there plan to add CMU support in the RTD configuration?"
ARTD-9052	Bug	[icu] Fix all M4, TABs, duplicated UUIDs ,,"Coding convention implies that no TAB is to be used in the code source files we deliver. (to avoid inconsistent displays of code alignment if TAB size is defined differently) Replace all duplicated UUIDs, to avoid generation crashes on customer side. Proposed solution: # Replace all TABs with 4 spaces. # Update your text editor settings to always use 4 spaces instead of a TAB # Replace duplicated UUIDs. # Fix all violation that reports at PluginsCheck report: [http://kara.ea.freescale.net/0/project/custom_plugincheck/details http://adriatic.ea.freescale.net/1/project/custom_plugincheck/details] Refer attachment for 2021.03.31 baseline.
ARTD-9034	New	New Feature [ADC] Updates for ctu hardware trigger optimization ,,"NewWorkDescription: The feature should be updated for K3 release because it was partially updated in ARTD-1434 Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]"

ID	Subtype	Headline and Description
ARTD-9136	Bug	[crypto] Fix file version checking<*> Detailed description (how to reproduce it): Fix all violation version checking Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: [...] Expected behavior: No file version checking errors. Please ensure all violations fix for your driver, reference link: [http://kara.ea.freescale.net/0/project/custom_file_verchecking/details] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...] - NewWorkDescription: Fix all file version checking for RTD drivers Requirement source: Attachment baseline report on 2021.04.01 Proposed solution optional: [...]
ARTD-9131	Bug	[ADC] DMA group with limit check enabled, still get status stream complete with out of range voltage ,,"Detailed description (how to reproduce it): DMA hw trigger group with out of range voltage still get status stream complete Preconditions: Dma hw trigger group config with AN_2: Range between 1000 and 3000 Voltage for AN_2: 1.8V (4095) Transfer by DMA with interrupt Test Case ID (internal TC that caught the defect) optional: Adc_TC_FCT_1401 Observed behavior: Set voltage to AN_2: 1.8V Enable hw trigger group and trigger Wait status as stream complete Expected: Timeout occurred Real status: time out was not reached and group status is stream complete Expected behavior: Group can not get status as stream complete because out of range voltage Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA

ID	Subtype	Headline and Description
ARTD-9201	Bug	s32k3 QSPI pin direction type<*> Detailed description (how to reproduce it): QSPI IO0 IO3 shoud be configuread as input/output for its direction property. Observed behavior: QSPI IO0 IO3 can be configured in S32DS CT as either input or output. But they cannot be configured as input/output. Proposed solution optional: It would be good that these pins can be configured as input/output and it would be good to add an "input/output" option in the attached dialog box.
ARTD-9208	Bug	[ADC] DMA HW trigger single one shot normal group with only 1 channel and with interrupt, is not working ,,"Detailed description (how to reproduce it): DMA HW trigger single one shot normal group transfer wrong place in data buffer Preconditions: Using DMA HW trigger one shot normal group Group have 1 channel Optimize streaming reorder off without interrupt = off Test Case ID (internal TC that caught the defect) optional: Adc_TC_FCT_0102 Adc_TC_FCT_0107 Adc_TC_FCT_0109 (Adc_TS_014 cfg 3) Observed behavior: Enable hw trigger dma 1 channel group Loop to trigger 3 times Read group in each trigger Status: Read group buffer did not update after 3 triggers Result buffer data have 3 elements after 3 triggers Expected behavior: Read group buffer update after 3 triggers Result buffer data have 1 elements after 3 triggers Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA

ID	Subtype	Headline and Description
ARTD-9209	New	New Feature [adc] [S32CT] Implement EPD/EPC support for HLD and IPL S32K3 ,,"Implement EPD/EPC support for HLD and IPLD. Please refer to [this post on Teams https://teams.microsoft.com/l/message/19:e451c595d3ba410c8f9c1f5efc19a8a3@thread.tacv2/1606904026692?tenantId=686ea1d3-bc2b-4c6f-a92c-d99c5c301635&groupId=f9decd68-7b74-4101-a4d2-ad54e86f727f&parentMessageId=1606904026692&teamName=Zebra&channelName=Configuration%20(code%2C%20DS%2C%20EB%2C%20etc)&createdTime=1606904026692] for additional details. From the presentation, the main focus should be on the following sections: Mapping XDM to Component EPD Importer EPD Generation EPC Importer EPC Generation "
ARTD-9210	Bug	ADC] CT ADC_SAR_IP missing the generated struct for ADC1<*> Detailed description (how to reproduce it): In CT, create the configuration for ADC0 and ADC1 then generate code => Missing the struct configuration for Adc_sar_1 !image-2021-02-26-15-37-57-027.png! Test Case ID (internal TC that caught the defect) optional: Adc_sar_TC_FCT_0001 Observed behavior: Missing the struct configuration for Adc_sar_1 Expected behavior: Can generate the struct configuration for Adc_sar_1 Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA

ID	Subtype	Headline and Description
ARTD-9211	Bug	[Platform][S32CC] S32CT generate redundancy Platform_Ipw_NonCoreConfigType structs when dissable S32K3XX_MSCM_CFG<*> Detailed description (how to reproduce it): 1. Creating new project for Platform on S32CT, add Platform, Ecuc, Os component to project. 2. Generate code with default config (*dissable generic interrupt settings configurable). 3. Opening Platform_Ipw_Cfg.c , Platform_Ipw_NonCoreConfigType structs is redundancy, Because When MSCM dissable Platform_Init not Initializes Platform_Ipw_InitNonCore. Opening IntCtrl_Ip_Cfg.c IntCtrl_Ip_GlobalRouteConfigType structs is redundancy. 4. Compare config generate CT and EB is different with config dissable MSCM. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: !image-2021-04-02-16-05-42-884.png! !image-2021-04-02-16-06-13-135.png! !image-2021-04-02-17-13-41-755.png! Expected behavior: Remove Platform_Ipw_NonCoreConfigType structs if dissable MSCM on S32CT const Platform_Ipw_NonCoreConfigType ipwNonCoreConfig = { NULL_PTR } ; In IntCtrl_Ip_Cfg.c : Remove IntCtrl_Ip_GlobalRouteConfigType structs and IntCtrl_Ip_IrqRouteConfigType structs Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-9204	Bug	CLONE - [SPI][FLEXIO] Shifter error flag set after latest frame is sent in slave mode<*> Shifter error flag set after latest frame is sent in slave mode. Currently, driver have added a workaround to prevent this issue. So it should be investigated to get the root cause of issue

ID	Subtype	Headline and Description
ARTD-9225	Bug	[ADC] Error appears in S32ConfigurationTool when AdcEnableThresholds is checked on a channel but AdcEnableWatchdogApi is disabled<*> Detailed description (how to reproduce it): 1. Create a DS project 2. Add Adc component 3. Enable AdcEnableWatchdogApi 4. Enable AdcEnableThresholds on any channel on any hardware unit 5. Disable AdcEnableWatchdogApi Observed behavior: This error is shown: "This Unit has configured some Channels that have enabled the watchdog feature and need to use interrupts, so the associated Watchdog interrupt must be enabled in Adc/AdcInterrupts container." Expected behavior: No error should be shown. Proposed solution optional: Whenever AdcEnableThresholds value is checked, it's enable state must also be checked.
ARTD-9226	New	New Feature [ADC] ADC_SAR IPL add support in configurator for ADC DMAEN and DMAR ,,"NewWorkDescription: ADC_SAR IPL add support in configurator for ADC DMAEN and DMAR Currently ADC SAR IP has support for updating DMAEN and DMAR only at runtime via dedicated functions. Support needs to be added also in configurator Requirement source: Improvement Proposed solution optional: Add checkbox in AdcHwUnit container: Enable DMA for End of Channel. If chain interrupts do not work in parallel with DMAEN true, then consider instead of checkbox, to add Adc Transfer Type enum ADC_INTERRUPT/ADC_DMA as in HLD (to make DMA vs INTERRUPT mutual exclusive) Add checkbox in channel configurator: End of conversion DMA enable. Update Adc_Sar_Ip_Init function "

ID	Subtype	Headline and Description
ARTD-9227	Bug	[ADC] DMA Clear Source cannot be configured in low-level driver configurator<*> Detailed description (how to reproduce it): DMA Clear Source cannot be configured in IPL configurator Adc Transfer Type is always ADC_INTERRUPT for ADC Unit, so DMA Clear Source is always disabled Preconditions: N.A. Test Case ID (internal TC that caught the defect) optional: N.A. Observed behavior: DMA Clear Source cannot be configured in IPL configurator Expected behavior: DMA Clear Source can be configured in IPL configurator Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: DMA Clear Source must always be configurable, Remove also Adc Transfer Type from IPL configurator, because it is not used, and Adc Sar Ip driver currently only offers support to configure DMAEN and DMAR using runtime functions. When ARTD-9226 is implemented, DMA Clear Source will become read-only when DMA is disabled.
ARTD-9233	New	New Feature [FLS] Support configuration of PFCR4[BLK4_PS] bitfield for C40 ,,"NewWorkDescription: Add support for the PFCR4[BLK4_PS] bitfields to allow the user to select the pipe to be used for accessing the flash block 4. !image-2021-04-04-15-03-19-551.png|thumbnail! Requirement source: S32K3xx_RM_Rev2DraftB.pdf (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Add list to select"
ARTD-9231	Bug	[ICU] Code generator of ICU_GET_INPUT_LEVEL_API incorrect<*> Detailed description (how to reproduce it): Logic S32CT code generation of macro ICU_GET_INPUT_LEVEL_API is wrong. When comparing to S32CT code generation EMIOS_ICU_GET_INPUT_LEVEL_API Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: !image-2021-04-03-21-04-39-946.png! !image-2021-04-03-21-05-48-189.png! Expected behavior: !image-2021-04-03-21-06-17-434.png! Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-9315	Bug	[ADC] Build fail: "DMA_LOGIC_CH_0_NOF_CFG_SGA_ELEMENTS" is undefined when using adc group with 1 channel, without scatter gather ,,"Detailed description (how to reproduce it): Build fail: ""DMA_LOGIC_CH_0_NOF_CFG_SGA_ELEMENTS"" is undefined when using adc group with 1 channel, without scatter gather Preconditions: Adc 0 using transfer type ADC_DMA and groups have only 1 channel Disable dmaLogicChannel_EnableScatterGather on mcl driver Test Case ID (internal TC that caught the defect) optional: Adc_TC_FCT_0101 Observed behavior: Build fail error: e:/gitwork_rt/output/S32XX_S32G2XX/adc/Adc_TS_014_cfg3_CORE4/generate_tresos/src/Adc_Ipw_VS_0_PBcfg.c"", line 270: error #20: identifier ""DMA_LOGIC_CH_0_NOF_CFG_SGA_ELEMENTS"" is undefined .au32DmaNumSgaElement = { DMA_LOGIC_CH_0_NOF_CFG_SGA_ELEMENTS, DMA_LOGIC_CH_1_NOF_CFG_SGA_ELEMENTS }, Expected behavior: Build done Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A

ID	Subtype	Headline and Description

ARTD-9415	New	New Feature
		
		[adc] Updated module to fully support CPR_RTD_00563
		,,"NewWorkDescription:
		Implement requirement:
		CPR_RTD_00563: If the parameter checking for the Initialization function is enabled, the Configuration pointer argument shall be checked with the following conditions:
		In the supportedConfigVariants VariantPreCompile and VariantLinkTime if only one configuration variant set is used, the initialization function does not need nor evaluate the passed argument. Thus the Configuration pointer shall have a NULL_PTR value.
		In the supportedConfigVariant VariantPostBuild or if multiple configuration variant sets are used, the initialization function requires the passed argument. Thus the Configuration pointer shall be different from NULL_PTR.
		If these conditions are not satisfied, a Development error with type <MIP>_E_INIT_FAILED shall be reported to Default Error Tracer (Det)
		Requirement source:
		AUTOSAR_SRS_BSWGeneral
		(e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...)
		Proposed solution optional:
		Generate the defined <MIP>_PRECOMPILE_SUPPORT in <Driver>_Cfg.h
		EBT Tresos:
		{code:c}
		#define <MIP>_PRECOMPILE_SUPPORT [!IF ""(IMPLEMENTATION_CONFIG_VARIANT != 'VariantPostBuild') and (variant:size() <= 1)""!](STD_ON)[!ELSE!](STD_OFF)[!ENDIF!]
		UCT:
		{code:c}
		[!
		var configSet = this[0];
		var functionalGroupsList = this[2];
		var implementationConfigVariant = configSet.getChildById(""ConfigTimeSupport.IMPLEMENTATION_CONFIG_VARIANT"").getValue();
		!]
		...
		#define <MIP>_PRECOMPILE_SUPPORT ($((implementationConfigVariant != ""VARIANT-POST-BUILD"") && (functionalGroupsList.length <= 1))? ""STD_ON"" : ""STD_OFF""$)
		In <Driver>.c the code that contained parameter checking for init function shall be:
		{code:c}
		#if (STD_ON == <MIP>_PRECOMPILE_SUPPORT)
		if (NULL_PTR != pConfigPtr)
		#else
		if (NULL_PTR == pConfigPtr)
		#endif / <MIP>_PRECOMPILE_SUPPORT /
		Note:
		The Module implementation prefix <Mip> shall be formed in the following way: <Ma>[_<vi>_<ai>] Where <Ma> is the Module abbreviation of the BSW Module (SWS_BSW_00101), <vi> is its vendorId and <ai> is its vendorApiInfix. The sub part in square brackets [_<vi>_<ai>] is omitted if no vendorApiInfix is defined for the BSW Module. For Complex Drivers and transformers, the <Mip> is directly derived from the apiServicePrefix.
		The Capitalized module implementation prefix <MIP> is the Module implementation prefix completely written in upper case.
		
		The requirement was already partially supported by ADC module, only update required to fully support this requirement is to update the way ADC_PRECOMPILE_SUPPORT is generated. Instead of it being generated only when precompile support is enabled, it will be always generated and will have STD_ON value when precompile support is enabled and STD_OFF when precompile support is disabled. The other change needed will be to update Adc_Init to throw {{ADC_E_PARAM_POINTER}} error instead of
		{ADC_E_PARAM_CONFIG}} when the wrong config parameter is given."

ID	Subtype	Headline and Description

ARTD-9430	New	New Feature
		
		[lin] Implement CPR_RTD_00563 to allow NULL_PTR at Init at precompile
		,,"NewWorkDescription:
		Implement requirement:
		CPR_RTD_00563: If the parameter checking for the Initialization function is enabled, the Configuration pointer argument shall be checked with the following conditions:
		In the supportedConfigVariants VariantPreCompile and VariantLinkTime if only one configuration variant set is used, the initialization function does not need nor evaluate the passed argument. Thus the Configuration pointer shall have a NULL_PTR value.
		In the supportedConfigVariant VariantPostBuild or if multiple configuration variant sets are used, the initialization function requires the passed argument. Thus the Configuration pointer shall be different from NULL_PTR.
		If these conditions are not satisfied, a Development error with type <MIP>_E_INIT_FAILED shall be reported to Default Error Tracer (Det)
		Requirement source:
		AUTOSAR_SRS_BSWGeneral
		(e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...)
		Proposed solution optional:
		Generate the defined <MIP>_PRECOMPILE_SUPPORT in <Driver>_Cfg.h
		EBT Tresos:
		{code:c}
		#define <MIP>_PRECOMPILE_SUPPORT [!IF ""(IMPLEMENTATION_CONFIG_VARIANT != 'VariantPostBuild') and (variant:size() <= 1)""!](STD_ON)[!ELSE!](STD_OFF)[!ENDIF!]
		UCT:
		{code:c}
		[!
		var configSet = this[0];
		var functionalGroupsList = this[2];
		var implementationConfigVariant = configSet.getChildById(""ConfigTimeSupport.IMPLEMENTATION_CONFIG_VARIANT"").getValue();
		!]
		...
		#define <MIP>_PRECOMPILE_SUPPORT ($((implementationConfigVariant != ""VARIANT-POST-BUILD"") && (functionalGroupsList.length <= 1))? ""STD_ON"" : ""STD_OFF""$)
		In <Driver>.c the code that contained parameter checking for init function shall be:
		{code:c}
		#if (STD_ON == <MIP>_PRECOMPILE_SUPPORT)
		if (NULL_PTR != pConfigPtr)
		#else
		if (NULL_PTR == pConfigPtr)
		#endif / <MIP>_PRECOMPILE_SUPPORT /
		Note:
		The Module implementation prefix <Mip> shall be formed in the following way: <Ma>[_<vi>_<ai>] Where <Ma> is the Module abbreviation of the BSW Module (SWS_BSW_00101), <vi> is its vendorId and <ai> is its vendorApiInfix. The sub part in square brackets [_<vi>_<ai>] is omitted if no vendorApiInfix is defined for the BSW Module. For Complex Drivers and transformers, the <Mip> is directly derived from the apiServicePrefix.
		The Capitalized module implementation prefix <MIP> is the Module implementation prefix completely written in upper case.
		"

ID	Subtype	Headline and Description

ARTD-9436	New	New Feature
		
		[port] Implement CPR_RTD_00563 to allow NULL_PTR at Init at precompile
		,,"NewWorkDescription:
		Implement requirement:
		CPR_RTD_00563: If the parameter checking for the Initialization function is enabled, the Configuration pointer argument shall be checked with the following conditions:
		In the supportedConfigVariants VariantPreCompile and VariantLinkTime if only one configuration variant set is used, the initialization function does not need nor evaluate the passed argument. Thus the Configuration pointer shall have a NULL_PTR value.
		In the supportedConfigVariant VariantPostBuild or if multiple configuration variant sets are used, the initialization function requires the passed argument. Thus the Configuration pointer shall be different from NULL_PTR.
		If these conditions are not satisfied, a Development error with type <MIP>_E_INIT_FAILED shall be reported to Default Error Tracer (Det)
		Requirement source:
		AUTOSAR_SRS_BSWGeneral
		(e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...)
		Proposed solution optional:
		Generate the defined <MIP>_PRECOMPILE_SUPPORT in <Driver>_Cfg.h
		EBT Tresos:
		{code:c}
		#define <MIP>_PRECOMPILE_SUPPORT [!IF ""(IMPLEMENTATION_CONFIG_VARIANT != 'VariantPostBuild') and (variant:size() <= 1)""!](STD_ON)[!ELSE!](STD_OFF)[!ENDIF!]
		UCT:
		{code:c}
		[!
		var configSet = this[0];
		var functionalGroupsList = this[2];
		var implementationConfigVariant = configSet.getChildById(""ConfigTimeSupport.IMPLEMENTATION_CONFIG_VARIANT"").getValue();
		!]
		...
		#define <MIP>_PRECOMPILE_SUPPORT ($((implementationConfigVariant != ""VARIANT-POST-BUILD"") && (functionalGroupsList.length <= 1))? ""STD_ON"" : ""STD_OFF""$)
		In <Driver>.c the code that contained parameter checking for init function shall be:
		{code:c}
		#if (STD_ON == <MIP>_PRECOMPILE_SUPPORT)
		if (NULL_PTR != pConfigPtr)
		#else
		if (NULL_PTR == pConfigPtr)
		#endif / <MIP>_PRECOMPILE_SUPPORT /
		Note:
		The Module implementation prefix <Mip> shall be formed in the following way: <Ma>[_<vi>_<ai>] Where <Ma> is the Module abbreviation of the BSW Module (SWS_BSW_00101), <vi> is its vendorId and <ai> is its vendorApiInfix. The sub part in square brackets [_<vi>_<ai>] is omitted if no vendorApiInfix is defined for the BSW Module. For Complex Drivers and transformers, the <Mip> is directly derived from the apiServicePrefix.
		The Capitalized module implementation prefix <MIP> is the Module implementation prefix completely written in upper case.
		"

ID	Subtype	Headline and Description

ARTD-9437	New	New Feature
		
		[pwm] Implement CPR_RTD_00563 to allow NULL_PTR at Init at precompile
		,,"NewWorkDescription:
		Implement requirement:
		CPR_RTD_00563: If the parameter checking for the Initialization function is enabled, the Configuration pointer argument shall be checked with the following conditions:
		In the supportedConfigVariants VariantPreCompile and VariantLinkTime if only one configuration variant set is used, the initialization function does not need nor evaluate the passed argument. Thus the Configuration pointer shall have a NULL_PTR value.
		In the supportedConfigVariant VariantPostBuild or if multiple configuration variant sets are used, the initialization function requires the passed argument. Thus the Configuration pointer shall be different from NULL_PTR.
		If these conditions are not satisfied, a Development error with type <MIP>_E_INIT_FAILED shall be reported to Default Error Tracer (Det)
		Requirement source:
		AUTOSAR_SRS_BSWGeneral
		(e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...)
		Proposed solution optional:
		Generate the defined <MIP>_PRECOMPILE_SUPPORT in <Driver>_Cfg.h
		EBT Tresos:
		{code:c}
		#define <MIP>_PRECOMPILE_SUPPORT [!IF ""(IMPLEMENTATION_CONFIG_VARIANT != 'VariantPostBuild') and (variant:size() <= 1)""!](STD_ON)[!ELSE!](STD_OFF)[!ENDIF!]
		UCT:
		{code:c}
		[!
		var configSet = this[0];
		var functionalGroupsList = this[2];
		var implementationConfigVariant = configSet.getChildById(""ConfigTimeSupport.IMPLEMENTATION_CONFIG_VARIANT"").getValue();
		!]
		...
		#define <MIP>_PRECOMPILE_SUPPORT ($((implementationConfigVariant != ""VARIANT-POST-BUILD"") && (functionalGroupsList.length <= 1))? ""STD_ON"" : ""STD_OFF""$)
		In <Driver>.c the code that contained parameter checking for init function shall be:
		{code:c}
		#if (STD_ON == <MIP>_PRECOMPILE_SUPPORT)
		if (NULL_PTR != pConfigPtr)
		#else
		if (NULL_PTR == pConfigPtr)
		#endif / <MIP>_PRECOMPILE_SUPPORT /
		Note:
		The Module implementation prefix <Mip> shall be formed in the following way: <Ma>[_<vi>_<ai>] Where <Ma> is the Module abbreviation of the BSW Module (SWS_BSW_00101), <vi> is its vendorId and <ai> is its vendorApiInfix. The sub part in square brackets [_<vi>_<ai>] is omitted if no vendorApiInfix is defined for the BSW Module. For Complex Drivers and transformers, the <Mip> is directly derived from the apiServicePrefix.
		The Capitalized module implementation prefix <MIP> is the Module implementation prefix completely written in upper case.
		"

ID	Subtype	Headline and Description

ARTD-9440	New	New Feature
		
		[sai] Implement CPR_RTD_00563 to allow NULL_PTR at Init at precompile
		,,"NewWorkDescription:
		Implement requirement:
		CPR_RTD_00563: If the parameter checking for the Initialization function is enabled, the Configuration pointer argument shall be checked with the following conditions:
		In the supportedConfigVariants VariantPreCompile and VariantLinkTime if only one configuration variant set is used, the initialization function does not need nor evaluate the passed argument. Thus the Configuration pointer shall have a NULL_PTR value.
		In the supportedConfigVariant VariantPostBuild or if multiple configuration variant sets are used, the initialization function requires the passed argument. Thus the Configuration pointer shall be different from NULL_PTR.
		If these conditions are not satisfied, a Development error with type <MIP>_E_INIT_FAILED shall be reported to Default Error Tracer (Det)
		Requirement source:
		AUTOSAR_SRS_BSWGeneral
		(e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...)
		Proposed solution optional:
		Generate the defined <MIP>_PRECOMPILE_SUPPORT in <Driver>_Cfg.h
		EBT Tresos:
		{code:c}
		#define <MIP>_PRECOMPILE_SUPPORT [!IF ""(IMPLEMENTATION_CONFIG_VARIANT != 'VariantPostBuild') and (variant:size() <= 1)""!](STD_ON)[!ELSE!](STD_OFF)[!ENDIF!]
		UCT:
		{code:c}
		[!
		var configSet = this[0];
		var functionalGroupsList = this[2];
		var implementationConfigVariant = configSet.getChildById(""ConfigTimeSupport.IMPLEMENTATION_CONFIG_VARIANT"").getValue();
		!]
		...
		#define <MIP>_PRECOMPILE_SUPPORT ($((implementationConfigVariant != ""VARIANT-POST-BUILD"") && (functionalGroupsList.length <= 1))? ""STD_ON"" : ""STD_OFF""$)
		In <Driver>.c the code that contained parameter checking for init function shall be:
		{code:c}
		#if (STD_ON == <MIP>_PRECOMPILE_SUPPORT)
		if (NULL_PTR != pConfigPtr)
		#else
		if (NULL_PTR == pConfigPtr)
		#endif / <MIP>_PRECOMPILE_SUPPORT /
		Note:
		The Module implementation prefix <Mip> shall be formed in the following way: <Ma>[_<vi>_<ai>] Where <Ma> is the Module abbreviation of the BSW Module (SWS_BSW_00101), <vi> is its vendorId and <ai> is its vendorApiInfix. The sub part in square brackets [_<vi>_<ai>] is omitted if no vendorApiInfix is defined for the BSW Module. For Complex Drivers and transformers, the <Mip> is directly derived from the apiServicePrefix.
		The Capitalized module implementation prefix <MIP> is the Module implementation prefix completely written in upper case.
		"

ID	Subtype	Headline and Description

ARTD-9441	New	New Feature
		
		[sent] Implement CPR_RTD_00563 to allow NULL_PTR at Init at precompile
		,,"NewWorkDescription:
		Implement requirement:
		CPR_RTD_00563: If the parameter checking for the Initialization function is enabled, the Configuration pointer argument shall be checked with the following conditions:
		In the supportedConfigVariants VariantPreCompile and VariantLinkTime if only one configuration variant set is used, the initialization function does not need nor evaluate the passed argument. Thus the Configuration pointer shall have a NULL_PTR value.
		In the supportedConfigVariant VariantPostBuild or if multiple configuration variant sets are used, the initialization function requires the passed argument. Thus the Configuration pointer shall be different from NULL_PTR.
		If these conditions are not satisfied, a Development error with type <MIP>_E_INIT_FAILED shall be reported to Default Error Tracer (Det)
		Requirement source:
		AUTOSAR_SRS_BSWGeneral
		(e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...)
		Proposed solution optional:
		Generate the defined <MIP>_PRECOMPILE_SUPPORT in <Driver>_Cfg.h
		EBT Tresos:
		{code:c}
		#define <MIP>_PRECOMPILE_SUPPORT [!IF ""(IMPLEMENTATION_CONFIG_VARIANT != 'VariantPostBuild') and (variant:size() <= 1)""!](STD_ON)[!ELSE!](STD_OFF)[!ENDIF!]
		UCT:
		{code:c}
		[!
		var configSet = this[0];
		var functionalGroupsList = this[2];
		var implementationConfigVariant = configSet.getChildById(""ConfigTimeSupport.IMPLEMENTATION_CONFIG_VARIANT"").getValue();
		!]
		...
		#define <MIP>_PRECOMPILE_SUPPORT ($((implementationConfigVariant != ""VARIANT-POST-BUILD"") && (functionalGroupsList.length <= 1))? ""STD_ON"" : ""STD_OFF""$)
		In <Driver>.c the code that contained parameter checking for init function shall be:
		{code:c}
		#if (STD_ON == <MIP>_PRECOMPILE_SUPPORT)
		if (NULL_PTR != pConfigPtr)
		#else
		if (NULL_PTR == pConfigPtr)
		#endif / <MIP>_PRECOMPILE_SUPPORT /
		Note:
		The Module implementation prefix <Mip> shall be formed in the following way: <Ma>[_<vi>_<ai>] Where <Ma> is the Module abbreviation of the BSW Module (SWS_BSW_00101), <vi> is its vendorId and <ai> is its vendorApiInfix. The sub part in square brackets [_<vi>_<ai>] is omitted if no vendorApiInfix is defined for the BSW Module. For Complex Drivers and transformers, the <Mip> is directly derived from the apiServicePrefix.
		The Capitalized module implementation prefix <MIP> is the Module implementation prefix completely written in upper case.
		"

ID	Subtype	Headline and Description
ARTD-9345	Bug	[CRC] When Dma Feature is enable, need to check that CrcDmaLogicChannelName is assigned value or not ,,"Preconditions: DMA feature is enable User did not configure dma channel Observed behavior: When generate code, user get an error without any guideline to fix it Expected behavior: Need to check that CrcDmaLogicChannelName is assigned value or not. If not, need to show: why user get the error how to fix it Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-9346	Bug	[S32CC][CRC] When multi cores enable, CrcPartitionRefOfChannel must be assigned. ,,"Preconditions: Step 1: Enable Multi cores feature Step 2: Add a Partition for CrcEcucPartitionRef Step 3: Add 2 configuration for Crc Channels Configuration Step 4: Only configure CrcPartitionRefOfChannel for 1st channel Observed behavior: Although 2nd channel was not configured CrcPartitionRefOfChannel But Configurator still generate configuration file successfully without error or generate an error without guideline for user about this issue (why issue happen, how to fix it) Expected behavior: Need to raise error this case
ARTD-9359	Bug	S32K3 CLKOUT_RUN is not mapped to PINs configuration<*> Detailed description (how to reproduce it): When configuring the pins, we found that CLKOUT_RUN and CLKOUT_STANDBY are not mapped to the desired pins. For example, PTD14, ALT7 function should be CLKOUT_RUN. But it's not present in PTD14 function options in the pins configuration tool. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: N/A Expected behavior: N/A

ID	Subtype	Headline and Description
ARTD-9398	Bug	[ADC] Wrong generated code for 'presampling internal voltage' when 'AdcBypassSampling' is 'false'<*> Detailed description (how to reproduce it): [ADC] Wrong generated code for 'presampling internal voltage' when 'AdcBypassSampling' is 'false' In EBT, Disable AdcBypassSampling Select AdcPresamplingInternalSignal0 is VREFH Select AdcPresamplingInternalSignal1 is VREFH Click generate code Verification Point: the presampling voltage is VREFH => FAILED The generated code is .aPresamplingSource = { ADC_SAR_IP_PRESAMPLE_VREFL, ADC_SAR_IP_PRESAMPLE_VREFL } The issue also occurs on S32CT. !image-2021-04-07-18-28-52-920.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description

ARTD-9456	New	New Feature
		
		[fls] Include the platform in a single point based on generated data
		,,"Generate the platform header include based on generated data. This way the platform name and specifics are centralized in one point only and to avoid using the compiler option define which is subject to change due to objective reasons.
		The proposal is to use a generated header file like: <Ip>_Ip_CfgDefines.h and centralize all platform header includes in it.
		Example for EB Tresos generator:
		[!NOCODE![!// Include specific header file
		[!IF ""node:exists(as:modconf(""Resource"")[1]/ResourceGeneral/ ResourceSubderivative)""![!//
		[!IF ""contains(as:modconf(""Resource"")[1]/ResourceGeneral/ResourceSubderivative, 's32k3')""![!//
		[!CODE![!WS ""0""!]#include ""S32K344_PIT.h""[!CR![!ENDCODE![!//
		[!ELSEIF ""contains(as:modconf(""Resource"")[1]/ResourceGeneral/ ResourceSubderivative, 's32g2')""![!//
		[!CODE![!WS ""0""!]#include ""S32G274A_PIT.h""[!CR![!ENDCODE![!//
		[!ELSEIF ""contains(as:modconf(""Resource"")[1]/ResourceGeneral/ ResourceSubderivative, 's32r45')""![!//
		[!CODE![!WS ""0""!]#include ""S32R45_PIT.h""[!CR![!ENDCODE![!//
		[!ENDIF![!//
		[!ENDIF![!//
		[!ENDNOCODE![!//
		Example for UCT as generator:
		[!
		if (scriptApi.getProfile().getMcuInfo().getPartNumber().contains(""S32K3""))
		{
		<code>#include ""S32K344_PIT.h""\n</code>
		} else if (scriptApi.getProfile().getMcuInfo().getPartNumber().contains(""S32G2""))
		{
		<code>#include ""S32G274A_PIT.h""\n</code>
		} else if (scriptApi.getProfile().getMcuInfo().getPartNumber().contains(""S32R45""))
		{
		<code>#include ""S32R45_PIT.h""\n</code>
		}
		!]
		"

ID	Subtype	Headline and Description

ARTD-9458	New	New Feature
		
		[gpt] Include the platform in a single point based on generated data
		,,"Generate the platform header include based on generated data. This way the platform name and specifics are centralized in one point only and to avoid using the compiler option define which is subject to change due to objective reasons.
		The proposal is to use a generated header file like: <lp>_lp_CfgDefines.h and centralize all platform header includes in it.
		Example for EB Tresos generator:
		[!NOCODE![!// Include specific header file
		[!IF ""node:exists(as:modconf(""Resource"")[1]/ResourceGeneral/ ResourceSubderivative)""![!//
		[!IF ""contains(as:modconf(""Resource"")[1]/ResourceGeneral/ResourceSubderivative, 's32k3')""![!//
		[!CODE![!WS ""0""!]#include ""S32K344_PIT.h""[!CR![!ENDCODE![!//
		[!ELSEIF ""contains(as:modconf(""Resource"")[1]/ResourceGeneral/ ResourceSubderivative, 's32g2')""![!//
		[!CODE![!WS ""0""!]#include ""S32G274A_PIT.h""[!CR![!ENDCODE![!//
		[!ELSEIF ""contains(as:modconf(""Resource"")[1]/ResourceGeneral/ ResourceSubderivative, 's32r45')""![!//
		[!CODE![!WS ""0""!]#include ""S32R45_PIT.h""[!CR![!ENDCODE![!//
		[!ENDIF![!//
		[!ENDIF![!//
		[!ENDNOCODE![!//
		Example for UCT as generator:
		[!
		if (scriptApi.getProfile().getMcuInfo().getPartNumber().contains(""S32K3""))
		{
		<code>#include ""S32K344_PIT.h""\n</code>
		} else if (scriptApi.getProfile().getMcuInfo().getPartNumber().contains(""S32G2""))
		{
		<code>#include ""S32G274A_PIT.h""\n</code>
		} else if (scriptApi.getProfile().getMcuInfo().getPartNumber().contains(""S32R45""))
		{
		<code>#include ""S32R45_PIT.h""\n</code>
		}
		!]
		"

ID	Subtype	Headline and Description

ARTD-9460	New	New Feature
		
		[icu] Include the platform in a single point based on generated data
		,,"Generate the platform header include based on generated data. This way the platform name and specifics are centralized in one point only and to avoid using the compiler option define which is subject to change due to objective reasons.
		The proposal is to use a generated header file like: <Ip>_Ip_CfgDefines.h and centralize all platform header includes in it.
		Example for EB Tresos generator:
		[!NOCODE![!// Include specific header file
		[!IF ""node:exists(as:modconf(""Resource"")[1]/ResourceGeneral/ ResourceSubderivative)""![!//
		[!IF ""contains(as:modconf(""Resource"")[1]/ResourceGeneral/ResourceSubderivative, 's32k3')""![!//
		[!CODE![!WS ""0""!]#include ""S32K344_PIT.h""[!CR![!ENDCODE![!//
		[!ELSEIF ""contains(as:modconf(""Resource"")[1]/ResourceGeneral/ ResourceSubderivative, 's32g2')""![!//
		[!CODE![!WS ""0""!]#include ""S32G274A_PIT.h""[!CR![!ENDCODE![!//
		[!ELSEIF ""contains(as:modconf(""Resource"")[1]/ResourceGeneral/ ResourceSubderivative, 's32r45')""![!//
		[!CODE![!WS ""0""!]#include ""S32R45_PIT.h""[!CR![!ENDCODE![!//
		[!ENDIF![!//
		[!ENDIF![!//
		[!ENDNOCODE![!//
		Example for UCT as generator:
		[!
		if (scriptApi.getProfile().getMcuInfo().getPartNumber().contains(""S32K3""))
		{
		<code>#include ""S32K344_PIT.h""\n</code>
		} else if (scriptApi.getProfile().getMcuInfo().getPartNumber().contains(""S32G2""))
		{
		<code>#include ""S32G274A_PIT.h""\n</code>
		} else if (scriptApi.getProfile().getMcuInfo().getPartNumber().contains(""S32R45""))
		{
		<code>#include ""S32R45_PIT.h""\n</code>
		}
		!]
		"

ID	Subtype	Headline and Description

ARTD-9469	New	New Feature
		
		[rm] Include the platform in a single point based on generated data
		,,"Generate the platform header include based on generated data. This way the platform name and specifics are centralized in one point only and to avoid using the compiler option define which is subject to change due to objective reasons.
		The proposal is to use a generated header file like: <lp>_lp_CfgDefines.h and centralize all platform header includes in it.
		Example for EB Tresos generator:
		[!NOCODE![!// Include specific header file
		[!IF ""node:exists(as:modconf(""Resource"")[1]/ResourceGeneral/ ResourceSubderivative)""![!//
		[!IF ""contains(as:modconf(""Resource"")[1]/ResourceGeneral/ResourceSubderivative, 's32k3')""![!//
		[!CODE![!WS ""0""!]#include ""S32K344_PIT.h""[!CR![!ENDCODE![!//
		[!ELSEIF ""contains(as:modconf(""Resource"")[1]/ResourceGeneral/ ResourceSubderivative, 's32g2')""![!//
		[!CODE![!WS ""0""!]#include ""S32G274A_PIT.h""[!CR![!ENDCODE![!//
		[!ELSEIF ""contains(as:modconf(""Resource"")[1]/ResourceGeneral/ ResourceSubderivative, 's32r45')""![!//
		[!CODE![!WS ""0""!]#include ""S32R45_PIT.h""[!CR![!ENDCODE![!//
		[!ENDIF![!//
		[!ENDIF![!//
		[!ENDNOCODE![!//
		Example for UCT as generator:
		[!
		if (scriptApi.getProfile().getMcuInfo().getPartNumber().contains(""S32K3""))
		{
		<code>#include ""S32K344_PIT.h""\n</code>
		} else if (scriptApi.getProfile().getMcuInfo().getPartNumber().contains(""S32G2""))
		{
		<code>#include ""S32G274A_PIT.h""\n</code>
		} else if (scriptApi.getProfile().getMcuInfo().getPartNumber().contains(""S32R45""))
		{
		<code>#include ""S32R45_PIT.h""\n</code>
		}
		!]
		"

ARTD-9523	Bug	[ADC] Compilation error when ADC EOC interrupt disabled and all configured groups are having without interrupt optimization enabled S32K3<*> NewWorkDescription: Compilation error when ADC EOC interrupt disabled and all configured groups are having without interrupt optimization enabled, because .pfEndOfNormalChainNotification = Adc_Ipw_Adc0EndNormalChainNotification, is generated in Adc_Sar_Ip_PBcfg.c Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: When all groups are configured with "without interrupt" feature enabled and ADC EOC interrupt is disabled in AdcInterrupts tab, .pfEndOfNormalChainNotification must be generated as NULL_PTR

ID	Subtype	Headline and Description
ARTD-9538	Bug	[ICU] Measurement properties and channel edge alignment are incorrectly generated for Autosar in DS<*> Detailed description (how to reproduce it): In ICU_MODE_SIGNAL_MEASUREMENT mode, when config channel's measurement property is ICU_DUTY_CYCLE, the output file is generated ICU_LOW_TIME. And in ICU_MODE_EDGE_COUNTER mode, when config a channel's edge alignment is ICU_BOTH_EDGES, the output file is generated ICU_FALLING_EDGE. Preconditions: Set up 2 channels of the same name but on 2 different instances of emios, when changing the properties of the second channel, the generate file does not change Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: When changing the properties of the second channel, the generate file does not change Expected behavior: The generate file must change according to the change of the channel Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Change Macro_GetLogicChannelInfo(EmiosChannelConfig.getChildById("Name").getValue()) to Macro_GetLogicChannelInfo(searchStr)
ARTD-9543	Bug	[ADC] Generating errors with BctuDevErrorDetect, BctuTimeoutMethod and BctuTimeoutValue when enabling Config Time Support ,,"Detailed description (how to reproduce it): Generating errors appear with BctuDevErrorDetect, BctuTimeoutMethod and BctuTimeoutValue when enabing config time support and click apply button !image-2021-03-31-08-57-12-099.png|thumbnail! !image-2021-03-31-09-00-18-136.png|thumbnail! The log disappears right away and no generating errors when click ""generate"" button or generate test by cmd Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-9537	Bug	[ICU][S32DS] Errors are reported when configuring multiple variants in DS<*> There are two mainly problem with S32DS when configuring many variant: Firstly, when i switch between variants (VS0,VS1, VS2) the node in IcuGeneral section in S32DS interface also change. This section should be not changeable when user switch to other VS. Secondly, some error with output configuration as the attached picture. Adittionally, checking with test suite Icu_TS_DS_M04 contains 10 config set.
ARTD-9548	Bug	[BASE][BUILD_ENV] Some compiler options are not the same between SOW and S32CT<*> Detailed description (how to reproduce it): Step 1: Create new project. Step 2: Select project > right click > Properties > C/C Build > Settings Step 3: Check compiler options and compare with SOW file Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: Some compiler options are not the same between SOW and S32CT : Linker: Duplicate: mcpu=cortex-m7 in RTD_Compiler_Option.xlsx In file *SOW*: Map*=<map_file_name>* but *CT* is: Map* Expected behavior: Update compiler option for CT the same with compiler option in SOW file.
ARTD-9557	Bug	[PORT] Clock out pin configuration generated wrong<*> Clock out pin configured wrong. Pls see attached.

ID	Subtype	Headline and Description
ARTD-9596	Bug	[ADC] Errors and missing exclusive areas in Bswmd.arxml<*> Detailed description (how to reproduce it): Exclusive areas not available in <Module>_Bswmd.arxml Incorrectly formatted <Module>_Bswmd.arxml Preconditions: N.A. Test Case ID (internal TC that caught the defect) optional: N.A. Observed behavior: Missing exclusive areas in Davinci after integrating RTD !image-2021-04-12-19-29-09-321.png|thumbnail! Expected behavior: All exclusive areas are included in <Module>_Bswmd.arxml and <Module>_Bswmd.arxml is valid Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution Fix the following issues and perform all the validation steps: Issue #1 Some exclusive areas are missing because "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" files are not using the pattern expected by bswmd_creator script: "is used in function" Solution #1 From https://jira.sw.nxp.com/browse/AMPT-5710, bswmd_creator is parsing files "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" and it's looking up for the "is used in function" pattern. Therefore, "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" files shall use the following pattern for describing each exclusive area: <MODULE>_EXCLUSIVE_AREA_09 is used in function <Module>_StartChannel ... Issue #2 Missing exclusive areas mapped to IPL functions 2.1 Exclusive areas not referenced by any function in Adc_Bswmd.arxml, missing: <CAN-ENTER-EXCLUSIVE-AREA-REF DEST="EXCLUSIVE-AREA"> E.g.:{code:java} ADC_EXCLUSIVE_AREA_12 is used in function Adc_Sar_Ip_DoCalibration 2.2 Exclusive areas missing completely from Adc_Bswmd.arxml E.g.:{code:java} ADC_EXCLUSIVE_AREA_73 is used in function Ctu_Ip_SetFifoThreshold Solution #2 The integration manual shall map exclusive areas to public HLD functions (*no internal functions should be mentioned*). This is done by adding in "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" all the public HLD functions that are using an exclusive area via calls to IPL functions. For example: ADC_EXCLUSIVE_AREA_12 is used in function Adc_Calibrate to protect the ADC_MCR register from read/modify/write operation in Adc_Sar_Ip_Powerup. ADC_EXCLUSIVE_AREA_13 is used in function Adc_Init to protect the ADC_MCR register from read/modify/write operation in Adc_Sar_Ip_Powerup. ADC_EXCLUSIVE_AREA_13 is used in function Adc_SelfTest to protect the ADC_MCR register from read/modify/write operation in Adc_Sar_Ip_Powerup. [...] Exclusive Areas implemented in Low level driver layer (IPL) ADC_EXCLUSIVE_AREA_12 is used in function Adc_Sar_Ip_DoCalibration to protect the updates for: ADC_MCR register ADC_EXCLUSIVE_AREA_13 is used in function Adc_Sar_Ip_Powerup to protect the updates for: ADC_MCR register
Release notes		This adds in "Adc_Bswmd.arxml" the ADC Exclusive Area 12 for Adc_Calibrate and ADC Exclusive Area 13 for Adc_Init and Adc_SelfTest. It also keeps the note in Integration Manual about the EAs being used by IPL API functions Adc_Sar_Ip_Powerup and Adc_Sar_Ip_DoCalibration. Issue #3 Using uppercase hexadecimals for non-autosar API service IDs. Solution #3

ID	Subtype	Headline and Description
ARTD-9598	Bug	[MCU] Generate different paths of Clock_Ip_Cfg_Defines.h between enable SDK and no enable SDK on S32DS<*> Preconditions: S32DS 3.4 Update 1 (B210204) SW32_RTD_4.4_1.0.0_HF01_D2102_DS_Updatesite Test Case 1 1. Create project without enable S32CT and SDK 2. Open Configuration Tools a+' Update code 3. Create project with enable S32CT and SDK 4. Open Configuration Tools a+' Update code 5. Compare path of file Clock_Ip_Cfg_Defines.h between project at step 2 and project at step 4 Observed behavior: 5. Different path: Step 2: path="generate/include/Clock_Ip_Cfg_Defines.h Step 4: path="board/Clock_Ip_Cfg_Defines.h" Expected behavior: 5. Same path
ARTD-9599	Bug	[RTD_4.4_S32CC_2.0.0] Could not open S32 RTD AUTOSAR 4.4 D2104 Release Notes on getting started page<*> Detailed description (how to reproduce it): 1. Open S32DS 2. Help > Getting Started Page > EXTENSIONS\RESOURCES tab. Select "S32 RTD AUTOSAR 4.4 D2104" package 3. Click on "S32 RTD AUTOSAR 4.4 D2104 Release Notes" to open Release Note Observed behavior: 3." Your file couldn't be accessed " because name of file is not match with name in itm.s32xx.rtd.collateral.PlatformSDK_S32G_2021_04.xml (Please see attached file) Expected behavior: 3. Open file successfully

ID	Subtype	Headline and Description
ARTD-9675	Bug	[adc] OsIf timeout implementation is non-uniform across drivers<*> Issue #1: The names of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Crypto, Pmic, Fls have "<Module>TimeoutOsifCounterType" Eep has "timeoutCounterType" Uart has "UartTimeoutType" The rest of them have "<Module>TimeoutMethod" Solution #1: All drivers shall rename the node introduced by ARTD-2232 to "<Module>TimeoutMethod". For example: CryptoTimeoutMethod FlsTimeoutMethod UartTimeoutMethod EepTimeoutMethod ... Issue #2: The names of the enumeration values of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Eep, Pmic have ["SYSTEM", "CUSTOM", "DUMMY'] Crypto has ["SYSTEM", "CUSTOM", "TICKS"] Fls has ["SYSTEM", "CUSTOM", "LOOP] Adc, Lin, Ocotp, Spi have ["SystemTimer", "CustomTimer", "DummyTimer"] Gpt has ["OSIF_COUNTER_SYSTEM, "OSIF_COUNTER_CUSTOM", "OSIF_COUNTER_NOT_USED"] The rest of them have ["OSIF_COUNTER_SYSTEM", "OSIF_COUNTER_CUSTOM", "OSIF_COUNTER_DUMMY"] Solution #2: All drivers shall rename the enumeration values of the node introduced by ARTD-2232 as follows: DummyTimer/Dummy/Ticks/etc > OSIF_COUNTER_DUMMY SystemTimer/System/etc >OSIF_COUNTER_SYSTEM CustomTimer/Custom/etc > OSIF_COUNTER_CUSTOM Issue #3: The available enumeration values of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Eth, Fr, I2c have only two enumeration values: ["OSIF_COUNTER_SYSTEM", "OSIF_COUNTER_CUSTOM" Solution #3: All drivers shall define the following three enumeration values for the node introduced by ARTD-2232: OSIF_COUNTER_DUMMY OSIF_COUNTER_SYSTEM OSIF_COUNTER_CUSTOM Issue #4: The default enumeration value of the node introduced by ARTD-2232 is inconsistent across drivers. For example: Eth, I2c, Uart have a default value of "OSIF_COUNTER_SYSTEM" Solution #4: All drivers shall set the default value of the node introduced by ARTD-2232 to "OSIF_COUNTER_DUMMY"

ID	Subtype	Headline and Description
ARTD-9676	Bug	[can] OsIf timeout implementation is non-uniform across drivers<*> Issue #1: The names of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Crypto, Pmic, Fls have "<Module>TimeoutOsifCounterType" Eep has "timeoutCounterType" Uart has "UartTimeoutType" The rest of them have "<Module>TimeoutMethod" Solution #1: All drivers shall rename the node introduced by ARTD-2232 to "<Module>TimeoutMethod". For example: CryptoTimeoutMethod FlsTimeoutMethod UartTimeoutMethod EepTimeoutMethod ... Issue #2: The names of the enumeration values of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Eep, Pmic have ["SYSTEM", "CUSTOM", "DUMMY'] Crypto has ["SYSTEM", "CUSTOM", "TICKS"] Fls has ["SYSTEM", "CUSTOM", "LOOP] Adc, Lin, Ocotp, Spi have ["SystemTimer", "CustomTimer", "DummyTimer"] Gpt has ["OSIF_COUNTER_SYSTEM, "OSIF_COUNTER_CUSTOM", "OSIF_COUNTER_NOT_USED"] The rest of them have ["OSIF_COUNTER_SYSTEM", "OSIF_COUNTER_CUSTOM", "OSIF_COUNTER_DUMMY"] Solution #2: All drivers shall rename the enumeration values of the node introduced by ARTD-2232 as follows: DummyTimer/Dummy/Ticks/etc > OSIF_COUNTER_DUMMY SystemTimer/System/etc >OSIF_COUNTER_SYSTEM CustomTimer/Custom/etc > OSIF_COUNTER_CUSTOM Issue #3: The available enumeration values of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Eth, Fr, I2c have only two enumeration values: ["OSIF_COUNTER_SYSTEM", "OSIF_COUNTER_CUSTOM" Solution #3: All drivers shall define the following three enumeration values for the node introduced by ARTD-2232: OSIF_COUNTER_DUMMY OSIF_COUNTER_SYSTEM OSIF_COUNTER_CUSTOM Issue #4: The default enumeration value of the node introduced by ARTD-2232 is inconsistent across drivers. For example: Eth, I2c, Uart have a default value of "OSIF_COUNTER_SYSTEM" Solution #4: All drivers shall set the default value of the node introduced by ARTD-2232 to "OSIF_COUNTER_DUMMY"

ID	Subtype	Headline and Description
ARTD-9681	Bug	[eep] OsIf timeout implementation is non-uniform across drivers<*> Issue #1: The names of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Crypto, Pmic, Fls have "<Module>TimeoutOsifCounterType" Eep has "timeoutCounterType" Uart has "UartTimeoutType" The rest of them have "<Module>TimeoutMethod" Solution #1: All drivers shall rename the node introduced by ARTD-2232 to "<Module>TimeoutMethod". For example: CryptoTimeoutMethod FlsTimeoutMethod UartTimeoutMethod EepTimeoutMethod ... Issue #2: The names of the enumeration values of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Eep, Pmic have ["SYSTEM", "CUSTOM", "DUMMY'] Crypto has ["SYSTEM", "CUSTOM", "TICKS"] Fls has ["SYSTEM", "CUSTOM", "LOOP] Adc, Lin, Ocotp, Spi have ["SystemTimer", "CustomTimer", "DummyTimer"] Gpt has ["OSIF_COUNTER_SYSTEM, "OSIF_COUNTER_CUSTOM", "OSIF_COUNTER_NOT_USED"] The rest of them have ["OSIF_COUNTER_SYSTEM", "OSIF_COUNTER_CUSTOM", "OSIF_COUNTER_DUMMY"] Solution #2: All drivers shall rename the enumeration values of the node introduced by ARTD-2232 as follows: DummyTimer/Dummy/Ticks/etc > OSIF_COUNTER_DUMMY SystemTimer/System/etc >OSIF_COUNTER_SYSTEM CustomTimer/Custom/etc > OSIF_COUNTER_CUSTOM Issue #3: The available enumeration values of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Eth, Fr, I2c have only two enumeration values: ["OSIF_COUNTER_SYSTEM", "OSIF_COUNTER_CUSTOM" Solution #3: All drivers shall define the following three enumeration values for the node introduced by ARTD-2232: OSIF_COUNTER_DUMMY OSIF_COUNTER_SYSTEM OSIF_COUNTER_CUSTOM Issue #4: The default enumeration value of the node introduced by ARTD-2232 is inconsistent across drivers. For example: Eth, I2c, Uart have a default value of "OSIF_COUNTER_SYSTEM" Solution #4: All drivers shall set the default value of the node introduced by ARTD-2232 to "OSIF_COUNTER_DUMMY"

ID	Subtype	Headline and Description
ARTD-9682	Bug	[eth] OsIf timeout implementation is non-uniform across drivers<*> Issue #1: The names of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Crypto, Pmic, Fls have "<Module>TimeoutOsifCounterType" Eep has "timeoutCounterType" Uart has "UartTimeoutType" The rest of them have "<Module>TimeoutMethod" Solution #1: All drivers shall rename the node introduced by ARTD-2232 to "<Module>TimeoutMethod". For example: CryptoTimeoutMethod FlsTimeoutMethod UartTimeoutMethod EepTimeoutMethod ... Issue #2: The names of the enumeration values of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Eep, Pmic have ["SYSTEM", "CUSTOM", "DUMMY'] Crypto has ["SYSTEM", "CUSTOM", "TICKS"] Fls has ["SYSTEM", "CUSTOM", "LOOP] Adc, Lin, Ocotp, Spi have ["SystemTimer", "CustomTimer", "DummyTimer"] Gpt has ["OSIF_COUNTER_SYSTEM, "OSIF_COUNTER_CUSTOM", "OSIF_COUNTER_NOT_USED"] The rest of them have ["OSIF_COUNTER_SYSTEM", "OSIF_COUNTER_CUSTOM", "OSIF_COUNTER_DUMMY"] Solution #2: All drivers shall rename the enumeration values of the node introduced by ARTD-2232 as follows: DummyTimer/Dummy/Ticks/etc > OSIF_COUNTER_DUMMY SystemTimer/System/etc >OSIF_COUNTER_SYSTEM CustomTimer/Custom/etc > OSIF_COUNTER_CUSTOM Issue #3: The available enumeration values of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Eth, Fr, I2c have only two enumeration values: ["OSIF_COUNTER_SYSTEM", "OSIF_COUNTER_CUSTOM" Solution #3: All drivers shall define the following three enumeration values for the node introduced by ARTD-2232: OSIF_COUNTER_DUMMY OSIF_COUNTER_SYSTEM OSIF_COUNTER_CUSTOM Issue #4: The default enumeration value of the node introduced by ARTD-2232 is inconsistent across drivers. For example: Eth, I2c, Uart have a default value of "OSIF_COUNTER_SYSTEM" Solution #4: All drivers shall set the default value of the node introduced by ARTD-2232 to "OSIF_COUNTER_DUMMY"

ID	Subtype	Headline and Description
ARTD-9683	Bug	[fls] OsIf timeout implementation is non-uniform across drivers<*> Issue #1: The names of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Crypto, Pmic, Fls have "<Module>TimeoutOsifCounterType" Eep has "timeoutCounterType" Uart has "UartTimeoutType" The rest of them have "<Module>TimeoutMethod" Solution #1: All drivers shall rename the node introduced by ARTD-2232 to "<Module>TimeoutMethod". For example: CryptoTimeoutMethod FlsTimeoutMethod UartTimeoutMethod EepTimeoutMethod ... Issue #2: The names of the enumeration values of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Eep, Pmic have ["SYSTEM", "CUSTOM", "DUMMY'] Crypto has ["SYSTEM", "CUSTOM", "TICKS"] Fls has ["SYSTEM", "CUSTOM", "LOOP] Adc, Lin, Ocotp, Spi have ["SystemTimer", "CustomTimer", "DummyTimer"] Gpt has ["OSIF_COUNTER_SYSTEM, "OSIF_COUNTER_CUSTOM", "OSIF_COUNTER_NOT_USED"] The rest of them have ["OSIF_COUNTER_SYSTEM", "OSIF_COUNTER_CUSTOM", "OSIF_COUNTER_DUMMY"] Solution #2: All drivers shall rename the enumeration values of the node introduced by ARTD-2232 as follows: DummyTimer/Dummy/Ticks/etc > OSIF_COUNTER_DUMMY SystemTimer/System/etc >OSIF_COUNTER_SYSTEM CustomTimer/Custom/etc > OSIF_COUNTER_CUSTOM Issue #3: The available enumeration values of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Eth, Fr, I2c have only two enumeration values: ["OSIF_COUNTER_SYSTEM", "OSIF_COUNTER_CUSTOM" Solution #3: All drivers shall define the following three enumeration values for the node introduced by ARTD-2232: OSIF_COUNTER_DUMMY OSIF_COUNTER_SYSTEM OSIF_COUNTER_CUSTOM Issue #4: The default enumeration value of the node introduced by ARTD-2232 is inconsistent across drivers. For example: Eth, I2c, Uart have a default value of "OSIF_COUNTER_SYSTEM" Solution #4: All drivers shall set the default value of the node introduced by ARTD-2232 to "OSIF_COUNTER_DUMMY"

ID	Subtype	Headline and Description
ARTD-9614	Bug	[S32XX] Project show duplicate file and folder after updating code with project which not attach SDK RTD<*> Precondition:* Open S32SD3.4 update1 which installed package S32CC_RTD_4_4_RTM_2_0_0_DS_updatesite_2104.zip Step: 1.Create project for S32R45/S32G2 2. Select Project > Open configuration by click to "Open S32 Configuration" icon in the toolbar 3. In Create a new configuration window, select core for processor > Finish 4. Update code 5. Import any example for S32R45/ S32G2 6. Open S32CT tool then update code Observed behavior: Project show duplicate file and folder in 'generate/include' ,'generate/src' and 'generate' Expected behavior: Project show only one 'generate' folder
ARTD-9643	New	New Feature CLONE - [SPI] Improvement SpiPhyUnit configuration can be stored to a pointer in Ip_StateStructure variable ,,"SpiPhyUnit configuration can be stored to a pointer in Ip_StateStructure variable. So, No need to copy many variables value to Ip_StateStructure in Ip_Init() anymore."
ARTD-9644	New	New Feature CLONE - [SPI] Improvement External device configuration can be stored to a pointer in Ip_StateStructure variable ,,"External device configuration can be stored to a pointer in Ip_StateStructure variable. So, No need to copy many variables value to Ip_StateStructure in Ip_SyncTransmit() or Ip_AsyncTransmit() anymore."

ID	Subtype	Headline and Description
ARTD-9653	Bug	[ADC] Adc_ReadGroup does not re-enable Dma HW Request and update destination address if limit check failed for Group Without Interrupt<*> Detailed description (how to reproduce it): Adc_ReadGroup does not re-enable Dma HW Request and update destination address if limit check failed for Group Without Interrupt. So the Dma Internal Buffer was not up to date at triggering second time Preconditions: Group hardware trigger oneshot Without interrupt = on Transferring by dma with 1 channel Limit check is enable range between from 1000 to 3000 Test Case ID (internal TC that caught the defect) optional: Adc_TC_FCT_1407 Adc_TC_FCT_1408 (Adc_TS_013 cfg 8) Observed behavior: Set voltage for ADC0 AN_2 as 1.8V (0xfff) Adc_EnableHardwareTrigger(t_u16AdcGroupType); Start trigger first time Loop until read group return E_OK Expect time out occured Set voltage for ADC0 AN_2 as 1V (0x93B) Start trigger second time Loop until read group return E_OK Expect time out not occured Real status time out occured because buffer u32DmaNoIrqBuffer was not updated Expected behavior: Buffer u32DmaNoIrqBuffer was updated Time out not occured with voltage in range Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Adc_TC_FCT_1408 is sw continuous group with same sequence and have the same issue: Buffer u32DmaNoIrqBuffer was not updated Proposed solution optional: NA

ID	Subtype	Headline and Description
ARTD-9659	Bug	[ICU] The MAX_PARTITIONS value and Icu_Config variable wrong in DS in HL<*> Detailed description (how to reproduce it): The MAX_PARTITIONS value is wrong in DS in HL. In EB tresos: MAX_PARTITIONS = maxcoreId 1 Icu_Config is declared as const Icu_ConfigType const Icu_Config [MAX_PARTITIONS] but in DS: MAX_PARTITIONS = size of 'IcuEcucPartitionRef' Icu_Config is declared as const Icu_ConfigType const Icu_Config [size of 'IcuEcucPartitionRef'] Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: MAX_PARTITIONS = size of 'IcuEcucPartitionRef' Icu_Config is declared as const Icu_ConfigType const Icu_Config [size of 'IcuEcucPartitionRef'] Expected behavior: MAX_PARTITIONS = maxcoreId 1 Icu_Config is declared as const Icu_ConfigType const Icu_Config [MAX_PARTITIONS] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update generate code for MAX_PARTITIONS in Icu_Cfg.h
ARTD-9661	Bug	[EB] All examples S32R45 but CORTEXM are S32G2XXM7<*> Detailed description (how to reproduce it): Step 1. Open the Windows command prompt window Step 2. Change the current directory to the example application folder Step 3. To generate the Tresos project of the example, execute the following command to build: make generate Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: All examples S32R45 but CORTEXM are S32G2XXM7. Detail was attached Expected behavior: CORTEXM update is S32R45XM7 for R45 of all examples Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-9672	Bug	[GPT] Disable the GptTimeoutMethod feature if it's not used<*> Detailed description (how to reproduce it): in case that GptTimeoutMethod features is not used should be readonly Preconditions: using a ds configuration Test Case ID (internal TC that caught the defect) optional: Ip_Pit_TC_FCT_0001 Observed behavior: GptTimeoutMethod feature is enabled in ds Expected behavior: GptTimeoutMethod feature should be disabled as it is in ebt Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: disable GptTimeoutMethod feature if it s not necessary
ARTD-9708	Bug	[RM][S32K3XX] Add Ip level parameter input checks<*> Detailed description (how to reproduce it): Do not check input parameters of functions yet Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Do not check input parameters of functions yet Expected behavior: Check input parameters of functions Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Check input parameters of functions

ID	Subtype	Headline and Description
ARTD-9705	Bug	[ADC] Adc_ReadGroup can return E_OK and result for uncomplete current group channel without interrupt if we did not read previous group<*> Detailed description (how to reproduce it): Adc_ReadGroup can return E_OK and result for uncomplete current group channel if we did not read previous group Preconditions: Limit check is enable Group without interrupt Test Case ID (internal TC that caught the defect) optional: Adc_TC_FCT_1410 Adc_TS_013 cfg 1 Observed behavior: Set voltage for AN_2 in range and data passing through limit check and not implement Adc_ReadGroup Adc_EnableHardwareTrigger(t_u16AdcGroupType); T_ADC_StartTrigger(t_u16AdcGroupType); T_TIMER_DelayMs(T_ADC_DELAY_VALUE); T_ADC_StopTrigger(t_u16AdcGroupType); Adc_DisableHardwareTrigger(t_u16AdcGroupType); Set voltage for AN_2 out of range Adc_EnableHardwareTrigger(t_u16AdcGroupType); EU_ASSERT(E_OK != Adc_ReadGroup(t_u16AdcGroupType, t_readGroupBuffer)); Adc_DisableHardwareTrigger(t_u16AdcGroupType); Expected: Adc_ReadGroup return E_NOT_OK because not triggering for current group Real status: Adc_ReadGroup return E_OK Expected behavior: Adc_ReadGroup return E_NOT_OK because not triggering for current group Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) CPR_RTD_00049.adc: Adc_ReadGroup shall return conversation results only if all channels of the triggered group have completed their conversion This issue related to ARTD-5796: [ADC] Using Adc_Sar_Ip_GetConvData for checking conversion is completed, based on valid bit, will not wait for conversion to finish if previously completed conversion wasn't read already Proposed solution optional: NA

ID	Subtype	Headline and Description
ARTD-9685	Bug	[gpt] OsIf timeout implementation is non-uniform across drivers<*> Issue #1: The names of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Crypto, Pmic, Fls have "<Module>TimeoutOsifCounterType" Eep has "timeoutCounterType" Uart has "UartTimeoutType" The rest of them have "<Module>TimeoutMethod" Solution #1: All drivers shall rename the node introduced by ARTD-2232 to "<Module>TimeoutMethod". For example: CryptoTimeoutMethod FlsTimeoutMethod UartTimeoutMethod EepTimeoutMethod ... Issue #2: The names of the enumeration values of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Eep, Pmic have ["SYSTEM", "CUSTOM", "DUMMY'] Crypto has ["SYSTEM", "CUSTOM", "TICKS"] Fls has ["SYSTEM", "CUSTOM", "LOOP] Adc, Lin, Ocotp, Spi have ["SystemTimer", "CustomTimer", "DummyTimer"] Gpt has ["OSIF_COUNTER_SYSTEM, "OSIF_COUNTER_CUSTOM", "OSIF_COUNTER_NOT_USED"] The rest of them have ["OSIF_COUNTER_SYSTEM", "OSIF_COUNTER_CUSTOM", "OSIF_COUNTER_DUMMY"] Solution #2: All drivers shall rename the enumeration values of the node introduced by ARTD-2232 as follows: DummyTimer/Dummy/Ticks/etc > OSIF_COUNTER_DUMMY SystemTimer/System/etc >OSIF_COUNTER_SYSTEM CustomTimer/Custom/etc > OSIF_COUNTER_CUSTOM Issue #3: The available enumeration values of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Eth, Fr, I2c have only two enumeration values: ["OSIF_COUNTER_SYSTEM", "OSIF_COUNTER_CUSTOM" Solution #3: All drivers shall define the following three enumeration values for the node introduced by ARTD-2232: OSIF_COUNTER_DUMMY OSIF_COUNTER_SYSTEM OSIF_COUNTER_CUSTOM Issue #4: The default enumeration value of the node introduced by ARTD-2232 is inconsistent across drivers. For example: Eth, I2c, Uart have a default value of "OSIF_COUNTER_SYSTEM" Solution #4: All drivers shall set the default value of the node introduced by ARTD-2232 to "OSIF_COUNTER_DUMMY"

ID	Subtype	Headline and Description
ARTD-9697	Bug	[sai] OsIf timeout implementation is non-uniform across drivers<*> Issue #1: The names of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Crypto, Pmic, Fls have "<Module>TimeoutOsifCounterType" Eep has "timeoutCounterType" Uart has "UartTimeoutType" The rest of them have "<Module>TimeoutMethod" Solution #1: All drivers shall rename the node introduced by ARTD-2232 to "<Module>TimeoutMethod". For example: CryptoTimeoutMethod FlsTimeoutMethod UartTimeoutMethod EepTimeoutMethod ... Issue #2: The names of the enumeration values of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Eep, Pmic have ["SYSTEM", "CUSTOM", "DUMMY'] Crypto has ["SYSTEM", "CUSTOM", "TICKS"] Fls has ["SYSTEM", "CUSTOM", "LOOP] Adc, Lin, Ocotp, Spi have ["SystemTimer", "CustomTimer", "DummyTimer"] Gpt has ["OSIF_COUNTER_SYSTEM, "OSIF_COUNTER_CUSTOM", "OSIF_COUNTER_NOT_USED"] The rest of them have ["OSIF_COUNTER_SYSTEM", "OSIF_COUNTER_CUSTOM", "OSIF_COUNTER_DUMMY"] Solution #2: All drivers shall rename the enumeration values of the node introduced by ARTD-2232 as follows: DummyTimer/Dummy/Ticks/etc > OSIF_COUNTER_DUMMY SystemTimer/System/etc >OSIF_COUNTER_SYSTEM CustomTimer/Custom/etc > OSIF_COUNTER_CUSTOM Issue #3: The available enumeration values of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Eth, Fr, I2c have only two enumeration values: ["OSIF_COUNTER_SYSTEM", "OSIF_COUNTER_CUSTOM" Solution #3: All drivers shall define the following three enumeration values for the node introduced by ARTD-2232: OSIF_COUNTER_DUMMY OSIF_COUNTER_SYSTEM OSIF_COUNTER_CUSTOM Issue #4: The default enumeration value of the node introduced by ARTD-2232 is inconsistent across drivers. For example: Eth, I2c, Uart have a default value of "OSIF_COUNTER_SYSTEM" Solution #4: All drivers shall set the default value of the node introduced by ARTD-2232 to "OSIF_COUNTER_DUMMY"

ID	Subtype	Headline and Description
ARTD-9699	Bug	[spi] OsIf timeout implementation is non-uniform across drivers<*> Issue #1: The names of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Crypto, Pmic, Fls have "<Module>TimeoutOsifCounterType" Eep has "timeoutCounterType" Uart has "UartTimeoutType" The rest of them have "<Module>TimeoutMethod" Solution #1: All drivers shall rename the node introduced by ARTD-2232 to "<Module>TimeoutMethod". For example: CryptoTimeoutMethod FlsTimeoutMethod UartTimeoutMethod EepTimeoutMethod ... Issue #2: The names of the enumeration values of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Eep, Pmic have ["SYSTEM", "CUSTOM", "DUMMY'] Crypto has ["SYSTEM", "CUSTOM", "TICKS"] Fls has ["SYSTEM", "CUSTOM", "LOOP] Adc, Lin, Ocotp, Spi have ["SystemTimer", "CustomTimer", "DummyTimer"] Gpt has ["OSIF_COUNTER_SYSTEM, "OSIF_COUNTER_CUSTOM", "OSIF_COUNTER_NOT_USED"] The rest of them have ["OSIF_COUNTER_SYSTEM", "OSIF_COUNTER_CUSTOM", "OSIF_COUNTER_DUMMY"] Solution #2: All drivers shall rename the enumeration values of the node introduced by ARTD-2232 as follows: DummyTimer/Dummy/Ticks/etc > OSIF_COUNTER_DUMMY SystemTimer/System/etc >OSIF_COUNTER_SYSTEM CustomTimer/Custom/etc > OSIF_COUNTER_CUSTOM Issue #3: The available enumeration values of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Eth, Fr, I2c have only two enumeration values: ["OSIF_COUNTER_SYSTEM", "OSIF_COUNTER_CUSTOM" Solution #3: All drivers shall define the following three enumeration values for the node introduced by ARTD-2232: OSIF_COUNTER_DUMMY OSIF_COUNTER_SYSTEM OSIF_COUNTER_CUSTOM Issue #4: The default enumeration value of the node introduced by ARTD-2232 is inconsistent across drivers. For example: Eth, I2c, Uart have a default value of "OSIF_COUNTER_SYSTEM" Solution #4: All drivers shall set the default value of the node introduced by ARTD-2232 to "OSIF_COUNTER_DUMMY"

ID	Subtype	Headline and Description
ARTD-9701	Bug	[uart] OsIf timeout implementation is non-uniform across drivers<*> Issue #1: The names of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Crypto, Pmic, Fls have "<Module>TimeoutOsifCounterType" Eep has "timeoutCounterType" Uart has "UartTimeoutType" The rest of them have "<Module>TimeoutMethod" Solution #1: All drivers shall rename the node introduced by ARTD-2232 to "<Module>TimeoutMethod". For example: CryptoTimeoutMethod FlsTimeoutMethod UartTimeoutMethod EepTimeoutMethod ... Issue #2: The names of the enumeration values of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Eep, Pmic have ["SYSTEM", "CUSTOM", "DUMMY'] Crypto has ["SYSTEM", "CUSTOM", "TICKS"] Fls has ["SYSTEM", "CUSTOM", "LOOP] Adc, Lin, Ocotp, Spi have ["SystemTimer", "CustomTimer", "DummyTimer"] Gpt has ["OSIF_COUNTER_SYSTEM, "OSIF_COUNTER_CUSTOM", "OSIF_COUNTER_NOT_USED"] The rest of them have ["OSIF_COUNTER_SYSTEM", "OSIF_COUNTER_CUSTOM", "OSIF_COUNTER_DUMMY"] Solution #2: All drivers shall rename the enumeration values of the node introduced by ARTD-2232 as follows: DummyTimer/Dummy/Ticks/etc > OSIF_COUNTER_DUMMY SystemTimer/System/etc >OSIF_COUNTER_SYSTEM CustomTimer/Custom/etc > OSIF_COUNTER_CUSTOM Issue #3: The available enumeration values of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Eth, Fr, I2c have only two enumeration values: ["OSIF_COUNTER_SYSTEM", "OSIF_COUNTER_CUSTOM" Solution #3: All drivers shall define the following three enumeration values for the node introduced by ARTD-2232: OSIF_COUNTER_DUMMY OSIF_COUNTER_SYSTEM OSIF_COUNTER_CUSTOM Issue #4: The default enumeration value of the node introduced by ARTD-2232 is inconsistent across drivers. For example: Eth, I2c, Uart have a default value of "OSIF_COUNTER_SYSTEM" Solution #4: All drivers shall set the default value of the node introduced by ARTD-2232 to "OSIF_COUNTER_DUMMY"

ID	Subtype	Headline and Description
ARTD-9702	Bug	[wdg] OsIf timeout implementation is non-uniform across drivers<*> Issue #1: The names of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Crypto, Pmic, Fls have "<Module>TimeoutOsifCounterType" Eep has "timeoutCounterType" Uart has "UartTimeoutType" The rest of them have "<Module>TimeoutMethod" Solution #1: All drivers shall rename the node introduced by ARTD-2232 to "<Module>TimeoutMethod". For example: CryptoTimeoutMethod FlsTimeoutMethod UartTimeoutMethod EepTimeoutMethod ... Issue #2: The names of the enumeration values of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Eep, Pmic have ["SYSTEM", "CUSTOM", "DUMMY'] Crypto has ["SYSTEM", "CUSTOM", "TICKS"] Fls has ["SYSTEM", "CUSTOM", "LOOP] Adc, Lin, Ocotp, Spi have ["SystemTimer", "CustomTimer", "DummyTimer"] Gpt has ["OSIF_COUNTER_SYSTEM, "OSIF_COUNTER_CUSTOM", "OSIF_COUNTER_NOT_USED"] The rest of them have ["OSIF_COUNTER_SYSTEM", "OSIF_COUNTER_CUSTOM", "OSIF_COUNTER_DUMMY"] Solution #2: All drivers shall rename the enumeration values of the node introduced by ARTD-2232 as follows: DummyTimer/Dummy/Ticks/etc > OSIF_COUNTER_DUMMY SystemTimer/System/etc >OSIF_COUNTER_SYSTEM CustomTimer/Custom/etc > OSIF_COUNTER_CUSTOM Issue #3: The available enumeration values of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Eth, Fr, I2c have only two enumeration values: ["OSIF_COUNTER_SYSTEM", "OSIF_COUNTER_CUSTOM" Solution #3: All drivers shall define the following three enumeration values for the node introduced by ARTD-2232: OSIF_COUNTER_DUMMY OSIF_COUNTER_SYSTEM OSIF_COUNTER_CUSTOM Issue #4: The default enumeration value of the node introduced by ARTD-2232 is inconsistent across drivers. For example: Eth, I2c, Uart have a default value of "OSIF_COUNTER_SYSTEM" Solution #4: All drivers shall set the default value of the node introduced by ARTD-2232 to "OSIF_COUNTER_DUMMY"

ID	Subtype	Headline and Description
ARTD-9737	Bug	[crypto] Errors and missing exclusive areas in Bswmd.arxml<*> Detailed description (how to reproduce it): Exclusive areas not available in <Module>_Bswmd.arxml Incorrectly formatted <Module>_Bswmd.arxml Preconditions: N.A. Test Case ID (internal TC that caught the defect) optional: N.A. Observed behavior: Missing exclusive areas in Davinci after integrating RTD !image-2021-04-12-19-29-09-321.png|thumbnail! Expected behavior: All exclusive areas are included in <Module>_Bswmd.arxml <Module>_Bswmd.arxml is valid Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution Fix the following issues and perform all the verification steps*: Issue #1 Some exclusive areas are missing because "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" files are not using the pattern expected by bswmd_creator script: "is used in function" Solution #1 From https://jira.sw.nxp.com/browse/AMPT-5710, bswmd_creator is parsing files "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" and it's looking up for the "is used in function" pattern. Therefore, "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" files shall use the following pattern for describing each exclusive area: <MODULE>_EXCLUSIVE_AREA_09 is used in function <Module>_StartChannel ... Issue #2 Missing exclusive areas mapped to IPL functions 2.1 Exclusive areas not referenced by any function in Adc_Bswmd.arxml, missing: <CAN-ENTER-EXCLUSIVE-AREA-REF DEST="EXCLUSIVE-AREA"> E.g.:{code:java} ADC_EXCLUSIVE_AREA_12 is used in function Adc_Sar_Ip_DoCalibration 2.2 Exclusive areas missing completely from Adc_Bswmd.arxml E.g.:{code:java} ADC_EXCLUSIVE_AREA_73 is used in function Ctu_Ip_SetFifoThreshold Solution #2 The integration manual shall map exclusive areas to public HLD functions (*no internal functions should be mentioned*). This is done by adding in "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" all the public HLD functions that are using an exclusive area via calls to IPL functions. For example: ADC_EXCLUSIVE_AREA_12 is used in function Adc_Calibrate to protect the ADC_MCR register from read/modify/write operation in Adc_Sar_Ip_Powerup. ADC_EXCLUSIVE_AREA_13 is used in function Adc_Init to protect the ADC_MCR register from read/modify/write operation in Adc_Sar_Ip_Powerup. ADC_EXCLUSIVE_AREA_13 is used in function Adc_SelfTest to protect the ADC_MCR register from read/modify/write operation in Adc_Sar_Ip_Powerup. [...] Exclusive Areas implemented in Low level driver layer (IPL) ADC_EXCLUSIVE_AREA_12 is used in function Adc_Sar_Ip_DoCalibration to protect the updates for: ADC_MCR register ADC_EXCLUSIVE_AREA_13 is used in function Adc_Sar_Ip_Powerup to protect the updates for: ADC_MCR register
Release notes		This adds in "Adc_Bswmd.arxml" the ADC Exclusive Area 12 for Adc_Calibrate and ADC Exclusive Area 13 for Adc_Init and Adc_SelfTest. It also keeps the note in Integration Manual about the EAs being used by IPL API functions Adc_Sar_Ip_Powerup and Adc_Sar_Ip_DoCalibration. Issue #3 Using uppercase hexadecimals for non-autosar API service IDs. Solution #3

ID	Subtype	Headline and Description
ARTD-9745	Bug	[i2c] Errors and missing exclusive areas in Bswmd.arxml<*> Detailed description (how to reproduce it): Exclusive areas not available in <Module>_Bswmd.arxml Incorrectly formatted <Module>_Bswmd.arxml Preconditions: N.A. Test Case ID (internal TC that caught the defect) optional: N.A. Observed behavior: Missing exclusive areas in Davinci after integrating RTD !image-2021-04-12-19-29-09-321.png|thumbnail! Expected behavior: All exclusive areas are included in <Module>_Bswmd.arxml <Module>_Bswmd.arxml is valid Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution Fix the following issues and perform all the verification steps*: Issue #1 Some exclusive areas are missing because "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" files are not using the pattern expected by bswmd_creator script: "is used in function" Solution #1 From https://jira.sw.nxp.com/browse/AMPT-5710, bswmd_creator is parsing files "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" and it's looking up for the "is used in function" pattern. Therefore, "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" files shall use the following pattern for describing each exclusive area: <MODULE>_EXCLUSIVE_AREA_09 is used in function <Module>_StartChannel ... Issue #2 Missing exclusive areas mapped to IPL functions 2.1 Exclusive areas not referenced by any function in Adc_Bswmd.arxml, missing: <CAN-ENTER-EXCLUSIVE-AREA-REF DEST="EXCLUSIVE-AREA"> E.g.:{code:java} ADC_EXCLUSIVE_AREA_12 is used in function Adc_Sar_Ip_DoCalibration 2.2 Exclusive areas missing completely from Adc_Bswmd.arxml E.g.:{code:java} ADC_EXCLUSIVE_AREA_73 is used in function Ctu_Ip_SetFifoThreshold Solution #2 The integration manual shall map exclusive areas to public HLD functions (*no internal functions should be mentioned*). This is done by adding in "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" all the public HLD functions that are using an exclusive area via calls to IPL functions. For example: ADC_EXCLUSIVE_AREA_12 is used in function Adc_Calibrate to protect the ADC_MCR register from read/modify/write operation in Adc_Sar_Ip_Powerup. ADC_EXCLUSIVE_AREA_13 is used in function Adc_Init to protect the ADC_MCR register from read/modify/write operation in Adc_Sar_Ip_Powerup. ADC_EXCLUSIVE_AREA_13 is used in function Adc_SelfTest to protect the ADC_MCR register from read/modify/write operation in Adc_Sar_Ip_Powerup. [...] Exclusive Areas implemented in Low level driver layer (IPL) ADC_EXCLUSIVE_AREA_12 is used in function Adc_Sar_Ip_DoCalibration to protect the updates for: ADC_MCR register ADC_EXCLUSIVE_AREA_13 is used in function Adc_Sar_Ip_Powerup to protect the updates for: ADC_MCR register
Release notes		This adds in "Adc_Bswmd.arxml" the ADC Exclusive Area 12 for Adc_Calibrate and ADC Exclusive Area 13 for Adc_Init and Adc_SelfTest. It also keeps the note in Integration Manual about the EAs being used by IPL API functions Adc_Sar_Ip_Powerup and Adc_Sar_Ip_DoCalibration. Issue #3 Using uppercase hexadecimals for non-autosar API service IDs. Solution #3

ID	Subtype	Headline and Description
ARTD-9750	Bug	[S32XX RTM][S32K1 EAR][S32K3 RTM] OCU: Errors and missing exclusive areas in Bswmd.arxml<*> Detailed description (how to reproduce it): Exclusive areas not available in <Module>_Bswmd.arxml Incorrectly formatted <Module>_Bswmd.arxml Preconditions: N.A. Test Case ID (internal TC that caught the defect) optional: N.A. Observed behavior: Missing exclusive areas in Davinci after integrating RTD !image-2021-04-12-19-29-09-321.png|thumbnail! Expected behavior: All exclusive areas are included in <Module>_Bswmd.arxml <Module>_Bswmd.arxml is valid Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution Fix the following issues and perform all the verification steps*: Issue #1 Some exclusive areas are missing because "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" files are not using the pattern expected by bswmd_creator script: "is used in function" Solution #1 From https://jira.sw.nxp.com/browse/AMPT-5710, bswmd_creator is parsing files "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" and it's looking up for the "is used in function" pattern. Therefore, "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" files shall use the following pattern for describing each exclusive area: <MODULE>_EXCLUSIVE_AREA_09 is used in function <Module>_StartChannel ... Issue #2 Missing exclusive areas mapped to IPL functions 2.1 Exclusive areas not referenced by any function in Adc_Bswmd.arxml, missing: <CAN-ENTER-EXCLUSIVE-AREA-REF DEST="EXCLUSIVE-AREA"> E.g.:{code:java} ADC_EXCLUSIVE_AREA_12 is used in function Adc_Sar_Ip_DoCalibration 2.2 Exclusive areas missing completely from Adc_Bswmd.arxml E.g.:{code:java} ADC_EXCLUSIVE_AREA_73 is used in function Ctu_Ip_SetFifoThreshold Solution #2 The integration manual shall map exclusive areas to public HLD functions (*no internal functions should be mentioned*). This is done by adding in "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" all the public HLD functions that are using an exclusive area via calls to IPL functions. For example: ADC_EXCLUSIVE_AREA_12 is used in function Adc_Calibrate to protect the ADC_MCR register from read/modify/write operation in Adc_Sar_Ip_Powerup. ADC_EXCLUSIVE_AREA_13 is used in function Adc_Init to protect the ADC_MCR register from read/modify/write operation in Adc_Sar_Ip_Powerup. ADC_EXCLUSIVE_AREA_13 is used in function Adc_SelfTest to protect the ADC_MCR register from read/modify/write operation in Adc_Sar_Ip_Powerup. [...] Exclusive Areas implemented in Low level driver layer (IPL) ADC_EXCLUSIVE_AREA_12 is used in function Adc_Sar_Ip_DoCalibration to protect the updates for: ADC_MCR register ADC_EXCLUSIVE_AREA_13 is used in function Adc_Sar_Ip_Powerup to protect the updates for: ADC_MCR register.
Release notes		This adds in "Adc_Bswmd.arxml" the ADC Exclusive Area 12 for Adc_Calibrate and ADC Exclusive Area 13 for Adc_Init and Adc_SelfTest. It also keeps the note in Integration Manual about the EAs being used by IPL API functions Adc_Sar_Ip_Powerup and Adc_Sar_Ip_DoCalibration. Issue #3 Using uppercase hexadecimals for non-autosar API service IDs

ID	Subtype	Headline and Description
ARTD-9754	Bug	[port] Errors and missing exclusive areas in Bswmd.arxml<*> Detailed description (how to reproduce it): Exclusive areas not available in <Module>_Bswmd.arxml Incorrectly formatted <Module>_Bswmd.arxml Preconditions: N.A. Test Case ID (internal TC that caught the defect) optional: N.A. Observed behavior: Missing exclusive areas in Davinci after integrating RTD !image-2021-04-12-19-29-09-321.png|thumbnail! Expected behavior: All exclusive areas are included in <Module>_Bswmd.arxml <Module>_Bswmd.arxml is valid Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution Fix the following issues and perform all the verification steps*: Issue #1 Some exclusive areas are missing because "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" files are not using the pattern expected by bswmd_creator script: "is used in function" Solution #1 From https://jira.sw.nxp.com/browse/AMPT-5710, bswmd_creator is parsing files "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" and it's looking up for the "is used in function" pattern. Therefore, "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" files shall use the following pattern for describing each exclusive area: <MODULE>_EXCLUSIVE_AREA_09 is used in function <Module>_StartChannel ... Issue #2 Missing exclusive areas mapped to IPL functions 2.1 Exclusive areas not referenced by any function in Adc_Bswmd.arxml, missing: <CAN-ENTER-EXCLUSIVE-AREA-REF DEST="EXCLUSIVE-AREA"> E.g.:{code:java} ADC_EXCLUSIVE_AREA_12 is used in function Adc_Sar_Ip_DoCalibration 2.2 Exclusive areas missing completely from Adc_Bswmd.arxml E.g.:{code:java} ADC_EXCLUSIVE_AREA_73 is used in function Ctu_Ip_SetFifoThreshold Solution #2 The integration manual shall map exclusive areas to public HLD functions (*no internal functions should be mentioned*). This is done by adding in "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" all the public HLD functions that are using an exclusive area via calls to IPL functions. For example: ADC_EXCLUSIVE_AREA_12 is used in function Adc_Calibrate to protect the ADC_MCR register from read/modify/write operation in Adc_Sar_Ip_Powerup. ADC_EXCLUSIVE_AREA_13 is used in function Adc_Init to protect the ADC_MCR register from read/modify/write operation in Adc_Sar_Ip_Powerup. ADC_EXCLUSIVE_AREA_13 is used in function Adc_SelfTest to protect the ADC_MCR register from read/modify/write operation in Adc_Sar_Ip_Powerup. [...] Exclusive Areas implemented in Low level driver layer (IPL) ADC_EXCLUSIVE_AREA_12 is used in function Adc_Sar_Ip_DoCalibration to protect the updates for: ADC_MCR register ADC_EXCLUSIVE_AREA_13 is used in function Adc_Sar_Ip_Powerup to protect the updates for: ADC_MCR register
Release notes		This adds in "Adc_Bswmd.arxml" the ADC Exclusive Area 12 for Adc_Calibrate and ADC Exclusive Area 13 for Adc_Init and Adc_SelfTest. It also keeps the note in Integration Manual about the EAs being used by IPL API functions Adc_Sar_Ip_Powerup and Adc_Sar_Ip_DoCalibration. Issue #3 Using uppercase hexadecimals for non-autosar API service IDs. Solution #3

ID	Subtype	Headline and Description
ARTD-9755	Bug	[pwm] Errors and missing exclusive areas in Bswmd.arxml<*> Detailed description (how to reproduce it): Exclusive areas not available in <Module>_Bswmd.arxml Incorrectly formatted <Module>_Bswmd.arxml Preconditions: N.A. Test Case ID (internal TC that caught the defect) optional: N.A. Observed behavior: Missing exclusive areas in Davinci after integrating RTD !image-2021-04-12-19-29-09-321.png|thumbnail! Expected behavior: All exclusive areas are included in <Module>_Bswmd.arxml <Module>_Bswmd.arxml is valid Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution Fix the following issues and perform all the verification steps*: Issue #1 Some exclusive areas are missing because "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" files are not using the pattern expected by bswmd_creator script: "is used in function" Solution #1 From https://jira.sw.nxp.com/browse/AMPT-5710, bswmd_creator is parsing files "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" and it's looking up for the "is used in function" pattern. Therefore, "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" files shall use the following pattern for describing each exclusive area: <MODULE>_EXCLUSIVE_AREA_09 is used in function <Module>_StartChannel ... Issue #2 Missing exclusive areas mapped to IPL functions 2.1 Exclusive areas not referenced by any function in Adc_Bswmd.arxml, missing: <CAN-ENTER-EXCLUSIVE-AREA-REF DEST="EXCLUSIVE-AREA"> E.g.:{code:java} ADC_EXCLUSIVE_AREA_12 is used in function Adc_Sar_Ip_DoCalibration 2.2 Exclusive areas missing completely from Adc_Bswmd.arxml E.g.:{code:java} ADC_EXCLUSIVE_AREA_73 is used in function Ctu_Ip_SetFifoThreshold Solution #2 The integration manual shall map exclusive areas to public HLD functions (*no internal functions should be mentioned*). This is done by adding in "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" all the public HLD functions that are using an exclusive area via calls to IPL functions. For example: ADC_EXCLUSIVE_AREA_12 is used in function Adc_Calibrate to protect the ADC_MCR register from read/modify/write operation in Adc_Sar_Ip_Powerup. ADC_EXCLUSIVE_AREA_13 is used in function Adc_Init to protect the ADC_MCR register from read/modify/write operation in Adc_Sar_Ip_Powerup. ADC_EXCLUSIVE_AREA_13 is used in function Adc_SelfTest to protect the ADC_MCR register from read/modify/write operation in Adc_Sar_Ip_Powerup. [...] Exclusive Areas implemented in Low level driver layer (IPL) ADC_EXCLUSIVE_AREA_12 is used in function Adc_Sar_Ip_DoCalibration to protect the updates for: ADC_MCR register ADC_EXCLUSIVE_AREA_13 is used in function Adc_Sar_Ip_Powerup to protect the updates for: ADC_MCR register
Release notes		This adds in "Adc_Bswmd.arxml" the ADC Exclusive Area 12 for Adc_Calibrate and ADC Exclusive Area 13 for Adc_Init and Adc_SelfTest. It also keeps the note in Integration Manual about the EAs being used by IPL API functions Adc_Sar_Ip_Powerup and Adc_Sar_Ip_DoCalibration. Issue #3 Using uppercase hexadecimals for non-autosar API service IDs. Solution #3

ID	Subtype	Headline and Description
ARTD-9758	Bug	[sai] Errors and missing exclusive areas in Bswmd.arxml<*> Detailed description (how to reproduce it): Exclusive areas not available in <Module>_Bswmd.arxml Incorrectly formatted <Module>_Bswmd.arxml Preconditions: N.A. Test Case ID (internal TC that caught the defect) optional: N.A. Observed behavior: Missing exclusive areas in Davinci after integrating RTD !image-2021-04-12-19-29-09-321.png|thumbnail! Expected behavior: All exclusive areas are included in <Module>_Bswmd.arxml <Module>_Bswmd.arxml is valid Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution Fix the following issues and perform all the verification steps*: Issue #1 Some exclusive areas are missing because "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" files are not using the pattern expected by bswmd_creator script: "is used in function" Solution #1 From https://jira.sw.nxp.com/browse/AMPT-5710, bswmd_creator is parsing files "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" and it's looking up for the "is used in function" pattern. Therefore, "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" files shall use the following pattern for describing each exclusive area: <MODULE>_EXCLUSIVE_AREA_09 is used in function <Module>_StartChannel ... Issue #2 Missing exclusive areas mapped to IPL functions 2.1 Exclusive areas not referenced by any function in Adc_Bswmd.arxml, missing: <CAN-ENTER-EXCLUSIVE-AREA-REF DEST="EXCLUSIVE-AREA"> E.g.:{code:java} ADC_EXCLUSIVE_AREA_12 is used in function Adc_Sar_Ip_DoCalibration 2.2 Exclusive areas missing completely from Adc_Bswmd.arxml E.g.:{code:java} ADC_EXCLUSIVE_AREA_73 is used in function Ctu_Ip_SetFifoThreshold Solution #2 The integration manual shall map exclusive areas to public HLD functions (*no internal functions should be mentioned*). This is done by adding in "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" all the public HLD functions that are using an exclusive area via calls to IPL functions. For example: ADC_EXCLUSIVE_AREA_12 is used in function Adc_Calibrate to protect the ADC_MCR register from read/modify/write operation in Adc_Sar_Ip_Powerup. ADC_EXCLUSIVE_AREA_13 is used in function Adc_Init to protect the ADC_MCR register from read/modify/write operation in Adc_Sar_Ip_Powerup. ADC_EXCLUSIVE_AREA_13 is used in function Adc_SelfTest to protect the ADC_MCR register from read/modify/write operation in Adc_Sar_Ip_Powerup. [...] Exclusive Areas implemented in Low level driver layer (IPL) ADC_EXCLUSIVE_AREA_12 is used in function Adc_Sar_Ip_DoCalibration to protect the updates for: ADC_MCR register ADC_EXCLUSIVE_AREA_13 is used in function Adc_Sar_Ip_Powerup to protect the updates for: ADC_MCR register
Release notes		This adds in "Adc_Bswmd.arxml" the ADC Exclusive Area 12 for Adc_Calibrate and ADC Exclusive Area 13 for Adc_Init and Adc_SelfTest. It also keeps the note in Integration Manual about the EAs being used by IPL API functions Adc_Sar_Ip_Powerup and Adc_Sar_Ip_DoCalibration. Issue #3 Using uppercase hexadecimals for non-autosar API service IDs. Solution #3

ID	Subtype	Headline and Description
ARTD-9763	Bug	[wdg] Errors and missing exclusive areas in Bswmd.arxml<*> Detailed description (how to reproduce it): Exclusive areas not available in <Module>_Bswmd.arxml Incorrectly formatted <Module>_Bswmd.arxml Preconditions: N.A. Test Case ID (internal TC that caught the defect) optional: N.A. Observed behavior: Missing exclusive areas in Davinci after integrating RTD !image-2021-04-12-19-29-09-321.png|thumbnail! Expected behavior: All exclusive areas are included in <Module>_Bswmd.arxml <Module>_Bswmd.arxml is valid Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution Fix the following issues and perform all the verification steps*: Issue #1 Some exclusive areas are missing because "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" files are not using the pattern expected by bswmd_creator script: "is used in function" Solution #1 From https://jira.sw.nxp.com/browse/AMPT-5710, bswmd_creator is parsing files "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" and it's looking up for the "is used in function" pattern. Therefore, "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" files shall use the following pattern for describing each exclusive area: <MODULE>_EXCLUSIVE_AREA_09 is used in function <Module>_StartChannel ... Issue #2 Missing exclusive areas mapped to IPL functions 2.1 Exclusive areas not referenced by any function in Adc_Bswmd.arxml, missing: <CAN-ENTER-EXCLUSIVE-AREA-REF DEST="EXCLUSIVE-AREA"> E.g.:{code:java} ADC_EXCLUSIVE_AREA_12 is used in function Adc_Sar_Ip_DoCalibration 2.2 Exclusive areas missing completely from Adc_Bswmd.arxml E.g.:{code:java} ADC_EXCLUSIVE_AREA_73 is used in function Ctu_Ip_SetFifoThreshold Solution #2 The integration manual shall map exclusive areas to public HLD functions (*no internal functions should be mentioned*). This is done by adding in "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" all the public HLD functions that are using an exclusive area via calls to IPL functions. For example: ADC_EXCLUSIVE_AREA_12 is used in function Adc_Calibrate to protect the ADC_MCR register from read/modify/write operation in Adc_Sar_Ip_Powerup. ADC_EXCLUSIVE_AREA_13 is used in function Adc_Init to protect the ADC_MCR register from read/modify/write operation in Adc_Sar_Ip_Powerup. ADC_EXCLUSIVE_AREA_13 is used in function Adc_SelfTest to protect the ADC_MCR register from read/modify/write operation in Adc_Sar_Ip_Powerup. [...] Exclusive Areas implemented in Low level driver layer (IPL) ADC_EXCLUSIVE_AREA_12 is used in function Adc_Sar_Ip_DoCalibration to protect the updates for: ADC_MCR register ADC_EXCLUSIVE_AREA_13 is used in function Adc_Sar_Ip_Powerup to protect the updates for: ADC_MCR register
Release notes		This adds in "Adc_Bswmd.arxml" the ADC Exclusive Area 12 for Adc_Calibrate and ADC Exclusive Area 13 for Adc_Init and Adc_SelfTest. It also keeps the note in Integration Manual about the EAs being used by IPL API functions Adc_Sar_Ip_Powerup and Adc_Sar_Ip_DoCalibration. Issue #3 Using uppercase hexadecimals for non-autosar API service IDs. Solution #3

ID	Subtype	Headline and Description
ARTD-9800	Bug	[ETH][S32CT] Incorrect constraint for EthEcucPartitionRefDef<*> Detailed description (how to reproduce it): # Enabled multicore (EthMulticoreSupport = true) # Configure 2 controllers and use the same partition for both controllers. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: An error is incorrectly reported by "EthEcucPartitionRefDef": "The referenced ECUC partition isn't used by any ETH controller (i.e. EthConfigSet/EthCtrlConfig/EthCtrlEcucPartitionRef)" even though it is used by 2 controllers. Expected behavior: No error is reported as it is a valid use case to have multiple controller assigned to the same partition. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: For node "EthEcucPartitionRefDef", the constraint counting the number of controllers referencing the partition should be changed to:{code:java} <constraint level="error" cond_expr="countOccurrences(system::getChildrenByASPath(`/AUTOSAR/EcucDefs/Eth/EthConfigSet/EthCtrlConfig/EthCtrlEcucPartitionRef`), x > (x.getValue() == $this.getValue())) >= 1" description="The referenced ECUC partition isn't used by any ETH controller (i.e. EthConfigSet/EthCtrlConfig/EthCtrlEcucPartitionRef)"/>
ARTD-9727	New	New Feature [GPT] Trigger Support for LPCMP ,,"The RTC configuration doesn't support the TRIGGER functionality for the LPCMP operation in STANDBY mode (section ""56.1.6 Interaction with RTC API to cause wakeup"" of the RM). For now, It has to be manually ""Ored"" in the application code. RTC->RTCC = RTC_RTCC_TRIG_EN_MASK;"

ID	Subtype	Headline and Description
ARTD-9731	Bug	[S32DS] Problematic Default Project<*> Detailed description (how to reproduce it): When creating a new empty project with the RTDs v0.9.0, it doesn't compile by default. To fix it, the user needs to Open the Peripherals CT, Add the Siul2Port component, and Update code and rebuild. The same conflict appears when creating a project from an Example, in this case, all the missing components have to be added. Preconditions: New S32DS Application Project, or New S32DS Project from Example. Observed behavior: Errors (3 items) fatal error: SchM_Mcu.h: (No such file or directory) Expected behavior: No Errors.

ID	Subtype	Headline and Description
ARTD-9732	Bug	[crypto] OsIf timeout implementation is non-uniform across drivers<*> Issue #1: The names of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Crypto, Pmic, Fls have "<Module>TimeoutOsifCounterType" Eep has "timeoutCounterType" Uart has "UartTimeoutType" The rest of them have "<Module>TimeoutMethod" Solution #1: All drivers shall rename the node introduced by ARTD-2232 to "<Module>TimeoutMethod". For example: CryptoTimeoutMethod FlsTimeoutMethod UartTimeoutMethod EepTimeoutMethod ... Issue #2: The names of the enumeration values of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Eep, Pmic have ["SYSTEM", "CUSTOM", "DUMMY'] Crypto has ["SYSTEM", "CUSTOM", "TICKS"] Fls has ["SYSTEM", "CUSTOM", "LOOP] Adc, Lin, Ocotp, Spi have ["SystemTimer", "CustomTimer", "DummyTimer"] Gpt has ["OSIF_COUNTER_SYSTEM, "OSIF_COUNTER_CUSTOM", "OSIF_COUNTER_NOT_USED"] The rest of them have ["OSIF_COUNTER_SYSTEM", "OSIF_COUNTER_CUSTOM", "OSIF_COUNTER_DUMMY"] Solution #2: All drivers shall rename the enumeration values of the node introduced by ARTD-2232 as follows: DummyTimer/Dummy/Ticks/etc > OSIF_COUNTER_DUMMY SystemTimer/System/etc >OSIF_COUNTER_SYSTEM CustomTimer/Custom/etc > OSIF_COUNTER_CUSTOM Issue #3: The available enumeration values of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Eth, Fr, I2c have only two enumeration values: ["OSIF_COUNTER_SYSTEM", "OSIF_COUNTER_CUSTOM" Solution #3: All drivers shall define the following three enumeration values for the node introduced by ARTD-2232: OSIF_COUNTER_DUMMY OSIF_COUNTER_SYSTEM OSIF_COUNTER_CUSTOM Issue #4: The default enumeration value of the node introduced by ARTD-2232 is inconsistent across drivers. For example: Eth, I2c, Uart have a default value of "OSIF_COUNTER_SYSTEM" Solution #4: All drivers shall set the default value of the node introduced by ARTD-2232 to "OSIF_COUNTER_DUMMY"

ID	Subtype	Headline and Description
ARTD-9833	New	New Feature [S32K3XX] Update MPU start end address format ,,"During configuring the MPU component in S32DS CT, the start address, end address and size of a region are in decimal format. It would be good if change its default format to hex value. See attached figures."
ARTD-14705	Bug	[BASE] "hasExclusiveOwnership" always throws error when the calling component is disabled ,,"Preconditions: S32DS 3.4 U1 B210415 S32CC_RTD_4_4_RTM_2_0_0_DS_updatesite_2104 (210413) Test Case ID (internal TC that caught the defect) optional: 1. Create project for S32R45 enable RTD 2. Open Peripherals tool 3. Add GMAC component 4. Disable GMAC component Observed behavior: The errors are still showed when disable component. The configurations in EthGeneral tab is still light. Expected behavior: The error should be disappeared and the configuration should be gray when disable component.
ARTD-9844	Bug	[CAN] [ds compared] wrong generated code for FifoWarnNotif/FifoOverflowNotif callbacks<*> Detailed description (how to reproduce it): CAN_TS_095 / S32K148 make generate for EB and S32CT => Verification point: two output should be similar => fail at this step code generated for fifo in all controllers (enhanced & legacy) in controller configuration array will be similar with latest controller. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: CAN_TC_FCT_0950 Observed behavior: !image-2021-04-16-14-52-34-442.png! Expected behavior: generated code of s32ct should be similar as EB's one Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-9852	Bug	[PORT] The BSWMD cannot link to the Non-ASR function<*> Detailed description (how to reproduce it): The PORT_EXCLUSIVE_AREA_04 do not linked to any API in after generate plugin with GENERATE_BSWMD_FILE=ON. The attachments are the output's BSWMD file and the exclusive input's .dox file. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: The PORT_EXCLUSIVE_AREA_04 do not linked to any API in after generate plugin with GENERATE_BSWMD_FILE=ON Expected behavior: The PORT_EXCLUSIVE_AREA_04 need to linked to Port_ResetPinMode Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-9905	Bug	[ADC]Header files found in src folder<*> For the components mentioned in the issue title, there are some header files misplaced under src folder and not under include folder. In Model-Based Design Toolbox for MATLAB and Simulink, we generate the projects automatically and need to copy all the dependencies. We explect to find only header files in the include and src files in src folder. This pattern is satisfied for all other modules but not for the mentioned ones. Also, the RTD veresion is 0.9.0 released on 26th of March, but in Jira I was not able to find this version marked as "Released". !image-2021-04-19-11-50-22-549.png!!image-2021-04-19-11-53-11-912.png! !image-2021-04-19-11-57-04-010.png! !image-2021-04-19-11-58-12-914.png!
ARTD-9911	New	New Feature [ADC] Improve documentation for Adc Set Clock Mode API ,,"NewWorkDescription: [ADC] Improve documentation for Adc Set Clock Mode API Add a separate chapter in ""Driver usage and configuration tips"" For details please see attached email thread."

ID	Subtype	Headline and Description
ARTD-9944	Bug	[CAN] Wrong constraint implementation for ECUC_Can_00113<*> Detailed description (how to reproduce it): Create S32K148 project Check range for Can Timeout Duration field in EB and S32CT Expected range: Range [1E-6 .. 65.535] (0.000001 > 65.535) EB range: 0.01 > 65.535 => uncorrect S32CT range: 0.00001 > 65.535 => uncorrect Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: detail in attached file Expected behavior: the range of EB and CT should be corrected as ECUC_Can_00113 srs Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description

ARTD-9991	New	New Feature
		
		[adc] Example project's name shall respect naming convention
		,,"1. What to do:
		All example projects shall respect the following naming convention:
		EBT Example Naming Convention:
		{code}<module_name>_<short_description>_<target>
		S32DS Example Naming Convention:
		HLD: {code}<module_name>_<short_description>_<target>
		Unshared IP: {code}<ip_name>_Ip_<short_description>_<target>
		Shared IP: {code}<ip_name>_<module_name>_Ip_<short_description>_<target>
		Where:
		<target> = <derivative> on platforms with a single core type
		<target> = <derivative>_<core_type> on platforms with multiple core types
		HLD Naming Examples:
		Eth_InternalLoopback_S32G274A_M7 for S32G2
		Eth_InternalLoopback_S32K148 for S32K1
		Eth_InternalLoopback_S32K344 for S32K3
		IP Naming Examples:
		Gmac_Ip_InternalLoopback_S32G274A_M7 for S32G2
		Enet_Ip_InternalLoopback_S32K148 for S32K1
		Gmac_Ip_InternalLoopback_S32K344 for S32K3
		2. How to do:
		To avoid having to manually maintain this, all the example makefiles shall contain the following:
		S32CC (where S32G274A will be replaced by the derivative you are targeting in that example):
		EXAMPLE_DERIVATIVE := S32G274A
		EXAMPLE_CORE_TYPE := M7
		ifeq ($(firstword $(SUPPORTED_CORE_TYPES)),$(lastword $(SUPPORTED_CORE_TYPES)))
		EXAMPLE_NAME := $(basename $(notdir $(lastword $(MAKEFILE_LIST))))_ $(EXAMPLE_DERIVATIVE)
		else
		EXAMPLE_NAME := $(basename $(notdir $(lastword $(MAKEFILE_LIST))))_ $(EXAMPLE_DERIVATIVE)_$(EXAMPLE_CORE_TYPE)
		endif
		To illustrate this, if your example's makefile is named ""Eth_InternalLoopback.mak"", then EXAMPLE_NAME will be evaluated to ""Eth_InternalLoopback_S32G274A_M7"".
		S32K1XX (where S32K148 will be replaced by the derivative you are targeting in that example):
		EXAMPLE_DERIVATIVE := S32K148
		ifeq ($(firstword $(SUPPORTED_CORE_TYPES)),$(lastword $(SUPPORTED_CORE_TYPES)))
		EXAMPLE_NAME := $(basename $(notdir $(lastword $(MAKEFILE_LIST))))_ $(EXAMPLE_DERIVATIVE)
		endif
		To illustrate this, if your example's makefile is named ""Eth_InternalLoopback.mak"", then EXAMPLE_NAME will be evaluated to ""Eth_InternalLoopback_S32K148"".
		S32K3XX (where S32K344 will be replaced by the derivative you are targeting in that example):
		EXAMPLE_DERIVATIVE := S32K344
		ifeq ($(firstword $(SUPPORTED_CORE_TYPES)),$(lastword $(SUPPORTED_CORE_TYPES)))
		EXAMPLE_NAME := $(basename $(notdir $(lastword $(MAKEFILE_LIST))))_ $(EXAMPLE_DERIVATIVE)
		endif
		To illustrate this, if your example's makefile is named ""Eth_InternalLoopback.mak"", then EXAMPLE_NAME will be evaluated to ""Eth_InternalLoopback_S32K344"".
		3. Caveats:
		For this to work properly, you need to:
		# Remove the platform/derivative name and configurator name from the filename of the makefile (e.g. ""Crc_Ip_Example_S32R45_DS.mak"" > ""Crc_Ip_Example.mak""). This will force you to create separate configurator and derivative folders (and

Release notes		**31 March 2023**

ID	Subtype	Headline and Description

ARTD-9995	New	New Feature
		
		[crypto] Example project's name shall respect naming convention
		,,"1. What to do:
		All example projects shall respect the following naming convention:
		EBT Example Naming Convention:
		{code}<module_name>_<short_description>_<target>
		S32DS Example Naming Convention:
		HLD: {code}<module_name>_<short_description>_<target>
		Unshared IP: {code}<ip_name>_Ip_<short_description>_<target>
		Shared IP: {code}<ip_name>_<module_name>_Ip_<short_description>_<target>
		Where:
		<target> = <derivative> on platforms with a single core type
		<target> = <derivative>_<core_type> on platforms with multiple core types
		HLD Naming Examples:
		Eth_InternalLoopback_S32G274A_M7 for S32G2
		Eth_InternalLoopback_S32K148 for S32K1
		Eth_InternalLoopback_S32K344 for S32K3
		IP Naming Examples:
		Gmac_Ip_InternalLoopback_S32G274A_M7 for S32G2
		Enet_Ip_InternalLoopback_S32K148 for S32K1
		Gmac_Ip_InternalLoopback_S32K344 for S32K3
		2. How to do:
		To avoid having to manually maintain this, all the example makefiles shall contain the following:
		S32CC (where S32G274A will be replaced by the derivative you are targeting in that example):
		EXAMPLE_DERIVATIVE := S32G274A
		EXAMPLE_CORE_TYPE := M7
		ifeq ($(firstword $(SUPPORTED_CORE_TYPES)),$(lastword $(SUPPORTED_CORE_TYPES)))
		EXAMPLE_NAME := $(basename $(notdir $(lastword $(MAKEFILE_LIST))))_ $(EXAMPLE_DERIVATIVE)
		else
		EXAMPLE_NAME := $(basename $(notdir $(lastword $(MAKEFILE_LIST))))_ $(EXAMPLE_DERIVATIVE)_$(EXAMPLE_CORE_TYPE)
		endif
		To illustrate this, if your example's makefile is named ""Eth_InternalLoopback.mak"", then EXAMPLE_NAME will be evaluated to ""Eth_InternalLoopback_S32G274A_M7"".
		S32K1XX (where S32K148 will be replaced by the derivative you are targeting in that example):
		EXAMPLE_DERIVATIVE := S32K148
		ifeq ($(firstword $(SUPPORTED_CORE_TYPES)),$(lastword $(SUPPORTED_CORE_TYPES)))
		EXAMPLE_NAME := $(basename $(notdir $(lastword $(MAKEFILE_LIST))))_ $(EXAMPLE_DERIVATIVE)
		endif
		To illustrate this, if your example's makefile is named ""Eth_InternalLoopback.mak"", then EXAMPLE_NAME will be evaluated to ""Eth_InternalLoopback_S32K148"".
		S32K3XX (where S32K344 will be replaced by the derivative you are targeting in that example):
		EXAMPLE_DERIVATIVE := S32K344
		ifeq ($(firstword $(SUPPORTED_CORE_TYPES)),$(lastword $(SUPPORTED_CORE_TYPES)))
		EXAMPLE_NAME := $(basename $(notdir $(lastword $(MAKEFILE_LIST))))_ $(EXAMPLE_DERIVATIVE)
		endif
		To illustrate this, if your example's makefile is named ""Eth_InternalLoopback.mak"", then EXAMPLE_NAME will be evaluated to ""Eth_InternalLoopback_S32K344"".
		3. Caveats:
		For this to work properly, you need to:
		# Remove the platform/derivative name and configurator name from the filename of the makefile (e.g. ""Crc_Ip_Example_S32R45_DS.mak"" > ""Crc_Ip_Example.mak""). This will force you to create separate configurator and derivative folders (and

Release notes		

ID	Subtype	Headline and Description

ARTD-9998	New	New Feature
		
		[eth] Example project's name shall respect naming convention
		,,"1. What to do:
		All example projects shall respect the following naming convention:
		EBT Example Naming Convention:
		{code}<module_name>_<short_description>_<target>
		S32DS Example Naming Convention:
		HLD: {code}<module_name>_<short_description>_<target>
		Unshared IP: {code}<ip_name>_Ip_<short_description>_<target>
		Shared IP: {code}<ip_name>_<module_name>_Ip_<short_description>_<target>
		Where:
		<target> = <derivative> on platforms with a single core type
		<target> = <derivative>_<core_type> on platforms with multiple core types
		HLD Naming Examples:
		Eth_InternalLoopback_S32G274A_M7 for S32G2
		Eth_InternalLoopback_S32K148 for S32K1
		Eth_InternalLoopback_S32K344 for S32K3
		IP Naming Examples:
		Gmac_Ip_InternalLoopback_S32G274A_M7 for S32G2
		Enet_Ip_InternalLoopback_S32K148 for S32K1
		Gmac_Ip_InternalLoopback_S32K344 for S32K3
		2. How to do:
		To avoid having to manually maintain this, all the example makefiles shall contain the following:
		S32CC (where S32G274A will be replaced by the derivative you are targeting in that example):
		EXAMPLE_DERIVATIVE := S32G274A
		EXAMPLE_CORE_TYPE := M7
		ifeq ($(firstword $(SUPPORTED_CORE_TYPES)),$(lastword $(SUPPORTED_CORE_TYPES)))
		EXAMPLE_NAME := $(basename $(notdir $(lastword $(MAKEFILE_LIST))))_ $(EXAMPLE_DERIVATIVE)
		else
		EXAMPLE_NAME := $(basename $(notdir $(lastword $(MAKEFILE_LIST))))_ $(EXAMPLE_DERIVATIVE)_$(EXAMPLE_CORE_TYPE)
		endif
		To illustrate this, if your example's makefile is named ""Eth_InternalLoopback.mak"", then EXAMPLE_NAME will be evaluated to ""Eth_InternalLoopback_S32G274A_M7"".
		S32K1XX (where S32K148 will be replaced by the derivative you are targeting in that example):
		EXAMPLE_DERIVATIVE := S32K148
		ifeq ($(firstword $(SUPPORTED_CORE_TYPES)),$(lastword $(SUPPORTED_CORE_TYPES)))
		EXAMPLE_NAME := $(basename $(notdir $(lastword $(MAKEFILE_LIST))))_ $(EXAMPLE_DERIVATIVE)
		endif
		To illustrate this, if your example's makefile is named ""Eth_InternalLoopback.mak"", then EXAMPLE_NAME will be evaluated to ""Eth_InternalLoopback_S32K148"".
		S32K3XX (where S32K344 will be replaced by the derivative you are targeting in that example):
		EXAMPLE_DERIVATIVE := S32K344
		ifeq ($(firstword $(SUPPORTED_CORE_TYPES)),$(lastword $(SUPPORTED_CORE_TYPES)))
		EXAMPLE_NAME := $(basename $(notdir $(lastword $(MAKEFILE_LIST))))_ $(EXAMPLE_DERIVATIVE)
		endif
		To illustrate this, if your example's makefile is named ""Eth_InternalLoopback.mak"", then EXAMPLE_NAME will be evaluated to ""Eth_InternalLoopback_S32K344"".
		3. Caveats:
		For this to work properly, you need to:
		# Remove the platform/derivative name and configurator name from the filename of the makefile (e.g. ""Crc_Ip_Example_S32R45_DS.mak"" > ""Crc_Ip_Example.mak""). This will force you to create separate configurator and derivative folders (and

Release notes		**31 March 2023**

ID	Subtype	Headline and Description
ARTD-9983	Bug	s32k3 FLS AutosarExt core selection<*> Detailed description (how to reproduce it): Create an S32K3 RTD SDK project and add the component "Fls", we can see the settings in "Fls Configuration => AutosarExt => Fls Using Core" is with wrong information. The core select pull-down list is not correct for S32K344 or S32K324 It still lists the CM33 core which is for s32k2tv not for s32k3xx See attached figure. Proposed solution optional: It should be FLS_CM7_CORE for S32K344 It should be FLS_CM7_CORE_0 or FLS_CM7_CORE_1 for S32K324
ARTD-9985	Bug	s32k324 s32ds project cannot add Fee component<*> Detailed description (how to reproduce it): Create an S32K324 project in S32DS3.4 with RTD 0.9.0. Try to add the component Fee, but it's missing in the list. I can see Fls but cannot see Fee. If creating an S32K344 project, it's able to add Fee component. Proposed solution optional: Add Fee component support for S32K324

ID	Subtype	Headline and Description

ARTD-10020	New	New Feature
		
		[sai] Example project's name shall respect naming convention
		,,"1. What to do:
		All example projects shall respect the following naming convention:
		EBT Example Naming Convention:
		{code}<module_name>_<short_description>_<target>
		S32DS Example Naming Convention:
		HLD: {code}<module_name>_<short_description>_<target>
		Unshared IP: {code}<ip_name>_Ip_<short_description>_<target>
		Shared IP: {code}<ip_name>_<module_name>_Ip_<short_description>_<target>
		Where:
		<target> = <derivative> on platforms with a single core type
		<target> = <derivative>_<core_type> on platforms with multiple core types
		HLD Naming Examples:
		Eth_InternalLoopback_S32G274A_M7 for S32G2
		Eth_InternalLoopback_S32K148 for S32K1
		Eth_InternalLoopback_S32K344 for S32K3
		IP Naming Examples:
		Gmac_Ip_InternalLoopback_S32G274A_M7 for S32G2
		Enet_Ip_InternalLoopback_S32K148 for S32K1
		Gmac_Ip_InternalLoopback_S32K344 for S32K3
		2. How to do:
		To avoid having to manually maintain this, all the example makefiles shall contain the following:
		S32CC (where S32G274A will be replaced by the derivative you are targeting in that example):
		EXAMPLE_DERIVATIVE := S32G274A
		EXAMPLE_CORE_TYPE := M7
		ifeq ($(firstword $(SUPPORTED_CORE_TYPES)),$(lastword $(SUPPORTED_CORE_TYPES)))
		EXAMPLE_NAME := $(basename $(notdir $(lastword $(MAKEFILE_LIST))))_ $(EXAMPLE_DERIVATIVE)
		else
		EXAMPLE_NAME := $(basename $(notdir $(lastword $(MAKEFILE_LIST))))_ $(EXAMPLE_DERIVATIVE)_$(EXAMPLE_CORE_TYPE)
		endif
		To illustrate this, if your example's makefile is named ""Eth_InternalLoopback.mak"", then EXAMPLE_NAME will be evaluated to ""Eth_InternalLoopback_S32G274A_M7"".
		S32K1XX (where S32K148 will be replaced by the derivative you are targeting in that example):
		EXAMPLE_DERIVATIVE := S32K148
		ifeq ($(firstword $(SUPPORTED_CORE_TYPES)),$(lastword $(SUPPORTED_CORE_TYPES)))
		EXAMPLE_NAME := $(basename $(notdir $(lastword $(MAKEFILE_LIST))))_ $(EXAMPLE_DERIVATIVE)
		endif
		To illustrate this, if your example's makefile is named ""Eth_InternalLoopback.mak"", then EXAMPLE_NAME will be evaluated to ""Eth_InternalLoopback_S32K148"".
		S32K3XX (where S32K344 will be replaced by the derivative you are targeting in that example):
		EXAMPLE_DERIVATIVE := S32K344
		ifeq ($(firstword $(SUPPORTED_CORE_TYPES)),$(lastword $(SUPPORTED_CORE_TYPES)))
		EXAMPLE_NAME := $(basename $(notdir $(lastword $(MAKEFILE_LIST))))_ $(EXAMPLE_DERIVATIVE)
		endif
		To illustrate this, if your example's makefile is named ""Eth_InternalLoopback.mak"", then EXAMPLE_NAME will be evaluated to ""Eth_InternalLoopback_S32K344"".
		3. Caveats:
		For this to work properly, you need to:
		# Remove the platform/derivative name and configurator name from the filename of the makefile (e.g. ""Crc_Ip_Example_S32R45_DS.mak"" > ""Crc_Ip_Example.mak""). This will force you to create separate configurator and derivative folders (and

Release notes		**31 March 2023**

ID	Subtype	Headline and Description

ARTD-10021	New	New Feature
		
		[sent] Example project's name shall respect naming convention
		,,"1. What to do:
		All example projects shall respect the following naming convention:
		EBT Example Naming Convention:
		{code}<module_name>_<short_description>_<target>
		S32DS Example Naming Convention:
		HLD: {code}<module_name>_<short_description>_<target>
		Unshared IP: {code}<ip_name>_Ip_<short_description>_<target>
		Shared IP: {code}<ip_name>_<module_name>_Ip_<short_description>_<target>
		Where:
		<target> = <derivative> on platforms with a single core type
		<target> = <derivative>_<core_type> on platforms with multiple core types
		HLD Naming Examples:
		Eth_InternalLoopback_S32G274A_M7 for S32G2
		Eth_InternalLoopback_S32K148 for S32K1
		Eth_InternalLoopback_S32K344 for S32K3
		IP Naming Examples:
		Gmac_Ip_InternalLoopback_S32G274A_M7 for S32G2
		Enet_Ip_InternalLoopback_S32K148 for S32K1
		Gmac_Ip_InternalLoopback_S32K344 for S32K3
		2. How to do:
		To avoid having to manually maintain this, all the example makefiles shall contain the following:
		S32CC (where S32G274A will be replaced by the derivative you are targeting in that example):
		EXAMPLE_DERIVATIVE := S32G274A
		EXAMPLE_CORE_TYPE := M7
		ifeq ($(firstword $(SUPPORTED_CORE_TYPES)),$(lastword $(SUPPORTED_CORE_TYPES)))
		EXAMPLE_NAME := $(basename $(notdir $(lastword $(MAKEFILE_LIST))))_ $(EXAMPLE_DERIVATIVE)
		else
		EXAMPLE_NAME := $(basename $(notdir $(lastword $(MAKEFILE_LIST))))_ $(EXAMPLE_DERIVATIVE)_$(EXAMPLE_CORE_TYPE)
		endif
		To illustrate this, if your example's makefile is named ""Eth_InternalLoopback.mak"", then EXAMPLE_NAME will be evaluated to ""Eth_InternalLoopback_S32G274A_M7"".
		S32K1XX (where S32K148 will be replaced by the derivative you are targeting in that example):
		EXAMPLE_DERIVATIVE := S32K148
		ifeq ($(firstword $(SUPPORTED_CORE_TYPES)),$(lastword $(SUPPORTED_CORE_TYPES)))
		EXAMPLE_NAME := $(basename $(notdir $(lastword $(MAKEFILE_LIST))))_ $(EXAMPLE_DERIVATIVE)
		endif
		To illustrate this, if your example's makefile is named ""Eth_InternalLoopback.mak"", then EXAMPLE_NAME will be evaluated to ""Eth_InternalLoopback_S32K148"".
		S32K3XX (where S32K344 will be replaced by the derivative you are targeting in that example):
		EXAMPLE_DERIVATIVE := S32K344
		ifeq ($(firstword $(SUPPORTED_CORE_TYPES)),$(lastword $(SUPPORTED_CORE_TYPES)))
		EXAMPLE_NAME := $(basename $(notdir $(lastword $(MAKEFILE_LIST))))_ $(EXAMPLE_DERIVATIVE)
		endif
		To illustrate this, if your example's makefile is named ""Eth_InternalLoopback.mak"", then EXAMPLE_NAME will be evaluated to ""Eth_InternalLoopback_S32K344"".
		3. Caveats:
		For this to work properly, you need to:
		# Remove the platform/derivative name and configurator name from the filename of the makefile (e.g. ""Crc_Ip_Example_S32R45_DS.mak"" > ""Crc_Ip_Example.mak""). This will force you to create separate configurator and derivative folders (and

Release notes		**31 March 2023**

ID	Subtype	Headline and Description

ARTD-10058	New	New Feature
		
		[gpt] Example project's name shall respect naming convention
		,,"1. What to do:
		All example projects shall respect the following naming convention:
		EBT Example Naming Convention:
		{code}<module_name>_<short_description>_<target>
		S32DS Example Naming Convention:
		HLD: {code}<module_name>_<short_description>_<target>
		Unshared IP: {code}<ip_name>_Ip_<short_description>_<target>
		Shared IP: {code}<ip_name>_<module_name>_Ip_<short_description>_<target>
		Where:
		<target> = <derivative> on platforms with a single core type
		<target> = <derivative>_<core_type> on platforms with multiple core types
		HLD Naming Examples:
		Eth_InternalLoopback_S32G274A_M7 for S32G2
		Eth_InternalLoopback_S32K148 for S32K1
		Eth_InternalLoopback_S32K344 for S32K3
		IP Naming Examples:
		Gmac_Ip_InternalLoopback_S32G274A_M7 for S32G2
		Enet_Ip_InternalLoopback_S32K148 for S32K1
		Gmac_Ip_InternalLoopback_S32K344 for S32K3
		2. How to do:
		To avoid having to manually maintain this, all the example makefiles shall contain the following:
		S32CC (where S32G274A will be replaced by the derivative you are targeting in that example):
		EXAMPLE_DERIVATIVE := S32G274A
		EXAMPLE_CORE_TYPE := M7
		ifeq ($(firstword $(SUPPORTED_CORE_TYPES)),$(lastword $(SUPPORTED_CORE_TYPES)))
		EXAMPLE_NAME := $(basename $(notdir $(lastword $(MAKEFILE_LIST))))_ $(EXAMPLE_DERIVATIVE)
		else
		EXAMPLE_NAME := $(basename $(notdir $(lastword $(MAKEFILE_LIST))))_ $(EXAMPLE_DERIVATIVE)_$(EXAMPLE_CORE_TYPE)
		endif
		To illustrate this, if your example's makefile is named ""Eth_InternalLoopback.mak"", then EXAMPLE_NAME will be evaluated to ""Eth_InternalLoopback_S32G274A_M7"".
		S32K1XX (where S32K148 will be replaced by the derivative you are targeting in that example):
		EXAMPLE_DERIVATIVE := S32K148
		ifeq ($(firstword $(SUPPORTED_CORE_TYPES)),$(lastword $(SUPPORTED_CORE_TYPES)))
		EXAMPLE_NAME := $(basename $(notdir $(lastword $(MAKEFILE_LIST))))_ $(EXAMPLE_DERIVATIVE)
		endif
		To illustrate this, if your example's makefile is named ""Eth_InternalLoopback.mak"", then EXAMPLE_NAME will be evaluated to ""Eth_InternalLoopback_S32K148"".
		S32K3XX (where S32K344 will be replaced by the derivative you are targeting in that example):
		EXAMPLE_DERIVATIVE := S32K344
		ifeq ($(firstword $(SUPPORTED_CORE_TYPES)),$(lastword $(SUPPORTED_CORE_TYPES)))
		EXAMPLE_NAME := $(basename $(notdir $(lastword $(MAKEFILE_LIST))))_ $(EXAMPLE_DERIVATIVE)
		endif
		To illustrate this, if your example's makefile is named ""Eth_InternalLoopback.mak"", then EXAMPLE_NAME will be evaluated to ""Eth_InternalLoopback_S32K344"".
		3. Caveats:
		For this to work properly, you need to:
		# Remove the platform/derivative name and configurator name from the filename of the makefile (e.g. ""Crc_Ip_Example_S32R45_DS.mak"" > ""Crc_Ip_Example.mak""). This will force you to create separate configurator and derivative folders (and

Release notes		

ID	Subtype	Headline and Description
ARTD-10104	Bug	[CAN] EPCtoDS importer fail when "Check ECUC-MODULE-DEF value" is selected ,,"Detailed description (how to reproduce it): Create a project on S32K148 Generate any configuration to get CAN.epc file Import to S32CT the above CAN.epc file (""Check ECUC-MODULE-DEF value"" is enabled by default) => error as in attached file Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: I see only CAN has this error. Expected behavior: No error when importing CAN.epc Proposed solution optional: [...]

ID	Subtype	Headline and Description

ARTD-10125	Bug	[PWM] eMIOS channel prescaler (clock divider) and prescaler clock source is not initialized when prescaler is disabled<*>
		
		Detailed description (how to reproduce it):
		The PWM driver does not initialize the eMIOS channel prescaler (UCEXTPRE) and eMIOS channel prescaler clock source (UCPRECLK) is case the prescaler clock (UCPREN) is disabled ("Clock prescaler" configuration parameter configured to EMIOS_PWM_CLOCK_NONE). The code which skips the initialization is as follows in Emios_Pwm_Ip_InitChannel:
		/ Configure internal prescaler /
		if (_EMIOS_PWM_CLOCK_NONE != userChCfg->internalPs)
		{
		Emios_Pwm_Ip_SetExtendedPrescaler(base, userChCfg->channelId, userChCfg->internalPs);
		Emios_Pwm_Ip_SetPrescalerSource(base, userChCfg->channelId, userChCfg->internalPsSrc);
		Emios_Pwm_Ip_SetPrescalerEnable(base, userChCfg->channelId, TRUE);
		}
		This is needed for the use case to have the PWM channel clock disabled after Pwm_Init() until it will be enabled by application.
		Preconditions:
		Prescaler clock disabled in eMIOS channel configuration.
		Test Case ID (internal TC that caught the defect) optional:
		N/A
		Observed behavior:
		eMIOS channel prescaler (UCEXTPRE) and eMIOS channel prescaler clock source (UCPRECLK) is not initialized by Pwm_Init() in case the prescaler clock (UCPREN) is disabled ("Clock prescaler" configuration parameter configured to EMIOS_PWM_CLOCK_NONE).
		Expected behavior:
		eMIOS channel prescaler (UCEXTPRE) and eMIOS channel prescaler clock source (UCPRECLK) is initialized by Pwm_Init() in case the prescaler clock (UCPREN) is disabled.
		Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)
		Proposed solution optional:
		Allow to initialize both prescaler (clock divider) and prescaler clock source even if prescaler is disabled.

ID	Subtype	Headline and Description
ARTD-10133	Bug	[can] Errors and missing exclusive areas in Bswmd.arxml<*> Detailed description (how to reproduce it): Exclusive areas not available in <Module>_Bswmd.arxml Incorrectly formatted <Module>_Bswmd.arxml Preconditions: N.A. Test Case ID (internal TC that caught the defect) optional: N.A. Observed behavior: Missing exclusive areas in Davinci after integrating RTD !image-2021-04-12-19-29-09-321.png|thumbnail! Expected behavior: All exclusive areas are included in <Module>_Bswmd.arxml <Module>_Bswmd.arxml is valid Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution Fix the following issues and perform all the verification steps*: Issue #1 Some exclusive areas are missing because "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" files are not using the pattern expected by bswmd_creator script: "is used in function" Solution #1 From https://jira.sw.nxp.com/browse/AMPT-5710, bswmd_creator is parsing files "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" and it's looking up for the "is used in function" pattern. Therefore, "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" files shall use the following pattern for describing each exclusive area: <MODULE>_EXCLUSIVE_AREA_09 is used in function <Module>_StartChannel ... Issue #2 Missing exclusive areas mapped to IPL functions 2.1 Exclusive areas not referenced by any function in Adc_Bswmd.arxml, missing: <CAN-ENTER-EXCLUSIVE-AREA-REF DEST="EXCLUSIVE-AREA"> E.g.:{code:java} ADC_EXCLUSIVE_AREA_12 is used in function Adc_Sar_Ip_DoCalibration 2.2 Exclusive areas missing completely from Adc_Bswmd.arxml E.g.:{code:java} ADC_EXCLUSIVE_AREA_73 is used in function Ctu_Ip_SetFifoThreshold Solution #2 The integration manual shall map exclusive areas to public HLD functions (*no internal functions should be mentioned*). This is done by adding in "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" all the public HLD functions that are using an exclusive area via calls to IPL functions. For example: ADC_EXCLUSIVE_AREA_12 is used in function Adc_Calibrate to protect the ADC_MCR register from read/modify/write operation in Adc_Sar_Ip_Powerup. ADC_EXCLUSIVE_AREA_13 is used in function Adc_Init to protect the ADC_MCR register from read/modify/write operation in Adc_Sar_Ip_Powerup. ADC_EXCLUSIVE_AREA_13 is used in function Adc_SelfTest to protect the ADC_MCR register from read/modify/write operation in Adc_Sar_Ip_Powerup. [...] Exclusive Areas implemented in Low level driver layer (IPL) ADC_EXCLUSIVE_AREA_12 is used in function Adc_Sar_Ip_DoCalibration to protect the updates for: ADC_MCR register ADC_EXCLUSIVE_AREA_13 is used in function Adc_Sar_Ip_Powerup to protect the updates for: ADC_MCR register
Release notes		This adds in "Adc_Bswmd.arxml" the ADC Exclusive Area 12 for Adc_Calibrate and ADC Exclusive Area 13 for Adc_Init and Adc_SelfTest. It also keeps the note in Integration Manual about the EAs being used by IPL API functions Adc_Sar_Ip_Powerup and Adc_Sar_Ip_DoCalibration. Issue #3 Using uppercase hexadecimals for non-autosar API service IDs. Solution #3

ID	Subtype	Headline and Description
ARTD-10157	New	New Feature [LIN][LPUART] update driver code according to all old requirements which have updates ,,"NewWorkDescription: There are an proposal changes for requirements on LPUART in Compare_Lpuart_Lin_Ip_Reqs_V2.xlsx(check latest version on https://crucible1.sw.nxp.com/cru/R-ARTD-496) file attached. The driver code should be updated according to all old requirements which have updates. All requirements removed and added, they will be implemented in other tickets. Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: NA"
ARTD-10160	Bug	[CanIf] EPCtoDS importer fail when "Check ECUC-MODULE-DEF value" is selected ,,"Detailed description (how to reproduce it): similar issue with https://jira.sw.nxp.com/browse/ARTD-10104, but for CANIF component Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: !image-2021-04-26-15-41-31-752.png! Expected behavior: !image-2021-04-26-15-42-23-609.png! Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-10177	Bug	[CAN] CanControllerBaudrateConfig elements is generated in unexpected order<*> Detailed description (how to reproduce it): CAN_TS_189: make generate => Can.epc, CanIf.epc import above .epcs to s32ct, generate code and run test => fail when using setBaudrate API with BaudRateConfigID param the generated order of baudrate array 's elements is unexpected Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: CAN_TC_FCT_1890 Observed behavior: please perform a comparation between attached output files Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description

ARTD-10178	Bug	[FLS]: When read data, sometime it will cause align error.
		
		,,"Detailed description (how to reproduce it):
		when I read a uint16 type variable, it will cause align problem and system will go to hard fault.
		After debug, I found the code implementation is not appropriate in file: C40_Ip.c, function: C40_Ip_Read_ProcesssData(). In this function, it will judge whether the address is alignment, but before the judgement, there has one sentence to initial the point, it will cause error when the address is not align with 4 bytes. so we need change the code.
		original code:
		uint32 u32ReadLength;
		uint32 u32TmpData = (uint32*)C40_Ip_u32ReadAddressPtr;
		suggest code:
		uint32 u32ReadLength;
		uint32 u32TmpData;
		/ Checking source is align/unaligned /
		u32CheckSourceAddress = ...;
		if (...)
		{
		/ Store data of source address /
		u32TmpData = (uint32*)C40_Ip_u32ReadAddressPtr;
		(uint32*)Fls_u32DestAddressPtr = u32TmpData;
		u32ReadLength = (uint32)FLS_SIZE_4BYTE;
		}
		else / unaligned or remain 4 bytes /
		{
		/ Store data of source address /
		u32TmpData = (uint8*)C40_Ip_u32ReadAddressPtr;
		(uint8*)Fls_u32DestAddressPtr = (uint8)u32TmpData;
		u32ReadLength = (uint32)FLS_SIZE_1BYTE;
		}
		Preconditions:
		NA
		Test Case ID (internal TC that caught the defect) optional:
		[...]
		Observed behavior:
		when We read a uint16 type variable, it will cause align problem and system will go to hard fault.
		Expected behavior:
		There are no hard fault when We read a uint16 type variable
		Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)
		Proposed solution optional:
		NA

ID	Subtype	Headline and Description
ARTD-10219	Bug	[CAN][EPC2CT importer] fifo filters list should have REQUIRE-INDEX option<*> Detailed description (how to reproduce it): CAN_TS_665 on S32K148 make generate GENERATOR := tresos => Can.epc, CanIf.epc import above .epcs to S32CT run the test => fail After comparing, many differences between two outputs (please take a look at attached files) This might relate to the absence of *REQUIRE-INDEX option on EB !image-2021-04-28-09-16-26-990.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: CAN_TS_665 Observed behavior: testcase can not run after import .epc to S32CT tool Expected behavior: Note:*_ ** I think it is better to add REQUIRE-INDEX option for all node that have type as list. for example: hw_objects, when mapping from EB to CT => the layout (appearance order on CT) is changed. The generated code is quitely identical but the look on CT-GUI is very different Proposed solution optional: [...]
ARTD-10220	New	New Feature [ADC] Fix and comment static analysis violations (MISRA + HIS + CERT-C) and VSMD reports S32K3XX ,,"Create MISRA, HIS & CERT-C reports VSMD reports Fix all violations for HIS MISRA VSMD reports Get LDRA static analysis report from ITG testing Fix all violations if any are found. Everything needs to be fixed (CCM <= 20, HIS LEVEL <= 6) in the code or commented in Coverity if it cannot be fixed. *Reference: MISRA Deviation List: [https://bitbucket.sw.nxp.com/projects/ASPA/repos/real_time_drivers/browse/Generic/SW%20Development/RTD%20MISRA%20Deviations.xlsx] [https://confluence.sw.nxp.com/pages/viewpage.action?pageId=133734230] RTD Quality Criteria: [https://bitbucket.sw.nxp.com/projects/ASPA/repos/real_time_drivers/browse/Generic/Quality%20Assurance/RTD%20AASWS%20Gate%20and%20Release%20Criteria.xlsx] VSMD report: 0 warning, 0 error for RTM release MISRA report: 0 unjustified MISRA violations HIS report: !image-2021-09-02-06-22-02-364.png! Guideline following: [https://confluence.sw.nxp.com/pages/viewpage.action?pageId=133734230]"

ID	Subtype	Headline and Description
ARTD-10265	New	New Feature [ADC] Update SetChannel feature ,,"NewWorkDescription: Implement/check SetChannel feature support on K1. Part of changes is checking if input channel is configured at initialization which impacts other platforms (K3 and G2) After implementing/checking the feature, requirements for it must be marked as 'fulfilled in': CPR_RTD_00328.adc CPR_RTD_00329.adc Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]"
ARTD-10279	Bug	[ICU][S32DS] The global driver variable generated with invalid 'static' keyword when configuring precompile mode in high layer<*> when driver in precompile mode and selecting no multicore , the building error appears as the output driver variable contains invalid keyword, the error as the following : !image-2021-05-04-13-33-25-860.png! this is due to the static is invalid as below: !image-2021-05-04-13-34-17-764.png!
ARTD-10287	New	New Feature [LIN] Flexio_lp should be configured frame size 8 bits for LIN frame ,,"NewWorkDescription: Currently, LIN driver over Flexio_lp is configured frame size 16 bits to transfer LIN frame. So, It can lead to total delay of LIN frame greater than normal as calculated in LIN specification: THeader_Maximum= 1.4 THeader_Nominal TResponse_Maximum= 1.4 TResponse_Nominal To transfer a break length, we can configure with frame size in TIMCMP register according to break length which is configured on EB or CT GUI. After break length was transferred, TIMCMP can be re-configured with frame size 8 bits. Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: NA"

ID	Subtype	Headline and Description
ARTD-10298	Bug	[WDG] Wrong generated code of some nodes (WdgEnableDirectService, WdgEnableClearResetRequest,..) ,,"Detailed description (how to reproduce it): Step 1: Prepare test with these config: WdgEnableDirectService of Instance 0 = false WdgEnableDirectService of Instance 1 = true Step 2: Generate the test Step 3: Check in generated file #define WDG_DIRECT_SERVICE_INSTANCE0 (STD_OFF) #define WDG_DIRECT_SERVICE_INSTANCE1(STD_ON) #define WDG_DIRECT_SERVICE (STD_ON) This issue is same with ClearResetRequest, WdgVersionInfoApi*. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: Wrong generated code with these config, this will make build fail because Wdg_43_Instance0_SetTriggerCondition guarded by WDG_DIRECT_SERVICE_INSTANCE0 define but Wdg_ChannelSetTriggerCondition guarded by WDG_DIRECT_SERVICE Expected behavior: Right generated code. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-10304	Bug	[CAN] Wrong MaxMbs in case of CanRamBlockSpecified<*> Detailed description (how to reproduce it): can_ts_1055 / s32K148 make generate GENERATOR:=tresos => Can.epc Import Can.epc to S32CT => build, run test fail Please see attached file for comparation between EB and S32CT Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: !image-2021-05-05-16-24-16-199.png! Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-10323	Bug	[CAN] [EB/CT compare] many significant differences for CAN_TS_066<*> Detailed description (how to reproduce it): CAN_TS_066 / S32K148 . make generate GENERATOR:=tresos => CAN.epc, CANif.epc . import aboves epc(s) to S32CT . build run test fail => see attached output files for detail specific ramblock will be generated wrongly for controllers with id > 0 Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: !image-2021-05-07-15-07-23-996.png! Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-10326	Bug	[FLS] In CT, Fls module under MCAL component, when the sector number more than 10, it will report error ,,"Detailed description (how to reproduce it): In CT, Fls module under MCAL component, when the sector number more than 10, it will report error. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: For example: I created Fls_sector0 Fls_sector9, and the fls physical sector is mapped from FLS_DATA_ARRAY_0_BLOCK_4_S0000 FLS_DATA_ARRAY_0_BLOCK_4_S0009. It works normal. Then I add one more sector named Fls_sector10. it will report error. and the physical sector mapped to FLS_DATA_ARRAY_0_BLOCK_4_S0010. I try to change the physical sector to FLS_DATA_ARRAY_0_BLOCK_4_S0011, then the error disappear, and i change back to FLS_DATA_ARRAY_0_BLOCK_4_S0010, it works ok. it's strange. Expected behavior: add more than 10 sectors according to the chip's real data flash size. example, if the chip data flash size is 128K, and each sector size is 8K, we should be add 16 sectors. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description

ARTD-10329	Bug	[ADC] Missing S32CT ADC configuration in IPL when only configuring ADC1 and incorrect DmaMuxSource in HLD<*>
		
		Detailed description (how to reproduce it):
		Issue 1: In ADC IPL with CT component, when configuring only ADC1 in UI
		There is no configuration for ADC1 is generated
		Issue 2: in ADC HLD with CT component, when ADC Dma counting node has no element, au8Adc_TransferringDmaMuxSource should be 0U as below
		#if (STD_ON == ADC_OPTIMIZE_DMA_STREAMING_GROUPS)
		.au8Adc_TransferringDmaMuxSource = \{ 0U, DMA_IP_REQ_MUX0_SARADC0 },
		#endif / (ADC_OPTIMIZE_DMA_STREAMING_GROUPS == STD_ON) /
		
		Preconditions:
		[...]
		Test Case ID (internal TC that caught the defect) optional:
		[...]
		Observed behavior:
		Missing ADC1 configuration
		Expected behavior:
		all configuration must be generated if configured
		Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)
		Proposed solution optional:
		[...]

ARTD-10355	Bug	[PWM] Fix HIS_PARAM and OVERRUN violation<*> Detailed description (how to reproduce it): HIS_PARAM|Measured value of PARAM metric 6.00 is higher than maximum value 5.00 allowed by the HIS metrics policy.|/ARTD-CIPWM-96/sources/S32CC_4.4/output/eclipse/plugins/Pwm_TS_T40D11M20I0R0/src/Pwm.c|Pwm_ValidateParamsPeriodDuty Misra report has the overrun violation as attached picture: Overrunning array "Ftm_Pwm_Ip_NotifIrq[instance]" of 12 bytes at byte offset 12 using index "channel 1U" (which evaluates to 6). Overrunning callee's array of size 6 by passing argument "channel 1U" (which evaluates to 6) in call to "Ftm_Pwm_Ip_UpdateChnInt". Overrunning callee's array of size 6 by passing argument "channel 1U" (which evaluates to 6) in call to "Ftm_Pwm_Ip_DisableCmpIrq". Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: HIS_PARAM violation Expected behavior: Has no HIS_PARAM violation Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Fix HIS_PARAM violation

ID	Subtype	Headline and Description
ARTD-10371	Bug	[I2c] I2c driver should support to transfer with buffer size up to uint16<*> For HLD, the u8BufferSize field from I2c_RequestType structure should be changed to type uint16.
ARTD-10373	Bug	[CRYPTO] Add Multiplicity related information to optional node HseKeyHandle in custom C01 xdm file<*> Add Multiplicity related information to optional node HseKeyHandle in custom C01 xdm file. Please update the following lines of the HseKeyHandle attribute: From: <a:a name="IMPLEMENTATIONCONFIGCLASS" type="IMPLEMENTATIONCONFIGCLASS"> <icc:v vclass="PreCompile">VariantPreCompile</icc:v> </a:a> To: <a:a name="IMPLEMENTATIONCONFIGCLASS" type="IMPLEMENTATIONCONFIGCLASS"> <icc:v mclass="PreCompile">VariantPreCompile</icc:v> <icc:v vclass="PreCompile">VariantPreCompile</icc:v> </a:a>
ARTD-10386	New	New Feature [ETH]Some functions have HIS_PARAM > 5 ,,"NewWorkDescription: Some functions have HIS_PARAM > 5: Gmac_Ip_MDIOReadMMD Gmac_Ip_MDIOWriteMMD GMAC_WriteManagementFrame Eth_Transmit Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: NA"
ARTD-10441	Bug	[S32K3] PlatformSDK - missing include dir "board" for GHS ,,"S32K3 RTD SDK does not add the ""board"" dir in the S32DS include paths for the GHS compiler. The compilation then fails on missing header file Clock_Ip_Cfg.h. If I manually add the ""board"" dir in the include paths, the build succeeds (see attached screenshot).

ID	Subtype	Headline and Description
ARTD-10403	New	New Feature [LIN] Update driver following PascalCase coding rule ,,"NewWorkDescription: remove pre fix in all variable following PascalCase except global variables Requirement source: PascalCase coding rule (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Update driver"
ARTD-10404	New	New Feature [LIN]Improve send/detect the wake up pulse ,,"NewWorkDescription: 1. For both LPUART_Lin_Ip and FLEXIO_Lin_Ip: For send wakeup pulse, we will no need to use timer to measure length of pulse. We just send 0xF0 or 0xF8, 0xFC, 0xFE, 0xFF(consider that 1 Start bit 0 is included in wakeup pulse). This way will allow us to generate a wake up pulse in 250us->5ms(we should generate maximum length if possible) To detect wakeup pulse longer 150us(we should detect minimum length if possible), we also check data received 0xFC or 0xFE or 0xFF(consider that 1 Start bit 0 is included in wakeup pulse). Frame error may be occurred and can be ignored if wakeup pulse received greater than the time of a frame. The LIN Baudrate from 1kbps->20kbps. So, the pulse always ensure in that range. Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Calculate number of bit in wakeup signal byte to send/receive depend on baudrate"
ARTD-10406	New	New Feature [LIN] Improve the way send or detect break field ,,"NewWorkDescription: 1. For FLEXIO_Lin_Ip only: For sending a break field, We will set frame size equal break length 13bits then framesize=12, Start bit 12bits data Stop bit(1bit break delimiter), so data=0x000. For detection break field in Slave mode. We will set frame size equal break length which is configured in ChannelList. To ensure the driver received correct break field, driver needs to compare with 0x00. And of course, break frame aways generate frame error when external master send break length greater than normal 11 bits of break detection. Frame size can be set via TIMCMPn register 2. For LPUART_Lin_Ip: the LPUART hardware already has mechanism to send or detect break field, so no need to improve. Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: NA"

ID	Subtype	Headline and Description
ARTD-10456	Bug	[ICU] The eMIOS_ICU cannot run into overflow callback function.<*> Detailed description (how to reproduce it): Create a project in which set an eMIOS channel to work in ICU signal measurement mode. You may select either global time base or channel internal counter for ICU channel. In both cases, overflow callback function cannot be accessed. In Emios_Icu_Ip_IrqHandler(), the variable bOverflow is set to FALSE and no any check in subsequent process and leads to unreachable overflow callback function. When using internal counter as ICU time base, the overflow callback function will be unconfigurable, like follow: !image-2021-05-13-11-01-35-146.png! Preconditions: S32DS 3.4 RTD 0.9.0 Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: The eMIOS_ICU cannot run into overflow callback function whenever overflow happen or not. Expected behavior: Overflow callback function should be accessible in ICU_MODE_SIGNAL_MEASUREMENT mode. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-10465	Bug	[GPT][S32DS] Stm_Ip_u32NextTargetValue undefined when config GPT change next timeout<*> When config GPT HLD on s32ct, enable GPT change next time out without enable ISR i got the build fail: !image-2020-12-18-15-09-38-225.png! [^Gpt.mex]
ARTD-10468	New	New Feature [CRC] Add support for CRC64 ,,"Detailed description (how to reproduce it): N/A Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: CRC driver code and configuration files do not support CRC64 mode Expected behavior: CRC driver code and configuration files must support CRC64 mode Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A"

ID	Subtype	Headline and Description
ARTD-10482	Bug	[ICU] Not able to configure eMIOS IPM mode for IcuUserModeForDutycycle parameter<*> Detailed description (how to reproduce it): For our application it is needed to use eMIOS IPM mode for ICU channel. We have seen in code that IPM low level function is available as follows: static inline void Emios_Icu_Ip_SignalMeasurementWithIPMMode (const uint8 u8ModuleIdx, const uint8 u8ChannelIdx, boolean bOverflow) { But in configuration of IcuUserModeForDutycycle parameter the IPM mode is missing. Preconditions: Using eMIOS channel IPM mode. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Not possible to configure eMIOS IPM mode for ICU channel Expected behavior: It is possible to configure eMIOS IPM mode for ICU channel Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Add IPM mode into configuration of IcuUserModeForDutycycle parameter.

ID	Subtype	Headline and Description

ARTD-10483	Bug	[PWM] eMIOS FEN bit always cleared while changing duty cycle for channels with DMA<*>
		
		Detailed description (how to reproduce it):
		We configure PWM channel which triggers DMA request (Flag Event response as EMIOS_PWM_DMA_REQUEST). After changing duty cycle we see that FEN bit is always cleared so no DMA request is generated.
		In "Emios_Pwm_Ip_SetDutyCycleOpwfmb" there is called "Emios_Pwm_Ip_SetInterruptRequest" before update of Reg
		A. The function Emios_Pwm_Ip_SetInterruptRequest checks if Emios_Pwm_Ip_aCheckEnableNotif[instance][channel] is set (in our case [0][9]) is "1", otherwise FEN is cleared:
		else
		{
		Emios_Pwm_Ip_aNotif[instance][channel] = (uint8)0U;
		Emios_Pwm_Ip_SetInterruptRequest(base, channel,
		(Emios_Pwm_Ip_aCheckEnableNotif[instance][channel] == 0U)? FALSE : TRUE);
		}
		The issue is that Emios_Pwm_Ip_aCheckEnableNotif[instance]
		[channel] is set to 1 only if function Emios_Pwm_Ip_SetFlagRequest (INSTANCE_0, 9, EMIOS_PWM_INTERRUPT_REQUEST) is called with parameter EMIOS_PWM_INTERRUPT_REQUEST. If it is called with EMIOS_PWM_DMA_REQUEST it will not be set and as such the FEN will then be cleared always while duty cycle is changed.
		Is there any way how to keep FEN enabled while changing duty cycle if the channel require DMA request (EMIOS_PWM_DMA_REQUEST)?
		Preconditions:
		Using eMIOS channel to generate DMA request (EMIOS_PWM_DMA_REQUEST).
		Test Case ID (internal TC that caught the defect) optional:
		N/A
		Observed behavior:
		FEN flag is always cleared while changing duty (no DMA request).
		Expected behavior:
		FEN flag is not cleared while changing duty cycle (so DMA request is generated).
		Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)
		Proposed solution optional:
		Do not clear FEN bit so that DMA request is generated.

ID	Subtype	Headline and Description
ARTD-10497	Bug	[SPI] FLEXIO does not work with AsyncTransmit when configure number instance of FLEXIO same to LPSPI<*> Detailed description (how to reproduce it): FLEXIO does not work with AsyncTransmit when configure number instance of FLEXIO same to LPSPI. As picture below, when I want to use FLEXIO_0, LPSPI configured must differ to instance 0. Note: This isssue can be occured on all of derivatives (K116, K118, K142, K144, K144W, K146, K148) !image-2021-05-17-09-24-31-276.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-10556	New	New Feature [LIN] Driver will generate a error if clock source too fast to refer ,,"NewWorkDescription: If clock source of any lin channel is too fast to refer, a error should be proposed to notify to user Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Add a checking clock source"
ARTD-10574	Bug	[mcu] Mcu_DistributePllClock function always returns E_NOT_OK when McuDevErrorDetect node is disabled<*> Detailed description (how to reproduce it): N/A Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Mcu_TC_FCT_0091 Observed behavior: Mcu_DistributePllClock function always returns E_NOT_OK when McuDevErrorDetect node is disabled Expected behavior: Need to update driver to return E_OK when McuDevErrorDetect node is disabled Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A

ID	Subtype	Headline and Description
ARTD-10713	Bug	[SPI] Many variables are having wrong naming.<*> Detailed description (how to reproduce it): Many variables are having wrong naming. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: None error Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-10733	Bug	[PWM] Critical AUTOSAR configuration parameter disabled and not usable<*> Detailed description (how to reproduce it): PWM configuration is not AUTOSAR compliant. Reference PwmMcuClockReferencePoint parameter is no longer used (being disabled in Pwm.xdm). This parameter is critical to determine PWM frequency based on the clock source in MCU. At application level this parameter is mandatory since without it correctly determining the frequency becomes problematic. This is not a catastrophic issue but is a serious issue, nevertheless... Preconditions: [none] Test Case ID (internal TC that caught the defect) optional: [none] Observed behavior: [see description] Expected behavior: [see description] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Enable reference to MCU clock parameter, use this parameter and divider from IP configuration to determine the number of tick. Autocalculate option should be enabled in XDM.

ID	Subtype	Headline and Description
ARTD-10736	Bug	[OCU][PWM][ICU][GPT] Timer drivers should have reference to MCL and MCU common configurations<*> _*Detailed description (how to reproduce it): When drivers use common resources from other drivers, these resources should be accessed via references to those drivers. For instance in case OCU, PWM and ICU when configured to use eMIOS IP, they might use a common bus configured in MCL. The configuration of each drivers should reference the bus configuration to access certain parameters that may be needed in their internal logic (number of configured counter ticks, dividers etc). Using a reference might also insure that invalid configuration of the bus are not exported to driver. Internal references which are NOT configured by the user SHOULD not be used since they might mask problems. PWM, OCU and GPT drivers should always use references to MCU driver even in cases where AUTOSAR does not require it since a reference to MCU clock will make much easier to determine the frequency of the given channel... For ICU this is not needed since in all cases the result of the ICU measurement is in ticks. Preconditions: [none] Test Case ID (internal TC that caught the defect) optional: [none] Observed behavior: [see description] Expected behavior: [see description] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:
ARTD-10779	New	New Feature [GPT] Add clarification in manuals if driver have conditional reentrant APIs ,,"There are APIs like ""Lptmr_Icu_Ip_EnableInterrupt with Reentrancy: Cond-Reentrant"" We need to add in manual clarification that this is related to EAs implementation to be used. The APIs are re-entrant as long as EAs are correctly implemented quarding the shared resource accessed in RMW operation."

ID	Subtype	Headline and Description
ARTD-10783	Bug	[gpt] Errors and missing exclusive areas in Bswmd.arxml<*> Detailed description (how to reproduce it): Exclusive areas not available in <Module>_Bswmd.arxml Incorrectly formatted <Module>_Bswmd.arxml Preconditions: N.A. Test Case ID (internal TC that caught the defect) optional: N.A. Observed behavior: Missing exclusive areas in Davinci after integrating RTD !image-2021-04-12-19-29-09-321.png|thumbnail! Expected behavior: All exclusive areas are included in <Module>_Bswmd.arxml <Module>_Bswmd.arxml is valid Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution Fix the following issues and perform all the verification steps*: Issue #1 Some exclusive areas are missing because "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" files are not using the pattern expected by bswmd_creator script: "is used in function" Solution #1 From https://jira.sw.nxp.com/browse/AMPT-5710, bswmd_creator is parsing files "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" and it's looking up for the "is used in function" pattern. Therefore, "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" files shall use the following pattern for describing each exclusive area: <MODULE>_EXCLUSIVE_AREA_09 is used in function <Module>_StartChannel ... Issue #2 Missing exclusive areas mapped to IPL functions 2.1 Exclusive areas not referenced by any function in Adc_Bswmd.arxml, missing: <CAN-ENTER-EXCLUSIVE-AREA-REF DEST="EXCLUSIVE-AREA"> E.g.:{code:java} ADC_EXCLUSIVE_AREA_12 is used in function Adc_Sar_Ip_DoCalibration 2.2 Exclusive areas missing completely from Adc_Bswmd.arxml E.g.:{code:java} ADC_EXCLUSIVE_AREA_73 is used in function Ctu_Ip_SetFifoThreshold Solution #2 The integration manual shall map exclusive areas to public HLD functions (*no internal functions should be mentioned*). This is done by adding in "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" all the public HLD functions that are using an exclusive area via calls to IPL functions. For example: ADC_EXCLUSIVE_AREA_12 is used in function Adc_Calibrate to protect the ADC_MCR register from read/modify/write operation in Adc_Sar_Ip_Powerup. ADC_EXCLUSIVE_AREA_13 is used in function Adc_Init to protect the ADC_MCR register from read/modify/write operation in Adc_Sar_Ip_Powerup. ADC_EXCLUSIVE_AREA_13 is used in function Adc_SelfTest to protect the ADC_MCR register from read/modify/write operation in Adc_Sar_Ip_Powerup. [...] Exclusive Areas implemented in Low level driver layer (IPL) ADC_EXCLUSIVE_AREA_12 is used in function Adc_Sar_Ip_DoCalibration to protect the updates for: ADC_MCR register ADC_EXCLUSIVE_AREA_13 is used in function Adc_Sar_Ip_Powerup to protect the updates for: ADC_MCR register
Release notes		This adds in "Adc_Bswmd.arxml" the ADC Exclusive Area 12 for Adc_Calibrate and ADC Exclusive Area 13 for Adc_Init and Adc_SelfTest. It also keeps the note in Integration Manual about the EAs being used by IPL API functions Adc_Sar_Ip_Powerup and Adc_Sar_Ip_DoCalibration. Issue #3 Using uppercase hexadecimals for non-autosar API service IDs. Solution #3

ID	Subtype	Headline and Description
ARTD-10899	New	New Feature [RM][S32K3][S32G] Analyze reentrancy of all apis and add support exclusive area for RM ,," Scan all IP: XRDC, MPU_M7, SEMA42, VIRT, AXBS, XBIC, PFLASH Analyze and update reentrancy NonASR_ServiceID.xml Xrdc_Ip_SetProcessID_Privileged is probably re-entrant function and need EA added. Look like MPU require interrupt disable to update regions need to analyze to add isr disable or add exernal assumption for customer"
ARTD-10911	Bug	[S32K3 RTM] OCU: Clock source and prescaler configuration do not match eMIOS ones<*> Detailed description (how to reproduce it): OCU eMIOS channel configuration has two parameters to describe clock sources: OcuClockSource (enum with the following labels OCU_SYSTEM_CLOCK, OCU_EXTERNAL_CLOCK, OCU_FIXED_FREQ_CLOCK) OcuEmiosBusSelect (enum with labels corresponding to buses: A, B/C/D, F or internal)Only the second parameter is usable but both parameters can be enabled and configured which is confusing. The bigger issues comes from the configuration of the prescaler which only allows DIV_1 to DIV_4 which limits the frequency ranges. The maximum divider should be DIV_16. I can assume that this is a porting issues since the used parameters exist on FTM IPs. Preconditions: none Test Case ID (internal TC that caught the defect) optional: none Observed behavior: Invalid frequency output. Expected behavior: see above Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Use only one clock/bus parameter (OcuClockSource) and update divider enum labels.

ID	Subtype	Headline and Description

ARTD-10925	Bug	[GPT] S32K3 PIT RTI generated code issue<*>
		
		Detailed description (how to reproduce it):
		Add PIT component and add both PIT timer channel and PIT RTI channel into the configuration.
		When code is generated for "Pit_Ip_Cfg_Defines.h":
		#define PIT_IP_RTI_USED (STD_ON)
		#define PIT_IP_REPORT_ERROR_STATUS (STD_OFF)
		In the generated code Pit_Ip_xxx_PBcfg.c, we can see that:
		Pit_Ip_ChannelConfigType PIT_0_ChannelConfig_PB[4U] =
		{
		/**@brief PitChannel_0 /
		{
		/ brief PIT Channel Id /
		0U,
		#if ((defined (PIT_IP_RTI_USED) && (PIT_IP_RTI_USED == STD_ON)) && (PIT_IP_REPORT_ERROR_STATUS == STD_ON)_*)
		/**< brief errorReportCallBack /
		NULL_PTR,
		#endif
		/ brief PIT Enable Interrupt /
		(boolean)(TRUE),
		/ brief PIT callback name /
		&Pit0_Ch0_Callback,
		/ brief PIT callbackparam /
		(uint8)0U
		}
		.....
		In above code, there is the macro "*_PIT_IP_REPORT_ERROR_STATUS " used in the structure.
		But in "Pit_Ip_Type.h", this macro is not used:
		typedef struct
		{
		uint8 hwChannel; /**< brief Timer channel number /
		#if (defined (PIT_IP_RTI_USED) && (PIT_IP_RTI_USED == STD_ON))
		errorReportCallBackType errorReportCallBack; /**< brief errorReportCallBack /
		#endif
		boolean enableInterrupt; /**< brief Enable interrupt generation /
		Pit_Ip_CallbackType callback; /**< brief callback /
		uint8 callbackParam; /**< brief callbackParam /
		} Pit_Ip_ChannelConfigType;
		So there will be compiling error.
		Proposed solution optional:
		I think the macro "*_PIT_IP_REPORT_ERROR_STATUS " should not be used in the generated code "Pit_Ip_xxx_PBcfg.c.

ID	Subtype	Headline and Description
ARTD-10923	Bug	[SAI] Tx and Rx can not work in the same time like duplex mode.<*> Detailed description (how to reproduce it): [When implement a new SAI Async transfer after starting a SAI Async receive with the same instance, test the Tx status, the issue happens, vice versa.] Preconditions: [RTD version 0.9.0, S32DS 3.4(GCC 9.2), SAI(master) communicate with codec sgtl5000(slave) in I2S protocol, both Tx and Rx used the same SAI instance, Rx work in Async mode, Tx work in Sync with other.] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [capture the Tx data line ,find nothing, Frame Sync has no signal, debug and find that the TE bit is not enabled at all, vice versa.] Expected behavior: [Tx and Rx can work well independent while another one is working, like duplex mode.] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [Remove the Rx status checking when prepare to implement Tx, vice versa.]
ARTD-10962	Bug	[ADC] Adc_ReadRawData read data from control channel index (SC index) instead of physical channel id<*> Detailed description (how to reproduce it): Adc_ReadRawData read data from control channel index (SC index) instead of physical channel id Preconditions: Adc_ReadRawData is enable Adc 0 group with channel SE6_ADCH6, SE14_ADCH14 Test Case ID (internal TC that caught the defect) optional: Adc_TC_1801 Adc_TS_021 Observed behavior: Start group of adc 0 Wait until complete flag of SC1 channel set Adc_ReadRawData with channel array {6, 14} Real status: wrong data in buffer read group {0 , 0} Complete flag check failed because input parameter is physical channel Expected behavior: Read group buffer matching with {0xE35, 0xE7C} Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA

ID	Subtype	Headline and Description
ARTD-10967	New	New Feature [SAI] SAI IP generate defines with instance number ,,"NewWorkDescription: SAI IP generate defines with instance number Update IPL example to replace defines from main.c: #define INST_SAI0 0U #define INST_SAI1 1U Requirement source: Usability improvement Proposed solution optional: name proposal (caps of configuration name)_(functional group name)_INSTANCE !image-2021-05-25-15-50-56-879.png|thumbnail! [...]"
ARTD-10970	Bug	[FLS] Initialization sequence needs to comply with HW timing restrictions.<*> Per attached discussions with design, the AHB domain / Serial Flash domain reset must meet certain timing restrictions. Also after this reset the DLL chain must be reconfigured.
ARTD-10996	Bug	[PORT] Pad keep enable (PKE) bit can't be set when PortPin Pull Keeper option is selected<*> Detailed description (how to reproduce it): Pad keep enable bit is not set when PortPin Pull Keeper option is selected, and the generation code is _.pullKeep = PORT_PULL_KEEP_DISABLED, Preconditions: Select _PortPin Pull Keeper in PORT configuration Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Pad keep enable bit is not set when PortPin Pull Keeper option is selected Expected behavior: Pad keep enable bit should be set when PortPin Pull Keeper option is selected Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: CE's comment: in _generate_PB/Siul2_Port_Ip_PBcfg.c_, the Pull keep option is fixed, without any condition check from EB tresos parameter: [!VAR "pullKeep_IP" = "'PORT_PULL_KEEP_DISABLED'"!][!// There should have a condition to check whether _PortPin Pull Keeper_ is selected.

ID	Subtype	Headline and Description
ARTD-11010	New	New Feature [S32K3XX][PORT] (ITG) Create test case to check PKE/DFE/IFE bit in MSCR register ,,"Detailed description (how to reproduce it):* in MSCR register, which was have many bits, but the test case did not cover the operation of all bit, it is missing test to check PKE, DSE, IFE bit Test Case ID (internal TC that caught the defect) optional:* NA Observed behavior: !image-2021-05-27-14-48-41-848.png! Expected behavior: update/ create test case to check the operation of this bit, it need to be work correctly Note:* in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA"
ARTD-11038	Bug	[FLS] Update code and data sections for S32K312 derivatives<*> Detailed description (how to reproduce it): Issues might appear because of different block arrangement of S32K314 derivatives. Please analyze the attached email related to this issue. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: No issue Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-11037	Bug	[CRYPTO] Memory placement not respected by GCC with -O0<*> Detailed description (how to reproduce it): This seems to be a GCC toolchain issue impacting RTD drivers. When the optimization is set to O0, the #pragma GCC section directives from the MemMap files have no effect when applied to uninitialized variables defined with the "static" storage class and instead the variable is linked to the default section (bss). One consequence in Crypto driver with S32K344 is that when using the default linker file and MPU settings from the RTD package, the variable Crypto_aHseSrvDescriptor is linked to cacheable memory and the Crypto_Exts_FormatKeyCatalogs function fails with error code CRYPTO_RET_INVALID_PARAM if the data cache is enabled (D_CACHE_ENABLE macro defined in preprocessor settings). Issue noticed with Crypto, but could affect other modules. Observed behavior: #pragma GCC section directive not effective for "static" uninitialized variables when optimization = O0 Expected behavior: Variable section applied according to the pragma directive

ID	Subtype	Headline and Description
ARTD-11048	Bug	[ICU] Cannot configure mode for ICU channel when IPV name does not contain IPV name<*> Detailed description (how to reproduce it): This clone is for tracking the CI build for linked issue. Driver changes are in place but need build to pass incorporating the latest changes for examples in plugin generation. Please see details also on cloned ticket.
ARTD-11072	New	New Feature [ADC] Add overwrite enable to high level configurator ,,"NewWorkDescription: Add overwrite enable to high level configurator !image-2021-05-28-19-29-32-180.png|thumbnail! Currently can be configured by LowLevel configurator MCAL did not support this in the past Requirement source: N.A. Proposed solution optional: [...]"
ARTD-11073	Bug	[SAI] Driver does not support disabling clock after transmission (BCE)<*> Detailed description (how to reproduce it): the bit clock continues to be generated even after transmission has been complete this has impact on power consumption. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Proposed solution optional: Possible solution would be to clear BCE from last interrupt (need to decide how to implement when using DMA) Add support for BCE disable clock after transmission To decide if parameter is per instance or transmission

ID	Subtype	Headline and Description
ARTD-11075	Bug	[MCU] IPs functions should not be visible at HLD layers<*> Detailed description (how to reproduce it): According requirement: CPR_RTD_00227.mcu*: The BSW modules header file <module name>.h shall only export these interfaces which are absolutely required by upper layers. Rationale: E.g. internal interfaces shall not be visible at upper layers. => IPs functions should not be visible at HLD layers But in mcu driver including follow: Mcu.h > Mcu_IPW_Types.h > Clock_Ip.h Mcu.h > Mcu_IPW_Types.h > Power_Ip.h Mcu.h > Mcu_IPW_Types.h > Ram_Ip.h Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: IPs functions visible at HLD layers Expected behavior: IPs functions should not be visible at HLD layers Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Change the include <Ip>_Ip.h into <module>_IPW.c

ID	Subtype	Headline and Description

ARTD-11130	Bug	[MCL][LCU] All SetSync function need to avoid hardfault when users only use only one instance (Precondition:enable only clock for this instance)<*>
		
		Detailed description (how to reproduce it):
		Initialize Mcu and enable clock for only one instance
		initialize only one instance
		Call all set_sync functions
		Observed behavior:
		Go to Hardfault when go over the command to set value for the remaining instance
		Expected behavior:
		All set sync functions can work correctly without any errors.
		Proposed solution optional:
		My first proposal is to have a runtime check for each instance:
		if(0U != MaskValue[LCU_IP_HW_INST_0])
		{
		}
		if(0U != MaskValue[LCU_IP_HW_INST_1])
		{
		}
		
		__
		My second proposal is to have a precompile #define that is generated based on the configuration:
		if nothing is configured for an instance, then that instance shall not be used during runtime.
		#if (LCU_INSTANCE_COUNT >= 1U)
		#if (LCU_INSTANCE0_IS_CONFIGURED == STD_ON)
		RegValue = g_ptLcuBaseInstPtrArray[LCU_IP_HW_INST_0]->OUTEN;
		RegValue &= MaskValue[LCU_IP_HW_INST_0];
		RegValue = DataValue[LCU_IP_HW_INST_0];
		g_ptLcuBaseInstPtrArray[LCU_IP_HW_INST_0]->OUTEN = RegValue;
		#endif
		#endif
		#if (LCU_INSTANCE_COUNT >= 2U)
		#if (LCU_INSTANCE1_IS_CONFIGURED == STD_ON)
		RegValue = g_ptLcuBaseInstPtrArray[LCU_IP_HW_INST_1]->OUTEN;
		RegValue &= MaskValue[LCU_IP_HW_INST_1];
		RegValue = DataValue[LCU_IP_HW_INST_1];
		g_ptLcuBaseInstPtrArray[LCU_IP_HW_INST_1]->OUTEN = RegValue;
		#endif
		#endif

ID	Subtype	Headline and Description
ARTD-11141	Bug	[UART] Not possible to configure 460800 for DesireBaudrate parameter<*> Detailed description (how to reproduce it): Baudrate 460800 is missing in configuration of DesireBaudrate parameter, see here the possible values in Uart.xdm where 460800 is missing: <v:var name="DesireBaudrate" type="ENUMERATION"> .... <a:da name="RANGE"> <a:v>LPUART_UART_BAUDRATE_1200</a:v> <a:v>LPUART_UART_BAUDRATE_2400</a:v> <a:v>LPUART_UART_BAUDRATE_4800</a:v> <a:v>LPUART_UART_BAUDRATE_7200</a:v> <a:v>LPUART_UART_BAUDRATE_9600</a:v> <a:v>LPUART_UART_BAUDRATE_14400</a:v> <a:v>LPUART_UART_BAUDRATE_19200</a:v> <a:v>LPUART_UART_BAUDRATE_28800</a:v> <a:v>LPUART_UART_BAUDRATE_38400</a:v> <a:v>LPUART_UART_BAUDRATE_57600</a:v> <a:v>LPUART_UART_BAUDRATE_115200</a:v> <a:v>LPUART_UART_BAUDRATE_230400</a:v> Missing baudrate 460800 here <a:v>LPUART_UART_BAUDRATE_921600</a:v> <a:v>LPUART_UART_BAUDRATE_1843200</a:v> </a:da> </v:var> Preconditions: Application requires to use baudrate 460800. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Not possible to configure baudrate 460800. Expected behavior: Allow to configure baudrate 460800. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Add baudrate 460800 for DesireBaudrate parameter.
ARTD-11168	Bug	[FLS]Header files found in src folder<*> For the components mentioned in the issue title, there are some header files misplaced under src folder and not under include folder. In Model-Based Design Toolbox for MATLAB and Simulink, we generate the projects automatically and need to copy all the dependencies. We explect to find only header files in the include and src files in src folder. This pattern is satisfied for all other modules but not for the mentioned ones. Also, the RTD veresion is 0.9.0 released on 26th of March, but in Jira I was not able to find this version marked as "Released". !image-2021-04-19-11-50-22-549.png!!image-2021-04-19-11-53-11-912.png! !image-2021-04-19-11-57-04-010.png! !image-2021-04-19-11-58-12-914.png!

ID	Subtype	Headline and Description
ARTD-11169	Bug	[SAI]Header files found in src folder<*> For the components mentioned in the issue title, there are some header files misplaced under src folder and not under include folder. In Model-Based Design Toolbox for MATLAB and Simulink, we generate the projects automatically and need to copy all the dependencies. We explect to find only header files in the include and src files in src folder. This pattern is satisfied for all other modules but not for the mentioned ones. Also, the RTD veresion is 0.9.0 released on 26th of March, but in Jira I was not able to find this version marked as "Released". !image-2021-04-19-11-50-22-549.png!!image-2021-04-19-11-53-11-912.png! !image-2021-04-19-11-57-04-010.png! !image-2021-04-19-11-58-12-914.png!
ARTD-11182	New	New Feature [SAI] S32ConfiguratorTool and Tresos remove .members from structs (for C90 compliance), keep generated files bit-exact with Tresos" ,,"Tresos and S32CT file generation remove .members from structs (for C90 compliance) Validate dev_tests after changes Validate that IPL example is still compiling after changes.
ARTD-11221	Bug	[ecum] Compiler warning with several module.<*> Detailed description (how to reproduce it): Please see: The [link|https://community.nxp.com/t5/S32K3-Internal-Community/S32K3-RTD-MCAL-Removing-Compiler-warnings-and-MISRA-compliance/td-p/1251888] for detail information. I also try to compile one of our example(eclipse\plugins \Lin_TS_T40D34M9I0R0\examples\EBT\Lin_Example_EBT_Lpuart) in the package SW32K3_RTD_4.4_0.9.0 and it also have many compiler warning. Please see attached file for more information. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Our driver still have compiler warning. Expected behavior: Fix all compiler warning in our RTD driver. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A

ID	Subtype	Headline and Description
ARTD-11223	Bug	[base] Compiler warning with several module.<*> Detailed description (how to reproduce it): Please see: The [link|https://community.nxp.com/t5/S32K3-Internal-Community/S32K3-RTD-MCAL-Removing-Compiler-warnings-and-MISRA-compliance/td-p/1251888] for detail information. I also try to compile one of our example(eclipse\plugins \Lin_TS_T40D34M9I0R0\examples\EBT\Lin_Example_EBT_Lpuart) in the package SW32K3_RTD_4.4_0.9.0 and it also have many compiler warning. Please see attached file for more information. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Our driver still have compiler warning. Expected behavior: Fix all compiler warning in our RTD driver. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-11224	Bug	[can] Compiler warning with several module.<*> Detailed description (how to reproduce it): Please see: The [link|https://community.nxp.com/t5/S32K3-Internal-Community/S32K3-RTD-MCAL-Removing-Compiler-warnings-and-MISRA-compliance/td-p/1251888] for detail information. I also try to compile one of our example(eclipse\plugins \Lin_TS_T40D34M9I0R0\examples\EBT\Lin_Example_EBT_Lpuart) in the package SW32K3_RTD_4.4_0.9.0 and it also have many compiler warning. Please see attached file for more information. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Our driver still have compiler warning. Expected behavior: Fix all compiler warning in our RTD driver. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A

ID	Subtype	Headline and Description
ARTD-11227	Bug	[pwm] Compiler warning with several module.<*> Detailed description (how to reproduce it): Please see: The [link|https://community.nxp.com/t5/S32K3-Internal-Community/S32K3-RTD-MCAL-Removing-Compiler-warnings-and-MISRA-compliance/td-p/1251888] for detail information. I also try to compile one of our example(eclipse\plugins \Lin_TS_T40D34M9I0R0\examples\EBT\Lin_Example_EBT_Lpuart) in the package SW32K3_RTD_4.4_0.9.0 and it also have many compiler warning. Please see attached file for more information. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Our driver still have compiler warning. Expected behavior: Fix all compiler warning in our RTD driver. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-11229	Bug	[platform] Compiler warning with several module.<*> Detailed description (how to reproduce it): Please see: The [link|https://community.nxp.com/t5/S32K3-Internal-Community/S32K3-RTD-MCAL-Removing-Compiler-warnings-and-MISRA-compliance/td-p/1251888] for detail information. I also try to compile one of our example(eclipse\plugins \Lin_TS_T40D34M9I0R0\examples\EBT\Lin_Example_EBT_Lpuart) in the package SW32K3_RTD_4.4_0.9.0 and it also have many compiler warning. Please see attached file for more information. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Our driver still have compiler warning. Expected behavior: Fix all compiler warning in our RTD driver. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-11204	New	New Feature [I2C] Lpi2c should receive more than 256 bytes per transfer ,,Lpi2c receive function is limited to receive 256 bytes per transfer. The number of bytes that could be received in one transfer should be increased.

ID	Subtype	Headline and Description
ARTD-11205	Bug	cannot support MII mode configuration in S32_CT<*> Detailed description (how to reproduce it): [.The TXD2 & TXD3 and RXD2 & RXD3 signals required by EMAC MII mode cannot be allocated in S32_CT, as they have only one signal name for TXD2&TXD3(txd), and RXD2&RXD3(rxd)]!image-2021-06-03-15-21-05-193.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [The TXD2 & TXD3 and RXD2 & RXD3 signals required by EMAC MII mode can be allocated in S32_CT successfully as RM descripted] !image-2021-06-03-15-24-24-948.png! Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-11248	Bug	[LIN] Update autobaud rate feature for K3<*> Detailed description (how to reproduce it): Need update driver to can start input capture from FTM time and stop it when get timer between a rising and falling edge on the sync byte is done.
ARTD-11374	Bug	[SPI] Jump to hardfault in Spi_JobTransferFinished is called twice<*> Detailed description (how to reproduce it): If Job result is failed but the Spi_Cancel is called in case don't know the job result. An hard fault will available because AsyncCrtSequenceState is assigned to null (The Spi_JobTransferFinished is called twice in both interrupt and Spi_Cancel) Preconditions: First Sequence is pending, after that call Spi_Cancel. But in this time, the tranferring job is failed. Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-11382	Bug	[PWM] Remove ASR specific validation from NonAsr component<*> Detailed description (how to reproduce it): build the plugins and s32ct component for PWM Create a new example for K3XX and add Emios_pwm_ip compoenent to the project A lot of errors are thrown in the error log because validation of some nodes require the HLD nodes to be present. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: Errors are thrown in the error log of S32DS from invalid validation constraints. !image-2021-06-08-16-39-47-179.png|thumbnail! After a look in the template file it seems that this impacts all IPs of PWM driver. Expected behavior: No errors are present for any of the IPL components. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Guard in the template file the validations that are using nodes from ASR mode. This should be done for all available IPs.
ARTD-11406	Bug	[FEE] Fix compiler warnings<*> Detailed description (how to reproduce it): See the attached file for more details Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: iar warnings Expected behavior: no warnings Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-11448	New	New Feature [SAI] Add the check for shared pins between Transmitter and Receiver ,,Add the check at configuration time that TX and RX do not use same lines simultaneously if full duplex mode is set

ID	Subtype	Headline and Description
ARTD-11528	New	New Feature [FEE] If these conditions are not satisfied. The Fee_Init() return FEE_E_INIT_FAILED ,,"NewWorkDescription: CPR_RTD_00563.fee:If the parameter checking for the driver's initialization function is enabled, the Configuration pointer argument shall be checked with the following conditions: In the supportedConfigVariants VariantPreCompile and VariantLinkTime if only one configuration variant set is used, the initialization function does not need nor evaluate the passed argument. Thus the Configuration pointer shall have a NULL_PTR value. In the supportedConfigVariant VariantPostBuild or if multiple configuration variant sets are used, the initialization function requires the passed argument. Thus the Configuration pointer shall be different from NULL_PTR. If these conditions are not satisfied, a Development error with type <MIP>_E_INIT_FAILED shall be reported to Development Error Tracer (Det) Requirement source: cPRD (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: NA"
ARTD-11644	New	New Feature [I2C] CPR_RTD_00190 regarding disabling Dem_SetEventStatus should be implemented ,,"CPR_RTD_00190.i2c should be implemented. All modules which need to call Dem module shall provide a configuration parameter for disabling all calls of Dem_SetEventStatus. If this parameter is activated, no call of Dem_SetEventStatus must be performed. Per default, the call of Dem_SetEventStatus shall be allowed."
ARTD-11663	Bug	[WDG] Some functions missing in UM chapter 6.2<*> Detailed description (how to reproduce it): Some functions missing in UM chapter 6.2 Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-11664	Bug	[I2C] Channel ID and channel index are not match on CT configuration<*> Detailed description (how to reproduce it): Channel ID and channel index are not match on CT configuration, it cause some problem if user config like that Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Add a constraint to check match between channel id and channel index
ARTD-11700	Bug	[PWM] Mismatch the macro definition<*> Detailed description (how to reproduce it): Mismatch the macro definition in Flexio IP layer #if (defined(FLEXIO_PWM_IP_HAS_PIN_OVERRIDE) && (FLEXIO_PWM_IP_HAS_PIN_OVERRIDE == STD_ON)) #if (defined(FLEXIO_PWM_IP_HAS_PIN_OVERRIDE) && (FLEXIO_PWM_IP_HAS_PIN_OVERRIDE == TRUE)) There are drivers that use '#if' preprocessor directives like follow: '#if (COMPILING_CONDITION == TRUE)' or '#if (COMPILING_CONDITION == STD_ON)', or both See also the discussions on this https://teams.microsoft.com/l/message/19:664e0ee3787240d2b4cbd1f568eaab8b@thread.tacv2/1623815330575?tenantId=686ea1d3-bc2b-4c6f-a92c-d99c5c301635&groupId=f9decd68-7b74-4101-a4d2-ad54e86f727f&parentMessageId=1623815330575&teamName=Zebra&channelName=Group%206&createdTime=1623815330575 Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: Need to align the macro definition Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Replace in the code 'COMPILING_CONDITION == TRUE' by 'COMPILING_CONDITION == STD_ON' for consistency; this will also help us to fix violations of 'MISRA Rule 10.3' and to avoid the issues reported in this PR https://bitbucket.sw.nxp.com/projects/ARTD/repos/base/pull-requests/520/overview?commentId=861452

ID	Subtype	Headline and Description
ARTD-11763	New	New Feature [GPT] Improve Predefine Timer functionality in Design Studio ,,"NewWorkDescription: PredefTimer functionality should automatically calculate the prescaler based on mcu clock reference and selected period value(1us or 100us) Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]"
ARTD-11761	New	New Feature [FLS] Investigate to remove unused configurations in the driver ,,"NewWorkDescription: Investigate the two unused nodes in FlsSectorList: *FlsProgrammingSize & *FlsPhysicalSectorUnlock If they are temporarily unused, they should be greyed out to notice to the users. In case of removing, these items should be considered: Check and remove the related constraint with other nodes Check and remove the corresponding resources in the resource files Remove generated code in *Fls_PBcfg.c and the corresponding structures in *Fls_Types.h*: paSectorUnlock Fls_ProgSizeType Remove the related CRC calculation in both generated code and the driver code Requirement source: (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Add list to select"
ARTD-11772	Bug	[PORT] Re-check all the bitfields in MSCR registers<*> Detailed description (how to reproduce it): Re-check all the bitfield in MSCR registers. Check one by one if that bitfield can be enabled/disabled when user using Port_Init and other functions. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Re-check all the bitfield in MSCR registers. Check one by one if that bitfield can be enabled/disabled when user using Port_Init and other functions. Expected behavior: All bitifields in MSCRs/PCRs should work correctly Proposed solution optional: All bitifields in MSCRs/PCRs should check again in the code

ID	Subtype	Headline and Description
ARTD-11781	Bug	[ICU] Prescaler configuration do not match eMIOS ones<*> Detailed description (how to reproduce it): The bigger issues comes from the configuration of the prescaler which only allows DIV_1 to DIV_4 which limits the frequency ranges. The maximum divider should be DIV_16. I can assume that this is a porting issues since the used parameters exist on FTM IPs. Preconditions: none Test Case ID (internal TC that caught the defect) optional: none Observed behavior: Invalid frequency output. Expected behavior: see above Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update divider enum labels.
ARTD-11786	Bug	[PWM] Error sequence of function Pwm_ipw_SetPeriodAndDuty.<*> Detailed description (how to reproduce it): According to S32K3 Reference Manual Rev 2 DraftC p1878 "59.5.3.7.1 Overview", you must configure AS1, BS1, AS2, and BS2 before exiting GPIO mode.(BS1/BS2 are for period and AS1/AS2 are for duty when used as PWM mode in MCAL.) In MCAL PWM Driver's Pwm_ipw_SetPeriodAndDuty(), they are configured as follows: aeuroeuroaeuroeuroEmios_Pwm_Ip_SetOutputToNormal() aeuroeuroaeuroeuroEmios_Pwm_Ip_SetPeriod() aeuroeuroaeuroeuroEmios_Pwm_Ip_SetDutyCycle() Because mode is changed before configuring period and duty, it is not following description in Reference Manual. This issue also the same with function Pwm_Ipw_SetDutyCycle, Pwm_Ipw_SetDutyCycle_NoUpdate, Pwm_Ipw_SetPeriodAndDuty_NoUpdate. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: The sequence in the Pwm_ipw_SetPeriodAndDuty is not following description in Reference Manual Expected behavior: The sequence in the Pwm_ipw_SetPeriodAndDuty should follow description in Reference Manual Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A

ID	Subtype	Headline and Description
ARTD-12099	Bug	[MCL] Prescaler configuration do not match eMIOS ones<*> Detailed description (how to reproduce it): The bigger issues comes from the configuration of the prescaler which only allows DIV_1 to DIV_4 which limits the frequency ranges. The maximum divider should be DIV_16. I can assume that this is a porting issues since the used parameters exist on FTM IPs. Preconditions: none Test Case ID (internal TC that caught the defect) optional: none Observed behavior: Invalid frequency output. Expected behavior: see above Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update divider enum labels.
ARTD-12116	Bug	[UART][FLEXIO_UART] Timer Status Flag should be clear if there is no more data to transfer, transmission after the last byte are sent ,,"Detailed description (how to reproduce it): !screenshot-1.png|thumbnail! Link: https://community.nxp.com/t5/Kinetis-Microcontrollers/Understanding-FlexIO/ta-p/1115419 As above information Timer Status Flag (TIMSTAT) should be clear in Flexio_Uart_Ip_CheckTxOperation function to write new data to the SHITBUF register to start the transaction. Preconditions: [...]N/A Test Case ID (internal TC that caught the defect) optional: [...]N/A Observed behavior: [...] Timer Status Flag was not cleared in Flexio_Uart_Ip_CheckTxOperation function Expected behavior: [...] Timer Status Flag should be clear in Flexio_Uart_Ip_CheckTxOperation function by Flexio_Mcl_Ip_ClearTimerStatus Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-12134	Bug	[WDG] The Gpt timer may be stop wrongly<*> Problem detailed description (how to reproduce it): Depending of the WD timeout configured at Tresos and the execution rate of the function that requests the WD refresh, the WD driver can request to stops the refreshment without a real timing issue. Issue scenario: From background, the function Wdg_ChannelSetTriggerCondition(...) is executed to request or not the next watchdog refresh using the Gpt_StopTimer(). The Wdg_ChannelSetTriggerCondition(...) gets the time elapse from the last watchdog refresh using the Gpt_GetTimeElapse (it's done in an isr from a hw timer) and evaluates against a variable Wdg_au32Timeout. The variable Wdg_au32Timeout is also recalculated inside of the function Wdg_ChannelTrigger(...). This function is executed at the hw's timer isr, the one that refresh the watchdog. If the Wdg_ChannelTrigger(...) is executed in the middle of the Wdg_ChannelSetTriggerCondition(...), just after get the time elapsed and before enters at the exclusive area, depending of the times configured at Tresos and the execution rate of our function, the 'if' can stop the timer and don't refresh the watchdog anymore. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional [...] Trigger: [...] Observed behavior: The GPT timer is incorrectly stopped Expected behavior: The GPT timer is not stopped Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution (Optional): CE's comment: Gpt_GetTimeElapse should be put in the same ciritical section with the if condition so that it should not be interrupted by GPT ISR or Wdg_ChannelTrigger. The issue was fixed in MCAL legacy: MCAL-18638

ID	Subtype	Headline and Description
ARTD-12179	Bug	[fr] Fix inconsistency related to using 'TRUE' or 'FALSE' instead of 'STD_ON' or 'STD_OFF' for '#if' preprocessor directives<*> Detailed description : There are drivers that use '_*#if*_' preprocessor directives like follow: '_#if (COMPILING_CONDITION == TRUE*)_' or '_#if (COMPILING_CONDITION == STD_ON*)_', or both See also the discussions on this [post.|https://teams.microsoft.com/l/message/19:664e0ee3787240d2b4cbd1f568eaab8b@thread.tacv2/1623815330575?tenantId=686ea1d3-bc2b-4c6f-a92c-d99c5c301635&groupId=f9decd68-7b74-4101-a4d2-ad54e86f727f&parentMessageId=1623815330575&teamName=Zebra&channelName=Group%206&createdTime=1623815330575] Proposed solution*: Replace in the code '_COMPILING_CONDITION == TRUE*_' by '_COMPILING_CONDITION == STD_ON*_' for consistency; this will also help us to fix violations of '_MISRA Rule 10.3_' and to avoid the issues reported in this [PR|https://bitbucket.sw.nxp.com/projects/ARTD/repos/base/pull-requests/520/overview?commentId=861452]
ARTD-12145	Bug	[LIN] While loop does not end in dummy timer<*> Detailed description (how to reproduce it): In dummy TimeoutTick = timeoutUs !image-2021-06-24-16-46-20-356.png! And ElaspseTime cannot lager or equal to TimeoutTicks [!image-2021-06-24-16-47-05-151.png|width=1065,height=204,id=x_0-weu-d9-48f34d87019cb538a178648310d33971!|https://eu-prod.asyncgw.teams.microsoft.com/v1/objects/0-weu-d9-48f34d87019cb538a178648310d33971/views/imgo] because ElapsedTime always assigned to 1 [!image-2021-06-24-16-47-25-926.png|width=845,height=117,id=x_0-weu-d6-fb6611fd73346c7fc5b2caf3c1de9e5e!|https://eu-prod.asyncgw.teams.microsoft.com/v1/objects/0-weu-d6-fb6611fd73346c7fc5b2caf3c1de9e5e/views/imgo] Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-12185	Bug	[BUILD_ENV] Enum size inconsistency<*> Detailed description (how to reproduce it): Inconsistency found between GHS and GCC compilers regarding enum size. Due to the fact that enum size is compiler dependent, I found that GHS build generates 4bytes for a simple enum, and GCC generates only 1 byte*. This breaks the order of the members in my structures, thus adding unnecessary padding. Unlike GCC 6.3, it seems that GCC 9.2 has short_enum built-in , thus keeping its size as small as possible according to the enum values. (empirical observation, not found in documentation) Preconditions: Enum example typedef enum { CAN_43_LLCE_RECEIVE = 0U, /**< @brief Regular Receive */ CAN_43_LLCE_RECEIVE_AF, /**< @brief Receive with Advanced Features*/ CAN_43_LLCE_TRANSMIT /**< @brief Transmit MB */ } Can_43_LLCE_ObjType; Test Case ID (internal TC that caught the defect) optional: Observed behavior: enums doesn't have the same size between ghs and gcc (versions corresponding to reported version) Expected behavior: enums having the same size Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Possible solutions: # Add short_enum to GHS cfg.mak => 1 byte # Add fno-short-enums to GCC cfg.mak => 4 bytes # Use attribute__((packed)) as an alternative to short_enum. I know this is compiler dependent, but the chances are that it's well understood by many compilers. GHS and GCC have the same understanding on this keyword for sure. If the keyword is understood the same by all your release compilers, it's an alternative.
ARTD-12202	New	New Feature [MCU] Add support callback notification when using the IPL only ,,"NewWorkDescription: Now Mcu doesn't support callback notification function at IPL. some callback function should be supported when using IP layer only. ex: POWER_IP_VLPSA_NOTIFICATION Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Add support callback notification at IPL"

ID	Subtype	Headline and Description
ARTD-12226	New	New Feature [adc] Replace "NO_INIT" with "CLEARED" in memory section macros" ,,"1. Replace "NO_INIT" with "CLEARED" in the memory section identifiers of both source code files and documentation. For example: <MIP>_START_SEC_VAR_NO_INIT_UNSPECIFIED > <MIP>_START_SEC_VAR_CLEARED_UNSPECIFIED <MIP>_STOP_SEC_VAR_NO_INIT_32 > <MIP>_STOP_SEC_VAR_CLEARED_32 ... 2. In file "sections_to_be_defined_in_memmaph.dox", perform the following replacement in the description field of the "CLEARED" (formerly "NO_INIT") sections: "These variables are never cleared and never initialized by start-up code." > "These variables are cleared to zero by start-up code." 3. Move all zero-initialized variables into the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" 4. Remove all explicit zero-initializers in the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed; / implicit zero initialization*/ #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h"

ID	Subtype	Headline and Description
ARTD-12230	New	New Feature [crypto] Replace "NO_INIT" with "CLEARED" in memory section macros" ,,"1. Replace "NO_INIT" with "CLEARED" in the memory section identifiers of both source code files and documentation. For example: <MIP>_START_SEC_VAR_NO_INIT_UNSPECIFIED > <MIP>_START_SEC_VAR_CLEARED_UNSPECIFIED <MIP>_STOP_SEC_VAR_NO_INIT_32 > <MIP>_STOP_SEC_VAR_CLEARED_32 ... 2. In file "sections_to_be_defined_in_memmaph.dox", perform the following replacement in the description field of the "CLEARED" (formerly "NO_INIT") sections: "These variables are never cleared and never initialized by start-up code." > "These variables are cleared to zero by start-up code." 3. Move all zero-initialized variables into the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" 4. Remove all explicit zero-initializers in the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed; / implicit zero initialization*/ #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h"

ID	Subtype	Headline and Description
ARTD-12231	New	New Feature [dem] Replace "NO_INIT" with "CLEARED" in memory section macros" ,,"1. Replace "NO_INIT" with "CLEARED" in the memory section identifiers of both source code files and documentation. For example: <MIP>_START_SEC_VAR_NO_INIT_UNSPECIFIED > <MIP>_START_SEC_VAR_CLEARED_UNSPECIFIED <MIP>_STOP_SEC_VAR_NO_INIT_32 > <MIP>_STOP_SEC_VAR_CLEARED_32 ... 2. In file "sections_to_be_defined_in_memmaph.dox", perform the following replacement in the description field of the "CLEARED" (formerly "NO_INIT") sections: "These variables are never cleared and never initialized by start-up code." > "These variables are cleared to zero by start-up code." 3. Move all zero-initialized variables into the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" 4. Remove all explicit zero-initializers in the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed; / implicit zero initialization*/ #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h"

ID	Subtype	Headline and Description
ARTD-12232	New	New Feature [det] Replace "NO_INIT" with "CLEARED" in memory section macros" ,,"1. Replace "NO_INIT" with "CLEARED" in the memory section identifiers of both source code files and documentation. For example: <MIP>_START_SEC_VAR_NO_INIT_UNSPECIFIED > <MIP>_START_SEC_VAR_CLEARED_UNSPECIFIED <MIP>_STOP_SEC_VAR_NO_INIT_32 > <MIP>_STOP_SEC_VAR_CLEARED_32 ... 2. In file "sections_to_be_defined_in_memmaph.dox", perform the following replacement in the description field of the "CLEARED" (formerly "NO_INIT") sections: "These variables are never cleared and never initialized by start-up code." > "These variables are cleared to zero by start-up code." 3. Move all zero-initialized variables into the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" 4. Remove all explicit zero-initializers in the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed; / implicit zero initialization*/ #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h"

ID	Subtype	Headline and Description
ARTD-12234	New	New Feature [ecum] Replace "NO_INIT" with "CLEARED" in memory section macros" ,,"1. Replace "NO_INIT" with "CLEARED" in the memory section identifiers of both source code files and documentation. For example: <MIP>_START_SEC_VAR_NO_INIT_UNSPECIFIED > <MIP>_START_SEC_VAR_CLEARED_UNSPECIFIED <MIP>_STOP_SEC_VAR_NO_INIT_32 > <MIP>_STOP_SEC_VAR_CLEARED_32 ... 2. In file "sections_to_be_defined_in_memmaph.dox", perform the following replacement in the description field of the "CLEARED" (formerly "NO_INIT") sections: "These variables are never cleared and never initialized by start-up code." > "These variables are cleared to zero by start-up code." 3. Move all zero-initialized variables into the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" 4. Remove all explicit zero-initializers in the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed; / implicit zero initialization*/ #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h"

ID	Subtype	Headline and Description
ARTD-12236	New	New Feature [eth] Replace "NO_INIT" with "CLEARED" in memory section macros" ,,"1. Replace "NO_INIT" with "CLEARED" in the memory section identifiers of both source code files and documentation. For example: <MIP>_START_SEC_VAR_NO_INIT_UNSPECIFIED > <MIP>_START_SEC_VAR_CLEARED_UNSPECIFIED <MIP>_STOP_SEC_VAR_NO_INIT_32 > <MIP>_STOP_SEC_VAR_CLEARED_32 ... 2. In file "sections_to_be_defined_in_memmaph.dox", perform the following replacement in the description field of the "CLEARED" (formerly "NO_INIT") sections: "These variables are never cleared and never initialized by start-up code." > "These variables are cleared to zero by start-up code." 3. Move all zero-initialized variables into the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" 4. Remove all explicit zero-initializers in the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed; / implicit zero initialization*/ #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h"

ID	Subtype	Headline and Description
ARTD-12240	New	New Feature [fls] Replace "NO_INIT" with "CLEARED" in memory section macros" ,,"1. Replace "NO_INIT" with "CLEARED" in the memory section identifiers of both source code files and documentation. For example: <MIP>_START_SEC_VAR_NO_INIT_UNSPECIFIED > <MIP>_START_SEC_VAR_CLEARED_UNSPECIFIED <MIP>_STOP_SEC_VAR_NO_INIT_32 > <MIP>_STOP_SEC_VAR_CLEARED_32 ... 2. In file "sections_to_be_defined_in_memmaph.dox", perform the following replacement in the description field of the "CLEARED" (formerly "NO_INIT") sections: "These variables are never cleared and never initialized by start-up code." > "These variables are cleared to zero by start-up code." 3. Move all zero-initialized variables into the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" 4. Remove all explicit zero-initializers in the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed; / implicit zero initialization*/ #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h"

ID	Subtype	Headline and Description
ARTD-12225	New	New Feature [ICU] Improve generation for K3 after ZSE update of SIUL2 IP files ,,"Detailed description (how to reproduce it): [Current generation of SIUL2 IP files(updated to support multiple instances of SIUL2 for ZSE) will conduct to a error in generation and build.] Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [Successfully generation and build.] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]"

ID	Subtype	Headline and Description
ARTD-12242	New	New Feature [gpt] Replace "NO_INIT" with "CLEARED" in memory section macros" ,,"1. Replace "NO_INIT" with "CLEARED" in the memory section identifiers of both source code files and documentation. For example: <MIP>_START_SEC_VAR_NO_INIT_UNSPECIFIED > <MIP>_START_SEC_VAR_CLEARED_UNSPECIFIED <MIP>_STOP_SEC_VAR_NO_INIT_32 > <MIP>_STOP_SEC_VAR_CLEARED_32 ... 2. In file "sections_to_be_defined_in_memmaph.dox", perform the following replacement in the description field of the "CLEARED" (formerly "NO_INIT") sections: "These variables are never cleared and never initialized by start-up code." > "These variables are cleared to zero by start-up code." 3. Move all zero-initialized variables into the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" 4. Remove all explicit zero-initializers in the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed; / implicit zero initialization*/ #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h"

ID	Subtype	Headline and Description
ARTD-12243	New	New Feature [i2c] Replace "NO_INIT" with "CLEARED" in memory section macros" ,,"1. Replace "NO_INIT" with "CLEARED" in the memory section identifiers of both source code files and documentation. For example: <MIP>_START_SEC_VAR_NO_INIT_UNSPECIFIED > <MIP>_START_SEC_VAR_CLEARED_UNSPECIFIED <MIP>_STOP_SEC_VAR_NO_INIT_32 > <MIP>_STOP_SEC_VAR_CLEARED_32 ... 2. In file "sections_to_be_defined_in_memmaph.dox", perform the following replacement in the description field of the "CLEARED" (formerly "NO_INIT") sections: "These variables are never cleared and never initialized by start-up code." > "These variables are cleared to zero by start-up code." 3. Move all zero-initialized variables into the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" 4. Remove all explicit zero-initializers in the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed; / implicit zero initialization*/ #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h"

ID	Subtype	Headline and Description
ARTD-12245	New	New Feature [icu] Replace "NO_INIT" with "CLEARED" in memory section macros" ,,"1. Replace "NO_INIT" with "CLEARED" in the memory section identifiers of both source code files and documentation. For example: <MIP>_START_SEC_VAR_NO_INIT_UNSPECIFIED > <MIP>_START_SEC_VAR_CLEARED_UNSPECIFIED <MIP>_STOP_SEC_VAR_NO_INIT_32 > <MIP>_STOP_SEC_VAR_CLEARED_32 ... 2. In file "sections_to_be_defined_in_memmaph.dox", perform the following replacement in the description field of the "CLEARED" (formerly "NO_INIT") sections: "These variables are never cleared and never initialized by start-up code." > "These variables are cleared to zero by start-up code." 3. Move all zero-initialized variables into the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" 4. Remove all explicit zero-initializers in the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed; / implicit zero initialization*/ #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h"

ID	Subtype	Headline and Description
ARTD-12249	New	New Feature [ocu] Replace "NO_INIT" with "CLEARED" in memory section macros" ,,"1. Replace "NO_INIT" with "CLEARED" in the memory section identifiers of both source code files and documentation. For example: <MIP>_START_SEC_VAR_NO_INIT_UNSPECIFIED > <MIP>_START_SEC_VAR_CLEARED_UNSPECIFIED <MIP>_STOP_SEC_VAR_NO_INIT_32 > <MIP>_STOP_SEC_VAR_CLEARED_32 ... 2. In file "sections_to_be_defined_in_memmaph.dox", perform the following replacement in the description field of the "CLEARED" (formerly "NO_INIT") sections: "These variables are never cleared and never initialized by start-up code." > "These variables are cleared to zero by start-up code." 3. Move all zero-initialized variables into the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" 4. Remove all explicit zero-initializers in the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed; / implicit zero initialization*/ #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h"

ID	Subtype	Headline and Description
ARTD-12251	New	New Feature [port] Replace "NO_INIT" with "CLEARED" in memory section macros" ,,"1. Replace "NO_INIT" with "CLEARED" in the memory section identifiers of both source code files and documentation. For example: <MIP>_START_SEC_VAR_NO_INIT_UNSPECIFIED > <MIP>_START_SEC_VAR_CLEARED_UNSPECIFIED <MIP>_STOP_SEC_VAR_NO_INIT_32 > <MIP>_STOP_SEC_VAR_CLEARED_32 ... 2. In file "sections_to_be_defined_in_memmaph.dox", perform the following replacement in the description field of the "CLEARED" (formerly "NO_INIT") sections: "These variables are never cleared and never initialized by start-up code." > "These variables are cleared to zero by start-up code." 3. Move all zero-initialized variables into the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" 4. Remove all explicit zero-initializers in the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed; / implicit zero initialization*/ #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h"

ID	Subtype	Headline and Description
ARTD-12252	New	New Feature [pwm] Replace "NO_INIT" with "CLEARED" in memory section macros" ,,"1. Replace "NO_INIT" with "CLEARED" in the memory section identifiers of both source code files and documentation. For example: <MIP>_START_SEC_VAR_NO_INIT_UNSPECIFIED > <MIP>_START_SEC_VAR_CLEARED_UNSPECIFIED <MIP>_STOP_SEC_VAR_NO_INIT_32 > <MIP>_STOP_SEC_VAR_CLEARED_32 ... 2. In file "sections_to_be_defined_in_memmaph.dox", perform the following replacement in the description field of the "CLEARED" (formerly "NO_INIT") sections: "These variables are never cleared and never initialized by start-up code." > "These variables are cleared to zero by start-up code." 3. Move all zero-initialized variables into the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" 4. Remove all explicit zero-initializers in the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed; / implicit zero initialization*/ #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h"

ID	Subtype	Headline and Description
ARTD-12255	New	New Feature [rte] Replace "NO_INIT" with "CLEARED" in memory section macros" ,,"1. Replace "NO_INIT" with "CLEARED" in the memory section identifiers of both source code files and documentation. For example: <MIP>_START_SEC_VAR_NO_INIT_UNSPECIFIED > <MIP>_START_SEC_VAR_CLEARED_UNSPECIFIED <MIP>_STOP_SEC_VAR_NO_INIT_32 > <MIP>_STOP_SEC_VAR_CLEARED_32 ... 2. In file "sections_to_be_defined_in_memmaph.dox", perform the following replacement in the description field of the "CLEARED" (formerly "NO_INIT") sections: "These variables are never cleared and never initialized by start-up code." > "These variables are cleared to zero by start-up code." 3. Move all zero-initialized variables into the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" 4. Remove all explicit zero-initializers in the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed; / implicit zero initialization*/ #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h"

ID	Subtype	Headline and Description
ARTD-12258	New	New Feature [sent] Replace "NO_INIT" with "CLEARED" in memory section macros" ,,"1. Replace "NO_INIT" with "CLEARED" in the memory section identifiers of both source code files and documentation. For example: <MIP>_START_SEC_VAR_NO_INIT_UNSPECIFIED > <MIP>_START_SEC_VAR_CLEARED_UNSPECIFIED <MIP>_STOP_SEC_VAR_NO_INIT_32 > <MIP>_STOP_SEC_VAR_CLEARED_32 ... 2. In file "sections_to_be_defined_in_memmaph.dox", perform the following replacement in the description field of the "CLEARED" (formerly "NO_INIT") sections: "These variables are never cleared and never initialized by start-up code." > "These variables are cleared to zero by start-up code." 3. Move all zero-initialized variables into the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" 4. Remove all explicit zero-initializers in the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed; / implicit zero initialization*/ #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h"

ID	Subtype	Headline and Description
ARTD-12259	New	New Feature [spi] Replace "NO_INIT" with "CLEARED" in memory section macros" ,,"1. Replace "NO_INIT" with "CLEARED" in the memory section identifiers of both source code files and documentation. For example: <MIP>_START_SEC_VAR_NO_INIT_UNSPECIFIED > <MIP>_START_SEC_VAR_CLEARED_UNSPECIFIED <MIP>_STOP_SEC_VAR_NO_INIT_32 > <MIP>_STOP_SEC_VAR_CLEARED_32 ... 2. In file "sections_to_be_defined_in_memmaph.dox", perform the following replacement in the description field of the "CLEARED" (formerly "NO_INIT") sections: "These variables are never cleared and never initialized by start-up code." > "These variables are cleared to zero by start-up code." 3. Move all zero-initialized variables into the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" 4. Remove all explicit zero-initializers in the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed; / implicit zero initialization*/ #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h"

ID	Subtype	Headline and Description
ARTD-12262	New	New Feature [wdg] Replace "NO_INIT" with "CLEARED" in memory section macros" ,,"1. Replace "NO_INIT" with "CLEARED" in the memory section identifiers of both source code files and documentation. For example: <MIP>_START_SEC_VAR_NO_INIT_UNSPECIFIED > <MIP>_START_SEC_VAR_CLEARED_UNSPECIFIED <MIP>_STOP_SEC_VAR_NO_INIT_32 > <MIP>_STOP_SEC_VAR_CLEARED_32 ... 2. In file "sections_to_be_defined_in_memmaph.dox", perform the following replacement in the description field of the "CLEARED" (formerly "NO_INIT") sections: "These variables are never cleared and never initialized by start-up code." > "These variables are cleared to zero by start-up code." 3. Move all zero-initialized variables into the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" 4. Remove all explicit zero-initializers in the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed; / implicit zero initialization*/ #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h"

ID	Subtype	Headline and Description
ARTD-12290	Bug	[LIN] - Flexio irq handler channel parameter is not correct<*> Detailed description (how to reproduce it): A flexio lin channel contains 2 hw flexio channels (pairs of shiftertimer) Configure a flexio lin channel. Use another Mcl Flexio channel than 0 and 1. Driver don't check driver is initialized in ISR of IPV Flexio Preconditions: Follow req CPR_RTD_00011.lin: ISR shall check whether its respective driver is initialized. If the driver is not initialized, the ISR shall only clear interrupt status flag and return immediately. This requirement is implemented from Lpuart !image-2021-07-09-09-39-22-271.png! Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: In this case, the Mcl Flexio Irq is called using the shifter+timer pair channel number. Inside Flexio Lin driver, there is different scheme of channels which are using the pairs of shifter timer. This is why the wrong channel is addressed. Expected behavior: In Flexio Lin Irq, the correct channel must be addressed. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Add an easing mapping between the Mcl Flexio channels (hardware channels) and Flexio Lin channels (driver channels)
ARTD-12330	Bug	[ICU]: When add ICU module, it rely on MCL module even I didn't add emios CH ,,"Detailed description (how to reproduce it): I add ICU module in my project, and in ICU module I didn't add any EMIOS channel. But when generate code, EB Tresos Studio report error related with EMIOS. I need add MCL module, in MCL module, I didn't configure any item, just keep default value, then that error disappeared. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-12333	New	New Feature [gpt] RTD Clock source selection duplication in RTC and clock component ,,RTD Clock source selection duplication in RTC and clock component. More details please see the attachment.

ID	Subtype	Headline and Description
ARTD-12350	Bug	[GPT][eMIOS] The GPT channel prescaler doesn't support Extended Prescaler.<*> Detailed description (how to reproduce it): The GPT channel prescaler is up to 4, not the available max value 16 described in RM. (Extended Prescaler not support) !image-2021-07-01-11-18-21-749.png! Preconditions: S32DS3.4 RTD v0.9.0, LLD Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: Extended Prescaler (up to 16 frequency division) support for GPT channel. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-12352	Bug	[S32K3 RTM] OCU: The master bus of OCU channel will be wrongly changed to MC mode.<*> Detailed description (how to reproduce it): In ConfigTools, we must set the master bus of OCU channel to MCB up counter mode, or it will report an errors like follow: !image-2021-07-01-12-46-51-520.png! However, the API Emios_Ocu_Ip_Init() in Emios_Ocu_Ip.c sets the master bus to MC up counter mode. It's inconsistent. !image-2021-07-01-12-50-27-320.png|width=1305,height=440! Preconditions: S32DS3.4 RTD v0.9.0, LLD Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: The master bus of OCU should be set to MCB mode. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-12356	New	New Feature [ICU]: The channel number of WKPU will mislead customers ,,"In S32K3, there are total 64 wake up channels, and the first four channels are a special internal wake up source, start from the fifth wake up source are from external pin pads. In the Port module and the in the reference document, the number for internal and external are indepdent. This cause the number which configured in ICU module are not equal to document and which in port module, this will let customer confused. Is there any method to import it. Like we can change to drop-down box. This problem also exist for the interrupt isr name in ICU module, it named for 0 to 63, but in the reference document, the external source from 0 to 59, and the internal source have a special name for each one. !image-2021-07-01-15-16-20-716.png! !image-2021-07-01-15-15-57-316.png! !image-2021-07-01-15-15-34-451.png!"
ARTD-12353	Bug	[PWM][eMIOS] The restoration operation of Interrupt is not carried out when using DAOC PWM mode.<*> Detailed description (how to reproduce it): When we using RTD to configure PWM, the interrupt will be disabled and global variable Emios_Pwm_Ip_aNotif of corresponding channel will be set to 1 if 0% or 100% duty is required. Normally, the restoration operation of interrupt will be carried out when set to other duty. Just for explanation, take the OPWMT PWM mode as an example like follow: !image-2021-07-01-13-56-39-589.png! However, when using DAOC PWM mode, the restoration operation of Interrupt is not carried out: !image-2021-07-01-13-44-20-879.png! Besides, in the config structure generated by Emios_Pwm component, if it is DAOC PWM mode, the generated mode is incorrect, it should be EMIOS_PWM_MODE_DAOC_FLAG: !image-2021-07-01-14-03-46-346.png! Preconditions: S32DS3.4 RTD v0.9.0, LLD Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: Fix the restoration operation of interrupt for DAOC PWM mode when set to non-zero and non-hundred duty. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-12354	Bug	[PWM][eMIOS] The DAOC PWM mode of RTD generates wrong PWM signal.<*> Detailed description (how to reproduce it): In the DAOC mode of PWM, the Period is gray and cannot be configured, but in Emios_Pwm_Ip_Irq.c, Emios_Pwm_Ip_IrqDaocHandler() will use this value, and this value is not the actual period (the actual period is related to the selected bus). This will cause the generated PWM to be incorrect. See follow pictures for more imformation: !image-2021-07-01-14-20-10-564.png! !image-2021-07-01-14-20-19-518.png! !image-2021-07-01-14-21-22-260.png! !image-2021-07-01-14-21-35-725.png! Preconditions: S32DS3.4 RTD v0.9.0, LLD Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: Fix the period configuration of DAOC PWM mode. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-12355	Bug	[ICU][eMIOS] There are some problems when using ICU component in CT.<*> Detailed description (how to reproduce it): 1. DMA doesn't support for ICU component in RTD 0.9.0 Beta 2. When the ICU channel selects a global bus as time base, there will be a error in CT. However, the Code can be generated normally. !image-2021-07-01-14-51-37-717.png! 3. The ICU channel prescaler is only up to 4, not the available max value 16 described in RM. (Extended Prescaler not support) !image-2021-07-01-14-52-52-624.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-12401	New	New Feature [S32K3 RTM] Driver activities for S32K3XX ,,"IPs list: [see SOW for details|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?viewid=49fc7681%2D6f70%2D4be1%2Dbc92%2Dc033431dbf2d&id=%2Fsites%2FZebra%2FShared%20Documents%2FProject%20Management%2FProjects%20Planning%2FSW32K3%5FRTD%5F4%2E4%5F1%2E0%2E0%2FSchedule] "
ARTD-12610	New	New Feature [S32K3 RTM] Driver activities for DEM ,,"IPs list: [see SOW for details|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?viewid=49fc7681%2D6f70%2D4be1%2Dbc92%2Dc033431dbf2d&id=%2Fsites%2FZebra%2FShared%20Documents%2FProject%20Management%2FProjects%20Planning%2FSW32K3%5FRTD%5F4%2E4%5F1%2E0%2E0%2FSchedule] "
ARTD-12619	New	New Feature [S32K3 RTM] Driver activities for BASE ,,"IPs list: [see SOW for details|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?viewid=49fc7681%2D6f70%2D4be1%2Dbc92%2Dc033431dbf2d&id=%2Fsites%2FZebra%2FShared%20Documents%2FProject%20Management%2FProjects%20Planning%2FSW32K3%5FRTD%5F4%2E4%5F1%2E0%2E0%2FSchedule] "
ARTD-12990	Bug	[UART] While loop is infinity in dummy timer<*> Detailed description (how to reproduce it): In Osif Dummy counter mode, OsIf_GetCounter always returns 0, then Uart_Ip_CheckTimeout always return FALSE Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: Fix issue Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-13000	Bug	[S32K1XX RTM] SPI: DMA Fast mode transmit with wrong default data<*> Detailed description (how to reproduce it): DMA Fastmode transmit with wrong default data When setup EB TX buffer with NULL_PTR for transmit with default data which configured at channel transferred on EB tresos. The data transmit from master is not correct. I have solution to fix, please take a look on that and fix this bug: in Lpspi_Ip_DmaFastConfig() function: !image-2021-07-02-17-56-45-437.png! in Lpspi_Ip_TxDmaTcdSGConfig() function: !image-2021-07-02-17-58-03-914.png! !image-2021-07-02-17-57-51-916.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: Spi_TC_FCT_10134 Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-13155	New	New Feature [FEE] Add support for bad Sector Management and Sector Retirement (part 2) ,,"NewWorkDescription: Add support for bad Sector Management and Sector Retirement (CPR_RTD_00505.fee). This involves removing Sectors from configuration when they become unusable. Rationale: some flash memory specs have low endurance/write cycles availability, which needs to be improved by the ability to retire bad sectors or locations affected by permanent ECC, at the expense of allocated flash size the endurance being a ppm specification."" Requirement source: cPRD (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: # Add support to manage sectors status and retire the bad ones # Add support to remove Sectors from configuration Update Fee_GetRunTimeInfo to include the sectors information Analyze the solution and add the method/scenario to users can replace bad sectors from configuration"

ID	Subtype	Headline and Description
ARTD-13165	Bug	[CAN] Controller remains bus-off state and cannot participate on CAN bus after restarting engine<*> Detailed description (how to reproduce it): After Bus-off event occurred, ESR1[FLTCONF] will be set to 11b (indicates bus-off state), Can_MainFunction_Busoff() or bus-off ISR will set the CAN controller to stop mode. Call Can_SetControllerMode(CAN_CS_STARTED) to exit bus-off state and starting transmit a new message but the data cannot be transmitted. ESR1[FLTCONF] still remains 11b even Can_SetControllerMode(CAN_CS_STARTED) has been executed successfully. !image-2021-07-06-11-16-02-886.png|width=1306,height=695! I have tried to request soft reset by asserting MCR[SOFTRST] before set controller to start mode and then the data can be transmitted successfully. It means that we should have a soft reset in restart the CAN controller after bus-off event occurred (as known is manual recover bus-off). Preconditions: Don't use auto bus-off recovery. Test Case ID (internal TC that caught the defect) optional: Can_TC_FCT_1012 Observed behavior: NA Expected behavior: NA Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-13167	New	New Feature [PORT] The Exclusive Areas should be reviewed and updated for S32K3/S32XX/ S32ZSE platforms ,,"NewWorkDescription: The Exclusive Areas for K1 platform are incorrect. Some of them are redundant (need to be removed), and the rest need to be renamed. Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Remove/Add/Renaming the Exclusive Areas in code for K1. From IPW to IPL. All exclusives should be existed in IPL. The ones in IPW should be removed. Update the UM/IM if needed Check and update RTE if needed"

ID	Subtype	Headline and Description
ARTD-13171	Bug	[S32CC][S32K3XX] Crypto driver doesn't raise an error when CryptoPrimitives configuraion fails<*> Detailed description (how to reproduce it): When config CryptoPrimitiveService is decrypt or encrypt , CryptoPrimitiveAlgorithmSecondaryFamily should be CRYPTO_ALGOFAM_NOT_SET or CRYPTO_ALGOFAM_CUSTOM but acctually ,config is CRYPTO_ALGOFAM_RNG or CRYPTO_ALGOFAM_AES When config CryptoPrimitiveService is decrypt or encrypt , driver EB not raise generate error . I try config same parameter on CT and Driver gen fail CRYPTO_ALGOFAM_RNG or CRYPTO_ALGOFAM_AES. You can see picture i cap screen bellow attachments site Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Driver not generate fail when config CryptoPrimitiveService is encrypt or decrypto and CryptoPrimitiveAlgorithmSecondaryFamily is CRYPTO_ALGOFAM_RNG or CRYPTO_ALGOFAM_AES at the same time Expected behavior: Driver raise gen fail when config fail Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-13193	New	New Feature [S32K3XX] Replace "NO_INIT" with "CLEARED" in memory section macros" ,,"1. Replace "NO_INIT" with "CLEARED" in the memory section identifiers of both source code files and documentation. For example: <MIP>_START_SEC_VAR_NO_INIT_UNSPECIFIED > <MIP>_START_SEC_VAR_CLEARED_UNSPECIFIED <MIP>_STOP_SEC_VAR_NO_INIT_32 > <MIP>_STOP_SEC_VAR_CLEARED_32 ... 2. In file "sections_to_be_defined_in_memmaph.dox", perform the following replacement in the description field of the "CLEARED" (formerly "NO_INIT") sections: "These variables are never cleared and never initialized by start-up code." > "These variables are cleared to zero by start-up code." 3. Move all zero-initialized variables into the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" 4. Remove all explicit zero-initializers in the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed; / implicit zero initialization*/ #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h"
ARTD-13728	New	New Feature [MCU] Add support for warm resetting the A53/M7 cores on S32XX ,,"NewWorkDescription: Add support for warm resetting the A53/M7 cores on S32XX Requirement source: N/A (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Add support for warm resetting the A53/M7 cores on S32XX"

ID	Subtype	Headline and Description
ARTD-13727	Bug	[PORT] Missing section memory for Port_Config pointer in S32K3XX<*> Detailed description (how to reproduce it): !image-2021-07-07-15-11-39-210.png! This array need to be placed into PORT_START/STOP_SEC_CONFIG_DATA_UNSPECIFIED Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Missing section memories for Port_Config array Expected behavior: Port_Config should be placed into a section memory Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-13826	New	New Feature [ICU] Evaluate if <IP>_Icu_Ip_EnableNotification and <IP>_Icu_Ip_DisableNotification are needed ,,"NewWorkDescription: Pls see [comment|https://bitbucket.sw.nxp.com/projects/ARTD/repos/icu/pull-requests/264/overview?commentId=873554] for more details Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: NA"

ID	Subtype	Headline and Description
ARTD-13827	Bug	[CRYPTO] Fix issue with define CRYPTO_ENABLE_ENC_AUTH_KEY_EXPORT not activated in EBT Crypto_Cfg.h file<*> Detailed description (how to reproduce it): When configuring CryptoKeyElements that are having the HSE Key Export checkbox ticket, the value of the define CRYPTO_ENABLE_ENC_AUTH_KEY_EXPORT in Crypto_Cfg.h is generated with STD_OFF value Preconditions: There is no keyElement configured with HSE Encrypted Key Import or HSE Authenticated Key Import options activated Test Case ID (internal TC that caught the defect) optional: Problem was discovered while building a new example application Observed behavior: CRYPTO_ENABLE_ENC_AUTH_KEY_EXPORT in Crypto_Cfg.h is generated with STD_OFF value Expected behavior: CRYPTO_ENABLE_ENC_AUTH_KEY_EXPORT in Crypto_Cfg.h is generated with STD_ON value Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: The CRYPTO_ENABLE_ENC_AUTH_KEY_EXPORT wrongly uses an internal variable computed for key import. Only need to update the variable to be the one computed for key export.
ARTD-13851	New	New Feature [ADC] Support External Dma for without Interrupts ,,"Consider to support AdcExtDMAChanEnable when AdcWithoutInterrupts is enabled. Proposed Solution: An alternative solution might be to use in this case the buffer registered by the user with Adc_SetupResultBuffer()"
ARTD-13951	Bug	[CRYPTO] Remove descriptor feeding feature code for the platforms without HSE firmware<*> Detailed description (how to reproduce it): At build time for S32K1XX platform warnings will be reported for {color:#172b4d}CRYPTO_ENABLE_FEED_HSE_DESC_SUPPORT macro because it is not defined. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: CRYPTO_ENABLE_FEED_HSE_DESC_SUPPORT is undefined. Expected behavior: CRYPTO_ENABLE_FEED_HSE_DESC_SUPPORT usage and the code incapsulated by the macro will be removed from plugin code. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: CRYPTO_ENABLE_FEED_HSE_DESC_SUPPORT usage and the code incapsulated by the macro should be removed from plugin code with M4 tags.

ID	Subtype	Headline and Description
ARTD-13954	New	New Feature [MCU][S32K3XX][BASE] SleepOnExit incompatible with current approach on supervisor/user mode ,,"NewWorkDescription: Problem: Sleep On Exit bit from System Control Register can only be written in supervisor mode The behavior is that at the exit from the next interrupt the core goes to sleep !image-2021-07-21-09-48-39-401.png|width=776,height=121! When the driver is called in user mode context writing this bit will do the following: SVC_GoToSupervisor Write SLEEPONEXIT SVC_GoToUser Because SVC_GoToUser is currently implemented using the svc handler (which is an interrupt) the result is that the core goes in sleep immediately after going back to user mode For detail please the email attached. Requirement source: CPR_RTD_00447.mcu Req Text*: The MCU driver shall offer support to control the exception return behavior of the currently executing core on a wake-up event triggered during SLEEP. The function void Mcu_SleepOnExit (boolean enableSleepOnExit) will enable/disable the automatic sleep entry on exception return. Requirement ticket: AAI-498 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: 2 step must be done in Base, platform and mcu driver to avoid this issue 1. Base and Platform will implement the transition from supervisor mode to user mode without using the SVC Handler? Instead, just writing the CONTROL bit? !image-2021-07-21-09-49-10-553.png|width=801,height=141! 2. Mcu driver implementation: Add another function to the API to enable/disable calling Power_Ip_EnableSleepOnExit in the driver right before the WFI. Note that a pre-compile switch might not be enough since the application could choose not to enable SleepOnExit before every sleep cycle."

ID	Subtype	Headline and Description

ARTD-13969	Bug	Remove warning when don't use D_CACHE_ENABLE macro<*>
		
		Detailed description (how to reproduce it):
		Warning happen when don't use D_CACHE_ENABLE macro
		Preconditions:
		[...]
		Test Case ID (internal TC that caught the defect) optional:
		[...]
		Observed behavior:
		[...]
		Expected behavior:
		There aren't warning when don't use D_CACHE_ENABLE macro
		Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)
		Proposed solution optional:
		Move those line
		uint32 ccsidr = 0U;
		uint32 sets = 0U;
		uint32 ways = 0U;
		into
		
		#ifdef D_CACHE_ENABLE
		uint32 ccsidr = 0U;
		uint32 sets = 0U;
		uint32 ways = 0U;
		...
		#endif

ARTD-14027	New	New Feature CLONE - [SPI] Create SPI feature for 1/2/4/8-bit half duplex mode ,,"NewWorkDescription: Implement 4-bit half duplex mode according requirements # The Spi driver shall be able to transfer in half duplex mode supporting 2/4/8-bit parallel transmission or reception on each clock edge. # A vendor specific pre-compile boolean configuration parameter SpiHalfDuplexModeSupport shall enable/disable this functionality. # By default this optional functionality and configuration parameters shall be disabled. ITWG ticket: https://jira.sw.nxp.com/browse/AAI-632 Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]"

ID	Subtype	Headline and Description
ARTD-14029	Bug	[WDG] Instance 1 code was incorrectly generated<*> Detailed description (how to reproduce it): Generation code in Wdg_43_Instance_1 was mismatched compares to the configuration values. Preconditions: Wdg_43_Instance_1 is added. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Generation code in Wdg_43_Instance_1 was mismatched compares to the configuration values. Expected behavior: Generation code in Wdg_43_Instance_1 should be correct compares to the configuration values. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: In Swt_43_Instance1_Ip_PBcfg.c when WdgModeConfig and WdgModeConfig are executed the WdgNo is empty : [!CALL "WdgModeConfig","WdgMode" = "'WdgSettingsSlow'","WdgNo" = """!] [!CALL "WdgModeConfig","WdgMode" = "'WdgSettingsFast'","WdgNo" = """!] this should be change to : [!CALL "WdgModeConfig","WdgMode" = "'WdgSettingsSlow'","WdgNo" = "'_43_Instance1'"!] [!CALL "WdgModeConfig","WdgMode" = "'WdgSettingsFast'","WdgNo" = "'_43_Instance1'"!] Same issue is present in Wdg_43_Instance1_PBcfg.c for WdgTriggerPeriod call. In Wdg_PluginMacros.m for WdgTriggerSourceClock variable also is not used the instance in path : [!VAR "WdgTriggerSourceClock" = "num:i(node:value(node:ref(./../../../Wdg/ELEMENTS/Wdg/WdgSettingsConfig/WdgExternalTriggerCounterRef)/GptChannelTickFrequency)div 1000)"!] this should be changed to : [!VAR "WdgTriggerSourceClock" = "num:i(node:value(node:ref(node:value(concat('./../../../Wdg',$WdgNo,'/ELEMENTS/Wdg/WdgSettingsConfig/','WdgExternalTriggerCounterRef')))/GptChannelTickFrequency)div 1000)"!]

ID	Subtype	Headline and Description
ARTD-14044	Bug	[SAI] Compile error with generation code with no EcuC<*> Detailed description (how to reproduce it): When generating code with no EcuC and no variant, the code can't be compiled: !image-2021-07-15-20-07-49-835.png! Preconditions: SAI generating code with no EcuC Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Compiled error with configuration code Expected behavior: Code can be compiled Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: In CDD_Sai_PbCfg.h, the below code is generated: #define SAI_CONFIG_PB \ extern const Sai_ConfigType Sai_Config;\ #define SAI_STOP_SEC_CONFIG_DATA_UNSPECIFIED #include "Sai_MemMap.h" It can be compiled if adding a blank line: #define SAI_CONFIG_PB \ extern const Sai_ConfigType Sai_Config;\ #define SAI_STOP_SEC_CONFIG_DATA_UNSPECIFIED #include "Sai_MemMap.h"

ID	Subtype	Headline and Description
ARTD-14119	Bug	[OS] OsApplicationCoreRef and OsAppEcucPartitionRef shall be implemented as parameters<*> Detailed description (how to reproduce it): In SW32K3_RTD_4.4_0.9.0_D2103 MCAL, many drivers use OsAppEcucPartitionRef and OsApplicationCoreRef as reference, for instance in Eth driver: [!LOOP "as:modconf('Os')[1]/OsApplication/*/OsAppEcucPartitionRef/*"!] [!IF "node:value(.) = $EcucPartitionRef"!] [!IF "node:refvalid(../../OsApplicationCoreRef/*[1])"!] [!VAR "CoreId" = "num:i(node:value(node:ref(../../OsApplicationCoreRef/*[1])/EcucCoreId))"!] In this case the OsAppEcucPartitionRef and OsApplicationCoreRef are used as an list. According with Autosar specification these two containers is EcucReferenceDef, which can be only one parameter, and they shall not be a list, which contains one or more parameters (see attachment). Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: In customer's OS, the OsAppEcucPartitionRef and OsApplicationCoreRef are implemented as parameter, while Eth driver is used as lists. As a result, the configuration and generation are failed. Expected behavior: OsApplicationCoreRef and OsAppEcucPartitionRef shall be implemented as parameters, instead of lists Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A

ID	Subtype	Headline and Description
ARTD-14120	Bug	[PWM] Unknown path with $pluginPath and unknown derivate when S32K3XX is not used<*> Detailed description (how to reproduce it): 1. In PWM, generators file is used path for ".m" file like : [!INCLUDE "?concat($pluginPath,'/generate_PB/Pwm_NotifyCheck_Src.m')"!] During customers integration, they created their own plugin and reference the generator from NXP delivered plugins. In this case, when MCAL is integrated, pluginPath will point to different location and Pwm_NotifyCheck_Src.m cannot be used. 2. With this piece of code [!IF "$derivate = 'S32K3XX'"!] #include "S32K344_EMIOS.h"[!ENDIF!] In customer's case the derivate is S32K34X so the include will not be generated. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Generation error regarding the path incorrect. Compile error regarding the mismatch derivate Expected behavior: Pwm_NotifyCheck_Src.m can be included when code generating. #include "S32K344_EMIOS.h" can be added in generation code. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-14125	New	New Feature [PWM][EMIOS] Investigate SetPhaseShif time improvements ,,"NewWorkDescription: According to the performance measurement done on PWM EMIOS IPL APIs the Emios_Pwm_Ip_SetPhaseShift can take up to 3.5 us to execute at default core/ pheripheral clock. Investigate if there are any improvements that can be done in the code to reduce the time needed to perform the update. Check if merging the phaseShift and dutyCycle will have a notable improvement. Investigate cases where safety checks can be omitted for a new specific motor control API. Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: One solution could be to not read form hw the current dutyCycle."

ID	Subtype	Headline and Description
ARTD-14126	New	New Feature [PWM][EMIOS] Investigate SetDutyCycle time improvements ,,"NewWorkDescription: According to the performance measurement done on PWM EMIOS IPL APIs the Emios_Pwm_Ip_SetDutyCycle can take up to 3.5 us to execute at default core/ pheripheral clock. Investigate if there are any improvements that can be done in the code to reduce the time needed to perform the update. Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]"
ARTD-14172	Bug	[UART] - ISR does not check if driver is initialized for Flexio Ip<*> Detailed description (how to reproduce it): Preconditions: Follow req CPR_RTD_00011.lin: ISR shall check whether its respective driver is initialized. If the driver is not initialized, the ISR shall only clear interrupt status flag and return immediately. Eventhough the Flexio Mcl Common Irq checks if the macro corresponding the Uart channels configured before the Flexio_Uart_Ip_Irq function is called, the Flexio_Uart_Ip_Init() may not have been initialized on the channel in use, This must be checked in the Flexio_Uart_Ip_IrqHandler. Lpuart driver approach can be applied. Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: Check if driver has been initialized for the channel in use. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Check driver state structure to be different than NULL_PTR
ARTD-14173	New	New Feature [PWM][EMIOS] Implement missing checks in S32CT generation ,,"NewWorkDescription: The S32CT pwm emios generation on K3 platform is missing the checks for mcl counter bus. These checks must be added in the S32CT component as these are present in the EBT plugin. Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]"

ID	Subtype	Headline and Description
ARTD-14220	Bug	[ADC] Adc_SetChannel function prototype does not match with requirement because of const qualifiers<*> Detailed description (how to reproduce it): Some function prototypes do not match with requirement Preconditions: Review new interface requirements Test Case ID (internal TC that caught the defect) optional: Review requirement Observed behavior: CPR_RTD_00329.adc: The optional API prototype shall be: void Adc_SetChannel(Adc_GroupType Group, Adc_GroupDefType Channel, #if (ADC_DELAY_AVAILABLE == STD_ON) uint16 Delays, uint32 ChannelUpdateMask, #endif / (ADC_DELAY_AVAILABLE == STD_ON) / Adc_ChannelIndexType NumberOfChannel); In driver: void Adc_SetChannel(const Adc_GroupType Group, const Adc_GroupDefType Channel, const uint16 Delays, const uint32 ChannelUpdateMask, const Adc_ChannelIndexType NumberOfChannel) SWS_Adc_00082: Service name: IoHwAb_AdcNotification - Syntax: void IoHwAb_AdcNotification(void) - In driver: Not found comment in ticket ARTD-14077 Expected behavior: Matching between requirement and driver Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-14236	New	New Feature CLONE - [S32K1 RTM] SPI: Improve IPL code to improve decision coverage when using DevAssert() ,,"NewWorkDescription: As IPL function below, we can not test with cases which go into conditions such as ExternalDevice=NULL_PTR. So, we need to change the implement way for these sketch. !image-2021-07-15-15-19-01-921.png! Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]"

ID	Subtype	Headline and Description
ARTD-14240	Bug	[UART] Conflict if using common callback in the same channel<*> Detailed description (how to reproduce it): If user uses the common callback in channel for his program, it will cause conflict, bcs the declaration of callback functions will generate several times in EB/CT generated code. It can cause the compiler warning for dupplicate declaration. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: Fix this issue Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-14242	Bug	[UART] In Abort case, Complete Send/Receive internal functions need to wait for finishing of current byte transmission ,,"Detailed description (how to reproduce it): In Abort function, Complete Send/Receive internal functions are called to finish the current transmission. But they need to wait for finishing of current byte transmission and afterward disable TE and RE. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: Fix this issue Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-14255	Bug	[ADC] aAdcUnitSupportCtuControlMode and aHwLogicalId are generated incorrectly on EB<*> Detailed description (how to reproduce it): aAdcUnitSupportCtuControlMode and aHwLogicalId are generated incorrectly aHwLogicalId: when only 1 ADC is configured then only 1 element is generated for this array instead of equal to max ADC unit aAdcUnitSupportCtuControlMode is always generated as 1 = unit enabled but actually unit is disabled Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: aAdcUnitSupportCtuControlMode and aHwLogicalId are generated correctly Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-14286	Bug	[ADC] Configure channel limit check with set channel feature is not working<*> Detailed description (how to reproduce it): Need to note that set limit check channel for group only in case this group configured with limit check channel Preconditions: Group configured with normal channel Test Case ID (internal TC that caught the defect) optional: Adc_TC_FCT_1401 Adc_TS_006 cfg 7 Observed behavior: Calling set channel to new channel with range ADC_RANGE_UNDER_LOW, AdcChannelLowLimit is 0 Set voltage for this new channel as 4V Enable Hw trigger group Start trigger Expected: group status is not streaming complete and timeout occurred Stop trigger Disable Hw trigger group Real status: group status is stream complete because in ISR AdcGroupLimitCheck variable set as FALSE Expected behavior: Timeout because of out range voltage Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA

ID	Subtype	Headline and Description
ARTD-14292	New	New Feature [ADC] Merge containers for channel configuration for chains and channel configuration array into single one for Adc_Sar_Ip component ,,"NewWorkDescription: In IPL, there are 2 containers for channel configurations that might confuse users when configuring for channels. Propose to merge them into single one Requirement source: Improvement Proposed solution optional: NA !image-2021-07-22-18-19-34-566.png!"
ARTD-14428	Bug	[GPT] Check and update the functions that don't match the requirements<*> Detailed description (how to reproduce it): Some function in "ReqExport.txt" file but does not include in "*.h" files of driver code pls see attached files for more details Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: NA Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Check and update for all APIs
ARTD-14306	New	New Feature [CAN] re-analysis Exclusive Area ,,"NewWorkDescription: some code changed, need to re-analyze EA Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]"

ID	Subtype	Headline and Description
ARTD-14304	Bug	Power_Ip_GetResetReason can not return MCU_WAKEUP_REASON<*> Detailed description (how to reproduce it): Power_Ip_GetResetReason API can not return MCU_WAKEUP_REASON after occurring reset event during standby mode. Because all registers of MC_ME will be reset after occurring reset event during standby mode, so Power_Ip_MC_ME_GetPreviousMode can not return POWER_IP_SOC_STANDBY_MODE which result Power_Ip_GetResetReason API can not return MCU_WAKEUP_REASON. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-14312	Bug	RTC TRIG_EN can not be configurated by any API<*> Detailed description (how to reproduce it): K3 MCAL does not provide any API to configure RTC's TRIG_EN bit. If using LPCMP to wake up MCU, RTC will cyclically[^RTC_Trigger_LPCMP_bug.pptx] trigger the LPCMP sample. If the voltage input is bigger than expected, MCU will be awakened. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-14322	New	New Feature [RM] [S32K3XX] Improve coding convention for Xbic Ip ,,"NewWorkDescription: File's name are not follow coding convention. XBIC_IP_ should change to Xbic_ip. Ex: XBIC_IP_Types.h change to Xbic_Ip_Types.h Remove useless file: XBIC_Ip_Cfg_Defines.h Update to include correct file's name after updating above. Update .mak file (for gen plugin) to correct file's name after updating above. Requirement source: N/A (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: As description"

ID	Subtype	Headline and Description
ARTD-14347	New	New Feature [BASE] Add header files for S32K312 ,,"NewWorkDescription: Add header files for S32K312 Requirement source: RM rev 2 Draft B (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: NA"
ARTD-14362	New	New Feature [RESOURCE] Add resource for S32K312 and S32K311 ,,"NewWorkDescription: Add resource for S32K312 and S32K311. Requirement source: (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: NA"
ARTD-14373	Bug	[Adc] UM does not specify that groups with 1 channel do not use DMA scatter gather<*> Detailed description (how to reproduce it): UM does not specify that groups with 1 channel do not use DMA scatter gather so this must be disabled in DMA channel config Expected behavior: UM contains all details regarding DMA config for this case Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Add note in "DMA transfer" chapter from 3.6 Driver usage and configuration tips Check if any other DMA scenarios/configs are not described by this chapter
ARTD-14375	Bug	[ADC] ADC_VALIDATE_APP_BUFFER_ALIGNMENT is never defined<*> Detailed description (how to reproduce it): ADC_VALIDATE_APP_BUFFER_ALIGNMENT is never defined, resulting in Adc_ValidateSetupBufferAlignment() never being actually called. Proposed solution optional: Check if this check is still needed/working, also in MCAL If needed define should be generated by config. Otherwise function code removed

ID	Subtype	Headline and Description
ARTD-14381	New	New Feature [MCU] SleepOnExit incompatible with current approach on supervisor/user mode ,,"NewWorkDescription: Problem: Sleep On Exit bit from System Control Register can only be written in supervisor mode The behavior is that at the exit from the next interrupt the core goes to sleep !image-2021-07-21-08-44-11-091.png|width=816,height=126! When the driver is called in user mode context writing this bit will do the following: SVC_GoToSupervisor Write SLEEPONEXIT SVC_GoToUser Because SVC_GoToUser is currently implemented using the svc handler (which is an interrupt) the result is that the core goes in sleep immediately after going back to user mode For detail please the email attached. Requirement source: CPR_RTD_00447.mcu Req Text*: The MCU driver shall offer support to control the exception return behavior of the currently executing core on a wake-up event triggered during SLEEP. The function void Mcu_SleepOnExit (boolean enableSleepOnExit) will enable/disable the automatic sleep entry on exception return. Requirement ticket: AAI-498 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: 2 step must be done in Base, platform and mcu driver to avoid this issue 1. Base and Platform will implement the transition from supervisor mode to user mode without using the SVC Handler? Instead, just writing the CONTROL bit? !image-2021-07-21-08-46-09-719.png|width=800,height=151! 2. Mcu driver implementation: Add another function to the API to enable/disable calling Power_Ip_EnableSleepOnExit in the driver right before the WFI. Note that a pre-compile switch might not be enough since the application could choose not to enable SleepOnExit before every sleep cycle."
ARTD-14384	New	New Feature [ETH]Fix build failed on K3 ,,"NewWorkDescription: Fixed build failed caused by general files Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Fixed build failed caused by general files"
ARTD-14400	Bug	[S32K3XX][RM] Mpu_M7 can't getResource on S32DS<*> Mpu_M7 can't getResource on S32DS, see on attach picture

ID	Subtype	Headline and Description
ARTD-14413	Bug	[SAI] Unfixed MISRA violations of rule 8.13<*> Detailed description (how to reproduce it): Unfixed MISRA violations for rule 8.13, outside list of accepted project level deviations (MISRA violations for Rules are only accepted in cases specified by column D with disclaimer from column E for document with project level deviations): aData is assigned to pData in the state structure which is used for both TX and RX, so cannot be const This ticket is raised to analyze and confirm if code can be refactored to avoid these violations. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-14409	New	New Feature [BUILD_ENV] Add support for S32K312 and S32K311 derivative ,,"NewWorkDescription: Add new derivatives. Requirement source: (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: NA"
ARTD-14436	Bug	[ADC] Reset sample index in ISR and bRuntimeUpdated status if runtime channels are updated by Adc_SetChannel<*> Detailed description (how to reproduce it): Reset sample index if runtime channels updated by Adc_SetChannel, before ISR is called or in extra notification Preconditions: NA Expected Voltage: Test Case ID (internal TC that caught the defect) optional: Adc_TC_FCT_1101 Adc_TS_017 cfg 3channelsBeforeStart Observed behavior: NA Real status: Wrong data in notification Expected behavior: NA Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA

ID	Subtype	Headline and Description
ARTD-14474	New	New Feature [RM] Add prefix "XRDC" for some definitions of Xrdc ip" ,,"NewWorkDescription: Some define of Xrdc don't have prefix "XRDC". it can make duplicate in header files !image-2021-07-29-14-48-04-296.png! Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Add prefix XRDC
ARTD-14478	New	New Feature [RM][S32K3XX] Fix gen fail in CT for Ip Pflash,Abxs,Xbic,Xrdc,VirtualWapper" ,,"NewWorkDescription: Update generating code of IP PFlash, Abxs, Xbic, Xrdc, Virtual Wrapper for S32K3XX in CT Requirement source: N/A (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Remove enable attribute of corresponding node
ARTD-14481	Bug	[MCU] The function Mcu_Ipw_CmuClearClockFailIrqFlags isn't called in HLD<*> Detailed description (how to reproduce it): The function Mcu_Ipw_CmuClearClockFailIrqFlags didn't be called in HLD !image-2021-07-29-17-18-43-915.png! Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: The function Mcu_Ipw_CmuClearClockFailIrqFlags didn't be called in HLD Expected behavior: Remove the function Mcu_Ipw_CmuClearClockFailIrqFlags in driver code Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description

ARTD-14485	Bug	[ADC] Configurator generates multiple times the notification prototype, when same notification is used for multiple groups
		
		,,"Detailed description (how to reproduce it):
		Tresos configurator generates multiple times the notification prototype, when same notification is used for multiple groups
		To check if also S32CT has same issue
		Preconditions:
		Have a configuration with multiple groups that use the same notification.
		Test Case ID (internal TC that caught the defect) optional:
		TS_Shared_000
		Observed behavior:
		Each notifications declared in the EB config is generated more than once:
		/
		brief ADC Notification functions.
		details ADC Nofification functions defined inside the Plugin.
		/
		extern void Notification_0(void);
		extern void Notification_1(void);
		extern void T_ADC_Notification(void);
		extern void T_ADC_Notification(void);
		extern void Notification_0(void);
		extern void Notification_0(void);
		extern void T_ADC_Notification(void);
		extern void T_ADC_Notification(void);
		extern void Notification_4(void);
		extern void Notification_5(void);
		extern void T_ADC_Notification(void);
		extern void Notification_1(void);
		extern void Notification_0(void);
		extern void Notification_0(void);
		extern void Notification_0(void);
		extern void Notification_0(void);
		extern void Notification_0(void);
		extern void Notification_0(void);
		extern void Notification_0(void);
		extern void Notification_0(void);
		Expected behavior:
		Each notification must be declared only once.
		Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)
		Proposed solution optional:
		[...]

ID	Subtype	Headline and Description
ARTD-14487	Bug	[ADC] IPW notification prototype is defined both in driver code as well as generated code<*> Detailed description (how to reproduce it): IPW notification prototype is defined both in Adc_Ipw_Irq.c file as well as Adc_Ip_PBCfg.h generated file. Preconditions: Use a HLD config that is using interrupts. Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: IPW notification prototype is defined both in driver code as well as generated code. Expected behavior: IPW notification should be defined only once. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Remove IPW notification prototype from Adc_Ipw_Irq.c.
ARTD-14490	Bug	[Mcl] error in field dmaLogicInstance_ConfigType of xdm file<*> Detailed description (how to reproduce it): In SW32K3_RTD_4.4_0.9.0_D2103 MCAL in Mcl schema file for dmaLogicInstance_ConfigType list is used this path on invalid check: <a:tst expr="(../../MclGeneral//MclDma/MclEnableDma ='true') ..... <a:tst expr="(../../MclGeneral//MclDma/MclEnableDma ='true') Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: express is MclGeneral//MclDma Expected behavior: express is MclGeneral/MclDma Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A

ID	Subtype	Headline and Description
ARTD-14495	Bug	[CAN] ecvd/Ip_FlexCAN fails to export data for multiple controllers<*> Detailed description (how to reproduce it): A*> add more than one controllers to s32k148/Ip_FlexCAN (IPL layer) projects with default configuration (fix all errors if have) export ecvd import ecvd => error as below: !image-2021-07-30-10-51-10-710.png! B*> !image-2021-07-30-10-56-02-840.png! C>* **_ please re-check if all required nodes are exported (e.g. pe_clock_frequency) !image-2021-07-30-11-05-31-694.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-14535	New	New Feature [port] Update pin signal configuration resources for S32K3xx Rev. 2 Draft D ,,"NewWorkDescription: Update resource for your driver following below derivatives for this release: S32K312: S32K312_172MQFP, S32K312_100MQFP S32K314: S32K314_257MAPBGA, S32K314_172MQFP S32K324: S32K324_257MAPBGA, S32K324_172MQFP S32K344: S32K344_257MAPBGA, S32K344_172MQFP Requirement source: S32K3xx Reference Manual, Rev. 2 Draft D, 07/2021, [Link|https://nxp1.sharepoint.com/:b:/r/sites/Zebra/Shared%20Documents/Documents/Platforms/S32K3xx/RM/S32K3xx_RM_Rev2DraftD.pdf?csf=1&web=1&e=6kLAfr] Proposed solution optional: Update driver resources"

ID	Subtype	Headline and Description
ARTD-14503	New	New Feature [crypto] Update resources via RM S32K3xx Rev. 2 Draft D ,,"NewWorkDescription: Update resource for your driver following below derivatives for this release: S32K312: S32K312_172MQFP, S32K312_100MQFP S32K314: S32K314_257MAPBGA, S32K314_172MQFP S32K324: S32K324_257MAPBGA, S32K324_172MQFP S32K344: S32K344_257MAPBGA, S32K344_172MQFP Requirement source: S32K3xx Reference Manual, Rev. 2 Draft D, 07/2021, [Link|https:// nxp1.sharepoint.com/:b:/r/sites/Zebra/Shared%20Documents/Documents/Platforms/ S32K3xx/RM/S32K3xx_RM_Rev2DraftD.pdf?csf=1&web=1&e=6kLAfr] Proposed solution optional: Update driver resources"
ARTD-14507	New	New Feature [fls] Update resources via RM S32K3xx Rev. 2 Draft D ,,"NewWorkDescription: Update resource for your driver following below derivatives for this release: S32K312: S32K312_172MQFP, S32K312_100MQFP S32K314: S32K314_257MAPBGA, S32K314_172MQFP S32K324: S32K324_257MAPBGA, S32K324_172MQFP S32K344: S32K344_257MAPBGA, S32K344_172MQFP Requirement source: S32K3xx Reference Manual, Rev. 2 Draft D, 07/2021, [Link|https:// nxp1.sharepoint.com/:b:/r/sites/Zebra/Shared%20Documents/Documents/Platforms/ S32K3xx/RM/S32K3xx_RM_Rev2DraftD.pdf?csf=1&web=1&e=6kLAfr] Proposed solution optional: Update driver resources"
ARTD-14508	New	New Feature [gpt] Update resources via RM S32K3xx Rev. 2 Draft D ,,"NewWorkDescription: Update resource for your driver following below derivatives for this release: S32K312: S32K312_172MQFP, S32K312_100MQFP S32K314: S32K314_257MAPBGA, S32K314_172MQFP S32K324: S32K324_257MAPBGA, S32K324_172MQFP S32K344: S32K344_257MAPBGA, S32K344_172MQFP Requirement source: S32K3xx Reference Manual, Rev. 2 Draft D, 07/2021, [Link|https:// nxp1.sharepoint.com/:b:/r/sites/Zebra/Shared%20Documents/Documents/Platforms/ S32K3xx/RM/S32K3xx_RM_Rev2DraftD.pdf?csf=1&web=1&e=6kLAfr] Proposed solution optional: Update driver resources"

ID	Subtype	Headline and Description
ARTD-14509	New	New Feature [i2c] Update resources via RM S32K3xx Rev. 2 Draft D ,,"NewWorkDescription: Update resource for your driver following below derivatives for this release: S32K312: S32K312_172MQFP, S32K312_100MQFP S32K314: S32K314_257MAPBGA, S32K314_172MQFP S32K324: S32K324_257MAPBGA, S32K324_172MQFP S32K344: S32K344_257MAPBGA, S32K344_172MQFP Requirement source: S32K3xx Reference Manual, Rev. 2 Draft D, 07/2021, [Link|https:// nxp1.sharepoint.com/:b:/r/sites/Zebra/Shared%20Documents/Documents/Platforms/ S32K3xx/RM/S32K3xx_RM_Rev2DraftD.pdf?csf=1&web=1&e=6kLAfr] Proposed solution optional: Update driver resources"
ARTD-14511	New	New Feature [icu] Update resources via RM S32K3xx Rev. 2 Draft D ,,"NewWorkDescription: Update resource for your driver following below derivatives for this release: S32K312: S32K312_172MQFP, S32K312_100MQFP S32K314: S32K314_257MAPBGA, S32K314_172MQFP S32K324: S32K324_257MAPBGA, S32K324_172MQFP S32K344: S32K344_257MAPBGA, S32K344_172MQFP Requirement source: S32K3xx Reference Manual, Rev. 2 Draft D, 07/2021, [Link|https:// nxp1.sharepoint.com/:b:/r/sites/Zebra/Shared%20Documents/Documents/Platforms/ S32K3xx/RM/S32K3xx_RM_Rev2DraftD.pdf?csf=1&web=1&e=6kLAfr] Proposed solution optional: Update driver resources"
ARTD-14515	New	New Feature [ocu] Update resources via RM S32K3xx Rev. 2 Draft D ,,"NewWorkDescription: Update resource for your driver following below derivatives for this release: S32K312: S32K312_172MQFP, S32K312_100MQFP S32K314: S32K314_257MAPBGA, S32K314_172MQFP S32K324: S32K324_257MAPBGA, S32K324_172MQFP S32K344: S32K344_257MAPBGA, S32K344_172MQFP Requirement source: S32K3xx Reference Manual, Rev. 2 Draft D, 07/2021, [Link|https:// nxp1.sharepoint.com/:b:/r/sites/Zebra/Shared%20Documents/Documents/Platforms/ S32K3xx/RM/S32K3xx_RM_Rev2DraftD.pdf?csf=1&web=1&e=6kLAfr] Proposed solution optional: Update driver resources"

ID	Subtype	Headline and Description
ARTD-14517	New	New Feature [port] Update resources via RM S32K3xx Rev. 2 Draft D ,,"NewWorkDescription: Update resource for your driver following below derivatives for this release: S32K312: S32K312_172MQFP, S32K312_100MQFP S32K314: S32K314_257MAPBGA, S32K314_172MQFP S32K324: S32K324_257MAPBGA, S32K324_172MQFP S32K344: S32K344_257MAPBGA, S32K344_172MQFP Requirement source: S32K3xx Reference Manual, Rev. 2 Draft D, 07/2021, [Link|https:// nxp1.sharepoint.com/:b:/r/sites/Zebra/Shared%20Documents/Documents/Platforms/ S32K3xx/RM/S32K3xx_RM_Rev2DraftD.pdf?csf=1&web=1&e=6kLAfr] Proposed solution optional: Update driver resources"
ARTD-14521	New	New Feature [sent] Update resources via RM S32K3xx Rev. 2 Draft D ,,"NewWorkDescription: Update resource for your driver following below derivatives for this release: S32K312: S32K312_172MQFP, S32K312_100MQFP S32K314: S32K314_257MAPBGA, S32K314_172MQFP S32K324: S32K324_257MAPBGA, S32K324_172MQFP S32K344: S32K344_257MAPBGA, S32K344_172MQFP Requirement source: S32K3xx Reference Manual, Rev. 2 Draft D, 07/2021, [Link|https:// nxp1.sharepoint.com/:b:/r/sites/Zebra/Shared%20Documents/Documents/Platforms/ S32K3xx/RM/S32K3xx_RM_Rev2DraftD.pdf?csf=1&web=1&e=6kLAfr] Proposed solution optional: Update driver resources"
ARTD-14522	New	New Feature [spi] Update resources via RM S32K3xx Rev. 2 Draft D ,,"NewWorkDescription: Update resource for your driver following below derivatives for this release: S32K312: S32K312_172MQFP, S32K312_100MQFP S32K314: S32K314_257MAPBGA, S32K314_172MQFP S32K324: S32K324_257MAPBGA, S32K324_172MQFP S32K344: S32K344_257MAPBGA, S32K344_172MQFP Requirement source: S32K3xx Reference Manual, Rev. 2 Draft D, 07/2021, [Link|https:// nxp1.sharepoint.com/:b:/r/sites/Zebra/Shared%20Documents/Documents/Platforms/ S32K3xx/RM/S32K3xx_RM_Rev2DraftD.pdf?csf=1&web=1&e=6kLAfr] Proposed solution optional: Update driver resources"

ID	Subtype	Headline and Description
ARTD-14534	Bug	[S32K3XX] [PORT] Driver missing config IFE bit when declare Port_Init<*> Detailed description (how to reproduce it): in S32K3XX, use Plugin_2872021.zip, config channel (only PTA5) with IFE = 1, check the status IFE bit in MSCR = 5 Preconditions: Port_Init need to support config all bit in MSCR if have Test Case ID (internal TC that caught the defect) optional: Port_TC_WBT_0015 Observed behavior: Port_Init did not have any action to config IFE bit !image-2021-07-30-13-52-25-522.png! Expected behavior: Driver need to be update config for IFE bit in MSCR Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-14587	Bug	[S32K3XX] [RM] Correct API prototypes to match the requirements<*> Detailed description (how to reproduce it): There are some wrong interfaces between requirement and driver. Detail in attachment file. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: different APIs prototype between driver and requirement Expected behavior: No different APIs Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update Driver or/and requirement

ID	Subtype	Headline and Description
ARTD-14615	Bug	[PWM] Stuck in interrupt function when re-enable notification for Flexio<*> Detailed description (how to reproduce it): When re-enable notification for channel flexio is 0 and 1, the stuck occurs in the interrupt function: Initilize 2 channels flexio 0 and 1 Loop for enable notification 2 channels. timerIrqMask variable will be set to 3(0x11) when re-enable notification for channel 0 timerIrqMask = timerIrqMask & ((uint8)0x01U << userCfg->timerId) in Flexio_Pwm_Ip_UpdateInterruptMode function will set timerIrqMask to 2(0x10)-> value 0 for channel 0. But interrupt still occur, it causes the program to get stuck in the interrupt function Preconditions: Build with GCC compiler Test Case ID (internal TC that caught the defect) optional: Pwm_TC_FCT_0213 Flexio Observed behavior: get stuck in the interrupt function Expected behavior: No stuck in the interrupt function Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-14664	Bug	[S32K3XX] [PORT] Driver generate error due to missing define INMUX in S32K312<*> Detailed description (how to reproduce it): in PVT_ARTD_PORT_V146, config test in derivative S32K312. Preconditions: driver will be support generate configuration successfully Test Case ID (internal TC that caught the defect) optional: Port_TC_WBT_0036/Port_TS_016 Observed behavior: driver for K312 can support till INMUX= 372 ==> ok !image-2021-08-03-10-30-51-332.png! But Port_PBcfg.c still declare to INMUX373 !image-2021-08-03-10-32-43-534.png! ==>make error !image-2021-08-03-10-29-37-452.png! Expected behavior: driver need to be update to generate config successfully in S32K312 Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA

ID	Subtype	Headline and Description
ARTD-14680	Bug	[LIN][BASE] - Update name of Ds component for Lin<*> Detailed description (how to reproduce it): The actual component name for Lin is Lin_43. It should be updated to Lin. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: HLD component should be named Lin. Not Lin_43. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: In base driver we should update for S32K1 platform from Lin_43 to Lin in the modules.h file. For Lin driver the makefile, the sdk_manifest the generation files should be updated in order to change the name for Lin component in Lin
ARTD-14681	Bug	[GPT] GptChannelTickFrequency need auto calculate by the prescaler and McuClockReferencePointFrequency<*> Detailed description (how to reproduce it): GptChannelTickFrequency can not calculate correct the frequency if have 2 instance of ipv (like FTM STM Emios) Preconditions: always get the prescaler of the 1st instance of the list. Test Case ID (internal TC that caught the defect) optional: GPT_TS_001 Observed behavior: GptChannelTickFrequency incorrect Expected behavior: Auto calculate the GptChannelTickFrequency by the prescaler and the mcu reference Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: need correct the node GptChannelTickFrequency to calculate the frequency
ARTD-14677	Bug	[Platform] Build failed at IntCtrl_Ip on S32K324<*> e:/Zebra/ARTD_S32K3_NOSASW/output/S32K3XX_S32K324_gcc/mcl/../../eclipse/plugins/Platform_TS_T40D34M9I0R0/src/IntCtrl_Ip.c: In function 'IntCtrl_Ip_GenerateDirectedCpuInterruptPrivileged': e:/Zebra/ARTD_S32K3_NOSASW/output/S32K3XX_S32K324_gcc/mcl/../../eclipse/plugins/Platform_TS_T40D34M9I0R0/src/IntCtrl_Ip.c:534:17: error: 'MSCM_IRCPnIRx' undeclared (first use in this function); did you mean 'MSCM_IRCPnIRx_Type'? 534 MSCM_IRCPnIRx->IRCPnIRx[core][irqId].IGR = 0x1U; MSCM_IRCPnIRx_Type

ID	Subtype	Headline and Description
ARTD-14679	Bug	[ADC] mismatch EB and S32CT when comparing code generation<*> Detailed description (how to reproduce it): There is some information that does not match EB and S32CT when comparing code generation. Generating the following devtest can reproduce the issue TS009 cfg2 with Dma configuration TS001 PC configuration to be fixed under ARTD-14726 from Ecuc Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: There is some information that does not match EB and S32CT when comparing code generation. Expected behavior: EB and S32CT codegen must be indentical Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-14684	Bug	[FLS] the SPTRCLR need clear after the driver sets BFGENCR to the appropiate LUT index<*> Detailed description (how to reproduce it): The default LUT id for AHB reads is zero as BFGENCR reset value is 0 (actually this is why LUT[0] has a reset value 0818_0403h, 2400_1C08h since its a "common" read sequence for most flash chips). In the Fls module, the QSPI_IP_AHB_LUT is defined as 1, and while the driver sets BFGENCR to the appropriate LUT index, it forgets to follow the RM recommendation: If the sequence pointer differs in the new and the previous sequences, you should reset it. See sequence pointer clear register for more information. This means that the driver should W1C into SPTRCLR.BFPTRC for the peripheral to operate correctly. the customer was having issues because of this, in their environment instead of implementing this, they exchanged QSPI_IP_AHB_LUT and QSPI_IP_COMMAND_LUT so QSPI_IP_AHB_LUT stays at 0. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: N/A Expected behavior: The the sequence pointers must be cleared in the initialization phase. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A

ID	Subtype	Headline and Description
ARTD-14687	New	New Feature [CRC][Optimize] Update bit reversal using tables ,,"NewWorkDescription: The CRC driver needs optimizations for bit reversal and table/software calculation. Proposed solution optional: 1. Update bit reversal using tables."
ARTD-14703	Bug	[ADC] Adc_Ipw_MapCTUTriggerIndex has invalid trigger index of trigger source array<*> Detailed description (how to reproduce it): When control mode is enabled, Adc_Ipw_MapCTUTriggerIndex might not query all members of array or point to out of range of array if number of hwtrigger is not equal to number of trigger in control mode The Adc_EnableCTUTrigger function is intended for trigger mode but Adc_Ipw_MapCTUTriggerIndex wrapping between trigger mode and control mode. This seems confusing users When supporting trigger mode, it points to AdcConfigSet/AdcHwTrigger }} but this array also contains trigger source directly to ADC not via BCTU/CTU while the name of function is Enable CTU trigger? Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: compile error Expected behavior: compiler no error Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:

ID	Subtype	Headline and Description
ARTD-14702	Bug	[S32K3XX] [PORT] Do not have any notification when config unavailable channel in S32K312<*> Detailed description (how to reproduce it): 1. with tag BLN_PORT_060, config test Port_TS_015 in S32K312, try to config channel PTA23 (not available in S32K312 Q172) 2. Cannot choose mode for channel Preconditions: if config not available channel, EB need to shown error about this driver need to support all available mode of channel Test Case ID (internal TC that caught the defect) optional: Port_TC_WBT_0010/Port_TS_015 Observed behavior: don't have any warning or error about this issue: !image-2021-08-04-17-23-26-354.png! don't see any mode: !image-2021-08-05-10-59-42-134.png! Expected behavior: driver need to be update to fix this issue Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-14726	New	New Feature [EcuC] Add requiresIndex to EcucPartition ,,"Detailed description (how to reproduce it): ADC get the list Partition from EcucPartitionCollection/EcucPartition array. When importing epc output from Ecuc of EB tresos to S32DS S32DS import the partition order following ""Name"" field but the order in EB following ""index"" column. this makes ADC has different in generated code bw Eb and CT !image-2021-08-05-14-46-19-370.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: ADC_TS_001 DevTest Observed behavior: [...] Expected behavior: generated code is indentical Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Use <REQUIRES-INDEX> attribute as the post in team [https://teams.microsoft.com/dl/launcher/ launcher.html?url=%2F_%23%2Fl%2Fmessage %2F19%3Ae451c595d3ba410c8f9c1f5efc19a8a3%40thread.tacv2%2F1618569101137%3FtenantId %3D686ea1d3-bc2b-4c6f-a92c-d99c5c301635%26groupId%3Df9decd68-7b74-4101- a4d2-ad54e86f727f%26parentMessageId%3D1618569101137%26teamName %3DZebra%26channelName%3DConfiguration%2520(code%252C %2520DS%252C%2520EB%252C%2520etc)%26createdTime %3D1618569101137&type=message&deeplinkId=7af9cc4b-4bf4-4f14-8e9c- c1a7f75cf125&directDl=true&msLaunch=true&enableMobilePage=true&suppressPrompt=true]"

ID	Subtype	Headline and Description
ARTD-14734	Bug	[CRYPTO] Remove unsupported key types from the NVM and RAM key catalogs<*> Detailed description (how to reproduce it): HSE_KEY_TYPE_SHARED_SECRET key group can only be used for RAM key catalog HSE_KEY_TYPE_RSA_PAIR key group can only be used for NVM key catalog. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Can configure select SHARED_SECRET from NVM key catalog Can configure select SHARED_SECRET from NVM key catalog Expected behavior: Remove SHARED_SECRET from NVM key catalog Remove RSA_PAIR from RAM key catalog Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-14750	Bug	[RM] Missing validate in configuration MPU M7<*> Detailed description (how to reproduce it): Missing validate in configuration MPU M7 => Missing define variable "Mpu_M7_Config" => Build fail Preconditions: Node "RM Enable MPU_M7 Support " is ON. Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: variable "Mpu_M7_Config" is called but hasn't been define. Expected behavior: Define variable "Mpu_M7_Config" if using "RM Enable MPU_M7 Support " Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-14756	Bug	[S32K3XX] [PORT] Port_SetPinMode affected to PKE value in MSCR<*> Detailed description (how to reproduce it): use tag PVT_ARTD_PORT_V150, config PKE enable in channel with MSCR = 80, check PKE bit after declare Port_SetPinMode to INOUT MODE 1 Preconditions: Port_SetPinMode just config mode (SSS value), not affect to PKE bit Test Case ID (internal TC that caught the defect) optional: Port_TS_005/Port_TC_WBT_0015 Observed behavior: Port_SetPinMode affect to PKE bit, 0x80001 was turn off PKE bit !image-2021-08-06-16-44-11-991.png! Expected behavior: Driver need to be update to fix this issue Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-14757	Bug	[SPI] Different in SpiFlexioEnable node location between EB and CT<*> Detailed description (how to reproduce it): In EB, the SpiFlexioEnable is located in SpiAutosarExt container but in CT it is SpiGeneral. Must be synchronous between them Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: SpiFlexioEnable is in different container in EB and HLD CT Expected behavior: in same container Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Synchronous them
ARTD-14824	New	New Feature [FEE] Add support for bad Sector Management and Sector Retirement (part 3) ,,"NewWorkDescription: Add support for bad Sector Management and Sector Retirement (CPR_RTD_00505.fee). This involves removing Sectors from configuration when they become unusable. Rationale: some flash memory specs have low endurance/write cycles availability, which needs to be improved by the ability to retire bad sectors or locations affected by permanent ECC, at the expense of allocated flash size the endurance being a ppm specification."" Requirement source: cPRD (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: # Update CT part # Update User manual to introduce the feature"

ID	Subtype	Headline and Description
ARTD-14835	Bug	[S32K3XX][PORT] Build fail on S32K312 due to Tspc_Port_Ip_Types.h include wrong file<*> Detailed description (how to reproduce it): When build wiring test for dio on S32K312, Tspc_Port_Ip_Types.h still include S32K344_TSPC.h => build fail !image-2021-08-09-17-02-36-007.png! !image-2021-08-09-17-03-36-352.png! Preconditions: Plugin from PVT_ARTD_PORT_V150 Test Case ID (internal TC that caught the defect) optional: Dio_TC_WIR_00100 Dio_TC_WIR_00201 Observed behavior: Build fail dio wiring test on S32K312 (using port module) Expected behavior: ext test build pass on S32K312 Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-14836	Bug	[BASE] OsIf_GetCoreID function always returns 0 with CORE_SETS is 1<*> Detailed description (how to reproduce it): N/A Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Crc_TC_FCT_0721 Observed behavior: OsIf_GetCoreID function always returns 0 with CORE_SETS is 1 because OSIF_ENABLE_MULTICORE_SUPPORT macro is only enabled in base module !image-2021-08-09-16-57-38-072.png|thumbnail! Expected behavior: Update driver code to return 1 when CORE_SETS is 1 Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-14852	New	New Feature [RM][S32K3XX] Improve for XBIC Ip ,,"NewWorkDescription: Create interface. Update function's name follow requirement improve code better update code for user mode support part Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: update follow description"

ID	Subtype	Headline and Description
ARTD-14861	Bug	[Platform][S32K3xx_RTM1.0.0] Build Failed on IAR with "Relocation failed" ,,"Detailed description (how to reproduce it): During build test either IAR8.40 or IAR8.50.1.0, got this log : Error[Lp002]: relocation failed: value out of range or illegal: 0xffff'ffff'ffff'd882 Kind : R_ARM_THM_JUMP11[0x66] Location: 0x40'49d6 ""SVC_Handler"" 0xe Module: e:\workspace\RTD_K3_RTM100\output\S32K3XX_S32K344_iar\fls \Fls_TS_000_cfgCORE0\out\exceptions_c.o Section: 8 (.mcal_text) Offset: 0xe Target : 0x40'225d ""SVCHandler_main"" Module: e:\workspace\RTD_K3_RTM100\output\S32K3XX_S32K344_iar\fls \Fls_TS_000_cfgCORE0\out\exceptions_c.o Section: 14 (.mcal_text) Offset: 0x1 Aslo, build failed existing when build on GCC_10.2 , please see the below log file attached . Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Build Failed Expected behavior: NA Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-14858	Bug	[S32K3XX] [PORT] Driver generate incorrect value OBE index when TSPC configuration<*> Detailed description (how to reproduce it): with tag BLN_PORT_063, port driver was generate incorrect OBE index of pins config TSPC enable Preconditions: Pins config TSPC enable need to have correct value in obe index Test Case ID (internal TC that caught the defect) optional: Port_TC_WBT_0024/Port_TS_007 Observed behavior: in generate TSPC of pins config: !image-2021-08-10-10-33-18-264.png! if value = 65535 (or 0xFFFF), the condition never was occur==> never enable OBE index for config pins: !image-2021-08-10-10-34-46-233.png! Expected behavior: Driver need to be update generate file of pins which was config TSPC enable Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA

ID	Subtype	Headline and Description
ARTD-14859	New	New Feature [RM] Review and update VIRT_WRAPPER IP ,,Review and update VIRT WRAPPER IP
ARTD-14862	Bug	[SPI] Add condition related to must enable pin configuration for Flexio on CT<*> Detailed description (how to reproduce it): Now, CT tool does not raise any an error if not configure for spi pins of flexio Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: No error is raised to notification for user Expected behavior: An error if pins is not configured Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Add an constraint on CT template file
ARTD-14897	Bug	[Mcl] Static_Dma_Ip_SetLogicChannelScatterGatherInit: can not return DMA_IP_STATUS_WRONG_CONFIG<*> Detailed description (how to reproduce it): Use config scatter/gather config and try to return DMA_IP_STATUS_WRONG_CONFIG but EB and CT just only support max is 256 scatter/gather > Can't config more than 256 So can not create test script for return case DMA_IP_STATUS_WRONG_CONFIG Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: Function: Static_Dma_Ip_SetLogicChannelScatterGatherInit !image-2021-08-10-18-08-25-330.png! Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-14898	New	New Feature [pinTool] supports parsing TSPC information in pin signal configuration generation ,,"NewWorkDescription: Update resource for your driver following below derivatives for this release: S32K312: S32K312_172MQFP, S32K312_100MQFP S32K314: S32K314_257MAPBGA, S32K314_172MQFP S32K324: S32K324_257MAPBGA, S32K324_172MQFP S32K344: S32K344_257MAPBGA, S32K344_172MQFP Requirement source: S32K3xx Reference Manual, Rev. 2 Draft D, 07/2021, [Link|https:// nxp1.sharepoint.com/:b:/r/sites/Zebra/Shared%20Documents/Documents/Platforms/ S32K3xx/RM/S32K3xx_RM_Rev2DraftD.pdf?csf=1&web=1&e=6kLAfr] Proposed solution optional: Update driver resources"
ARTD-14899	Bug	[ADC] Adc_Sar_Init should disable channels/features if not enabled/configured<*> There are some features/channels that are considered as disabled in generated configuration but when calling Adc_Sar_Init function, it does not disable these ones on hardware and keep them as default or previous state Proposal to disable them if not used
ARTD-14978	New	New Feature [ADC] Remove per Group indexation of pResultsBufferPtr ,,"NewWorkDescription: Remove per Group indexation of pResultsBufferPtr, because it is part of Adc_GroupConfigurationType, so can already be accessed per group: Adc_pCfgPtr[u32CoreId]->pGroups[GroupIndex].pResultsBufferPtr[Group] "
ARTD-15056	Bug	S32K3 CT Pins ID Length Issue<*> Detailed description (how to reproduce it): If the PIN ID in the configuration tool is set with a long string, the generated pin name MACRO might be with error in "Siul2_Port_Ip_Cfg.h". Please see attached figure for an example. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Proposed solution optional: Either limit the pin ID length or change the generated MACRO in header file.

ID	Subtype	Headline and Description
ARTD-15057	Bug	[Base] ADC_AMSIO bit is in correct in ADC Header<*> The latest RM Rev2 DraftD chapter 57.5.2.66 Analog Miscellaneous In/Out register (AMSIO) AMSIO_HSEN has 2 bit but current header file show only 1 bit #define ADC_AMSIO_HSEN_MASK (0x20000U) #define ADC_AMSIO_HSEN_SHIFT (17U) #define ADC_AMSIO_HSEN_WIDTH (1U) It must be: #define ADC_AMSIO_HSEN_MASK (0x60000U) #define ADC_AMSIO_HSEN_SHIFT (17U) #define ADC_AMSIO_HSEN_WIDTH (2U) This is document issue. Please refer to attachment if needed !image-2021-08-11-15-31-59-192.png!
ARTD-15059	Bug	[RM] Missing validate in configurating PFlash<*> Detailed description (how to reproduce it): Missing configuration "PflashMasterProtection_0" =>Define array " Pflash_Config_VS_0[0]" with size = 0 => Build Fail => Build fail Preconditions: Node "RM Enable Plfash Support" ON. Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-15062	Bug	[LIN] Features Lin Frame Timeout Disable only applied with case node is slave.<*> Detailed description (how to reproduce it): About features Lin Frame Timeout Disable, Now driver only applied with case node is slave, lacking with case node is master for LPUART Driver don't need to checking timer out when master node transmits header frame for FLEXIO Preconditions: !image-2021-08-11-17-17-53-703.png! Test Case ID (internal TC that caught the defect) optional: Lin_TC_FCT_0019 Observed behavior: NA Expected behavior: NA Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA

ID	Subtype	Headline and Description
ARTD-15070	Bug	ICU: The header file included for derivative 312 is not correct for IPs used<*> Detailed description (how to reproduce it): Header file included for derivative 312 is the one for 344. !image-2021-08-11-16-59-53-745.png|width=369,height=98! !image-2021-08-11-17-00-18-696.png|width=418,height=111! !image-2021-08-11-17-00-53-075.png! Preconditions: use 312 derivative for EBT test or DS example Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: Incorrect derivative header file used Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-15076	Bug	[S32K312] [PORT] Driver was generated redundant unavailable pins<*> Detailed description (how to reproduce it): execute tag: BLN_PORT_064, run test internal test port, over the Port_Init function Preconditions: Port_Init will be config all used pins and unused pins of derivative, which was available in IOMUX for K312 Test Case ID (internal TC that caught the defect) optional: Port_TS_006/Port_TC_WBT_0018 Observed behavior: The pin 148 was generate unavailable but still write GPDO==> hard fault when execute Port_Init !image-2021-08-12-10-24-49-156.png! !image-2021-08-12-10-26-53-760.png! Expected behavior: Driver need to be update unused pin available according IOMUX Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA

ID	Subtype	Headline and Description
ARTD-15082	Bug	[I2c] Fix driver build fail on S32K312<*> Detailed description (how to reproduce it): [...] !image-2021-08-12-11-40-42-244.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-15088	New	New Feature [S32K3xx] add dummy value into some fields of Port resources ,,"NewWorkDescription: Add one dummy value into the following resources of Port for CT using: Port.Siul2InstanceMscrIdxStart Port.Siul2InstanceMscrIdxEnd Port.Siul2MaxNumConfiguredMscrs Port.Num16PinsBlocks Requirement source: Development (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]"
ARTD-15115	Bug	[S32K3][SPI] Build fail relate to include S32K324_[IPV].h<*> Detailed description (how to reproduce it): When use resource S32K324 to build test, Flexio_Spi_Ip_Cfg.h and Lpspi_Ip_Cfg.h are including S32K324_FLEXIO.h and S32K324_LPSPI.h. But both of headers don't exist in base/header. Currently, base/header includes S32K344 and S32K312 only. Preconditions: Using resource S32K324 Test Case ID (internal TC that caught the defect) optional: Spi_TS_009 Observed behavior: NA Expected behavior: NA Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-15101	New	New Feature [icu] Create dev tests to be run on the target ,," NewWorkDescription: Create functional development tests that can be run on the target and that test the main functionality of the driver. The purpose of the development tests is to validate that the driver does not have S1 and S2 bugs. The dev tests will be executed on remote setups from Bamboo when running the EXECUTE CI option from ManifestValidator*, when applying a new TAG in the manifest. Implementation Notes The tests should be designed in a way such that no external hardware is required. Use as much as possible the features of the boards that we have available, by using internal loopback or connecting pins to each other on the same board*. The intent is to have one identical setup for all the drivers that can run the development tests, triggered from Bamboo. Also, this will make it easier to duplicate the setup for debugging, without keeping the board used by Bamboo busy. For that, update the wiring information in the shared document ([https://nxp1.sharepoint.com/:x:/r/sites/Zebra/Shared%20Documents/Testing/Dev_tests/DevTests_Wiring.xlsx?d=we0b72309cbad4044960d6c095a90de5c&csf=1&web=1&e=CLWKeW)| https://nxp1.sharepoint.com/:x:/r/sites/Zebra/Shared%20Documents/Testing/Dev_tests/DevTests_Wiring.xlsx?d=we0b72309cbad4044960d6c095a90de5c&csf=1&web=1&e=CLWKeW]. Group test cases in test suites. Define different test suites when a different configuration is needed (either for your driver or for dependencies). Tests with multiple configurations (M4 tags in configuration) are allowed and can be used for variating certain configuration options, when needed. If possible, reusing the shared configuration, the test used for static analysis, or parts of the examples is encouraged as it will reduce maintenance effort. However, if this is not possible, it is not mandatory to reuse configurations or code. The wiring used for examples should be the same as for the development tests. Exceptions will be discussed, but the intent is to have the same hardware setup for both dev tests and examples. Before closing this activity you should: # Update the wiring information here: [https://nxp1.sharepoint.com/:x:/r/sites/Zebra/Shared%20Documents/Testing/Dev_tests/DevTests_Wiring.xlsx?d=we0b72309cbad4044960d6c095a90de5c&csf=1&web=1&e=CLWKeW] # Inform the PE team, or a person in RTD with admin privileges on the Bamboo plans to update the list of development tests to be run on the hardware # Test the development tests, first by using the remote hardware setups, then by using the Bamboo custom builds or even the manifest validator Extra notes The remote run support from beart is used for running the tests from Bamboo on the boards. Running the tests on the board is a skippable step, as for now we have no support for pre-silicon run (like running on the simulator) from Bamboo. This activity will be started on K3, as a pilot. For the rest of the platforms, the ""_*Development tests and execution*_"" ticket raised by the PM will be used for porting these tests. Wiki for dev tests: [https://confluence.sw.nxp.com/display/AUTORD/Development+test] (Work In Progress, any input is appreciated) Requirement source: G0 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: See description"

ID	Subtype	Headline and Description
ARTD-15128	New	New Feature [S32K3XX][PORT] Separate the functions in IP layer ,,"NewWorkDescription: There are some functions in IP layer which do not represent for any requirements in IP layer. They are used for HLD. Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Move these functions to IPW "
ARTD-15133	Bug	[RM] Wrong generation code for MPU M7 IP<*> Detailed description (how to reproduce it): Wrong generation code for MPU_M7's Region config Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-15136	Bug	[S32K3xx][RTM100][Port] DSE fields are not available for some pins<*> Detailed description (how to reproduce it): Use the newest tag of PORT (PVT_ARTD_PORT_V152) to generate plugins. Open tresos and use resource s32k314_mapbga257 in Resource module then open Port module. Add some mscr pins whose DSE's field are available mentioned in K344_ioMux (23, 114, 156, 158, 164, 167, 168, 174, 180, 181, 185, 188, 189, 191, 198, 199, 200, 205, 207, 208, 209, 210, 211, 212, 213, 214, 215, 216, 217, 218, 219) Observed behavior: DSE's field of those pins are not available to configurate !image-2021-08-13-12-03-38-672.png|width=536,height=350! Expected behavior: Those pins' DSE field must be configurable according to IOMux Proposed solution optional: It looks like that the resource mentioned in Port drivers excluded those pin mscr number so that the drivers does not let users configurate DSE's field. !image-2021-08-13-12-08-01-921.png|width=1411,height=741!

ID	Subtype	Headline and Description
ARTD-15148	Bug	[BASE] Some wizard data files are missing the copyright header<*> Detailed description (how to reproduce it): At least Clock_Ip_Cfg_Defines.h, Clock_Ip_Cfg_Defines.c, Clock_Ip_PBcfg.c, Clock_Ip_PBcfg.h, Clock_Ip_Cfg.c, Clock_Ip_Cfg.h, Siul2_Port_Ip_Cfg.c, Siul2_Port_Ip_Cfg.h are missing the comment header block including the copyright Preconditions: None Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Missing copyright Expected behavior: Comment header block should be there Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Review the files in Base and add the comment header block
ARTD-15151	Bug	[Uart] Update code follow new changes of requirement<*> Detailed description (how to reproduce it): Update code follow req changes on ticket: https://jira.sw.nxp.com/browse/AAI-907 Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-15155	Bug	[S32K3][SPI] Issue with Spi_lpw_au8LpspiHWUnitMapping array<*> Detailed description (how to reproduce it): In the function Spi_lpw_Init, we use Spi_lpw_au8LpspiHWUnitMapping to allocate HWUnitId which is compatible with HWUnit->Instance: !image-2021-08-13-17-16-12-567.png|width=450,height=89! But size Spi_lpw_au8LpspiHWUnitMapping (LPSPI_IP_NUMBER_OF_INSTANCES) is the number of configured LPSPI instance: static Lpspi_lp_StateStructureType Lpspi_lp_axStateStructure[LPSPI_IP_NUMBER_OF_INSTANCES]; !image-2021-08-13-17-19-26-295.png|width=475,height=174! This causes: when we configure 2 instances (LPSPI0, LPSPI2), we can't allocate HWUnitId of LPSPI2. Because Spi_lpw_au8LpspiHWUnitMapping's size is 2 (_LPSPI_IP_NUMBER_OF_INSTANCES = 2) and it needs the 3rd element for LPSPI2 (HWUnit->Instance = 2) Preconditions: NA Test Case ID (internal TC that caught the defect) optional: Spi_TS_003 Observed behavior: NA Expected behavior: NA Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-15144	Bug	[ADC] ADC group INTERRUPT contains only one channel cannot be converted, in case both INTERRUPT and DMA method are used in ADC HW Unit ,,"Detailed description (how to reproduce it): When ADC_DMA_SUPPORTED parameter is configured as TRUE and configure at least one group uses INTERURPT and one group uses DMA method, then a conversion is started for a group using INTERRUPT me that contains only 1 channel, the system crashes although that specific group is not configured for a HW Unit that uses DMA as transfer type. Preconditions: ADC_DMA_SUPPORTED parameter is configured as TRUE. Create two HW instance, one uses INTERRUPT (e.g. HwUnit_0) and one uses DMA (e.g. HwUnit_1). Configure one group (e.g. Adc0Group0) with only one channel in HwUnit_0 and one group in HwUnit_1 (e.g. Adc1Group0). Start group conversion with Adc0Group0 Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: After finished conversion for Adc0Group0 (the group uses INTERRUPT method and contains only one channel), the code hit ISR then jumped to Adc_Ipw_UpdateGroupState(). When executing this piece of code: !dma_adc.jpg|width=743,height=230! the system was crashed. Expected behavior: In case both INTERRUPT and DMA are considered for ADC group conversion, the conversion for group uses INTERRUPT method and only contains one channel shall be successful, without any system crashed. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-15156	New	New Feature [ICU][S32K3XX] Error for callback in timestamp mode ,,"In timestamp mode, the function Icu_ReportEvents is used for overflow notification but it is also calling the function Timestamp1_Notification : !image-2021-08-13-17-55-40-559.png! In the init function for emios, the notification enable variable is turned, so the callback function is always called when not calling the function notification to enable first. !image-2021-08-13-18-01-57-071.png! And the master bus A is initialized into internal bus as due to this value : !image-2021-08-13-18-03-51-099.png! !image-2021-08-13-18-04-36-038.png! "

ID	Subtype	Headline and Description
ARTD-15275	New	New Feature [icu] Update resources via RM S32K3xx Rev2 ,,"NewWorkDescription: Update resource for your driver following below derivatives for this release: S32K312: S32K312_172MQFP, S32K312_100MQFP S32K314: S32K314_257MAPBGA, S32K314_172MQFP S32K324: S32K324_257MAPBGA, S32K324_172MQFP S32K344: S32K344_257MAPBGA, S32K344_172MQFP Requirement source: Reference Manual|S32K3xx Reference Manual, Rev. 2, 08/2021, [Link|https:// nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx? originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3 %5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared %20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FS32K3xx %5FRM%5FRev2%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents %2FDocuments%2FPlatforms%2FS32K3xx%2FRM] Datasheet|S32K3xx Data Sheet, Rev. 2 - 08/2021, [Link|https:// nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx? originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3 %5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared %20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FS32K3xx %5FDS%5FRev2%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents %2FDocuments%2FPlatforms%2FS32K3xx%2FDS] Proposed solution optional: Update driver resources"

ID	Subtype	Headline and Description
ARTD-15283	New	New Feature [rm] Update resources via RM S32K3xx Rev2 ,,"NewWorkDescription: Update resource for your driver following below derivatives for this release: S32K312: S32K312_172MQFP, S32K312_100MQFP S32K314: S32K314_257MAPBGA, S32K314_172MQFP S32K324: S32K324_257MAPBGA, S32K324_172MQFP S32K344: S32K344_257MAPBGA, S32K344_172MQFP Requirement source: Reference Manual|S32K3xx Reference Manual, Rev. 2, 08/2021, [Link|https:// nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx? originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3 %5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared %20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FS32K3xx %5FRM%5FRev2%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents %2FDocuments%2FPlatforms%2FS32K3xx%2FRM] Datasheet|S32K3xx Data Sheet, Rev. 2 - 08/2021, [Link|https:// nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx? originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3 %5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared %20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FS32K3xx %5FDS%5FRev2%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents %2FDocuments%2FPlatforms%2FS32K3xx%2FDS] Proposed solution optional: Update driver resources"

ID	Subtype	Headline and Description
ARTD-15286	New	New Feature [spi] Update resources via RM S32K3xx Rev2 ,,"NewWorkDescription: DS: update baudrate configuration follow 12.1.1 LPSPI section: S32K314, S32K324, S32K344, S32K322, and S32K342 supports data rate up to 20 Mbps, S32K312 and S32K311 supports data rate up to 15 Mbps. Only one LPSPI instance support 20 MHz in loopback mode that is LPSPI0 All LPSPIs supports a minimum a 10 MHz data rate on standard plus pads and 7.5 MHz on standard pads. Requirement source: Reference Manual|S32K3xx Reference Manual, Rev. 2, 08/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FS32K3xx%5FRM%5FRev2%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM] Datasheet|S32K3xx Data Sheet, Rev. 2 - 08/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FS32K3xx%5FDS%5FRev2%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS] Proposed solution optional: the range of baudrate will be handle by some variables in resource files to be compatible with each instance"

ID	Subtype	Headline and Description
ARTD-15287	New	New Feature [uart] Update resources via RM S32K3xx Rev2 ,,"NewWorkDescription: Update resource for your driver following below derivatives for this release: S32K312: S32K312_172MQFP, S32K312_100MQFP S32K314: S32K314_257MAPBGA, S32K314_172MQFP S32K324: S32K324_257MAPBGA, S32K324_172MQFP S32K344: S32K344_257MAPBGA, S32K344_172MQFP Requirement source: Reference Manual|S32K3xx Reference Manual, Rev. 2, 08/2021, [Link|https:// nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx? originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3 %5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared %20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FS32K3xx %5FRM%5FRev2%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents %2FDocuments%2FPlatforms%2FS32K3xx%2FRM] Datasheet|S32K3xx Data Sheet, Rev. 2 - 08/2021, [Link|https:// nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx? originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3 %5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared %20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FS32K3xx %5FDS%5FRev2%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents %2FDocuments%2FPlatforms%2FS32K3xx%2FDS] Proposed solution optional: Update driver resources"
ARTD-15216	Bug	[CAN] EB/S32CT comparation fail at can_ts_1455<*> Detailed description (how to reproduce it): build/run can_ts_1455 for EB and S32CT / s32k344 can_ts_1455 fail with S32CT Please look at attached output for analysis Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: CAN_TC_FCT_14550 Observed behavior: difference between generated code of two tools Expected behavior: same generated code between s32ct and EB Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A

ID	Subtype	Headline and Description
ARTD-15217	New	New Feature [S32K3xx] Dio add support Virtual Wrapper into Dio HLD CT ,,"NewWorkDescription: Virtual wrapper has been supported on EB tresos from release K3 beta, but it's not available on S32CT > Add Virtual Wrapper functionality into Dio HLD CT The changes included: update code generation for Virtual Wrapper update configuration and node validation for Virtual Wrapper Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]"
ARTD-15219	Bug	[ICU] The ICU of eMIOS will get wrong Signal Measurement if bus counter is used.<*> Detailed description (how to reproduce it): In Emios_Icu_Ip_Irq.c, there are two static functions which cannot work as expected and lead to wrong Signal Measurement result when bus counter is used. static inline uint32 Emios_Icu_Ip_GetChannelClockMode*(): !image-2021-08-16-09-22-26-072.png! The OR operation should be AND operation to get the right channel clock mode. static inline uint32 Emios_Icu_Ip_ReadCounterBus*() This function is used to get the period of bus counter. When Bus Diverse, Bus A or Bus F is selected, this function will get channel clock mode first (mentioned above) and then check whether it is equal to EMIOS_ICU_MCB_INT_CLOCK_U32 or not. Just take case Bus F as an example: !image-2021-08-16-09-45-37-474.png! In this process, there are two wrong points: # The clock mode is wrong as mentioned above. # The u32Period will be wrong if the clock mode is not equal to* EMIOS_ICU_MCB_INT_CLOCK_U32 because there is no any bus counter mode which uses Register B as period register (refer to RM 59.5.3.14 and 59.5.3.15). As a consequence, the ICU of eMIOS will get wrong Signal Measurement result if bus counter is used. Preconditions: This issue will happen only when IcuEmiosBusSelect is set to Bus A, Bus F or Bus Diverse. !image-2021-08-16-10-57-28-438.png! Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-15226	Bug	[Spi] No error raise when SpiMaxDmaFastTransfert not enable and Dma Fast transfer support<*> Detailed description (how to reproduce it): To support Dma Fast transfer, SpiPhyUnit is used by External Device in Job must has SpiMaxDmaFastTransfer enabled. Preconditions: SpiEnableDmaFastTransfer is True SpiEnableDmaFastTransferSupport is True SpiGlobalDmaEnable is True Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: NA Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Raise an error
ARTD-15229	New	New Feature [RM][S32K3XX] Improve XRDC driver code related to PID ,,"NewWorkDescription: Update master cores which are available for PID. Use of PIDm[PID] can be aborted if a core already had a built-in PID register (indicated in HWCFG2 register) Fix build warning in S32DS Requirement source: (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: NA"
ARTD-15220	New	New Feature [S32K3XX][DIO] The Exclusive Areas should be reviewed and updated ,,"NewWorkDescription: The Exclusive Areas for K3 platform are incorrect. Some of them are redundant (need to be removed), and the rest need to be renamed. Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Remove/Add/Renaming the Exclusive Areas in code for K1. From IPW to IPL. All exclusives should be existed in IPL. The ones in IPW should be removed. #include SchM_Dio.h should be moved from IPW to IPL Update the UM/IM if needed Check and update RTE if needed"

ID	Subtype	Headline and Description
ARTD-15227	New	New Feature [RM] [S32K3] Fix build fail on S32DS ,,"NewWorkDescription: Build fail on DS as below: !image-2021-08-16-10-48-10-464.png! Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Correct generated files"
ARTD-15295	Bug	[WDG] Incorrect generated code between Instances<*> Detailed description (how to reproduce it): I compared generated code between instance and saw some incorrect generated value. I note in excel file in the attachment. Please review it and update generated code. If there are any nodes that you will not update, please comment the reason why. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: Incorrect generated code between instances. Please see attach files to more details. Expected behavior: Correct generated code. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-15296	Bug	S32K3 Port Configuration<*> In the SPI example, the port (SIUL2) is initialized by baremetal code, not by Port_Init(). Is there any limitation in using Port ? I tried to configure a different SPI example, but found that the port is not set as I desired. For example, I set PTE1 (MSCR129) as LPSPI0_SCK. The MSCR_SSS value for this port (MSCR129) is 2. It's no problem But the MSCR_OBE should be 1. I can see in the generated code that MSCR129 value is 2 instead of 0x00200002. So when I run the code, I found that MSCR129 is set to LPSPI0_SCK output but the MSCR_OBE bit is 0. So the SPI cannot run properly. Could you please advise what might be wrong or missing in my PORT settings?

ID	Subtype	Headline and Description
ARTD-15301	Bug	[S32K3XX][S32K3XX_100] Initialization handler interrupt fail by Platform InstallIrqHandler function<*> Detailed description (how to reproduce it): Installing interrupt handler by Platform_Init funcition or Platform_InstallIrqHandler funcition and Enable interrupt, after that generate interrupt trigger. The driver can't into interrupt handler. Maybe handler funciton initaization failed. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Platform_TS_001 Observed behavior: N/A Expected behavior: The diver install handler funcition successful Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-15306	Bug	[RM] Wrong syntax when call function Mpu_M7_Ip_Deinit_Privileged()<*> Detailed description (how to reproduce it): Missing () when call function Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Fix syntax call function
ARTD-15307	Bug	[S32K3XX] Failure at building on S32K312 with GHS, GCC compilers ,,"Detailed description (how to reproduce it): N/A Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Failure at building on S32K312 with GHS, GCC compilers because ram overflow(http://ceram.ea.freescale.net/1/project/ar_int_crc_ghs/details) Expected behavior: Build success on S32K312 Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A

ID	Subtype	Headline and Description
ARTD-15311	Bug	[WDG] Findings need to fix follow to Code Checklist Review<*> Detailed description (how to reproduce it): Something didn't follow to coding rule (checklist in ticket: https://jira.sw.nxp.com/browse/ARTD-9123) Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Need to fix
ARTD-15312	Bug	[SAI] Fix code review and UML review check list items failed<*> Detailed description (how to reproduce it): Fix code review and UML review check list items failed Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-15313	New	New Feature [BASE] Update header files for S32K344 corresponding RM rev 2 ,,"NewWorkDescription: Update header files for S32K344 corresponding RM rev 2 Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]"

ID	Subtype	Headline and Description
ARTD-15318	Bug	[BASE] Templating engine does not correctly report Java exceptions<*> Detailed description (how to reproduce it): 1. Make the setup from UCT-4375 2. The error message is undefined As we analyzed it, this is from a bug in templatingengine.js file. !image-2021-08-16-17-38-59-868.png! error.stack doesn't exist. error variable is from class *IllegalFormatConversionException, so you can use the next variant: scriptApi.logError(error);* ** (the result will be like in next print) !image-2021-08-16-17-38-23-705.png!
ARTD-15325	Bug	[S32K3XX][S32K3XX_100] The project build fail by some base pointer incorrect<*> Detailed description (how to reproduce it): Create test for platform module, add platform, base to project, clean generate, parse build, some base pointer is incorrect Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Platform_TS_001 Observed behavior: !image-2021-08-17-09-52-15-708.png! Expected behavior: Modifier base pointer Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-15329	Bug	[CRYPTO] EB Tresos doesn't raise error when CryptoKeyElementRefs are duplicated<*> Detailed description (how to reproduce it): In CryptoKeyType category , CryptoKeyElementRef column selects 2 same Refs But EB Tresos dosen't raise any error when CryptoKeyElementRefs are duplicated Preconditions: tag CRYPTO_078 Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: CryptoKeyElementRefs can be duplicated and not raise any error Expected behavior: [EB Tresos raises an error "*A reference to a CryptoKeyElement with the same CryptoKeyElementId already exists in the reference list "when CryptoKeyElementRefs are duplicated Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA

ID	Subtype	Headline and Description
ARTD-15337	Bug	[S32K312] I3C clock is not enabled on AIPS_0<*> Detailed description (how to reproduce it): [...] Run I3C test on K312 board Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] I3C clock is not enabled in sys_init function. Expected behavior: [...] I3C clock is enabled in sys_init function. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...] Change value of PRTN0_COFB1_CLKEN_REQ_MASK_U32 to 0x000137DFU
ARTD-15393	New	New Feature [S32K3XX][FLS] Update code after performing review Code_Review_Checklist and Design_Review_Checklist ,,"NewWorkDescription: Update code after performing review code_review_checklist and design_review_checklist report. Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: NA"

ID	Subtype	Headline and Description

ARTD-15396	Bug	[GPT]Marco PIT_0_CHANNELS_NUMBER is generated incorrectly when not using channel PIT_0_CH_RTI<*>
		
		Detailed description (how to reproduce it):
		When not using PIT_0_CH_RTI channel but using other channels of PIT_0 to run the test, I got the following problem:
		marco PIT_0_CHANNELS_NUMBER always generates 5 so the loop of Pit_Ip_GetInterruptBit function with channel equal to 4 was incorrect resulting in hard_fault error because we don't have the resource PIT_0_CH_4
		static inline uint32 Pit_Ip_GetInterruptBit(uint8 instance, uint8 channel)
		{
		uint32 returnFlag = 0U;
		#if (defined (PIT_IP_RTI_USED) && (PIT_IP_RTI_USED == STD_ON))
		if (RTI == channel)
		{
		returnFlag = ((pitBase[instance]->RTI_TCTRL & PIT_RTI_TCTRL_TIE_MASK) >> PIT_RTI_TCTRL_TIE_SHIFT);
		}
		else
		#endif
		{
		returnFlag = ((pitBase[instance]->TIMER[channel].TCTRL & PIT_TCTRL_TIE_MASK) >> PIT_TCTRL_TIE_SHIFT);
		}
		return returnFlag;
		}
		#endif
		Preconditions:
		When not using PIT_0_CH_RTI channel but using other channels of PIT_0
		Test Case ID (internal TC that caught the defect) optional:
		Gpt_TC_FCT_3016(Gpt_TS_303)
		Observed behavior:
		marco PIT_0_CHANNELS_NUMBER was incorrectly generated causing the loop in the Pit_Ip_GetInterruptBit function to be incorrect
		Expected behavior:
		marco PIT_0_CHANNELS_NUMBER is correctly generated so that the loop in the Pit_Ip_GetInterruptBit function is correct
		Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)
		Proposed solution optional:
		marco PIT_0_CHANNELS_NUMBER has a value of 4 when the channel PIT_0_CH_RTI is not used

ID	Subtype	Headline and Description
ARTD-15445	Bug	[I2c] Fix build fail driver due Mcl update<*> Detailed description (how to reproduce it): [...] !image-2021-08-18-10-39-52-742.png! Preconditions: [...] N/A Test Case ID (internal TC that caught the defect) optional: [...] I2c_TS_WIR_001 Observed behavior: [...] test case build fail Expected behavior: [...] Test case build pass Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-15473	New	New Feature [BASE] Add support for linker flash in S32K312 ,,"NewWorkDescription: Add support for linker flash in S32K312 Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: NA"
ARTD-15475	New	New Feature [BASE] Update header files for S32K312 corresponding RM rev 2 ,,"NewWorkDescription: Update header files for S32K312 corresponding RM rev 2 Requirement source: RM rev 2 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: NA"

ID	Subtype	Headline and Description
ARTD-15466	New	New Feature [BUILD_ENV] Create subchapter in IM about User mode configuration in AutosarOS ,,"NewWorkDescription: Create subchapter in IM about User mode configuration in AutosarOS. This will help user understand our User Mode approach and know what needs to be done in AutosarOS. Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Create subchapter in IM about User mode configuration in AutosarOS."
ARTD-15470	New	New Feature [RM][S32K3XX] Derivative S32K312 does not support IP Sema42 ,,"NewWorkDescription: S32K312 does not support IP Sema4, but DS and EB tresos still allow user to config Sema4 on this derivative. Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Raise an error when user try to config Sema4 on derivative S32K312"
ARTD-15474	Bug	[ETH] Update driver according to S32K3xx Reference Manual & Datasheet (Rev2)<*> Detailed description (how to reproduce it): Driver needs changing due to changes of new RM (S32K3xx Reference Manual, Rev. 2, 08/2021). Changes have been reviewed in ARTD-15242 Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: Driver changes according to new RM Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update driver code according to new header files (S32K344_EMAC.h...)

ID	Subtype	Headline and Description

ARTD-15483	New	New Feature
		
		[RM][S32K3XX] add XBIC APIs to enable/disable per Slave/Master Port of integrity checking on runtime
		,,"NewWorkDescription:
		Add new APIs:
		For HLD
		void Rm_XbicEnableMasterFeedbackCheck(uint32 xbicInstance, uint8 masterPort, boolean bFeedbackCheckEnable);
		void Rm_XbicEnableSlaveEDCCheck(uint32 xbicInstance, uint8 slavePort, boolean bEDCCheckEnable);
		For Ip:
		void Xbic_Ip_EnableMasterFeedbackCheck(uint32 xbicInstance, uint8 masterPort, boolean bFeedbackCheckEnable);
		void Xbic_Ip_EnableSlaveEDCCheck(uint32 xbicInstance, uint8 slavePort, boolean bEDCCheckEnable);
		Requirement source:
		NA
		(e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...)
		Proposed solution optional:
		NA"

ARTD-15484	New	New Feature [SPI] Synchronous between Spi.component and Spi.xdm ,,"NewWorkDescription: Some node in xdm and component is different type that is prescribed in NXP_RTD_AUTOSAR_S32CT.pptx as SpiChannelHalfDuplexSupport Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Remove node of component is not available in xdmd Change to array with node having optional attribute "

ID	Subtype	Headline and Description
ARTD-15491	Bug	[Wdg] Some DEM error nodes are redundant<*> Detailed description (how to reproduce it): Step 1: Run command: Clean generate any TS in list test of WDG Step 2: Check interface Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: Some DEM error nodes are redundant: WDG_E_CORRUPT_CONFIG, WDG_E_UNLOCKED, WDG_E_INVALID_PARAMETER, WDG_E_FORBIDDEN_INVOCATION, WDG_E_INVALID_CALL Please see the attached file for more detail. Expected behavior: Remove all Dem node not use Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-15529	New	New Feature [MCU] Support configuration for Callback Notification in IPL ,,"NewWorkDescription: Now Mcu doesn't support callback notification function at IPL. some callback function should be supported when using IP layer only. ex: POWER_IP_VLPSA_NOTIFICATION Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Add support callback notification at IPL"

ID	Subtype	Headline and Description

ARTD-15536	Bug	[WDG] Issue with unlock - lock sequence when config WdgOsifTimeoutVal = 0<*>
		
		Detailed description (how to reproduce it):
		I created a test can cover the case Wdg can not unlock with config like this WdgOsifTimeoutVal: = 0 and this can help cover the error case in Swt_Ip_Unlock
		if(ElapsedTicks >= TimeoutTicks)
		{
		ret = SWT_IP_STATUS_ERROR;
		}
		My test step is:
		Step 1: Init Wdg with SlowMode*: WdgOsifTimeoutVal: = 0 and WdgSettingsSlow_WdgSoftLockConfiguration := true
		Step 2: After Init, Bit Softlock (SLK) will set to 1
		Step 3: Call SetMode to set new mode FastMode
		(WdgSettingsFast_WdgSoftLockConfiguration: true)
		Step 4: SetMode will still return error in Swt_Ip_Unlock but bit SLK is also clear to 0 (that mean Wdg can unlock) and wdg is not lock again after SetMode function.
		Preconditions:
		[...]
		Test Case ID (internal TC that caught the defect) optional:
		[...]
		Observed behavior:
		Swt_Ip_Unlock return error but bit SLK can still clear to 0 means Wdg can unlock and Wdg is also not lock again
		Expected behavior:
		Swt_Ip_Unlock return error show the correct status of Wdg and Wdg can lock again
		Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)
		Proposed solution optional:
		Issue Wdg can not lock again
		!image-2021-08-20-09-42-21-628.png|thumbnail!
		Ip function will check Unlock first, with WdgOsifTimeoutVal: = 0 and current lock mode is Softlock, Swt_Ip_Unlock will return error and it can not go to the Swt_Ip_Lock

ID	Subtype	Headline and Description

ARTD-15539	Bug	[WDG] Swt_Ip_ClearResetRequest return error but RRR bit can still clear<*>
		
		Detailed description (how to reproduce it):
		Step1: Init with Slowmode WdgOsifTimeoutVal:=0,
		Also config MC_RGM to use feature SwtResetOnly
		Step2: Wait until Reset Request Flag (RRF) is set (can delay until timeout or use while until RRF is set)
		Step3: RRF bit is 1, Call ClearResetRequest function
		Step4: With current config WdgOsifTimeoutVal:=0, Swt_Ip_ClearResetRequest will return error at
		if(ElapsedTicks >= TimeoutTicks)
		{
		ret = SWT_IP_STATUS_TIMEOUT;
		}
		But after ClearResetRequest function, RRF bit is also can clear although Swt_Ip_ClearResetRequest return error
		Preconditions:
		[...]
		Test Case ID (internal TC that caught the defect) optional:
		[...]
		Observed behavior:
		Swt_Ip_ClearResetRequest return error but RRF bit can clear
		Expected behavior:
		Driver show the correct status
		Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)
		Proposed solution optional:
		[...]

ARTD-15545	Bug	[OCU] Registers of eMios master reset after call Ocu_Deintit function, not report error when config channel matches materbus channel config ,,"Detailed description (how to reproduce it): PVT_OCU_ARTD_12352_V01 in branch ARTD-12352-s32k3-rtm-ocu-the-master-bus-of-ocu-channel-will-be-wrongly-changed-to-mc-mode When config channel in EB, we choose eMios0_ch0 for materbus in Mcl and after choose it for Ocu channel config but EB not report error We called Mcl_Init function to config selected materbus, and call in test suite before come in test case, when come test case and call Ocu_Deinit function it reset all registers of materbus had config Test Case ID (internal TC that caught the defect) optional: OCU_TC_FCT_0041 in Ocu_TS_002 Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-15555	New	New Feature [FLS] Update code following to Rule 29 of Naming Convention ,,"NewWorkDescription: Update local variables, function parameters and struct members using only PascalCase naming, without any special prefix Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]"
ARTD-15554	Bug	[S32K3 RTM] UART: An internal Error occurred when add Flexio_Uart component in S32DS3.4<*> Detailed description (how to reproduce it): The problem found when adding Flexio_Uart in S32DS3.4 for S32K344 derivative. I saw that in Flexio component file the parameter pass into hasExclusiveOwnership function is LPUART !image-2021-08-20-14-59-50-324.png|thumbnail! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: An internal Error occurred when add Flexio_Uart component in S32DS3.4 !image-2021-08-20-14-56-12-258.png|thumbnail! Expected behavior: Flexio_Uart component can be added without error in S32DS3.4 Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A

ID	Subtype	Headline and Description
ARTD-15561	Bug	[S32K3XX][S32K3XX_100] IntCtrl_Ip_Init function should clear pending interrupt status before enabling any IRQ interrupt<*> Detailed description (how to reproduce it): Calling IntCtrl_Ip_Init function need clear pending before Enable IRQ interrupt. For example: By some way, Some pending are turned on after that User call IntCtrl_Ip_Init, and then it enable IRQ interrupt, because handler_interrupt not install yet, So Project will handfault, test not run. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Platform_TS_001 Observed behavior: Run over IntCtrl_Ip_Init function, some pending interrupt are set. It makes the pointer into undefine_handler Expected behavior: Clear pending Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: add Clear pending function !image-2021-08-23-15-07-03-363.png!
ARTD-15564	Bug	[LIN]Lin_GetStatus() returns incorrect status for S32K3XX<*> Detailed description (how to reproduce it): The device is master node. The device sent a frame on the bus. Use other device(CANoe) to disturb the stop bit of data byte to create a error frame. Call Lin_GetStatus() function to check status after have an error on the TX frame. Observed behavior: Lin_GetStatus() has return LIN_RX_ERROR. Expected behavior: Lin_GetStatus() has return LIN_TX_ERROR. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Define node state events where frame error interrupt can occur. In FrameError Irq handler, call GotoIdleState function, it will stop transfer and save current node state to previous note state variable. In GetStatus function, for each Node state, we return the appropriate status.

ID	Subtype	Headline and Description

ARTD-15565	Bug	[LIN] Lpuart_Lin_Ip_GetStatus returns the cause of the error incorrect when have frame error for K3XX<*>
		
		Detailed description (how to reproduce it):
		The device is master node.
		The device receive a frame on the bus.
		Use other device(CANoe) to disturb the stop bit of data byte to create a error frame(framing error).
		Call Lpuart_Lin_Ip_GetStatus() function to check status after have an error on the RX frame.
		Observed behavior:
		Lpuart_Lin_Ip_GetStatus() returns LPUART_LIN_IP_STATUS_RX_HEADER_ERROR
		Expected behavior:
		Lpuart_Lin_Ip_GetStatus() returns LPUART_LIN_IP_STATUS_RX_ERROR
		Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)
		Proposed solution optional:
		Please recheck the condition when check the cause of frame error:
		case LPUART_LIN_IP_FRAME_ERROR:
		/ Found cause of the error from header or reponse /
		if (LPUART_LIN_IP_NODE_STATE_RECV_DATA{color:#de350b} != LinCurrentState->PreviousNodeState)
		_{
		_RetStatus = LPUART_LIN_IP_STATUS_RX_ERROR;
		_}
		else
		{
		RetStatus = LPUART_LIN_IP_STATUS_RX_HEADER_ERROR;
		}

ARTD-15567	New	New Feature [OS] Add S32K312 to sdk_manifest_os.xml ,,"NewWorkDescription: Add S32K312 to sdk_manifest_os.xml Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: NA"

ID	Subtype	Headline and Description
ARTD-15578	New	New Feature [S32K3XX][PORT] Some functions in IP layer which do not appear on requirement should be reviewed and updated ,,"NewWorkDescription: The Exclusive Areas for K3 platform are incorrect. Some of them are redundant (need to be removed), and the rest need to be renamed. Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Remove/Add/Renaming the Exclusive Areas in code for K1. From IPW to IPL. All exclusives should be existed in IPL. The ones in IPW should be removed. #include SchM_Dio.h should be moved from IPW to IPL Update the UM/IM if needed Check and update RTE if needed"
ARTD-15597	Bug	[CAN] FlexCAN_ConfigTimestampModule should not have write access directly to DCMRWF1 causing impacting to other modules<*> Detailed description (how to reproduce it): as implemented in driver: !image-2021-08-23-12-15-12-607.png! this will overwrite other bits: !image-2021-08-23-12-15-36-020.png! Preconditions: Review code Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: FlexCAN_ConfigTimestampModule writes directly to DCMRWF1 Expected behavior: FlexCAN_ConfigTimestampModule will read modify write to DCMRWF1 Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: change to RMW instead of Write to DCMRWF1 register

ID	Subtype	Headline and Description
ARTD-15587	Bug	[MCU]have some error when build CT and EBT example mcu module<*> Detailed description (how to reproduce it): [have some error and warning when build all mcu example by platform and base module] Preconditions: PVT_DEM_S32K3_1.0.0_V01 PVT_DET_S32K3_1.0.0_V01 PVT_OS_S32K3_1.0.0_V01 PVT_BASE_S32K3_1.0.0_V17 PVT_S32K3XX_S32K3_ARTD_14610_V16 feature/ARTD-12393-s32k3-rtm-mcu-tresos-and-ds-examples Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: please check in all example. !image-2021-08-23-10-26-09-724.png! !image-2021-08-23-10-26-48-288.png! Expected behavior: not error for base,platform module when build mcu example Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-15596	Bug	[Mcl] Emios_Mcl_Ip_VS_0_PBcfg.h of EB generate missing macro<*> Detailed description (how to reproduce it): In the MCL module enable emios ip. In the file Emios_Mcl_Ip_VS_0_PBcfg.h of S32CT have generate macro MCL_EMIOS_LOGIC_CH0 but in the EB not generate this macro. I need this macro for test some function for mcl look like Mcl_Emios_SetReloadInterval, Mcl_Emios_SetCounterBusPeriod Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: MCT_TS_402 Observed behavior: In the EB not generate macro MCL_EMIOS_LOGIC_CH0 Expected behavior: The EB generate macro MCL_EMIOS_LOGIC_CH0 in Emios_Mcl_Ip_VS_0_PBcfg.h file look like CT Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-15602	New	New Feature [RM][S32K3XX] Disable AXBS for derivative S32K312 which is not supported ,,"NewWorkDescription: Disable AXBS for derivative S32K312 which is not supported Requirement source: NA Proposed solution optional: Disable, AXBS for derivative S32K312 which is not supported"
ARTD-15603	New	New Feature [RM][S32K3XX] Improve AXBS driver code ,,"NewWorkDescription: Update code for user mode support Recheck resource follow RM Requirement source: NA Proposed solution optional: update follow description"
ARTD-15606	New	New Feature [RM][S32K3XX] Add corresponding header files for S32K314, S32K324 derivatives" ,,"NewWorkDescription: Include header file for S32K314 and S32K324 derivative Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: K314 and K324 share the same header file with K344

ID	Subtype	Headline and Description

ARTD-15610	New	New Feature
		
		[FLS] All trusted functions should NOT defined as static or inline functions and should listed out in IM
		,,"NewWorkDescription:
		There are some points that need to be checked in each modules:
		1. All trusted functions should NOT defined as static or inline functions*, so OS Application can be able to call them from outside RTD drivers.
		Check in driver code all IP functions that needs to be called as trusted functions using macros OsIf_Trusted_Call[_Return][1-6params].
		Ensure these functions are defined without ""static"" or ""inline"" keywords, so OS Application can use ""extern"" keyword to declare and call them outside RTD drivers.
		For example:
		a. OsIf_Trusted_Call1param(*Adc_Sar_ClrUserAccessAllowed*, pBase);
		Adc_Sar_ClrUserAccessAllowed() function should be defined without ""static"" or ""inline"" as:
		void Adc_Sar_ClrUserAccessAllowed(const ADC_Type const pBase)
		{
		CLR_USER_ACCESS_ALLOWED((uint32)pBase, SAR_ADC_PROT_MEM_U32);
		}
		b. OsIf_Trusted_Call_Return1param(*C40_Ip_SetLockProtect*, Fls_VirtualSector);
		C40_Ip_SetLockProtect() function should be defined without ""static"" or ""inline"" as:
		C40_Ip_StatusType C40_Ip_SetLockProtect(C40_Ip_VirtualSectorsType Fls_VirtualSector)
		{
		}
		2. Create a new separate header file <IpName>_Ip_TrustedFunctions.h for each IPV has trusted functions, the AutosarOS just needs to include this new header file when using user mode is used.
		In <IpName>_Ip_TrustedFunctions.h:
		Declare all trusted functions with ""extern"" keyword like:
		extern void C40_Ip_SetLockProtect(C40_Ip_VirtualSectorsType Fls_VirtualSector);
		Include all header files contain the definition of all types which are used by parameters or return type of those trusted functions.
		3. All these trusted functions need to be configured in OS, so they must be clearly listed in the driver IM (chapter 5.7 User Mode Support)
		List these functions follow guiding mentioned in slide 17 Coding RTD_RunningInUserMode.pptx
		All functions should be listed out in the table like:
		Function syntax||Description||Available via
		void C40_Ip_SetLockProtect(
		C40_Ip_VirtualSectorsType Fls_VirtualSector
		)|Set lock bit for flash sectors|C40_Ip_TrustedFunctions.h
		4. Subchapter ""*User Mode configuration in AutosarOS*"" needs to be added in IM:
		!image-2021-08-19-09-26-20-823.png|thumbnail!
		In order to add this subchapter, there are 2 files added in build_env: user_mode_support.dox, user_mode_config_in_autosar_os.dox (added on the ticket ARTD-15466).
		In module repository, each module needs to rename from user_mode_support*.dox to user_mode_config_in_module*.dox and also its title from ""*User Mode support*"" to ""*User Mode configuration in the module*"".
		Please refer the silde [Coding RTD_RunningInUserMode.pptx|https://nxp1.sharepoint.com/:p:/r/sites/Zebra/Shared%20Documents/General/Zebra%20Training/Coding%20-%20RTD_RunningInUserMode.pptx?d=w21c9578fff794ff387db07a106880274&csf=1&web=1&e=lpbnNC] to understand more about User mode implementation in RTD.
		For Testing side*: Ensure that we have test scenarios mentioned from slides 22->25 Coding RTD_RunningInUserMode.pptx. Follow slide 23 to ensure we have one test suite to check all trusted functions able to call from outside RTD drivers.
		Requirement source:
		RTD implementation
		(e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...)
		Proposed solution optional:
		Follow Coding RTD_RunningInUserMode.pptx"

Release notes		

ID	Subtype	Headline and Description
ARTD-15609	New	New Feature [FLS] Reduce parameters of functions which violated HIS_PARAM checker for C40_Ip layer ,,"NewWorkDescription: Reduce parameters of functions which violated HIS_PARAM checker Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]"
ARTD-15659	Bug	[ICU][S32K3XX] The Standby mode for WKPU need supported in Wkpu_Ip_Init() function<*> Detailed description (how to reproduce it): The platform S32K3XX has WKPU HW available for standby feature. This feature is a requirement (CPR_RTD_00403.icu) as following: The Icu driver shall provide an optional configuration parameter to support wakeup IP operation across STANDBY. Per default this optional functionality and configuration parameters shall be disabled,. If the configuration parameter is enabled, the following shall be respected: The driver shall NOT CLEAR the interrupt flag or the interrupt enable bit, after a wakeup event. The driver shall make sure it will correctly service the wakeup event, if this event occurred before init. This is done to support the hardware functionality of IP's that may have flags set after the occurred wakeup event that leads to a memory clear." Preconditions: ICU_WKPU_STANDBY_WAKEUP_SUPPORT = STD_ON Test Case ID (internal TC that caught the defect) optional: Icu_TC_WBT_0040 Observed behavior: [...] Expected behavior: The driver WKPU shall NOT CLEAR the interrupt flag or the interrupt enable bit, after a wakeup event follow to the req CPR_RTD_00403.icu. Proposed solution optional: when mode standby for wkpu hardware is turned on in EB, In the function Wkpu_Ip_Init() need to check the condition ICU_WKPU_STANDBY_WAKEUP_SUPPORT to implement this feature.

ID	Subtype	Headline and Description
ARTD-15668	Bug	[ADC] Fix findings from code review checklist<*> Detailed description (how to reproduce it): Fix findings according to code checklist Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: NA Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-15669	Bug	[CAN] re-implement SWS_Can_00384<*> Detailed description (how to reproduce it): SWS_Can_00384|Each time the CAN controller state machine is triggered with the state transition value CAN_CS_STARTED, the function Can_SetControllerMode shall re-initialize the CAN controller with the same controller configuration set previously used by functions Can_SetBaudrate or Can_Init. but as implemented in the code. driver just switch from stopped state (disable mode) to started state(normal mode) => a re-init (reset all then init again) is necessary to reset buffers, fifo, bus-off,.. Test Case ID (internal TC that caught the defect) optional:__*Preconditions: NA Observed behavior: driver didn't re-init controller when started state required Expected behavior: driver does re-init controller when started state required Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: call FlexCan_Ip_Init at Ipw_SetcontrollertoStart and re-configure baudrate by Can_au16ControllerBaudRateSel and Can_Ipw_eClockMode which are saved at runtime

ID	Subtype	Headline and Description
ARTD-15693	New	New Feature [adc] Enable ECPD generation for IP components (CPR_RTD_00544) ,,"Note: This feature must be implemented by all the modules for which this ticket was cloned (including CDDs). No clone shall be closed with ""Not Applicable"" or ""No Action Taken"". How to implement: # Add ""options_expr"" tags (containing all the necessary options) for the fields of the IP component(s). Please refer to the slides covering ""EPD Generation"" in Reference #2 below. # To ensure that the ECPD is generated only for your component, modify line 512 in ""mcu_data/components/PlatformSDK_S32K3_2021_08/system/codegenerator.js"" as follows: {code:javascript} if (configComponent.isOptionSet(""ecucDefinitionCollection"") && (configComponent.getId() === ""Gmac"")) { where you can replace ""Gmac"" with the ID of your IP component. # Check that there are no errors reported in the Problems view and that the ECPD has been generated in Code Preview. How to validate: # Manually create an EBT plugin using the previously generated ECPD. To achieve this: ## Unzip https://jira.sw.nxp.com/secure/attachment/828304/Ip_TS_T40D34M10I0R0.zip in the ""output/eclipse/plugins"" folder of your K3 work tree / repository. ## Open ""Ip_TS_T40D34M10I0R0/plugin.xml"" and replace all occurrences of ""Gmac"" with the ID of your IP component. # Create an EBT project (File > New > Configuration Project > Project Name: TstIp > Next > ECU ID: someId; Target: CORTEXM/S32K3XX > Finish) and add the previously created module (Right click on TstIp in Project Explorer > Module Configurations... > Double click on your module > OK) CHECKPOINT 1: The module should have been successfully imported into the project. # Go to S32DS and create a valid project using your IP component (or use an already existing one). Please assign a value other than the default value to each setting to avoid default values in this configuration{color}*. Rename your IP component instance and discard the ""_1"" prefix (e.g. ""Gmac_1"" > ""Gmac""): {panel}!screenshot-1.png! # Generate the [LT/PB]Cfg.h/.c files of your IP component and save them somewhere to avoid overwriting them in a later step. We'll call this set of files OriginalGenerateFiles_. # Generate the ECVD file for your IP component instance (Global Settings > EcvdGenerationMethod = INDIVIDUAL > EcvdOutputPath = <EcvdOutputDir> > Click on the ""Generate Configuration"" button) # Import the previously generated ECVD file in your EBT project (Right click on TstIp in Project Explorer > Im and Exporters... > Green Button > Next > File Name: <Browse and select the ECVD file> > Next > Enable path mapping > Finish > Run Importer) CHECKPOINT 2: The ECVD file should have been successfully applied to your module. # Save (CTRL S) and generate the project (Right click on TstIp in Project Explorer > Generate Project) to trigger the EPC generation. CHECKPOINT 3: The EPC file should have been successfully generated (TstIp/output/output/<Ip>.epc) # Import the previously generated EPC file in your S32DS project (File > Import > Import ECU Configuration > Path: <EpcOutputDir> > Check ""Merge into current configuration"" > Check ""Check ECUC-MODULE-DEF"" value > CHECKPOINT 4: The EPC file should have been successfully imported into your S32DS project. If you get the error ""The required modules are not available for the current configuration"", it means that the ECUC-MODULE-DEF check has failed and you're not properly using M4_XDM_AR_PKG_NAME in your IP component. # Generate again the [LT/PB]Cfg.h/.c files of your IP component and save them somewhere without overwriting the previous set of files. We'll call this new set of files ImportedGenerateFiles_. # Compare the OriginalGenerateFiles set with the ImportedGenerateFiles set. CHECKPOINT 5: The comparison should be binary identical. There should be no
Release notes		

ID	Subtype	Headline and Description
ARTD-15699	New	New Feature [eth] Enable ECPD generation for IP components (CPR_RTD_00544) ,,"Note: This feature must be implemented by all the modules for which this ticket was cloned (including CDDs). No clone shall be closed with ""Not Applicable"" or ""No Action Taken"". How to implement: # Add ""options_expr"" tags (containing all the necessary options) for the fields of the IP component(s). Please refer to the slides covering ""EPD Generation"" in Reference #2 below. # To ensure that the ECPD is generated only for your component, modify line 512 in ""mcu_data/components/PlatformSDK_S32K3_2021_08/system/codegenerator.js"" as follows: {code:javascript} if (configComponent.isOptionSet(""ecucDefinitionCollection"") && (configComponent.getId() === ""Gmac"")) { where you can replace ""Gmac"" with the ID of your IP component. # Check that there are no errors reported in the Problems view and that the ECPD has been generated in Code Preview. How to validate: # Manually create an EBT plugin using the previously generated ECPD. To achieve this: ## Unzip https://jira.sw.nxp.com/secure/attachment/828304/Ip_TS_T40D34M10I0R0.zip in the ""output/eclipse/plugins"" folder of your K3 work tree / repository. ## Open ""Ip_TS_T40D34M10I0R0/plugin.xml"" and replace all occurrences of ""Gmac"" with the ID of your IP component. # Create an EBT project (File > New > Configuration Project > Project Name: TstIp > Next > ECU ID: someId; Target: CORTEXM/S32K3XX > Finish) and add the previously created module (Right click on TstIp in Project Explorer > Module Configurations... > Double click on your module > OK) CHECKPOINT 1: The module should have been successfully imported into the project. # Go to S32DS and create a valid project using your IP component (or use an already existing one). Please assign a value other than the default value to each setting to avoid default values in this configuration{color}*. Rename your IP component instance and discard the ""_1"" prefix (e.g. ""Gmac_1"" > ""Gmac""): {panel}!screenshot-1.png! # Generate the [LT/PB]Cfg.h/.c files of your IP component and save them somewhere to avoid overwriting them in a later step. We'll call this set of files OriginalGenerateFiles_. # Generate the ECVD file for your IP component instance (Global Settings > EcvdGenerationMethod = INDIVIDUAL > EcvdOutputPath = <EcvdOutputDir> > Click on the ""Generate Configuration"" button) # Import the previously generated ECVD file in your EBT project (Right click on TstIp in Project Explorer > Im and Exporters... > Green Button > Next > File Name: <Browse and select the ECVD file> > Next > Enable path mapping > Finish > Run Importer) CHECKPOINT 2: The ECVD file should have been successfully applied to your module. # Save (CTRL S) and generate the project (Right click on TstIp in Project Explorer > Generate Project) to trigger the EPC generation. CHECKPOINT 3: The EPC file should have been successfully generated (TstIp/output/output/<Ip>.epc) # Import the previously generated EPC file in your S32DS project (File > Import > Import ECU Configuration > Path: <EpcOutputDir> > Check ""Merge into current configuration"" > Check ""Check ECUC-MODULE-DEF"" value > CHECKPOINT 4: The EPC file should have been successfully imported into your S32DS project. If you get the error ""The required modules are not available for the current configuration"", it means that the ECUC-MODULE-DEF check has failed and you're not properly using M4_XDM_AR_PKG_NAME in your IP component. # Generate again the [LT/PB]Cfg.h/.c files of your IP component and save them somewhere without overwriting the previous set of files. We'll call this new set of files ImportedGenerateFiles_. # Compare the OriginalGenerateFiles set with the ImportedGenerateFiles set.
Release notes		

ID	Subtype	Headline and Description
ARTD-15700	New	New Feature [fls] Enable ECPD generation for IP components (CPR_RTD_00544) ,,"Note: This feature must be implemented by all the modules for which this ticket was cloned (including CDDs). No clone shall be closed with ""Not Applicable"" or ""No Action Taken"". How to implement: # Add ""options_expr"" tags (containing all the necessary options) for the fields of the IP component(s). Please refer to the slides covering ""EPD Generation"" in Reference #2 below. # To ensure that the ECPD is generated only for your component, modify line 512 in ""mcu_data/components/PlatformSDK_S32K3_2021_08/system/codegenerator.js"" as follows: {code:javascript} if (configComponent.isOptionSet(""ecucDefinitionCollection"") && (configComponent.getId() === ""Gmac"")) { where you can replace ""Gmac"" with the ID of your IP component. # Check that there are no errors reported in the Problems view and that the ECPD has been generated in Code Preview. How to validate: # Manually create an EBT plugin using the previously generated ECPD. To achieve this: ## Unzip https://jira.sw.nxp.com/secure/attachment/828304/Ip_TS_T40D34M10I0R0.zip in the ""output/eclipse/plugins"" folder of your K3 work tree / repository. ## Open ""Ip_TS_T40D34M10I0R0/plugin.xml"" and replace all occurrences of ""Gmac"" with the ID of your IP component. # Create an EBT project (File > New > Configuration Project > Project Name: TstIp > Next > ECU ID: someId; Target: CORTEXM/S32K3XX > Finish) and add the previously created module (Right click on TstIp in Project Explorer > Module Configurations... > Double click on your module > OK) CHECKPOINT 1: The module should have been successfully imported into the project. # Go to S32DS and create a valid project using your IP component (or use an already existing one). Please assign a value other than the default value to each setting to avoid default values in this configuration{color}*. Rename your IP component instance and discard the ""_1"" prefix (e.g. ""Gmac_1"" > ""Gmac""): {panel}!screenshot-1.png! # Generate the [LT/PB]Cfg.h/.c files of your IP component and save them somewhere to avoid overwriting them in a later step. We'll call this set of files OriginalGenerateFiles_. # Generate the ECVD file for your IP component instance (Global Settings > EcvdGenerationMethod = INDIVIDUAL > EcvdOutputPath = <EcvdOutputDir> > Click on the ""Generate Configuration"" button) # Import the previously generated ECVD file in your EBT project (Right click on TstIp in Project Explorer > Im and Exporters... > Green Button > Next > File Name: <Browse and select the ECVD file> > Next > Enable path mapping > Finish > Run Importer) CHECKPOINT 2: The ECVD file should have been successfully applied to your module. # Save (CTRL S) and generate the project (Right click on TstIp in Project Explorer > Generate Project) to trigger the EPC generation. CHECKPOINT 3: The EPC file should have been successfully generated (TstIp/output/output/<Ip>.epc) # Import the previously generated EPC file in your S32DS project (File > Import > Import ECU Configuration > Path: <EpcOutputDir> > Check ""Merge into current configuration"" > Check ""Check ECUC-MODULE-DEF"" value > CHECKPOINT 4: The EPC file should have been successfully imported into your S32DS project. If you get the error ""The required modules are not available for the current configuration"", it means that the ECUC-MODULE-DEF check has failed and you're not properly using M4_XDM_AR_PKG_NAME in your IP component. # Generate again the [LT/PB]Cfg.h/.c files of your IP component and save them somewhere without overwriting the previous set of files. We'll call this new set of files ImportedGenerateFiles_. # Compare the OriginalGenerateFiles set with the ImportedGenerateFiles set.
Release notes		

ID	Subtype	Headline and Description
ARTD-15703	New	New Feature [i2c] Enable ECPD generation for IP components (CPR_RTD_00544) ,,"Note: This feature must be implemented by all the modules for which this ticket was cloned (including CDDs). No clone shall be closed with ""Not Applicable"" or ""No Action Taken"". How to implement: # Add ""options_expr"" tags (containing all the necessary options) for the fields of the IP component(s). Please refer to the slides covering ""EPD Generation"" in Reference #2 below. # To ensure that the ECPD is generated only for your component, modify line 512 in ""mcu_data/components/PlatformSDK_S32K3_2021_08/system/codegenerator.js"" as follows: {code:javascript} if (configComponent.isOptionSet(""ecucDefinitionCollection"") && (configComponent.getId() === ""Gmac"")) { where you can replace ""Gmac"" with the ID of your IP component. # Check that there are no errors reported in the Problems view and that the ECPD has been generated in Code Preview. How to validate: # Manually create an EBT plugin using the previously generated ECPD. To achieve this: ## Unzip https://jira.sw.nxp.com/secure/attachment/828304/Ip_TS_T40D34M10I0R0.zip in the ""output/eclipse/plugins"" folder of your K3 work tree / repository. ## Open ""Ip_TS_T40D34M10I0R0/plugin.xml"" and replace all occurrences of ""Gmac"" with the ID of your IP component. # Create an EBT project (File > New > Configuration Project > Project Name: TstIp > Next > ECU ID: someId; Target: CORTEXM/S32K3XX > Finish) and add the previously created module (Right click on TstIp in Project Explorer > Module Configurations... > Double click on your module > OK) CHECKPOINT 1: The module should have been successfully imported into the project. # Go to S32DS and create a valid project using your IP component (or use an already existing one). Please assign a value other than the default value to each setting to avoid default values in this configuration{color}*. Rename your IP component instance and discard the ""_1"" prefix (e.g. ""Gmac_1"" > ""Gmac""): {panel}!screenshot-1.png! # Generate the [LT/PB]Cfg.h/.c files of your IP component and save them somewhere to avoid overwriting them in a later step. We'll call this set of files OriginalGenerateFiles_. # Generate the ECVD file for your IP component instance (Global Settings > EcvdGenerationMethod = INDIVIDUAL > EcvdOutputPath = <EcvdOutputDir> > Click on the ""Generate Configuration"" button) # Import the previously generated ECVD file in your EBT project (Right click on TstIp in Project Explorer > Im and Exporters... > Green Button > Next > File Name: <Browse and select the ECVD file> > Next > Enable path mapping > Finish > Run Importer) CHECKPOINT 2: The ECVD file should have been successfully applied to your module. # Save (CTRL S) and generate the project (Right click on TstIp in Project Explorer > Generate Project) to trigger the EPC generation. CHECKPOINT 3: The EPC file should have been successfully generated (TstIp/output/output/<Ip>.epc) # Import the previously generated EPC file in your S32DS project (File > Import > Import ECU Configuration > Path: <EpcOutputDir> > Check ""Merge into current configuration"" > Check ""Check ECUC-MODULE-DEF"" value > CHECKPOINT 4: The EPC file should have been successfully imported into your S32DS project. If you get the error ""The required modules are not available for the current configuration"", it means that the ECUC-MODULE-DEF check has failed and you're not properly using M4_XDM_AR_PKG_NAME in your IP component. # Generate again the [LT/PB]Cfg.h/.c files of your IP component and save them somewhere without overwriting the previous set of files. We'll call this new set of files ImportedGenerateFiles_. # Compare the OriginalGenerateFiles set with the ImportedGenerateFiles set. CHECKPOINT 5: The comparison should be binary identical. There should be no
Release notes		

ID	Subtype	Headline and Description
ARTD-15709	New	New Feature [ocu] Enable ECPD generation for IP components (CPR_RTD_00544) ,,"Note: This feature must be implemented by all the modules for which this ticket was cloned (including CDDs). No clone shall be closed with ""Not Applicable"" or ""No Action Taken"". How to implement: # Add ""options_expr"" tags (containing all the necessary options) for the fields of the IP component(s). Please refer to the slides covering ""EPD Generation"" in Reference #2 below. # To ensure that the ECPD is generated only for your component, modify line 512 in ""mcu_data/components/PlatformSDK_S32K3_2021_08/system/codegenerator.js"" as follows: {code:javascript} if (configComponent.isOptionSet(""ecucDefinitionCollection"") && (configComponent.getId() === ""Gmac"")) { where you can replace ""Gmac"" with the ID of your IP component. # Check that there are no errors reported in the Problems view and that the ECPD has been generated in Code Preview. How to validate: # Manually create an EBT plugin using the previously generated ECPD. To achieve this: ## Unzip https://jira.sw.nxp.com/secure/attachment/828304/Ip_TS_T40D34M10I0R0.zip in the ""output/eclipse/plugins"" folder of your K3 work tree / repository. ## Open ""Ip_TS_T40D34M10I0R0/plugin.xml"" and replace all occurrences of ""Gmac"" with the ID of your IP component. # Create an EBT project (File > New > Configuration Project > Project Name: TstIp > Next > ECU ID: someId; Target: CORTEXM/S32K3XX > Finish) and add the previously created module (Right click on TstIp in Project Explorer > Module Configurations... > Double click on your module > OK) CHECKPOINT 1: The module should have been successfully imported into the project. # Go to S32DS and create a valid project using your IP component (or use an already existing one). Please assign a value other than the default value to each setting to avoid default values in this configuration{color}*. Rename your IP component instance and discard the ""_1"" prefix (e.g. ""Gmac_1"" > ""Gmac""): {panel}!screenshot-1.png! # Generate the [LT/PB]Cfg.h/.c files of your IP component and save them somewhere to avoid overwriting them in a later step. We'll call this set of files OriginalGenerateFiles_. # Generate the ECVD file for your IP component instance (Global Settings > EcvdGenerationMethod = INDIVIDUAL > EcvdOutputPath = <EcvdOutputDir> > Click on the ""Generate Configuration"" button) # Import the previously generated ECVD file in your EBT project (Right click on TstIp in Project Explorer > Im and Exporters... > Green Button > Next > File Name: <Browse and select the ECVD file> > Next > Enable path mapping > Finish > Run Importer) CHECKPOINT 2: The ECVD file should have been successfully applied to your module. # Save (CTRL S) and generate the project (Right click on TstIp in Project Explorer > Generate Project) to trigger the EPC generation. CHECKPOINT 3: The EPC file should have been successfully generated (TstIp/output/output/<Ip>.epc) # Import the previously generated EPC file in your S32DS project (File > Import > Import ECU Configuration > Path: <EpcOutputDir> > Check ""Merge into current configuration"" > Check ""Check ECUC-MODULE-DEF"" value > CHECKPOINT 4: The EPC file should have been successfully imported into your S32DS project. If you get the error ""The required modules are not available for the current configuration"", it means that the ECUC-MODULE-DEF check has failed and you're not properly using M4_XDM_AR_PKG_NAME in your IP component. # Generate again the [LT/PB]Cfg.h/.c files of your IP component and save them somewhere without overwriting the previous set of files. We'll call this new set of files ImportedGenerateFiles_. # Compare the OriginalGenerateFiles set with the ImportedGenerateFiles set. CHECKPOINT 5: The comparison should be binary identical. There should be no
Release notes		

ID	Subtype	Headline and Description
ARTD-15711	New	New Feature [platform] Enable ECPD generation for IP components (CPR_RTD_00544) ,,"Note: This feature must be implemented by all the modules for which this ticket was cloned (including CDDs). No clone shall be closed with ""Not Applicable"" or ""No Action Taken"". How to implement: # Add ""options_expr"" tags (containing all the necessary options) for the fields of the IP component(s). Please refer to the slides covering ""EPD Generation"" in Reference #2 below. # To ensure that the ECPD is generated only for your component, modify line 512 in ""mcu_data/components/PlatformSDK_S32K3_2021_08/system/codegenerator.js"" as follows: {code:javascript} if (configComponent.isOptionSet(""ecucDefinitionCollection"") && (configComponent.getId() === ""Gmac"")) { where you can replace ""Gmac"" with the ID of your IP component. # Check that there are no errors reported in the Problems view and that the ECPD has been generated in Code Preview. How to validate: # Manually create an EBT plugin using the previously generated ECPD. To achieve this: ## Unzip https://jira.sw.nxp.com/secure/attachment/828304/Ip_TS_T40D34M10I0R0.zip in the ""output/eclipse/plugins"" folder of your K3 work tree / repository. ## Open ""Ip_TS_T40D34M10I0R0/plugin.xml"" and replace all occurrences of ""Gmac"" with the ID of your IP component. # Create an EBT project (File > New > Configuration Project > Project Name: TstIp > Next > ECU ID: someId; Target: CORTEXM/S32K3XX > Finish) and add the previously created module (Right click on TstIp in Project Explorer > Module Configurations... > Double click on your module > OK) CHECKPOINT 1: The module should have been successfully imported into the project. # Go to S32DS and create a valid project using your IP component (or use an already existing one). Please assign a value other than the default value to each setting to avoid default values in this configuration{color}*. Rename your IP component instance and discard the ""_1"" prefix (e.g. ""Gmac_1"" > ""Gmac""): {panel}!screenshot-1.png! # Generate the [LT/PB]Cfg.h/.c files of your IP component and save them somewhere to avoid overwriting them in a later step. We'll call this set of files OriginalGenerateFiles_. # Generate the ECVD file for your IP component instance (Global Settings > EcvdGenerationMethod = INDIVIDUAL > EcvdOutputPath = <EcvdOutputDir> > Click on the ""Generate Configuration"" button) # Import the previously generated ECVD file in your EBT project (Right click on TstIp in Project Explorer > Im and Exporters... > Green Button > Next > File Name: <Browse and select the ECVD file> > Next > Enable path mapping > Finish > Run Importer) CHECKPOINT 2: The ECVD file should have been successfully applied to your module. # Save (CTRL S) and generate the project (Right click on TstIp in Project Explorer > Generate Project) to trigger the EPC generation. CHECKPOINT 3: The EPC file should have been successfully generated (TstIp/output/output/<Ip>.epc) # Import the previously generated EPC file in your S32DS project (File > Import > Import ECU Configuration > Path: <EpcOutputDir> > Check ""Merge into current configuration"" > Check ""Check ECUC-MODULE-DEF"" value > CHECKPOINT 4: The EPC file should have been successfully imported into your S32DS project. If you get the error ""The required modules are not available for the current configuration"", it means that the ECUC-MODULE-DEF check has failed and you're not properly using M4_XDM_AR_PKG_NAME in your IP component. # Generate again the [LT/PB]Cfg.h/.c files of your IP component and save them somewhere without overwriting the previous set of files. We'll call this new set of files ImportedGenerateFiles_. # Compare the OriginalGenerateFiles set with the ImportedGenerateFiles set.
Release notes		

ID	Subtype	Headline and Description
ARTD-15715	New	New Feature [rm] Enable ECPD generation for IP components (CPR_RTD_00544) ,,"Note: This feature must be implemented by all the modules for which this ticket was cloned (including CDDs). No clone shall be closed with ""Not Applicable"" or ""No Action Taken"". How to implement: # Add ""options_expr"" tags (containing all the necessary options) for the fields of the IP component(s). Please refer to the slides covering ""EPD Generation"" in Reference #2 below. # To ensure that the ECPD is generated only for your component, modify line 512 in ""mcu_data/components/PlatformSDK_S32K3_2021_08/system/codegenerator.js"" as follows: {code:javascript} if (configComponent.isOptionSet(""ecucDefinitionCollection"") && (configComponent.getId() === ""Gmac"")) { where you can replace ""Gmac"" with the ID of your IP component. # Check that there are no errors reported in the Problems view and that the ECPD has been generated in Code Preview. How to validate: # Manually create an EBT plugin using the previously generated ECPD. To achieve this: ## Unzip https://jira.sw.nxp.com/secure/attachment/828304/Ip_TS_T40D34M10I0R0.zip in the ""output/eclipse/plugins"" folder of your K3 work tree / repository. ## Open ""Ip_TS_T40D34M10I0R0/plugin.xml"" and replace all occurrences of ""Gmac"" with the ID of your IP component. # Create an EBT project (File > New > Configuration Project > Project Name: TstIp > Next > ECU ID: someId; Target: CORTEXM/S32K3XX > Finish) and add the previously created module (Right click on TstIp in Project Explorer > Module Configurations... > Double click on your module > OK) CHECKPOINT 1: The module should have been successfully imported into the project. # Go to S32DS and create a valid project using your IP component (or use an already existing one). Please assign a value other than the default value to each setting to avoid default values in this configuration{color}*. Rename your IP component instance and discard the ""_1"" prefix (e.g. ""Gmac_1"" > ""Gmac""): {panel}!screenshot-1.png! # Generate the [LT/PB]Cfg.h/.c files of your IP component and save them somewhere to avoid overwriting them in a later step. We'll call this set of files OriginalGenerateFiles_. # Generate the ECVD file for your IP component instance (Global Settings > EcvdGenerationMethod = INDIVIDUAL > EcvdOutputPath = <EcvdOutputDir> > Click on the ""Generate Configuration"" button) # Import the previously generated ECVD file in your EBT project (Right click on TstIp in Project Explorer > Im and Exporters... > Green Button > Next > File Name: <Browse and select the ECVD file> > Next > Enable path mapping > Finish > Run Importer) CHECKPOINT 2: The ECVD file should have been successfully applied to your module. # Save (CTRL S) and generate the project (Right click on TstIp in Project Explorer > Generate Project) to trigger the EPC generation. CHECKPOINT 3: The EPC file should have been successfully generated (TstIp/output/output/<Ip>.epc) # Import the previously generated EPC file in your S32DS project (File > Import > Import ECU Configuration > Path: <EpcOutputDir> > Check ""Merge into current configuration"" > Check ""Check ECUC-MODULE-DEF"" value > CHECKPOINT 4: The EPC file should have been successfully imported into your S32DS project. If you get the error ""The required modules are not available for the current configuration"", it means that the ECUC-MODULE-DEF check has failed and you're not properly using M4_XDM_AR_PKG_NAME in your IP component. # Generate again the [LT/PB]Cfg.h/.c files of your IP component and save them somewhere without overwriting the previous set of files. We'll call this new set of files ImportedGenerateFiles_. # Compare the OriginalGenerateFiles set with the ImportedGenerateFiles set. CHECKPOINT 5: The comparison should be binary identical. There should be no
Release notes		

ID	Subtype	Headline and Description
ARTD-15716	New	New Feature [sai] Enable ECPD generation for IP components (CPR_RTD_00544) ,,"Note: This feature must be implemented by all the modules for which this ticket was cloned (including CDDs). No clone shall be closed with ""Not Applicable"" or ""No Action Taken"". How to implement: # Add ""options_expr"" tags (containing all the necessary options) for the fields of the IP component(s). Please refer to the slides covering ""EPD Generation"" in Reference #2 below. # To ensure that the ECPD is generated only for your component, modify line 512 in ""mcu_data/components/PlatformSDK_S32K3_2021_08/system/codegenerator.js"" as follows: {code:javascript} if (configComponent.isOptionSet(""ecucDefinitionCollection"") && (configComponent.getId() === ""Gmac"")) { where you can replace ""Gmac"" with the ID of your IP component. # Check that there are no errors reported in the Problems view and that the ECPD has been generated in Code Preview. How to validate: # Manually create an EBT plugin using the previously generated ECPD. To achieve this: ## Unzip https://jira.sw.nxp.com/secure/attachment/828304/Ip_TS_T40D34M10I0R0.zip in the ""output/eclipse/plugins"" folder of your K3 work tree / repository. ## Open ""Ip_TS_T40D34M10I0R0/plugin.xml"" and replace all occurrences of ""Gmac"" with the ID of your IP component. # Create an EBT project (File > New > Configuration Project > Project Name: TstIp > Next > ECU ID: someId; Target: CORTEXM/S32K3XX > Finish) and add the previously created module (Right click on TstIp in Project Explorer > Module Configurations... > Double click on your module > OK) CHECKPOINT 1: The module should have been successfully imported into the project. # Go to S32DS and create a valid project using your IP component (or use an already existing one). Please assign a value other than the default value to each setting to avoid default values in this configuration{color}*. Rename your IP component instance and discard the ""_1"" prefix (e.g. ""Gmac_1"" > ""Gmac""): {panel}!screenshot-1.png! # Generate the [LT/PB]Cfg.h/.c files of your IP component and save them somewhere to avoid overwriting them in a later step. We'll call this set of files OriginalGenerateFiles_. # Generate the ECVD file for your IP component instance (Global Settings > EcvdGenerationMethod = INDIVIDUAL > EcvdOutputPath = <EcvdOutputDir> > Click on the ""Generate Configuration"" button) # Import the previously generated ECVD file in your EBT project (Right click on TstIp in Project Explorer > Im and Exporters... > Green Button > Next > File Name: <Browse and select the ECVD file> > Next > Enable path mapping > Finish > Run Importer) CHECKPOINT 2: The ECVD file should have been successfully applied to your module. # Save (CTRL S) and generate the project (Right click on TstIp in Project Explorer > Generate Project) to trigger the EPC generation. CHECKPOINT 3: The EPC file should have been successfully generated (TstIp/output/output/<Ip>.epc) # Import the previously generated EPC file in your S32DS project (File > Import > Import ECU Configuration > Path: <EpcOutputDir> > Check ""Merge into current configuration"" > Check ""Check ECUC-MODULE-DEF"" value > CHECKPOINT 4: The EPC file should have been successfully imported into your S32DS project. If you get the error ""The required modules are not available for the current configuration"", it means that the ECUC-MODULE-DEF check has failed and you're not properly using M4_XDM_AR_PKG_NAME in your IP component. # Generate again the [LT/PB]Cfg.h/.c files of your IP component and save them somewhere without overwriting the previous set of files. We'll call this new set of files ImportedGenerateFiles_. # Compare the OriginalGenerateFiles set with the ImportedGenerateFiles set. CHECKPOINT 5: The comparison should be binary identical. There should be no
Release notes		

ID	Subtype	Headline and Description
ARTD-15717	New	New Feature [sent] Enable ECPD generation for IP components (CPR_RTD_00544) ,,"Note: This feature must be implemented by all the modules for which this ticket was cloned (including CDDs). No clone shall be closed with ""Not Applicable"" or ""No Action Taken"". How to implement: # Add ""options_expr"" tags (containing all the necessary options) for the fields of the IP component(s). Please refer to the slides covering ""EPD Generation"" in Reference #2 below. # To ensure that the ECPD is generated only for your component, modify line 512 in ""mcu_data/components/PlatformSDK_S32K3_2021_08/system/codegenerator.js"" as follows: {code:javascript} if (configComponent.isOptionSet(""ecucDefinitionCollection"") && (configComponent.getId() === ""Gmac"")) { where you can replace ""Gmac"" with the ID of your IP component. # Check that there are no errors reported in the Problems view and that the ECPD has been generated in Code Preview. How to validate: # Manually create an EBT plugin using the previously generated ECPD. To achieve this: ## Unzip https://jira.sw.nxp.com/secure/attachment/828304/Ip_TS_T40D34M10I0R0.zip in the ""output/eclipse/plugins"" folder of your K3 work tree / repository. ## Open ""Ip_TS_T40D34M10I0R0/plugin.xml"" and replace all occurrences of ""Gmac"" with the ID of your IP component. # Create an EBT project (File > New > Configuration Project > Project Name: TstIp > Next > ECU ID: someId; Target: CORTEXM/S32K3XX > Finish) and add the previously created module (Right click on TstIp in Project Explorer > Module Configurations... > Double click on your module > OK) CHECKPOINT 1: The module should have been successfully imported into the project. # Go to S32DS and create a valid project using your IP component (or use an already existing one). Please assign a value other than the default value to each setting to avoid default values in this configuration{color}*. Rename your IP component instance and discard the ""_1"" prefix (e.g. ""Gmac_1"" > ""Gmac""): {panel}!screenshot-1.png! # Generate the [LT/PB]Cfg.h/.c files of your IP component and save them somewhere to avoid overwriting them in a later step. We'll call this set of files OriginalGenerateFiles_. # Generate the ECVD file for your IP component instance (Global Settings > EcvdGenerationMethod = INDIVIDUAL > EcvdOutputPath = <EcvdOutputDir> > Click on the ""Generate Configuration"" button) # Import the previously generated ECVD file in your EBT project (Right click on TstIp in Project Explorer > Im and Exporters... > Green Button > Next > File Name: <Browse and select the ECVD file> > Next > Enable path mapping > Finish > Run Importer) CHECKPOINT 2: The ECVD file should have been successfully applied to your module. # Save (CTRL S) and generate the project (Right click on TstIp in Project Explorer > Generate Project) to trigger the EPC generation. CHECKPOINT 3: The EPC file should have been successfully generated (TstIp/output/output/<Ip>.epc) # Import the previously generated EPC file in your S32DS project (File > Import > Import ECU Configuration > Path: <EpcOutputDir> > Check ""Merge into current configuration"" > Check ""Check ECUC-MODULE-DEF"" value > CHECKPOINT 4: The EPC file should have been successfully imported into your S32DS project. If you get the error ""The required modules are not available for the current configuration"", it means that the ECUC-MODULE-DEF check has failed and you're not properly using M4_XDM_AR_PKG_NAME in your IP component. # Generate again the [LT/PB]Cfg.h/.c files of your IP component and save them somewhere without overwriting the previous set of files. We'll call this new set of files ImportedGenerateFiles_. # Compare the OriginalGenerateFiles set with the ImportedGenerateFiles set. CHECKPOINT 5: The comparison should be binary identical. There should be no
Release notes		

ID	Subtype	Headline and Description
ARTD-15718	New	New Feature [spi] Enable ECPD generation for IP components (CPR_RTD_00544) ,,"Note: This feature must be implemented by all the modules for which this ticket was cloned (including CDDs). No clone shall be closed with ""Not Applicable"" or ""No Action Taken"". How to implement: # Add ""options_expr"" tags (containing all the necessary options) for the fields of the IP component(s). Please refer to the slides covering ""EPD Generation"" in Reference #2 below. # To ensure that the ECPD is generated only for your component, modify line 512 in ""mcu_data/components/PlatformSDK_S32K3_2021_08/system/codegenerator.js"" as follows: {code:javascript} if (configComponent.isOptionSet(""ecucDefinitionCollection"") && (configComponent.getId() === ""Gmac"")) { where you can replace ""Gmac"" with the ID of your IP component. # Check that there are no errors reported in the Problems view and that the ECPD has been generated in Code Preview. How to validate: # Manually create an EBT plugin using the previously generated ECPD. To achieve this: ## Unzip https://jira.sw.nxp.com/secure/attachment/828304/Ip_TS_T40D34M10I0R0.zip in the ""output/eclipse/plugins"" folder of your K3 work tree / repository. ## Open ""Ip_TS_T40D34M10I0R0/plugin.xml"" and replace all occurrences of ""Gmac"" with the ID of your IP component. # Create an EBT project (File > New > Configuration Project > Project Name: TstIp > Next > ECU ID: someId; Target: CORTEXM/S32K3XX > Finish) and add the previously created module (Right click on TstIp in Project Explorer > Module Configurations... > Double click on your module > OK) CHECKPOINT 1: The module should have been successfully imported into the project. # Go to S32DS and create a valid project using your IP component (or use an already existing one). Please assign a value other than the default value to each setting to avoid default values in this configuration{color}*. Rename your IP component instance and discard the ""_1"" prefix (e.g. ""Gmac_1"" > ""Gmac""): {panel}!screenshot-1.png! # Generate the [LT/PB]Cfg.h/.c files of your IP component and save them somewhere to avoid overwriting them in a later step. We'll call this set of files OriginalGenerateFiles_. # Generate the ECVD file for your IP component instance (Global Settings > EcvdGenerationMethod = INDIVIDUAL > EcvdOutputPath = <EcvdOutputDir> > Click on the ""Generate Configuration"" button) # Import the previously generated ECVD file in your EBT project (Right click on TstIp in Project Explorer > Im and Exporters... > Green Button > Next > File Name: <Browse and select the ECVD file> > Next > Enable path mapping > Finish > Run Importer) CHECKPOINT 2: The ECVD file should have been successfully applied to your module. # Save (CTRL S) and generate the project (Right click on TstIp in Project Explorer > Generate Project) to trigger the EPC generation. CHECKPOINT 3: The EPC file should have been successfully generated (TstIp/output/output/<Ip>.epc) # Import the previously generated EPC file in your S32DS project (File > Import > Import ECU Configuration > Path: <EpcOutputDir> > Check ""Merge into current configuration"" > Check ""Check ECUC-MODULE-DEF"" value > CHECKPOINT 4: The EPC file should have been successfully imported into your S32DS project. If you get the error ""The required modules are not available for the current configuration"", it means that the ECUC-MODULE-DEF check has failed and you're not properly using M4_XDM_AR_PKG_NAME in your IP component. # Generate again the [LT/PB]Cfg.h/.c files of your IP component and save them somewhere without overwriting the previous set of files. We'll call this new set of files ImportedGenerateFiles_. # Compare the OriginalGenerateFiles set with the ImportedGenerateFiles set. CHECKPOINT 5: The comparison should be binary identical. There should be no
Release notes		

ID	Subtype	Headline and Description
ARTD-15720	New	New Feature [uart] Enable ECPD generation for IP components (CPR_RTD_00544) ,,"Note: This feature must be implemented by all the modules for which this ticket was cloned (including CDDs). No clone shall be closed with ""Not Applicable"" or ""No Action Taken"". How to implement: # Add ""options_expr"" tags (containing all the necessary options) for the fields of the IP component(s). Please refer to the slides covering ""EPD Generation"" in Reference #2 below. # To ensure that the ECPD is generated only for your component, modify line 512 in ""mcu_data/components/PlatformSDK_S32K3_2021_08/system/codegenerator.js"" as follows: {code:javascript} if (configComponent.isOptionSet(""ecucDefinitionCollection"") && (configComponent.getId() === ""Gmac"")) { where you can replace ""Gmac"" with the ID of your IP component. # Check that there are no errors reported in the Problems view and that the ECPD has been generated in Code Preview. How to validate: # Manually create an EBT plugin using the previously generated ECPD. To achieve this: ## Unzip https://jira.sw.nxp.com/secure/attachment/828304/Ip_TS_T40D34M10I0R0.zip in the ""output/eclipse/plugins"" folder of your K3 work tree / repository. ## Open ""Ip_TS_T40D34M10I0R0/plugin.xml"" and replace all occurrences of ""Gmac"" with the ID of your IP component. # Create an EBT project (File > New > Configuration Project > Project Name: TstIp > Next > ECU ID: someId; Target: CORTEXM/S32K3XX > Finish) and add the previously created module (Right click on TstIp in Project Explorer > Module Configurations... > Double click on your module > OK) CHECKPOINT 1: The module should have been successfully imported into the project. # Go to S32DS and create a valid project using your IP component (or use an already existing one). Please assign a value other than the default value to each setting to avoid default values in this configuration{color}*. Rename your IP component instance and discard the ""_1"" prefix (e.g. ""Gmac_1"" > ""Gmac""): {panel}!screenshot-1.png! # Generate the [LT/PB]Cfg.h/.c files of your IP component and save them somewhere to avoid overwriting them in a later step. We'll call this set of files OriginalGenerateFiles_. # Generate the ECVD file for your IP component instance (Global Settings > EcvdGenerationMethod = INDIVIDUAL > EcvdOutputPath = <EcvdOutputDir> > Click on the ""Generate Configuration"" button) # Import the previously generated ECVD file in your EBT project (Right click on TstIp in Project Explorer > Im and Exporters... > Green Button > Next > File Name: <Browse and select the ECVD file> > Next > Enable path mapping > Finish > Run Importer) CHECKPOINT 2: The ECVD file should have been successfully applied to your module. # Save (CTRL S) and generate the project (Right click on TstIp in Project Explorer > Generate Project) to trigger the EPC generation. CHECKPOINT 3: The EPC file should have been successfully generated (TstIp/output/output/<Ip>.epc) # Import the previously generated EPC file in your S32DS project (File > Import > Import ECU Configuration > Path: <EpcOutputDir> > Check ""Merge into current configuration"" > Check ""Check ECUC-MODULE-DEF"" value > CHECKPOINT 4: The EPC file should have been successfully imported into your S32DS project. If you get the error ""The required modules are not available for the current configuration"", it means that the ECUC-MODULE-DEF check has failed and you're not properly using M4_XDM_AR_PKG_NAME in your IP component. # Generate again the [LT/PB]Cfg.h/.c files of your IP component and save them somewhere without overwriting the previous set of files. We'll call this new set of files ImportedGenerateFiles_. # Compare the OriginalGenerateFiles set with the ImportedGenerateFiles set.
Release notes		

ID	Subtype	Headline and Description
ARTD-15721	New	New Feature [wdg] Enable ECPD generation for IP components (CPR_RTD_00544) ,,"Note: This feature must be implemented by all the modules for which this ticket was cloned (including CDDs). No clone shall be closed with ""Not Applicable"" or ""No Action Taken"". How to implement: # Add ""options_expr"" tags (containing all the necessary options) for the fields of the IP component(s). Please refer to the slides covering ""EPD Generation"" in Reference #2 below. # To ensure that the ECPD is generated only for your component, modify line 512 in ""mcu_data/components/PlatformSDK_S32K3_2021_08/system/codegenerator.js"" as follows: {code:javascript} if (configComponent.isOptionSet(""ecucDefinitionCollection"") && (configComponent.getId() === ""Gmac"")) { where you can replace ""Gmac"" with the ID of your IP component. # Check that there are no errors reported in the Problems view and that the ECPD has been generated in Code Preview. How to validate: # Manually create an EBT plugin using the previously generated ECPD. To achieve this: ## Unzip https://jira.sw.nxp.com/secure/attachment/828304/Ip_TS_T40D34M10I0R0.zip in the ""output/eclipse/plugins"" folder of your K3 work tree / repository. ## Open ""Ip_TS_T40D34M10I0R0/plugin.xml"" and replace all occurrences of ""Gmac"" with the ID of your IP component. # Create an EBT project (File > New > Configuration Project > Project Name: TstIp > Next > ECU ID: someId; Target: CORTEXM/S32K3XX > Finish) and add the previously created module (Right click on TstIp in Project Explorer > Module Configurations... > Double click on your module > OK) CHECKPOINT 1: The module should have been successfully imported into the project. # Go to S32DS and create a valid project using your IP component (or use an already existing one). Please assign a value other than the default value to each setting to avoid default values in this configuration{color}*. Rename your IP component instance and discard the ""_1"" prefix (e.g. ""Gmac_1"" > ""Gmac""): {panel}!screenshot-1.png! # Generate the [LT/PB]Cfg.h/.c files of your IP component and save them somewhere to avoid overwriting them in a later step. We'll call this set of files OriginalGenerateFiles_. # Generate the ECVD file for your IP component instance (Global Settings > EcvdGenerationMethod = INDIVIDUAL > EcvdOutputPath = <EcvdOutputDir> > Click on the ""Generate Configuration"" button) # Import the previously generated ECVD file in your EBT project (Right click on TstIp in Project Explorer > Im and Exporters... > Green Button > Next > File Name: <Browse and select the ECVD file> > Next > Enable path mapping > Finish > Run Importer) CHECKPOINT 2: The ECVD file should have been successfully applied to your module. # Save (CTRL S) and generate the project (Right click on TstIp in Project Explorer > Generate Project) to trigger the EPC generation. CHECKPOINT 3: The EPC file should have been successfully generated (TstIp/output/output/<Ip>.epc) # Import the previously generated EPC file in your S32DS project (File > Import > Import ECU Configuration > Path: <EpcOutputDir> > Check ""Merge into current configuration"" > Check ""Check ECUC-MODULE-DEF"" value > CHECKPOINT 4: The EPC file should have been successfully imported into your S32DS project. If you get the error ""The required modules are not available for the current configuration"", it means that the ECUC-MODULE-DEF check has failed and you're not properly using M4_XDM_AR_PKG_NAME in your IP component. # Generate again the [LT/PB]Cfg.h/.c files of your IP component and save them somewhere without overwriting the previous set of files. We'll call this new set of files ImportedGenerateFiles_. # Compare the OriginalGenerateFiles set with the ImportedGenerateFiles set.
Release notes		

ID	Subtype	Headline and Description
ARTD-15732	Bug	[Platform] Exceptions.c build at failed in GCC 10.2<*> Detailed description (how to reproduce it): The exceptions.c file build at failed only in GCC 10.2 compiler in line number 53: ASM_KEYWORD(".section .mcal_text"); !image-2021-08-25-13-13-54-525.png! [^build_cmd.txt] Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: Uart_TS_WIR_0001 Observed behavior: Error message: D:\Tools\cygwin64\tmp\ccxI35gv.s: Assembler messages: D:\Tools\cygwin64\tmp\ccxI35gv.s:30: Error: changed section attributes for .mcal_text D:\Tools\cygwin64\tmp\ccxI35gv.s:40: Error: changed section attributes for .mcal_text D:\Tools\cygwin64\tmp\ccxI35gv.s:43: Error: changed section attributes for .mcal_text D:\Tools\cygwin64\tmp\ccxI35gv.s:50: Error: changed section attributes for .mcal_text Expected behavior: Build at passed in GCC 10.2 compiler Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-15735	Bug	[PORT] Fix violation rules of code and design checklist<*> Detailed description (how to reproduce it): After review checklist, there is some violation rule, refer to linked ticket Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: After review checklist, there is some violation rule Expected behavior: All violation need to be fixed Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A

ID	Subtype	Headline and Description
ARTD-15740	Bug	[SENT][S32CT] Cannot update code for Sent on CT<*> Detailed description (how to reproduce it): Create a project for Sent on peripheral tool. After the configurating completed without error on any component->choose update code button >Error occurred and the code couldn't be generated. !image-2021-08-25-15-34-06-104.png! !image-2021-08-25-15-34-59-400.png! This issue happens on both HLD and IPL. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Expected behavior: NA Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-15734	New	New Feature [RM][S32K3XX] Update RM Configuration and codegen for CT ,,"NewWorkDescription: Update configuration file for RM module (add some validation related to Sema4 and memory region control) Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Attach below "
ARTD-15737	Bug	[ICU][S32K3XX] Build error for CCOV<*> The error due to the macro is not generated as below: Notice for 2 ipv Silu2 and LPCMP: !image-2021-08-25-15-33-43-997.png!

ID	Subtype	Headline and Description
ARTD-15744	Bug	[LIN] Function Lin_GetStatus return status LIN_RX_ERROR in case master send a incorrect response with IPV: FLEXIO<*> Detailed description (how to reproduce it): Create a error in stop bit of data byte 1 while a response is transmitting, driver will return status LIN_RX_ERROR. Preconditions: Because IPV FlexIO don't support hardware detect frame error. Thus, when a error in stop bit of data byte occurred (IPVs LPUART or LinFLexD support hardware detect frame error always generate a frame error in same case), with IPV FlexIO driver handle this error by function Flexio_Lin_Ip_ErrInterruptHandler and set LinCurrentState->CurrentEventId = FLEXIO_LIN_IP_RX_OVERRUN_ERROR. Function Lin_Getstatus will check LinCurrentState->CurrentEventId = FLEXIO_LIN_IP_RX_OVERRUN_ERROR and return value status in function Flexio_Lin_Ip_GetStatusFromRxOverrunError. But in this function driver only implemented with case RX error occur. Thus, driver will return status LIN_RX_ERROR. !image-2021-08-25-16-50-49-124.png|width=695,height=256! Test Case ID (internal TC that caught the defect) optional: Lin_TC_FCT_0214 Observed behavior: return LIN_RX_ERROR Expected behavior: return LIN_TX_ERROR Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA

ID	Subtype	Headline and Description
ARTD-15824	Bug	[crypto] [S32K 1.0.0] Fix all violations (HIS + MISRA + VSMD reports)<*> Detailed description (how to reproduce it): Create HIS MISRA VSMD reports Fix all violations for HIS MISRA VSMD reports *Reference: MISRA Deviation List: [https://bitbucket.sw.nxp.com/projects/ASPA/repos/real_time_drivers/browse/Generic/SW%20Development/RTD%20MISRA%20Deviations.xlsx] [https://confluence.sw.nxp.com/pages/viewpage.action?pageId=133734230] RTD Quality Criteria: [https://bitbucket.sw.nxp.com/projects/ASPA/repos/real_time_drivers/browse/Generic/Quality%20Assurance/RTD%20AASWS%20Gate%20and%20Release%20Criteria.xlsx] VSMD report: 0 warning, 0 error for RTM release MISRA report: 0 unjustified MISRA violations HIS report: !image-2021-08-30-12-26-52-249.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] All violations fix and follow RTD Quality Criteria Proposed solution optional: Fix all MISRA, HIS, VSMD violations

ID	Subtype	Headline and Description
ARTD-15826	Bug	[eth] [S32K 1.0.0] Fix all violations (HIS + MISRA + VSMD reports)<*> Detailed description (how to reproduce it): Create HIS MISRA VSMD reports Fix all violations for HIS MISRA VSMD reports *Reference: MISRA Deviation List: [https://bitbucket.sw.nxp.com/projects/ASPA/repos/real_time_drivers/browse/Generic/SW%20Development/RTD%20MISRA%20Deviations.xlsx] [https://confluence.sw.nxp.com/pages/viewpage.action?pageId=133734230] RTD Quality Criteria: [https://bitbucket.sw.nxp.com/projects/ASPA/repos/real_time_drivers/browse/Generic/Quality%20Assurance/RTD%20AASWS%20Gate%20and%20Release%20Criteria.xlsx] VSMD report: 0 warning, 0 error for RTM release MISRA report: 0 unjustified MISRA violations HIS report: !image-2021-08-30-12-26-52-249.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] All violations fix and follow RTD Quality Criteria Proposed solution optional: Fix all MISRA, HIS, VSMD violations

ID	Subtype	Headline and Description
ARTD-15827	Bug	[fee] [S32K 1.0.0] Fix all violations (HIS + MISRA + VSMD reports)<*> Detailed description (how to reproduce it): Create HIS MISRA VSMD reports Fix all violations for HIS MISRA VSMD reports *Reference: MISRA Deviation List: [https://bitbucket.sw.nxp.com/projects/ASPA/repos/real_time_drivers/browse/Generic/SW%20Development/RTD%20MISRA%20Deviations.xlsx] [https://confluence.sw.nxp.com/pages/viewpage.action?pageId=133734230] RTD Quality Criteria: [https://bitbucket.sw.nxp.com/projects/ASPA/repos/real_time_drivers/browse/Generic/Quality%20Assurance/RTD%20AASWS%20Gate%20and%20Release%20Criteria.xlsx] VSMD report: 0 warning, 0 error for RTM release MISRA report: 0 unjustified MISRA violations HIS report: !image-2021-08-30-12-26-52-249.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] All violations fix and follow RTD Quality Criteria Proposed solution optional: Fix all MISRA, HIS, VSMD violations

ID	Subtype	Headline and Description
ARTD-15828	Bug	[fls] [S32K3 1.0.0] Fix all violations (HIS + MISRA + VSMD reports)<*> Detailed description (how to reproduce it): Create HIS MISRA VSMD reports Fix all violations for HIS MISRA VSMD reports *Reference: MISRA Deviation List: [https://bitbucket.sw.nxp.com/projects/ASPA/repos/real_time_drivers/browse/Generic/SW%20Development/RTD%20MISRA%20Deviations.xlsx] [https://confluence.sw.nxp.com/pages/viewpage.action?pageId=133734230] RTD Quality Criteria: [https://bitbucket.sw.nxp.com/projects/ASPA/repos/real_time_drivers/browse/Generic/Quality%20Assurance/RTD%20AASWS%20Gate%20and%20Release%20Criteria.xlsx] VSMD report: 0 warning, 0 error for RTM release MISRA report: 0 unjustified MISRA violations HIS report: !image-2021-08-30-12-26-52-249.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] All violations fix and follow RTD Quality Criteria Proposed solution optional: Fix all MISRA, HIS, VSMD violations

ID	Subtype	Headline and Description
ARTD-15830	Bug	[i2c] [S32K 1.0.0] Fix all violations (HIS + MISRA + VSMD reports)<*> Detailed description (how to reproduce it): Create HIS MISRA VSMD reports Fix all violations for HIS MISRA VSMD reports *Reference: MISRA Deviation List: [https://bitbucket.sw.nxp.com/projects/ASPA/repos/real_time_drivers/browse/Generic/SW%20Development/RTD%20MISRA%20Deviations.xlsx] [https://confluence.sw.nxp.com/pages/viewpage.action?pageId=133734230] RTD Quality Criteria: [https://bitbucket.sw.nxp.com/projects/ASPA/repos/real_time_drivers/browse/Generic/Quality%20Assurance/RTD%20AASWS%20Gate%20and%20Release%20Criteria.xlsx] VSMD report: 0 warning, 0 error for RTM release MISRA report: 0 unjustified MISRA violations HIS report: !image-2021-08-30-12-26-52-249.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] All violations fix and follow RTD Quality Criteria Proposed solution optional: Fix all MISRA, HIS, VSMD violations

ID	Subtype	Headline and Description
ARTD-15832	Bug	[icu] [S32K 1.0.0] Fix all violations (HIS + MISRA + VSMD reports)<*> Detailed description (how to reproduce it): Create HIS MISRA VSMD reports Fix all violations for HIS MISRA VSMD reports *Reference: MISRA Deviation List: [https://bitbucket.sw.nxp.com/projects/ASPA/repos/real_time_drivers/browse/Generic/SW%20Development/RTD%20MISRA%20Deviations.xlsx] [https://confluence.sw.nxp.com/pages/viewpage.action?pageId=133734230] RTD Quality Criteria: [https://bitbucket.sw.nxp.com/projects/ASPA/repos/real_time_drivers/browse/Generic/Quality%20Assurance/RTD%20AASWS%20Gate%20and%20Release%20Criteria.xlsx] VSMD report: 0 warning, 0 error for RTM release MISRA report: 0 unjustified MISRA violations HIS report: !image-2021-08-30-12-26-52-249.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] All violations fix and follow RTD Quality Criteria Proposed solution optional: Fix all MISRA, HIS, VSMD violations

ID	Subtype	Headline and Description
ARTD-15838	Bug	[port] [S32K 1.0.0] Fix all violations (HIS + MISRA + VSMD reports)<*> Detailed description (how to reproduce it): Create HIS MISRA VSMD reports Fix all violations for HIS MISRA VSMD reports *Reference: MISRA Deviation List: [https://bitbucket.sw.nxp.com/projects/ASPA/repos/real_time_drivers/browse/Generic/SW%20Development/RTD%20MISRA%20Deviations.xlsx] [https://confluence.sw.nxp.com/pages/viewpage.action?pageId=133734230] RTD Quality Criteria: [https://bitbucket.sw.nxp.com/projects/ASPA/repos/real_time_drivers/browse/Generic/Quality%20Assurance/RTD%20AASWS%20Gate%20and%20Release%20Criteria.xlsx] VSMD report: 0 warning, 0 error for RTM release MISRA report: 0 unjustified MISRA violations HIS report: !image-2021-08-30-12-26-52-249.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] All violations fix and follow RTD Quality Criteria Proposed solution optional: Fix all MISRA, HIS, VSMD violations

ID	Subtype	Headline and Description
ARTD-15840	Bug	[rm] [S32K 1.0.0] Fix all violations (HIS + MISRA + VSMD reports)<*> Detailed description (how to reproduce it): Create HIS MISRA VSMD reports Fix all violations for HIS MISRA VSMD reports *Reference: MISRA Deviation List: [https://bitbucket.sw.nxp.com/projects/ASPA/repos/real_time_drivers/browse/Generic/SW%20Development/RTD%20MISRA%20Deviations.xlsx] [https://confluence.sw.nxp.com/pages/viewpage.action?pageId=133734230] RTD Quality Criteria: [https://bitbucket.sw.nxp.com/projects/ASPA/repos/real_time_drivers/browse/Generic/Quality%20Assurance/RTD%20AASWS%20Gate%20and%20Release%20Criteria.xlsx] VSMD report: 0 warning, 0 error for RTM release MISRA report: 0 unjustified MISRA violations HIS report: !image-2021-08-30-12-26-52-249.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] All violations fix and follow RTD Quality Criteria Proposed solution optional: Fix all MISRA, HIS, VSMD violations

ID	Subtype	Headline and Description
ARTD-15844	Bug	[uart] [S32K 1.0.0] Fix all violations (HIS + MISRA + VSMD reports)<*> Detailed description (how to reproduce it): Create HIS MISRA VSMD reports Fix all violations for HIS MISRA VSMD reports *Reference: MISRA Deviation List: [https://bitbucket.sw.nxp.com/projects/ASPA/repos/real_time_drivers/browse/Generic/SW%20Development/RTD%20MISRA%20Deviations.xlsx] [https://confluence.sw.nxp.com/pages/viewpage.action?pageId=133734230] RTD Quality Criteria: [https://bitbucket.sw.nxp.com/projects/ASPA/repos/real_time_drivers/browse/Generic/Quality%20Assurance/RTD%20AASWS%20Gate%20and%20Release%20Criteria.xlsx] VSMD report: 0 warning, 0 error for RTM release MISRA report: 0 unjustified MISRA violations HIS report: !image-2021-08-30-12-26-52-249.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] All violations fix and follow RTD Quality Criteria Proposed solution optional: Fix all MISRA, HIS, VSMD violations
ARTD-15846	Bug	[ADC] Fix all duplicated UUIDs<*> Coding convention implies that no TAB is to be used in the code source files we deliver. (to avoid inconsistent displays of code alignment if TAB size is defined differently) Replace all duplicated UUIDs, to avoid generation crashes on customer side. Proposed solution: # Replace all TABs with 4 spaces. # Update your text editor settings to always use 4 spaces instead of a TAB # Replace duplicated UUIDs. # Fix all violation that reports at PluginsCheck report: [http://somov.ea.freescale.net/1/project/custom_plugincheck/details] Refer attachment for 2021.08.30 baseline.

ID	Subtype	Headline and Description
ARTD-15856	Bug	[i2c] [S32K3 1.0.0] Fix all M4, TABs, duplicated UUIDs ,,"Coding convention implies that no TAB is to be used in the code source files we deliver. (to avoid inconsistent displays of code alignment if TAB size is defined differently) Replace all duplicated UUIDs, to avoid generation crashes on customer side. Proposed solution: # Replace all TABs with 4 spaces. # Update your text editor settings to always use 4 spaces instead of a TAB # Replace duplicated UUIDs. # Fix all violation that reports at PluginsCheck report: [http://somov.ea.freescale.net/1/project/custom_plugincheck/details] Refer attachment for 2021.08.30 baseline.
ARTD-15858	Bug	[icu] [S32K3 1.0.0] Fix all M4, TABs, duplicated UUIDs ,,"Coding convention implies that no TAB is to be used in the code source files we deliver. (to avoid inconsistent displays of code alignment if TAB size is defined differently) Replace all duplicated UUIDs, to avoid generation crashes on customer side. Proposed solution: # Replace all TABs with 4 spaces. # Update your text editor settings to always use 4 spaces instead of a TAB # Replace duplicated UUIDs. # Fix all violation that reports at PluginsCheck report: [http://somov.ea.freescale.net/1/project/custom_plugincheck/details] Refer attachment for 2021.08.30 baseline.
ARTD-15863	Bug	[platform] [S32K3 1.0.0] Fix all M4, TABs, duplicated UUIDs ,,"Coding convention implies that no TAB is to be used in the code source files we deliver. (to avoid inconsistent displays of code alignment if TAB size is defined differently) Replace all duplicated UUIDs, to avoid generation crashes on customer side. Proposed solution: # Replace all TABs with 4 spaces. # Update your text editor settings to always use 4 spaces instead of a TAB # Replace duplicated UUIDs. # Fix all violation that reports at PluginsCheck report: [http://somov.ea.freescale.net/1/project/custom_plugincheck/details] Refer attachment for 2021.08.30 baseline.

ID	Subtype	Headline and Description
ARTD-15866	Bug	[rm] [S32K3 1.0.0] Fix all M4, TABs, duplicated UUIDs ,,"Coding convention implies that no TAB is to be used in the code source files we deliver. (to avoid inconsistent displays of code alignment if TAB size is defined differently) Replace all duplicated UUIDs, to avoid generation crashes on customer side. Proposed solution: # Replace all TABs with 4 spaces. # Update your text editor settings to always use 4 spaces instead of a TAB # Replace duplicated UUIDs. # Fix all violation that reports at PluginsCheck report: [http://somov.ea.freescale.net/1/project/custom_plugincheck/details] Refer attachment for 2021.08.30 baseline.
ARTD-15870	Bug	[uart] [S32K3 1.0.0] Fix all M4, TABs, duplicated UUIDs ,,"Coding convention implies that no TAB is to be used in the code source files we deliver. (to avoid inconsistent displays of code alignment if TAB size is defined differently) Replace all duplicated UUIDs, to avoid generation crashes on customer side. Proposed solution: # Replace all TABs with 4 spaces. # Update your text editor settings to always use 4 spaces instead of a TAB # Replace duplicated UUIDs. # Fix all violation that reports at PluginsCheck report: [http://somov.ea.freescale.net/1/project/custom_plugincheck/details] Refer attachment for 2021.08.30 baseline.
ARTD-15871	Bug	[wdg] [S32K3 1.0.0] Fix all M4, TABs, duplicated UUIDs ,,"Coding convention implies that no TAB is to be used in the code source files we deliver. (to avoid inconsistent displays of code alignment if TAB size is defined differently) Replace all duplicated UUIDs, to avoid generation crashes on customer side. Proposed solution: # Replace all TABs with 4 spaces. # Update your text editor settings to always use 4 spaces instead of a TAB # Replace duplicated UUIDs. # Fix all violation that reports at PluginsCheck report: [http://somov.ea.freescale.net/1/project/custom_plugincheck/details] Refer attachment for 2021.08.30 baseline.

ID	Subtype	Headline and Description
ARTD-15762	Bug	[ICU][S32K3XX] Build error when using DMA with signal measurement mode<*> In function Icu_SignalMeasurementDmaProcessing(), the variable ChannelIndex is declared twice and sub function Icu_Ipw_GetPWandPeriod() is not declared in ipw file : !image-2021-08-26-16-13-49-316.png! The function Icu_Ipw_GetPWandPeriod() need to be declared in IPW Layer is to get the value of period and pulse width after calculating with DMA.
ARTD-15765	Bug	[WDG] SWT_IP_CLEAR_RESET_REQUEST node not available but generate code still = STD_ON in S32CT<*> Detailed description (how to reproduce it): Step 1: Create new project into S32CT Step 2: Add Swt_Ip_1 component into project and Step 3: Config " Swt Disable Allowed" node is OFF, same as my picture ! image-2021-08-26-17-18-12-327.png! Step 4: Update code and Check code generated Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: SWT_IP_CLEAR_RESET_REQUEST node not available but generate code still = STD_ON !image-2021-08-26-17-20-24-477.png! Expected behavior: When the SWT_IP_DEINIT node is OFF the SWT_IP_CLEAR_RESET_REQUEST node must also be OFF Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-15773	New	New Feature [BASE] Add support for REQUIRES-INDEX in generateEcpd.js ,,"NewWorkDescription: Add support for REQUIRES-INDEX in generateEcpd.js Requirement source: AUTOSAR_TPS_ECUConfiguration (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Add support for REQUIRES-INDEX in generateEcpd.js"

ID	Subtype	Headline and Description
ARTD-15779	Bug	[LIN] Driver should clear all bit values that do not belong in the actual data bitfield when reading the data register<*> Detailed description (how to reproduce it): Before recording the data read from a register, the driver shall filter the value read from the data register clearing all bit values that do not belong in the actual data bitfield. Configured data alignment in the register shall also be considered Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: NA Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA

ID	Subtype	Headline and Description
ARTD-15786	Bug	[S32K3XX][FLEXIO_I2C]send stop frame after FLEXIO_I2C_IP_DMA_ERROR_STATUS make bus busy<*> Detailed description (how to reproduce it): [...] set up Maf send use Flexio_I2c_Ip_MasterReceiveData to receive with InValid_Rx_buffer adress to raise an DMA error after Driver get DMA_IP_CH_ERROR_STATE in Flexio_I2c_Ip_MasterDmaTransferErrorHandler(), Driver will send a stop bit with value 0 make bus busy. Flexio_I2c_Ip_WriteShifterBuffer(BaseAddr, TX_SHIFTER(ResourceIndex), (((uint32)FLEXIO_I2C_IP_STOP_BYTE_VALUE_U32)<<24U), FLEXIO_SHIFTER_RW_MODE_BIT_SWAP); Preconditions: [...] N/A Test Case ID (internal TC that caught the defect) optional: [...] Ip_Flexio_TC_FCT_2023 Observed behavior: [...] after Driver get DMA_IP_CH_ERROR_STATE in Flexio_I2c_Ip_MasterDmaTransferErrorHandler(), Driver will send a stop bit with value 0 make bus busy. Flexio_I2c_Ip_WriteShifterBuffer(BaseAddr, TX_SHIFTER(ResourceIndex), (((uint32)FLEXIO_I2C_IP_STOP_BYTE_VALUE_U32)<<24U), FLEXIO_SHIFTER_RW_MODE_BIT_SWAP); Expected behavior: [...] after Driver get DMA_IP_CH_ERROR_STATE in Flexio_I2c_Ip_MasterDmaTransferErrorHandler(), Driver need stop transfer Flexio_I2c_Ip_MasterStopTransfer() Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) N/A Proposed solution optional: [...]N/A

ID	Subtype	Headline and Description
ARTD-15787	Bug	[ICU][S32K3XX] Fix bug wrong DMA macro generation in DS<*> Detailed description (how to reproduce it): When enable Icu DMA support, DS generate wrong macro EMIOS_ICU_MODE_WITHOUT_DMA instead EMIOS_ICU_MODE_WITH_DMA. Reason is get wrong id as follow image: !image-2021-08-27-11-29-48-041.png|width=1110,height=67! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: Icu_TC_WBT_0302 Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Correct ID
ARTD-15795	Bug	[ETH]Error occurred for Timestamp nodes in Post build mode<*> Detailed description (how to reproduce it): Postbuild with multiple variants enabled. because EthTimeStampRequiredAccuracy with multiple variant = false refer to node McuClockReferencePointFrequency has multiple variant. Preconditions: Postbuild with multiple variants enabled. Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: error reported at INVALID of node EthTimeStampRequiredAccuracy Expected behavior: No error reported Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Change nodes EthTimeStampRequiredAccuracy and EthTimeStampReferenceClock with: <a:a name="POSTBUILDVARIANTVALUE" value="true"/> <a:a name="POSTBUILDVARIANTMULTIPLICITY" value="true"/>
ARTD-15792	Bug	[DIO] Missing rte_dio dependency in sdk_manifest<*> Detailed description (how to reproduce it): In sdk_manifest, platform.driver.siul2_dio is missing the dependency platform.driver.rte_dio Expected behavior: platform.driver.siul2_dio should have the dependency platform.driver.rte_dio Proposed solution optional: correct sdk_manifest

ID	Subtype	Headline and Description
ARTD-15797	Bug	[S32K3] S32DS driver raise error incorrectly<*> Detailed description (how to reproduce it): When config key on S32DS with key_export = true but key_type in key_catalog is no in group (AES, HMAC, TDES) e.g ECC_PAIR , driver still raise error " HSE Key Export is enabled requiring CryptoKeyElement with CryptoKeyElementId = 99 " Preconditions: NA Observed behavior: Driver raise error " HSE Key Export is enabled requiring CryptoKeyElement with CryptoKeyElementId = 99 " when config key_export=true and key_type = ECC_PAIR Expected behavior: Driver doesn't raise error when config key_export=true and key_type in group (ECC_PAIR, ECC_PUB, RSA_PAIR, RSA_PUB) Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-15801	Bug	[WDG] Correct error codes in Wdg_Channel.c<*> Detailed description (how to reproduce it): 1. In Wdg_Channel.c, in Wdg_ChannelClearResetRequest, the Det_ReportRuntimeError API is called with error id WDG_E_PARAM_TIMEOUT, which is related to the timeout parametere of the Wdg_SetTriggerCondition api. 2. WDG_E_PARAM_CONFIG should be used to report that the accessed resource is not available on the current core. Some Det's use this error id instead of WDG_E_PARAM_MODE: in Wdg_ChannelInit in the line1363 valid = Wdg_ChannelValidateMode(Wdg_apConfigPtr[Wdg_Instance]->Wdg_DefaultMode, WDG_INIT_ID, WDG_E_PARAM_CONFIG, Wdg_Instance); In Wdg_VadidateHardwareSetting() Proposed solution optional: 1. Add a new error code WDG_E_STATUS_TIMEOUT = 0x16, to be used by the Wdg_ClearResetRequest() API. This define should be guarded by the same #ifdefs as the API. 2. Replace WDG_E_PARAM_CONFIG with WDG_E_PARAM_MODE where mentioned. 3. Update the error codes descriptions as in the Requirement SWS_Wdg_00010 as described in https://crucible1.sw.nxp.com/cru/R-ARTD-1027.

ID	Subtype	Headline and Description
ARTD-15900	Bug	[RM] Diff output CT and EB for Virt Wrapper<*> Detailed description (how to reproduce it): diff output EB and CT for Virt_Wrapper See more attachments Preconditions: generate output EB and CT then compare Test Case ID (internal TC that caught the defect) optional: Rm_TC_FCT_0002 Observed behavior: diff output EB and CT for Virt_Wrapper Expected behavior: same output EB and CT for Virt_Wrapper Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: same output EB and CT for Virt_Wrapper
ARTD-15916	Bug	[GPT] RTC GptChannelTickFrequency is not matched with GPT clock sources<*> Detailed description (how to reproduce it): The RTC GptChannelTickFrequency is mismatched when choosing different clock sources: RTC_IP_CLOCK_SOURCE_2 (FIRC 48M), but GptChannelTickFrequency is 128000 RTC_IP_CLOCK_SOURCE_1 (SIRC 32K), but GptChannelTickFrequency is 16000000 RTC_IP_CLOCK_SOURCE_3 (FXOSC 8-40M, dynamic value), but GptChannelTickFrequency is always 32000 Preconditions: Choose RTC as GPT channel hw Test Case ID (internal TC that caught the defect) optional: Ip_Rtc_TC_FCT_0001(Ip_Rtc_TS_001) Observed behavior: RTC GptChannelTickFrequency is mismatched when choosing different clock sources Expected behavior: Correct RTC GptChannelTickFrequency when choosing different clock sources. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A

ID	Subtype	Headline and Description
ARTD-15917	Bug	[Port][CTHL] Wrong register's bit setting for unused pins<*> Detailed description (how to reproduce it): Use Plugin_2882021 and generate the layout for S32DS. Add Port component and config for NotUsedPortPin as below: PortPin Pull Enable = True PortPin Pull Select = True Update source code and find Port_xxx_PBcfg.c Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: The register setting for the PortPin Pull Select was wrong, It must be set on 11th bit. !image-2021-08-30-18-05-59-304.png! In this case, it must be 0x00082800 Expected behavior: The register must be set correctly.
ARTD-15915	Bug	[ADC] Internal buffer u32DmaNoIrqBuffer was not cleared after read group of previous test case in DMA without interrupt feature<*> Detailed description (how to reproduce it): Internal buffer u32DmaNoIrqBuffer was not cleared after read group of previous test case in DMA without interrupt feature Preconditions: Transfer type DMA Group sw injected oneshot without interrupt Test Case ID (internal TC that caught the defect) optional: Adc_TC_FCT_0111 Adc_TS_007 cfg 2 Observed behavior: Start injected oneshot group Wait until read group return E_OK Real status: Read group always reuturn E_OK because internal buffer u32DmaNoIrqBuffer still have valid data from previous test case Expected behavior: u32DmaNoIrqBuffer was cleared or make data invalid after read group and deinit Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA

ID	Subtype	Headline and Description
ARTD-15924	Bug	[UART] Driver should clear all bit values that do not belong in the actual data bitfield when reading the data register<*> Detailed description (how to reproduce it): Before recording the data read from a register, the driver shall filter the value read from the data register clearing all bit values that do not belong in the actual data bitfield. Configured data alignment in the register shall also be considered Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: NA Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-15931	Bug	[RM] [S32K3] Function Sema42_Ip_GetResetGateIndex is missing return SEMA42_RESET_GATE_ALL<*> Detailed description (how to reproduce it): Please check Requirement SEMA42_IP_009_001 Function Sema42_Ip_GetResetGateIndex is missing return SEMA42_RESET_GATE_ALL if all gates have been targetted for reset. !image-2021-08-31-10-28-32-582.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-16026	Bug	[S32K3 RTM] Functions ArrayIntegrityCheck and UserMarginReadCheck should return an error when calling them with the wrong DomainID<*> Detailed description (how to reproduce it): Step1: Call C40_Ip_MainInterfaceWrite or C40_Ip_MainInterfaceSectorErase with wrong DomainID Step2: Call C40_Ip_ArrayIntegrityCheck or C40_Ip_UserMarginReadCheck with correct param, the return status will be Error Test Case ID (internal TC that caught the defect) optional: Ip_C40_TC_1012 Observed behavior: variable C40_Ip_CurrentTicks is not reset before use C40_Ip_ArrayIntegrityCheck or C40_Ip_UserMarginReadCheck return error in this case Expected behavior: variable C40_Ip_CurrentTicks is reset before use C40_Ip_ArrayIntegrityCheck or C40_Ip_UserMarginReadCheck will return success in this case
ARTD-16222	New	New Feature [RM] S32K3 Validate values from hardware before return. ,,"NewWorkDescription: Update driver follow Measure Applied in FMEA report in attachment. Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: NA"
ARTD-16263	Bug	[UART] Flexio receiver function not work when using DMA<*> Detailed description (how to reproduce it): In the Flexio_Uart_Ip.c file, seem that _Flexio_Uart_Ip_CompleteReceiveUsingDma() function has been suspended in while loop that is used to check for the data is completely shifted out of shift register. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: Test case Uart_WBT_TC_0010.c Observed behavior: [...] Expected behavior: While loop should be executed to get timer status instead of shifter status to avoid suspend. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-16266	Bug	[Mcl] S32CT not generate configuration structure for routing interrupt<*> Detailed description (how to reproduce it): Create new project and add MCL. In to project using EMIOS and enable multicore. Enable interrupt for emios in platform for both core 0 and 1. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: MCL_TS_430, MCL_TS_431 Observed behavior: In the file IntCtrl_Ip_Cfg.h defined struct intRouteConfigEcucPartition_0 but in the IntCtrl_Ip_Cfg.c, I don't see it. That gives error when i build test: !image-2021-09-01-10-14-09-159.png! Expected behavior: Struct intRouteConfigEcucPartition_0 generated in IntCtrl_Ip_Cfg.c like when generate with EB Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-16268	Bug	[FLS][S32K3XX_RTM_100] Diff output CT and EB<*> Detailed description (how to reproduce it): See more pictures in attachments Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Diff output EB and CT Expected behavior: Same output when generating by EB and CT Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Same output when generating by EB and CT
ARTD-16271	Bug	[ICU][S32K3XX] Error for DMA configuration in S32DS<*> In configuration in DS, there are 2 channel configured for DMA mode (Emios0_CH1 and Emios1_CH22 as config file attached), but the output generation generate until 3 channel with DMA mode. !image-2021-09-01-11-36-44-548.png! The test name in testing side folder: Icu_TS_DS_031 with the mex file attached.

ID	Subtype	Headline and Description
ARTD-16281	Bug	[Port][CTHL] Unexpected warning occurs after configurating some pins<*> Detailed description (how to reproduce it): Use Plugin_192021 and generate the S32DS layout. Create a new project and add Port component. Choose randomly PortPin MSCR from 128 to 219, set PortPin Mode to any Input mode (mentioned in Io_mux) Case ID (internal TC that caught the defect) optional: N/A Observed behavior: A warning is shown up as follow: !image-2021-09-01-14-58-20-903.png! Its applied for the last pin configurated in one container (the bigger container number takes this warnings), that means something like this: multi container: !image-2021-09-01-15-05-24-668.png! one container: !image-2021-09-01-15-05-44-803.png! Expected behavior: No wrong warnings are shown up.
ARTD-16286	Bug	[ETH] DET error shall not be reported if Eth driver is un-initialized in Eth_MainFunction<*> Detailed description (how to reproduce it): In Eth_MainFunction, DET error is reported in case Eth driver is un-initialized. According with Autosar requirements if the module is not initialized and the main function is executed no error should be reported. !SWS_BSW_00037.png|width=618,height=98! Preconditions: Eth_MainFunction() is called before Eth_Init(), or Eth_Init() is called without success. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: In case driver is un-initialized, Eth_MainFunction() raises DET report. Expected behavior: In case driver is un-initialized, Eth_MainFunction() shall not raise DET report and return immediately. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: CE's comment: as workaround from customers, they have disabled the Det from Eth configuration. Their major issue is that Eth variables that are used in Eth_MainFunction are initialized in Eth_Init. Since the Eth_MainFunction is executed before Eth_Init there will be an exception reported by the Os because the accessed variables are not initialized. !Eth_apCtrlConfig_undefined.png! Please consider also this aspect when analysis.

ID	Subtype	Headline and Description
ARTD-16289	New	New Feature [icu] Increase code exposure numbers ,,"NewWorkDescription: Expose as much of the driver code as possible (this will be checked with the code exposure tool). Code exposure target is minimum 90% Code exposure for gpt driver is around 72% in this moment Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]"
ARTD-16296	Bug	[Port][CTHL] No constrain for VirtWrapperSupport feature<*> Detailed description (how to reproduce it): Use Plugin_192021 and generate the S32DS layout. Add Port component and configurate the setting for VirtWrapperSupport (It will need to enable PortMulticoreSupport and dependency modules such as Os, ECuC,...) Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: The project running with VirtWrapperSupport enabled in Port component can be generated and built successfully with both below scenarios: # Rm component isn't added # Rm component is added but the RmVirtWrapperConfigurable node isn't enabled Expected behavior: If Port component enables the VirtWrapperSupport, Rm component must be added and RmVirtWrapperConfigurable node must be enabled. Proposed solution optional: Add constrains for Virtual Wrapper feature.

ID	Subtype	Headline and Description
ARTD-16335	Bug	[adc] [EBT] OsApplicationCoreRef and OsAppEcucPartitionRef shall be accessed as parameters<*> Note: This issue is only affecting EBT configuration and source files! Detailed description (how to reproduce it): Our OS stub configuration defined OsAppEcucPartitionRef and OsApplicationCoreRef as lists, but the AUTOSAR specification defines them as optional parameters. We fixed this in the OS module, but now all the other modules that depend on OS to implement multicore features are affected. Preconditions: Create a multicore configuration. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: OsAppEcucPartitionRef and OsApplicationCoreRef are accessed as lists. As a result, the configuration and generation are failing. Expected behavior: OsAppEcucPartitionRef and OsApplicationCoreRef are accessed as parameters. As a result, the configuration and generation are successful. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: # Replace all occurrences of {code}OsApplicationCoreRef/*[1] with {code}OsApplicationCoreRef # Replace all occurrences of {code}OsAppEcucPartitionRef/*[1] with {code}OsAppEcucPartitionRef Warning: Do not forget to adjust relative paths if needed (e.g. in SELECT-expressions).
ARTD-16336	Bug	[base] [EBT] OsApplicationCoreRef and OsAppEcucPartitionRef shall be accessed as parameters<*> Note: This issue is only affecting EBT configuration and source files! Detailed description (how to reproduce it): Our OS stub configuration defined OsAppEcucPartitionRef and OsApplicationCoreRef as lists, but the AUTOSAR specification defines them as optional parameters. We fixed this in the OS module, but now all the other modules that depend on OS to implement multicore features are affected. Preconditions: Create a multicore configuration. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: OsAppEcucPartitionRef and OsApplicationCoreRef are accessed as lists. As a result, the configuration and generation are failing. Expected behavior: OsAppEcucPartitionRef and OsApplicationCoreRef are accessed as parameters. As a result, the configuration and generation are successful. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: # Replace all occurrences of {code}OsApplicationCoreRef/*[1] with {code}OsApplicationCoreRef # Replace all occurrences of {code}OsAppEcucPartitionRef/*[1] with {code}OsAppEcucPartitionRef Warning: Do not forget to adjust relative paths if needed (e.g. in SELECT-expressions).

ID	Subtype	Headline and Description
ARTD-16337	Bug	[can] [EBT] OsApplicationCoreRef and OsAppEcucPartitionRef shall be accessed as parameters<*> Note: This issue is only affecting EBT configuration and source files! Detailed description (how to reproduce it): Our OS stub configuration defined OsAppEcucPartitionRef and OsApplicationCoreRef as lists, but the AUTOSAR specification defines them as optional parameters. We fixed this in the OS module, but now all the other modules that depend on OS to implement multicore features are affected. Preconditions: Create a multicore configuration. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: OsAppEcucPartitionRef and OsApplicationCoreRef are accessed as lists. As a result, the configuration and generation are failing. Expected behavior: OsAppEcucPartitionRef and OsApplicationCoreRef are accessed as parameters. As a result, the configuration and generation are successful. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: # Replace all occurrences of {code}OsApplicationCoreRef/*[1] with {code}OsApplicationCoreRef # Replace all occurrences of {code}OsAppEcucPartitionRef/*[1] with {code}OsAppEcucPartitionRef Warning: Do not forget to adjust relative paths if needed (e.g. in SELECT-expressions).
ARTD-16340	Bug	[crypto] [EBT] OsApplicationCoreRef and OsAppEcucPartitionRef shall be accessed as parameters<*> Note: This issue is only affecting EBT configuration and source files! Detailed description (how to reproduce it): Our OS stub configuration defined OsAppEcucPartitionRef and OsApplicationCoreRef as lists, but the AUTOSAR specification defines them as optional parameters. We fixed this in the OS module, but now all the other modules that depend on OS to implement multicore features are affected. Preconditions: Create a multicore configuration. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: OsAppEcucPartitionRef and OsApplicationCoreRef are accessed as lists. As a result, the configuration and generation are failing. Expected behavior: OsAppEcucPartitionRef and OsApplicationCoreRef are accessed as parameters. As a result, the configuration and generation are successful. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: # Replace all occurrences of {code}OsApplicationCoreRef/*[1] with {code}OsApplicationCoreRef # Replace all occurrences of {code}OsAppEcucPartitionRef/*[1] with {code}OsAppEcucPartitionRef Warning: Do not forget to adjust relative paths if needed (e.g. in SELECT-expressions).

ID	Subtype	Headline and Description
ARTD-16342	Bug	[eth] [EBT] OsApplicationCoreRef and OsAppEcucPartitionRef shall be accessed as parameters<*> Note: This issue is only affecting EBT configuration and source files! Detailed description (how to reproduce it): Our OS stub configuration defined OsAppEcucPartitionRef and OsApplicationCoreRef as lists, but the AUTOSAR specification defines them as optional parameters. We fixed this in the OS module, but now all the other modules that depend on OS to implement multicore features are affected. Preconditions: Create a multicore configuration. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: OsAppEcucPartitionRef and OsApplicationCoreRef are accessed as lists. As a result, the configuration and generation are failing. Expected behavior: OsAppEcucPartitionRef and OsApplicationCoreRef are accessed as parameters. As a result, the configuration and generation are successful. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: # Replace all occurrences of {code}OsApplicationCoreRef/*[1] with {code}OsApplicationCoreRef # Replace all occurrences of {code}OsAppEcucPartitionRef/*[1] with {code}OsAppEcucPartitionRef Warning: Do not forget to adjust relative paths if needed (e.g. in SELECT-expressions).
ARTD-16345	Bug	[gpt] [EBT] OsApplicationCoreRef and OsAppEcucPartitionRef shall be accessed as parameters<*> Note: This issue is only affecting EBT configuration and source files! Detailed description (how to reproduce it): Our OS stub configuration defined OsAppEcucPartitionRef and OsApplicationCoreRef as lists, but the AUTOSAR specification defines them as optional parameters. We fixed this in the OS module, but now all the other modules that depend on OS to implement multicore features are affected. Preconditions: Create a multicore configuration. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: OsAppEcucPartitionRef and OsApplicationCoreRef are accessed as lists. As a result, the configuration and generation are failing. Expected behavior: OsAppEcucPartitionRef and OsApplicationCoreRef are accessed as parameters. As a result, the configuration and generation are successful. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: # Replace all occurrences of {code}OsApplicationCoreRef/*[1] with {code}OsApplicationCoreRef # Replace all occurrences of {code}OsAppEcucPartitionRef/*[1] with {code}OsAppEcucPartitionRef Warning: Do not forget to adjust relative paths if needed (e.g. in SELECT-expressions).

ID	Subtype	Headline and Description
ARTD-16299	New	New Feature [BASE] Update Can_GeneralTypes.h with SWS_CanTrcv_00164 and SWS_CanTrcv_00165 ,,Update Can_GeneralTypes.h with SWS_CanTrcv_00164 and SWS_CanTrcv_00165
ARTD-16346	Bug	[i2c] [EBT] OsApplicationCoreRef and OsAppEcucPartitionRef shall be accessed as parameters<*> Note: This issue is only affecting EBT configuration and source files! Detailed description (how to reproduce it): Our OS stub configuration defined OsAppEcucPartitionRef and OsApplicationCoreRef as lists, but the AUTOSAR specification defines them as optional parameters. We fixed this in the OS module, but now all the other modules that depend on OS to implement multicore features are affected. Preconditions: Create a multicore configuration. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: OsAppEcucPartitionRef and OsApplicationCoreRef are accessed as lists. As a result, the configuration and generation are failing. Expected behavior: OsAppEcucPartitionRef and OsApplicationCoreRef are accessed as parameters. As a result, the configuration and generation are successful. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: # Replace all occurrences of {code}OsApplicationCoreRef/*[1] with {code}OsApplicationCoreRef # Replace all occurrences of {code}OsAppEcucPartitionRef/*[1] with {code}OsAppEcucPartitionRef Warning: Do not forget to adjust relative paths if needed (e.g. in SELECT-expressions).

ID	Subtype	Headline and Description
ARTD-16352	Bug	[ocu] [EBT] OsApplicationCoreRef and OsAppEcucPartitionRef shall be accessed as parameters<*> Note: This issue is only affecting EBT configuration and source files! Detailed description (how to reproduce it): Our OS stub configuration defined OsAppEcucPartitionRef and OsApplicationCoreRef as lists, but the AUTOSAR specification defines them as optional parameters. We fixed this in the OS module, but now all the other modules that depend on OS to implement multicore features are affected. Preconditions: Create a multicore configuration. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: OsAppEcucPartitionRef and OsApplicationCoreRef are accessed as lists. As a result, the configuration and generation are failing. Expected behavior: OsAppEcucPartitionRef and OsApplicationCoreRef are accessed as parameters. As a result, the configuration and generation are successful. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: # Replace all occurrences of {code}OsApplicationCoreRef/*[1] with {code}OsApplicationCoreRef # Replace all occurrences of {code}OsAppEcucPartitionRef/*[1] with {code}OsAppEcucPartitionRef Warning: Do not forget to adjust relative paths if needed (e.g. in SELECT-expressions).
ARTD-16354	Bug	[platform] [EBT] OsApplicationCoreRef and OsAppEcucPartitionRef shall be accessed as parameters<*> Note: This issue is only affecting EBT configuration and source files! Detailed description (how to reproduce it): Our OS stub configuration defined OsAppEcucPartitionRef and OsApplicationCoreRef as lists, but the AUTOSAR specification defines them as optional parameters. We fixed this in the OS module, but now all the other modules that depend on OS to implement multicore features are affected. Preconditions: Create a multicore configuration. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: OsAppEcucPartitionRef and OsApplicationCoreRef are accessed as lists. As a result, the configuration and generation are failing. Expected behavior: OsAppEcucPartitionRef and OsApplicationCoreRef are accessed as parameters. As a result, the configuration and generation are successful. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: # Replace all occurrences of {code}OsApplicationCoreRef/*[1] with {code}OsApplicationCoreRef # Replace all occurrences of {code}OsAppEcucPartitionRef/*[1] with {code}OsAppEcucPartitionRef Warning: Do not forget to adjust relative paths if needed (e.g. in SELECT-expressions).

ID	Subtype	Headline and Description
ARTD-16355	Bug	[port] [EBT] OsApplicationCoreRef and OsAppEcucPartitionRef shall be accessed as parameters<*> Note: This issue is only affecting EBT configuration and source files! Detailed description (how to reproduce it): Our OS stub configuration defined OsAppEcucPartitionRef and OsApplicationCoreRef as lists, but the AUTOSAR specification defines them as optional parameters. We fixed this in the OS module, but now all the other modules that depend on OS to implement multicore features are affected. Preconditions: Create a multicore configuration. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: OsAppEcucPartitionRef and OsApplicationCoreRef are accessed as lists. As a result, the configuration and generation are failing. Expected behavior: OsAppEcucPartitionRef and OsApplicationCoreRef are accessed as parameters. As a result, the configuration and generation are successful. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: # Replace all occurrences of {code}OsApplicationCoreRef/*[1] with {code}OsApplicationCoreRef # Replace all occurrences of {code}OsAppEcucPartitionRef/*[1] with {code}OsAppEcucPartitionRef Warning: Do not forget to adjust relative paths if needed (e.g. in SELECT-expressions).
ARTD-16359	Bug	[sai] [EBT] OsApplicationCoreRef and OsAppEcucPartitionRef shall be accessed as parameters<*> Note: This issue is only affecting EBT configuration and source files! Detailed description (how to reproduce it): Our OS stub configuration defined OsAppEcucPartitionRef and OsApplicationCoreRef as lists, but the AUTOSAR specification defines them as optional parameters. We fixed this in the OS module, but now all the other modules that depend on OS to implement multicore features are affected. Preconditions: Create a multicore configuration. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: OsAppEcucPartitionRef and OsApplicationCoreRef are accessed as lists. As a result, the configuration and generation are failing. Expected behavior: OsAppEcucPartitionRef and OsApplicationCoreRef are accessed as parameters. As a result, the configuration and generation are successful. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: # Replace all occurrences of {code}OsApplicationCoreRef/*[1] with {code}OsApplicationCoreRef # Replace all occurrences of {code}OsAppEcucPartitionRef/*[1] with {code}OsAppEcucPartitionRef Warning: Do not forget to adjust relative paths if needed (e.g. in SELECT-expressions).

ID	Subtype	Headline and Description
ARTD-16361	Bug	[spi] [EBT] OsApplicationCoreRef and OsAppEcucPartitionRef shall be accessed as parameters<*> Note: This issue is only affecting EBT configuration and source files! Detailed description (how to reproduce it): Our OS stub configuration defined OsAppEcucPartitionRef and OsApplicationCoreRef as lists, but the AUTOSAR specification defines them as optional parameters. We fixed this in the OS module, but now all the other modules that depend on OS to implement multicore features are affected. Preconditions: Create a multicore configuration. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: OsAppEcucPartitionRef and OsApplicationCoreRef are accessed as lists. As a result, the configuration and generation are failing. Expected behavior: OsAppEcucPartitionRef and OsApplicationCoreRef are accessed as parameters. As a result, the configuration and generation are successful. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: # Replace all occurrences of {code}OsApplicationCoreRef/*[1] with {code}OsApplicationCoreRef # Replace all occurrences of {code}OsAppEcucPartitionRef/*[1] with {code}OsAppEcucPartitionRef Warning: Do not forget to adjust relative paths if needed (e.g. in SELECT-expressions).
ARTD-16363	Bug	[uart] [EBT] OsApplicationCoreRef and OsAppEcucPartitionRef shall be accessed as parameters<*> Note: This issue is only affecting EBT configuration and source files! Detailed description (how to reproduce it): Our OS stub configuration defined OsAppEcucPartitionRef and OsApplicationCoreRef as lists, but the AUTOSAR specification defines them as optional parameters. We fixed this in the OS module, but now all the other modules that depend on OS to implement multicore features are affected. Preconditions: Create a multicore configuration. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: OsAppEcucPartitionRef and OsApplicationCoreRef are accessed as lists. As a result, the configuration and generation are failing. Expected behavior: OsAppEcucPartitionRef and OsApplicationCoreRef are accessed as parameters. As a result, the configuration and generation are successful. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: # Replace all occurrences of {code}OsApplicationCoreRef/*[1] with {code}OsApplicationCoreRef # Replace all occurrences of {code}OsAppEcucPartitionRef/*[1] with {code}OsAppEcucPartitionRef Warning: Do not forget to adjust relative paths if needed (e.g. in SELECT-expressions).

ID	Subtype	Headline and Description
ARTD-16364	Bug	[wdg] [EBT] OsApplicationCoreRef and OsAppEcucPartitionRef shall be accessed as parameters<*> Note: This issue is only affecting EBT configuration and source files! Detailed description (how to reproduce it): Our OS stub configuration defined OsAppEcucPartitionRef and OsApplicationCoreRef as lists, but the AUTOSAR specification defines them as optional parameters. We fixed this in the OS module, but now all the other modules that depend on OS to implement multicore features are affected. Preconditions: Create a multicore configuration. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: OsAppEcucPartitionRef and OsApplicationCoreRef are accessed as lists. As a result, the configuration and generation are failing. Expected behavior: OsAppEcucPartitionRef and OsApplicationCoreRef are accessed as parameters. As a result, the configuration and generation are successful. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: # Replace all occurrences of {code}OsApplicationCoreRef/*[1] with {code}OsApplicationCoreRef # Replace all occurrences of {code}OsAppEcucPartitionRef/*[1] with {code}OsAppEcucPartitionRef Warning: Do not forget to adjust relative paths if needed (e.g. in SELECT-expressions).
ARTD-16387	Bug	[crypto] [SWS_BSW_00037] Main functions of un-initialized modules shall return immediately<*> !SWS_BSW_00037.png|width=620,height=100! Detailed description (how to reproduce it): In Mdl_MainFunction, according to SWS_BSW_00037, if the module is not initialized and the main function is executed then no error shall be reported and the main function shall return immediately. Preconditions: Mdl_MainFunction() is called before Mdl_Init() or Mdl_Init() is called without success. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: In case the driver is un-initialized, Mdl_MainFunction() raises a DET error or doesn't return immediately. Expected behavior: In case the driver is un-initialized, Mdl_MainFunction() doesn't raise a DET error and returns immediately. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: In the main function(s), check if the module has been initialized and return immediately if not. Don't rely on the values of un-initialized variables (besides the global driver state).

ID	Subtype	Headline and Description
ARTD-16393	Bug	[fls] [SWS_BSW_00037] Main functions of un-initialized modules shall return immediately<*> !SWS_BSW_00037.png|width=620,height=100! Detailed description (how to reproduce it): In Mdl_MainFunction, according to SWS_BSW_00037, if the module is not initialized and the main function is executed then no error shall be reported and the main function shall return immediately. Preconditions: Mdl_MainFunction() is called before Mdl_Init() or Mdl_Init() is called without success. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: In case the driver is un-initialized, Mdl_MainFunction() raises a DET error or doesn't return immediately. Expected behavior: In case the driver is un-initialized, Mdl_MainFunction() doesn't raise a DET error and returns immediately. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: In the main function(s), check if the module has been initialized and return immediately if not. Don't rely on the values of un-initialized variables (besides the global driver state).
ARTD-16381	New	New Feature [S32K3XX][S32K3XX] (ITG) Add fault label to support testing side create test fault ,,"NewWorkDescription: The CPXNUM register has 32 bitfields but the actual data value is only 2 bit => The data filed from CPXNUM register is masked before data is recorded by MSCM_CPXNUM_CPN_MASK The value read from the CPXNUM register is always 2 bit, so testing side need a support form driver to check MSCM_CPXNUM_CPN_MASK by add a fault label in driver code. Requirement source: Requirement [CPR_RTD_00285]: Before recording the data read from a register, the driver shall filter the value read from the data register clearing all bit values that do not belong in the actual data bitfield. Configured data alignment in the register shall also be considered. (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: after reading the value from the CPXNUM register add fault lable: MCAL_FAULT_INJECTION_POINT(<manual_name>); mask by MSCM_CPXNUM_CPN_MASK Note: MCAL_FAULT_INJECTION_POINT defined in ""Mcal.h"" Eg: !image-2021-09-06-11-00-10-769.png! Change to: !image-2021-09-06-11-01-33-671.png!"

ID	Subtype	Headline and Description
ARTD-16382	Bug	[RM] Diff output CT and EB<*> Detailed description (how to reproduce it): See more pictures in attachment Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: diff output of EB with CT Expected behavior: Same output of EB with CT Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Fix for same output between EB and CT !image-2021-09-06-10-37-33-889.png|thumbnail! !image-2021-09-06-10-43-52-052.png|thumbnail! ! image-2021-09-06-10-45-36-157.png|thumbnail! !image-2021-09-06-10-50-48-077.png|thumbnail! !image-2021-09-06-10-58-06-267.png|thumbnail! ! image-2021-09-06-11-00-39-791.png|thumbnail! !image-2021-09-06-11-01-23-997.png|thumbnail! !image-2021-09-06-11-01-52-012.png|thumbnail! ! image-2021-09-06-11-02-30-654.png|thumbnail!
ARTD-16373	Bug	[S32K3XX][I2C][S32CT] do not accept NULL_PTR value in I2c Callback and I2c Error Callback node on S32CT as Ebt<*> Detailed description (how to reproduce it): [...] create a K3XX project on S32DS and add I2c_cdd module. and enable I2c callback and i2c error callback too. Expect: In fields of them don't accept NULL_PTR value as EBT Preconditions: [...] N/A Test Case ID (internal TC that caught the defect) optional: [...] N/A Observed behavior: [...] In fields of them accept NULL_PTR value Expected behavior: [...] Expect: In fields of them don't accept NULL_PTR value as EBT Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) N/A Proposed solution optional: [...]N/A

ID	Subtype	Headline and Description
ARTD-16375	Bug	[CAN] Ip_Flexcan fails to return out-of-range status / enabled fd / s32k312<*> Detailed description (how to reproduce it): Initialize Flexcan_0/s32k312/IPL with invalid maxmb value: payload 16, maxmb = 43 Verificaition point: FlexCAN_Ip_Init return FLEXCAN_STATUS_BUFF_OUT_OF_RANGE => fail at this step Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Ip_FlexCAN_TC_FCT_2080 Observed behavior: behavior does not match requirement Expected behavior: driver should return out-of-range status Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-16402	Bug	[SENT] Fix run fail on sent example<*> Detailed description (how to reproduce it): There are some sent example failed on run Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: All example are passed Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Debug and investigate problem of sent example
ARTD-16399	Bug	[ADC] Update driver according to some requirements with Verification Criteria is "Review" implemented differently ,,"After complete to Review all the requirements with Verification Criteria is ""Review"", I found some requirement implemented different to the expectation due to the description did not match, missing condition to check dependency node, attribute was set to ReadOnly... Check the excel for further information and fixed if needed

ID	Subtype	Headline and Description
ARTD-16405	New	New Feature [BASE] Add new header files for S32K314 and S32K324 ,,"NewWorkDescription: Add new header files for S32K314 and S32K324 Requirement source: RM rev 2 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional:"
ARTD-16409	Bug	[ICU][S32K3XX] The function Icu_GetPulseWidth is not working<*> In the function Icu_GetPulseWidth, the sub function Icu_ValidateSignalMeasureWithoutInterrupt is to check the condition of node IcuSignalMeasureWithoutInterrupt, when this node is ON but the macro ICU_GET_PULSE_WIDTH_API guarded to use the function Icu_GetPulseWidth still be STD_OFF. So this function can not be used. !image-2021-09-06-17-12-59-734.png! And the function Icu_GetPulseWidth is misssing the ipw layer function Icu_Ipw_GetPulseWidth. o user can not use it. !image-2021-09-06-17-19-31-292.png!
ARTD-16425	New	New Feature [crypto] Review changes according new Header files (S32K314/S32K324, RM Rev.2)" ,,"Review changes according to new header files for S32K314 and S32K324 Update drivers (if needed) Remember to update on UM/ IM in quality documentation ticket Reference: Base tag: *PVT_BASE_S32K3_1.0.0_V23 Base commit: [https://bitbucket.sw.nxp.com/projects/ARTD/repos/base/commits/91fb682863c2717eba1fc8e0135cbf9f7549a5f6] Reference Manual document: S32K3xx Reference Manual, Rev. 2, 08/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FS32K3xx%5FRM%5FRev2%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM] S32K3xx Data Sheet, Rev. 2 - 08/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FS32K3xx%5FDS%5FRev2%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS]

ID	Subtype	Headline and Description
ARTD-16427	New	New Feature [eth] Review changes according new Header files (S32K314/S32K324, RM Rev.2)" ,,"Review changes according to new header files for S32K314 and S32K324 Update drivers (if needed) Remember to update on UM/ IM in quality documentation ticket Reference: Base tag: *PVT_BASE_S32K3_1.0.0_V23 Base commit: [https://bitbucket.sw.nxp.com/projects/ARTD/repos/base/commits/91fb682863c2717eba1fc8e0135cbf9f7549a5f6] Reference Manual document: S32K3xx Reference Manual, Rev. 2, 08/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FS32K3xx%5FRM%5FRev2%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM] S32K3xx Data Sheet, Rev. 2 - 08/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FS32K3xx%5FDS%5FRev2%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS]
ARTD-16430	New	New Feature [gpt] Review changes according new Header files (S32K314/S32K324, RM Rev.2)" ,,"Review changes according to new header files for S32K314 and S32K324 Update drivers (if needed) Remember to update on UM/ IM in quality documentation ticket Reference: Base tag: *PVT_BASE_S32K3_1.0.0_V23 Base commit: [https://bitbucket.sw.nxp.com/projects/ARTD/repos/base/commits/91fb682863c2717eba1fc8e0135cbf9f7549a5f6] Reference Manual document: S32K3xx Reference Manual, Rev. 2, 08/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FS32K3xx%5FRM%5FRev2%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM] S32K3xx Data Sheet, Rev. 2 - 08/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FS32K3xx%5FDS%5FRev2%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS]

ID	Subtype	Headline and Description
ARTD-16431	New	New Feature [i2c] Review changes according new Header files (S32K314/S32K324, RM Rev.2)" ,,"Review changes according to new header files for S32K314 and S32K324 Update drivers (if needed) Remember to update on UM/ IM in quality documentation ticket Reference: Base tag: *PVT_BASE_S32K3_1.0.0_V23 Base commit: [https://bitbucket.sw.nxp.com/projects/ARTD/repos/base/commits/91fb682863c2717eba1fc8e0135cbf9f7549a5f6] Reference Manual document: S32K3xx Reference Manual, Rev. 2, 08/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FS32K3xx%5FRM%5FRev2%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM] S32K3xx Data Sheet, Rev. 2 - 08/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FS32K3xx%5FDS%5FRev2%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS]
ARTD-16433	New	New Feature [icu] Review changes according new Header files (S32K314/S32K324, RM Rev.2)" ,,"Review changes according to new header files for S32K314 and S32K324 Update drivers (if needed) Remember to update on UM/ IM in quality documentation ticket Reference: Base tag: *PVT_BASE_S32K3_1.0.0_V23 Base commit: [https://bitbucket.sw.nxp.com/projects/ARTD/repos/base/commits/91fb682863c2717eba1fc8e0135cbf9f7549a5f6] Reference Manual document: S32K3xx Reference Manual, Rev. 2, 08/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FS32K3xx%5FRM%5FRev2%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM] S32K3xx Data Sheet, Rev. 2 - 08/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FS32K3xx%5FDS%5FRev2%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS]

ID	Subtype	Headline and Description
ARTD-16438	New	New Feature [platform] Review changes according new Header files (S32K314/S32K324, RM Rev.2)" ,,"Review changes according to new header files for S32K314 and S32K324 Update drivers (if needed) Remember to update on UM/ IM in quality documentation ticket Reference: Base tag: *PVT_BASE_S32K3_1.0.0_V23 Base commit: [https://bitbucket.sw.nxp.com/projects/ARTD/repos/base/commits/91fb682863c2717eba1fc8e0135cbf9f7549a5f6] Reference Manual document: S32K3xx Reference Manual, Rev. 2, 08/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FS32K3xx%5FRM%5FRev2%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM] S32K3xx Data Sheet, Rev. 2 - 08/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FS32K3xx%5FDS%5FRev2%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS]
ARTD-16439	New	New Feature [port] Review changes according new Header files (S32K314/S32K324, RM Rev.2)" ,,"Review changes according to new header files for S32K314 and S32K324 Update drivers (if needed) Remember to update on UM/ IM in quality documentation ticket Reference: Base tag: *PVT_BASE_S32K3_1.0.0_V23 Base commit: [https://bitbucket.sw.nxp.com/projects/ARTD/repos/base/commits/91fb682863c2717eba1fc8e0135cbf9f7549a5f6] Reference Manual document: S32K3xx Reference Manual, Rev. 2, 08/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FS32K3xx%5FRM%5FRev2%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM] S32K3xx Data Sheet, Rev. 2 - 08/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FS32K3xx%5FDS%5FRev2%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS]

ID	Subtype	Headline and Description
ARTD-16443	New	New Feature [sent] Review changes according new Header files (S32K314/S32K324, RM Rev.2)" ,,"Review changes according to new header files for S32K314 and S32K324 Update drivers (if needed) Remember to update on UM/ IM in quality documentation ticket Reference: Base tag: *PVT_BASE_S32K3_1.0.0_V23 Base commit: [https://bitbucket.sw.nxp.com/projects/ARTD/repos/base/commits/91fb682863c2717eba1fc8e0135cbf9f7549a5f6] Reference Manual document: S32K3xx Reference Manual, Rev. 2, 08/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FS32K3xx%5FRM%5FRev2%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM] S32K3xx Data Sheet, Rev. 2 - 08/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FS32K3xx%5FDS%5FRev2%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS]
ARTD-16444	New	New Feature [spi] Review changes according new Header files (S32K314/S32K324, RM Rev.2)" ,,"Review changes according to new header files for S32K314 and S32K324 Update drivers (if needed) Remember to update on UM/ IM in quality documentation ticket Reference: Base tag: *PVT_BASE_S32K3_1.0.0_V23 Base commit: [https://bitbucket.sw.nxp.com/projects/ARTD/repos/base/commits/91fb682863c2717eba1fc8e0135cbf9f7549a5f6] Reference Manual document: S32K3xx Reference Manual, Rev. 2, 08/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FS32K3xx%5FRM%5FRev2%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM] S32K3xx Data Sheet, Rev. 2 - 08/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FS32K3xx%5FDS%5FRev2%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS]

ID	Subtype	Headline and Description

ARTD-16449	New	New Feature
		
		[base] All trusted functions should NOT defined as static or inline functions and should listed out in IM
		,,"NewWorkDescription:
		There are some points that need to be checked in each modules:
		1. All trusted functions should NOT defined as static or inline functions*, so OS Application can be able to call them from outside RTD drivers.
		Check in driver code all IP functions that needs to be called as trusted functions using macros OsIf_Trusted_Call[_Return][1-6params].
		Ensure these functions are defined without ""static"" or ""inline"" keywords, so OS Application can use ""extern"" keyword to declare and call them outside RTD drivers.
		For example:
		a. OsIf_Trusted_Call1param(*Adc_Sar_ClrUserAccessAllowed*, pBase);
		Adc_Sar_ClrUserAccessAllowed() function should be defined without ""static"" or ""inline"" as:
		void Adc_Sar_ClrUserAccessAllowed(const ADC_Type const pBase)
		{
		CLR_USER_ACCESS_ALLOWED((uint32)pBase, SAR_ADC_PROT_MEM_U32);
		}
		b. OsIf_Trusted_Call_Return1param(*C40_Ip_SetLockProtect*, Fls_VirtualSector);
		C40_Ip_SetLockProtect() function should be defined without ""static"" or ""inline"" as:
		C40_Ip_StatusType C40_Ip_SetLockProtect(C40_Ip_VirtualSectorsType Fls_VirtualSector)
		{
		}
		2. Create a new separate header file <IpName>_Ip_TrustedFunctions.h for each IPV has trusted functions, the AutosarOS just needs to include this new header file when user mode is used.
		In <IpName>_Ip_TrustedFunctions.h:
		Declare all trusted functions with ""extern"" keyword like:
		extern void C40_Ip_SetLockProtect(C40_Ip_VirtualSectorsType Fls_VirtualSector);
		Include all header files contain the definition of all types which are used by parameters or return type of those trusted functions.
		3. All these trusted functions need to be configured in OS, so they must be clearly listed in the driver IM (chapter 5.7 User Mode Support)
		List these functions follow guiding mentioned in slide 17 Coding RTD_RunningInUserMode.pptx
		All functions should be listed out in the table like:
		Function syntax||Description||Available via
		void C40_Ip_SetLockProtect(
		C40_Ip_VirtualSectorsType Fls_VirtualSector
		)|Set lock bit for flash sectors|C40_Ip_TrustedFunctions.h
		4. Subchapter ""*User Mode configuration in AutosarOS*"" needs to be added in IM:
		!image-2021-08-19-09-26-20-823.png|thumbnail!
		In order to add this subchapter, there are 2 files added in build_env: user_mode_support.dox, user_mode_config_in_autosar_os.dox (added on the ticket ARTD-15466).
		In module repository, each module needs to rename from user_mode_support*.dox to user_mode_config_in_module*.dox and also its title from ""*User Mode support*"" to ""*User Mode configuration in the module*"".
		Please refer the silde [Coding RTD_RunningInUserMode.pptx|https://nxp1.sharepoint.com/:p:/r/sites/Zebra/Shared%20Documents/General/Zebra%20Training/Coding%20-%20RTD_RunningInUserMode.pptx?d=w21c9578fff794ff387db07a106880274&csf=1&web=1&e=lpbnNC] to understand more about User mode implementation in RTD.
		For Testing side*: Ensure that we have test scenarios mentioned from slides 22->25 Coding RTD_RunningInUserMode.pptx. Follow slide 23 to ensure we have one test suite to check all trusted functions able to call from outside RTD drivers.
		Refer to the implementation example on FLS:* ARTD-15610
		Requirement source:
		RTD implementation
		(e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...)
		Proposed solution optional:
		Follow Coding RTD_RunningInUserMode.pptx"

ID	Subtype	Headline and Description

ARTD-16450	New	New Feature
		
		[platform] All trusted functions should NOT defined as static or inline functions and should listed out in IM
		,,"NewWorkDescription:
		There are some points that need to be checked in each modules:
		1. All trusted functions should NOT defined as static or inline functions*, so OS Application can be able to call them from outside RTD drivers.
		Check in driver code all IP functions that needs to be called as trusted functions using macros OsIf_Trusted_Call[_Return][1-6params].
		Ensure these functions are defined without ""static"" or ""inline"" keywords, so OS Application can use ""extern"" keyword to declare and call them outside RTD drivers.
		For example:
		a. OsIf_Trusted_Call1param(*Adc_Sar_ClrUserAccessAllowed*, pBase);
		Adc_Sar_ClrUserAccessAllowed() function should be defined without ""static"" or ""inline"" as:
		void Adc_Sar_ClrUserAccessAllowed(const ADC_Type const pBase)
		{
		CLR_USER_ACCESS_ALLOWED((uint32)pBase, SAR_ADC_PROT_MEM_U32);
		}
		b. OsIf_Trusted_Call_Return1param(*C40_Ip_SetLockProtect*, Fls_VirtualSector);
		C40_Ip_SetLockProtect() function should be defined without ""static"" or ""inline"" as:
		C40_Ip_StatusType C40_Ip_SetLockProtect(C40_Ip_VirtualSectorsType Fls_VirtualSector)
		{
		}
		2. Create a new separate header file <IpName>_Ip_TrustedFunctions.h for each IPV has trusted functions, the AutosarOS just needs to include this new header file when user mode is used.
		In <IpName>_Ip_TrustedFunctions.h:
		Declare all trusted functions with ""extern"" keyword like:
		extern void C40_Ip_SetLockProtect(C40_Ip_VirtualSectorsType Fls_VirtualSector);
		Include all header files contain the definition of all types which are used by parameters or return type of those trusted functions.
		3. All these trusted functions need to be configured in OS, so they must be clearly listed in the driver IM (chapter 5.7 User Mode Support)
		List these functions follow guiding mentioned in slide 17 Coding RTD_RunningInUserMode.pptx
		All functions should be listed out in the table like:
		Function syntax||Description||Available via
		void C40_Ip_SetLockProtect(
		C40_Ip_VirtualSectorsType Fls_VirtualSector
		)|Set lock bit for flash sectors|C40_Ip_TrustedFunctions.h
		4. Subchapter ""*User Mode configuration in AutosarOS*"" needs to be added in IM:
		!image-2021-08-19-09-26-20-823.png|thumbnail!
		In order to add this subchapter, there are 2 files added in build_env: user_mode_support.dox, user_mode_config_in_autosar_os.dox (added on the ticket ARTD-15466).
		In module repository, each module needs to rename from user_mode_support*.dox to user_mode_config_in_module*.dox and also its title from ""*User Mode support*"" to ""*User Mode configuration in the module*"".
		Please refer the silde [Coding RTD_RunningInUserMode.pptx|https://nxp1.sharepoint.com/:p:/r/sites/Zebra/Shared%20Documents/General/Zebra%20Training/Coding%20-%20RTD_RunningInUserMode.pptx?d=w21c9578fff794ff387db07a106880274&csf=1&web=1&e=lpbnNC] to understand more about User mode implementation in RTD.
		For Testing side*: Ensure that we have test scenarios mentioned from slides 22->25 Coding RTD_RunningInUserMode.pptx. Follow slide 23 to ensure we have one test suite to check all trusted functions able to call from outside RTD drivers.
		Refer to the implementation example on FLS:* ARTD-15610
		Requirement source:
		RTD implementation
		(e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...)
		Proposed solution optional:
		Follow Coding RTD_RunningInUserMode.pptx"

ID	Subtype	Headline and Description

ARTD-16456	New	New Feature
		
		[spi] All trusted functions should NOT defined as static or inline functions and should listed out in IM
		,,"NewWorkDescription:
		There are some points that need to be checked in each modules:
		1. All trusted functions should NOT defined as static or inline functions*, so OS Application can be able to call them from outside RTD drivers.
		Check in driver code all IP functions that needs to be called as trusted functions using macros OsIf_Trusted_Call[_Return][1-6params].
		Ensure these functions are defined without ""static"" or ""inline"" keywords, so OS Application can use ""extern"" keyword to declare and call them outside RTD drivers.
		For example:
		a. OsIf_Trusted_Call1param(*Adc_Sar_ClrUserAccessAllowed*, pBase);
		Adc_Sar_ClrUserAccessAllowed() function should be defined without ""static"" or ""inline"" as:
		void Adc_Sar_ClrUserAccessAllowed(const ADC_Type const pBase)
		{
		CLR_USER_ACCESS_ALLOWED((uint32)pBase, SAR_ADC_PROT_MEM_U32);
		}
		b. OsIf_Trusted_Call_Return1param(*C40_Ip_SetLockProtect*, Fls_VirtualSector);
		C40_Ip_SetLockProtect() function should be defined without ""static"" or ""inline"" as:
		C40_Ip_StatusType C40_Ip_SetLockProtect(C40_Ip_VirtualSectorsType Fls_VirtualSector)
		{
		}
		2. Create a new separate header file <IpName>_Ip_TrustedFunctions.h for each IPV has trusted functions, the AutosarOS just needs to include this new header file when user mode is used.
		In <IpName>_Ip_TrustedFunctions.h:
		Declare all trusted functions with ""extern"" keyword like:
		extern void C40_Ip_SetLockProtect(C40_Ip_VirtualSectorsType Fls_VirtualSector);
		Include all header files contain the definition of all types which are used by parameters or return type of those trusted functions.
		3. All these trusted functions need to be configured in OS, so they must be clearly listed in the driver IM (chapter 5.7 User Mode Support)
		List these functions follow guiding mentioned in slide 17 Coding RTD_RunningInUserMode.pptx
		All functions should be listed out in the table like:
		Function syntax||Description||Available via
		void C40_Ip_SetLockProtect(
		C40_Ip_VirtualSectorsType Fls_VirtualSector
		)|Set lock bit for flash sectors|C40_Ip_TrustedFunctions.h
		4. Subchapter ""*User Mode configuration in AutosarOS*"" needs to be added in IM:
		!image-2021-08-19-09-26-20-823.png|thumbnail!
		In order to add this subchapter, there are 2 files added in build_env: user_mode_support.dox, user_mode_config_in_autosar_os.dox (added on the ticket ARTD-15466).
		In module repository, each module needs to rename from user_mode_support*.dox to user_mode_config_in_module*.dox and also its title from ""*User Mode support*"" to ""*User Mode configuration in the module*"".
		Please refer the silde [Coding RTD_RunningInUserMode.pptx|https://nxp1.sharepoint.com/:p:/r/sites/Zebra/Shared%20Documents/General/Zebra%20Training/Coding%20-%20RTD_RunningInUserMode.pptx?d=w21c9578fff794ff387db07a106880274&csf=1&web=1&e=lpbnNC] to understand more about User mode implementation in RTD.
		For Testing side*: Ensure that we have test scenarios mentioned from slides 22->25 Coding RTD_RunningInUserMode.pptx. Follow slide 23 to ensure we have one test suite to check all trusted functions able to call from outside RTD drivers.
		Refer to the implementation example on FLS:* ARTD-15610
		Requirement source:
		RTD implementation
		(e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...)
		Proposed solution optional:
		Follow Coding RTD_RunningInUserMode.pptx"

Release notes		

ID	Subtype	Headline and Description

ARTD-16457	New	New Feature
		
		[i2c] All trusted functions should NOT defined as static or inline functions and should listed out in IM
		,,"NewWorkDescription:
		There are some points that need to be checked in each modules:
		1. All trusted functions should NOT defined as static or inline functions*, so OS Application can be able to call them from outside RTD drivers.
		Check in driver code all IP functions that needs to be called as trusted functions using macros OsIf_Trusted_Call[_Return][1-6params].
		Ensure these functions are defined without ""static"" or ""inline"" keywords, so OS Application can use ""extern"" keyword to declare and call them outside RTD drivers.
		For example:
		a. OsIf_Trusted_Call1param(*Adc_Sar_ClrUserAccessAllowed*, pBase);
		Adc_Sar_ClrUserAccessAllowed() function should be defined without ""static"" or ""inline"" as:
		void Adc_Sar_ClrUserAccessAllowed(const ADC_Type const pBase)
		{
		CLR_USER_ACCESS_ALLOWED((uint32)pBase, SAR_ADC_PROT_MEM_U32);
		}
		b. OsIf_Trusted_Call_Return1param(*C40_Ip_SetLockProtect*, Fls_VirtualSector);
		C40_Ip_SetLockProtect() function should be defined without ""static"" or ""inline"" as:
		C40_Ip_StatusType C40_Ip_SetLockProtect(C40_Ip_VirtualSectorsType Fls_VirtualSector)
		{
		}
		2. Create a new separate header file <IpName>_Ip_TrustedFunctions.h for each IPV has trusted functions, the AutosarOS just needs to include this new header file when user mode is used.
		In <IpName>_Ip_TrustedFunctions.h:
		Declare all trusted functions with ""extern"" keyword like:
		extern void C40_Ip_SetLockProtect(C40_Ip_VirtualSectorsType Fls_VirtualSector);
		Include all header files contain the definition of all types which are used by parameters or return type of those trusted functions.
		3. All these trusted functions need to be configured in OS, so they must be clearly listed in the driver IM (chapter 5.7 User Mode Support)
		List these functions follow guiding mentioned in slide 17 Coding RTD_RunningInUserMode.pptx
		All functions should be listed out in the table like:
		Function syntax||Description||Available via
		void C40_Ip_SetLockProtect(
		C40_Ip_VirtualSectorsType Fls_VirtualSector
		)|Set lock bit for flash sectors|C40_Ip_TrustedFunctions.h
		4. Subchapter ""*User Mode configuration in AutosarOS*"" needs to be added in IM:
		!image-2021-08-19-09-26-20-823.png|thumbnail!
		In order to add this subchapter, there are 2 files added in build_env: user_mode_support.dox, user_mode_config_in_autosar_os.dox (added on the ticket ARTD-15466).
		In module repository, each module needs to rename from user_mode_support*.dox to user_mode_config_in_module*.dox and also its title from ""*User Mode support*"" to ""*User Mode configuration in the module*"".
		Please refer the silde [Coding RTD_RunningInUserMode.pptx|https://nxp1.sharepoint.com/:p:/r/sites/Zebra/Shared%20Documents/General/Zebra%20Training/Coding%20-%20RTD_RunningInUserMode.pptx?d=w21c9578fff794ff387db07a106880274&csf=1&web=1&e=lpbnNC] to understand more about User mode implementation in RTD.
		For Testing side*: Ensure that we have test scenarios mentioned from slides 22->25 Coding RTD_RunningInUserMode.pptx. Follow slide 23 to ensure we have one test suite to check all trusted functions able to call from outside RTD drivers.
		Refer to the implementation example on FLS:* ARTD-15610
		Requirement source:
		RTD implementation
		(e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...)
		Proposed solution optional:
		Follow Coding RTD_RunningInUserMode.pptx"

Release notes		

ID	Subtype	Headline and Description

ARTD-16458	New	New Feature
		
		[lin] All trusted functions should NOT defined as static or inline functions and should listed out in IM
		,,"NewWorkDescription:
		There are some points that need to be checked in each modules:
		1. All trusted functions should NOT defined as static or inline functions*, so OS Application can be able to call them from outside RTD drivers.
		Check in driver code all IP functions that needs to be called as trusted functions using macros OsIf_Trusted_Call[_Return][1-6params].
		Ensure these functions are defined without ""static"" or ""inline"" keywords, so OS Application can use ""extern"" keyword to declare and call them outside RTD drivers.
		For example:
		a. OsIf_Trusted_Call1param(*Adc_Sar_ClrUserAccessAllowed*, pBase);
		Adc_Sar_ClrUserAccessAllowed() function should be defined without ""static"" or ""inline"" as:
		void Adc_Sar_ClrUserAccessAllowed(const ADC_Type const pBase)
		{
		CLR_USER_ACCESS_ALLOWED((uint32)pBase, SAR_ADC_PROT_MEM_U32);
		}
		b. OsIf_Trusted_Call_Return1param(*C40_Ip_SetLockProtect*, Fls_VirtualSector);
		C40_Ip_SetLockProtect() function should be defined without ""static"" or ""inline"" as:
		C40_Ip_StatusType C40_Ip_SetLockProtect(C40_Ip_VirtualSectorsType Fls_VirtualSector)
		{
		}
		2. Create a new separate header file <IpName>_Ip_TrustedFunctions.h for each IPV has trusted functions, the AutosarOS just needs to include this new header file when user mode is used.
		In <IpName>_Ip_TrustedFunctions.h:
		Declare all trusted functions with ""extern"" keyword like:
		extern void C40_Ip_SetLockProtect(C40_Ip_VirtualSectorsType Fls_VirtualSector);
		Include all header files contain the definition of all types which are used by parameters or return type of those trusted functions.
		3. All these trusted functions need to be configured in OS, so they must be clearly listed in the driver IM (chapter 5.7 User Mode Support)
		List these functions follow guiding mentioned in slide 17 Coding RTD_RunningInUserMode.pptx
		All functions should be listed out in the table like:
		Function syntax||Description||Available via
		void C40_Ip_SetLockProtect(
		C40_Ip_VirtualSectorsType Fls_VirtualSector
		)|Set lock bit for flash sectors|C40_Ip_TrustedFunctions.h
		4. Subchapter ""*User Mode configuration in AutosarOS*"" needs to be added in IM:
		!image-2021-08-19-09-26-20-823.png|thumbnail!
		In order to add this subchapter, there are 2 files added in build_env: user_mode_support.dox, user_mode_config_in_autosar_os.dox (added on the ticket ARTD-15466).
		In module repository, each module needs to rename from user_mode_support*.dox to user_mode_config_in_module*.dox and also its title from ""*User Mode support*"" to ""*User Mode configuration in the module*"".
		Please refer the silde [Coding RTD_RunningInUserMode.pptx|https://nxp1.sharepoint.com/:p:/r/sites/Zebra/Shared%20Documents/General/Zebra%20Training/Coding%20-%20RTD_RunningInUserMode.pptx?d=w21c9578fff794ff387db07a106880274&csf=1&web=1&e=lpbnNC] to understand more about User mode implementation in RTD.
		For Testing side*: Ensure that we have test scenarios mentioned from slides 22->25 Coding RTD_RunningInUserMode.pptx. Follow slide 23 to ensure we have one test suite to check all trusted functions able to call from outside RTD drivers.
		Refer to the implementation example on FLS:* ARTD-15610
		Requirement source:
		RTD implementation
		(e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...)
		Proposed solution optional:
		Follow Coding RTD_RunningInUserMode.pptx"

ID	Subtype	Headline and Description

ARTD-16460	New	New Feature
		
		[uart] All trusted functions should NOT defined as static or inline functions and should listed out in IM
		,,"NewWorkDescription:
		There are some points that need to be checked in each modules:
		1. All trusted functions should NOT defined as static or inline functions*, so OS Application can be able to call them from outside RTD drivers.
		Check in driver code all IP functions that needs to be called as trusted functions using macros OsIf_Trusted_Call[_Return][1-6params].
		Ensure these functions are defined without ""static"" or ""inline"" keywords, so OS Application can use ""extern"" keyword to declare and call them outside RTD drivers.
		For example:
		a. OsIf_Trusted_Call1param(*Adc_Sar_ClrUserAccessAllowed*, pBase);
		Adc_Sar_ClrUserAccessAllowed() function should be defined without ""static"" or ""inline"" as:
		void Adc_Sar_ClrUserAccessAllowed(const ADC_Type const pBase)
		{
		CLR_USER_ACCESS_ALLOWED((uint32)pBase, SAR_ADC_PROT_MEM_U32);
		}
		b. OsIf_Trusted_Call_Return1param(*C40_Ip_SetLockProtect*, Fls_VirtualSector);
		C40_Ip_SetLockProtect() function should be defined without ""static"" or ""inline"" as:
		C40_Ip_StatusType C40_Ip_SetLockProtect(C40_Ip_VirtualSectorsType Fls_VirtualSector)
		{
		}
		2. Create a new separate header file <IpName>_Ip_TrustedFunctions.h for each IPV has trusted functions, the AutosarOS just needs to include this new header file when user mode is used.
		In <IpName>_Ip_TrustedFunctions.h:
		Declare all trusted functions with ""extern"" keyword like:
		extern void C40_Ip_SetLockProtect(C40_Ip_VirtualSectorsType Fls_VirtualSector);
		Include all header files contain the definition of all types which are used by parameters or return type of those trusted functions.
		3. All these trusted functions need to be configured in OS, so they must be clearly listed in the driver IM (chapter 5.7 User Mode Support)
		List these functions follow guiding mentioned in slide 17 Coding RTD_RunningInUserMode.pptx
		All functions should be listed out in the table like:
		Function syntax||Description||Available via
		void C40_Ip_SetLockProtect(
		C40_Ip_VirtualSectorsType Fls_VirtualSector
		)|Set lock bit for flash sectors|C40_Ip_TrustedFunctions.h
		4. Subchapter ""*User Mode configuration in AutosarOS*"" needs to be added in IM:
		!image-2021-08-19-09-26-20-823.png|thumbnail!
		In order to add this subchapter, there are 2 files added in build_env: user_mode_support.dox, user_mode_config_in_autosar_os.dox (added on the ticket ARTD-15466).
		In module repository, each module needs to rename from user_mode_support*.dox to user_mode_config_in_module*.dox and also its title from ""*User Mode support*"" to ""*User Mode configuration in the module*"".
		Please refer the silde [Coding RTD_RunningInUserMode.pptx|https://nxp1.sharepoint.com/:p:/r/sites/Zebra/Shared%20Documents/General/Zebra%20Training/Coding%20-%20RTD_RunningInUserMode.pptx?d=w21c9578fff794ff387db07a106880274&csf=1&web=1&e=lpbnNC] to understand more about User mode implementation in RTD.
		For Testing side*: Ensure that we have test scenarios mentioned from slides 22->25 Coding RTD_RunningInUserMode.pptx. Follow slide 23 to ensure we have one test suite to check all trusted functions able to call from outside RTD drivers.
		Refer to the implementation example on FLS:* ARTD-15610
		Requirement source:
		RTD implementation
		(e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...)
		Proposed solution optional:
		Follow Coding RTD_RunningInUserMode.pptx"

Release notes		

ID	Subtype	Headline and Description

ARTD-16464	New	New Feature
		
		[rm] All trusted functions should NOT defined as static or inline functions and should listed out in IM
		,,"NewWorkDescription:
		There are some points that need to be checked in each modules:
		1. All trusted functions should NOT defined as static or inline functions*, so OS Application can be able to call them from outside RTD drivers.
		Check in driver code all IP functions that needs to be called as trusted functions using macros OsIf_Trusted_Call[_Return][1-6params].
		Ensure these functions are defined without ""static"" or ""inline"" keywords, so OS Application can use ""extern"" keyword to declare and call them outside RTD drivers.
		For example:
		a. OsIf_Trusted_Call1param(*Adc_Sar_ClrUserAccessAllowed*, pBase);
		Adc_Sar_ClrUserAccessAllowed() function should be defined without ""static"" or ""inline"" as:
		void Adc_Sar_ClrUserAccessAllowed(const ADC_Type const pBase)
		{
		CLR_USER_ACCESS_ALLOWED((uint32)pBase, SAR_ADC_PROT_MEM_U32);
		}
		b. OsIf_Trusted_Call_Return1param(*C40_Ip_SetLockProtect*, Fls_VirtualSector);
		C40_Ip_SetLockProtect() function should be defined without ""static"" or ""inline"" as:
		C40_Ip_StatusType C40_Ip_SetLockProtect(C40_Ip_VirtualSectorsType Fls_VirtualSector)
		{
		}
		2. Create a new separate header file <IpName>_Ip_TrustedFunctions.h for each IPV has trusted functions, the AutosarOS just needs to include this new header file when user mode is used.
		In <IpName>_Ip_TrustedFunctions.h:
		Declare all trusted functions with ""extern"" keyword like:
		extern void C40_Ip_SetLockProtect(C40_Ip_VirtualSectorsType Fls_VirtualSector);
		Include all header files contain the definition of all types which are used by parameters or return type of those trusted functions.
		3. All these trusted functions need to be configured in OS, so they must be clearly listed in the driver IM (chapter 5.7 User Mode Support)
		List these functions follow guiding mentioned in slide 17 Coding RTD_RunningInUserMode.pptx
		All functions should be listed out in the table like:
		Function syntax||Description||Available via
		void C40_Ip_SetLockProtect(
		C40_Ip_VirtualSectorsType Fls_VirtualSector
		)|Set lock bit for flash sectors|C40_Ip_TrustedFunctions.h
		4. Subchapter ""*User Mode configuration in AutosarOS*"" needs to be added in IM:
		!image-2021-08-19-09-26-20-823.png|thumbnail!
		In order to add this subchapter, there are 2 files added in build_env: user_mode_support.dox, user_mode_config_in_autosar_os.dox (added on the ticket ARTD-15466).
		In module repository, each module needs to rename from user_mode_support*.dox to user_mode_config_in_module*.dox and also its title from ""*User Mode support*"" to ""*User Mode configuration in the module*"".
		Please refer the silde [Coding RTD_RunningInUserMode.pptx|https://nxp1.sharepoint.com/:p:/r/sites/Zebra/Shared%20Documents/General/Zebra%20Training/Coding%20-%20RTD_RunningInUserMode.pptx?d=w21c9578fff794ff387db07a106880274&csf=1&web=1&e=lpbnNC] to understand more about User mode implementation in RTD.
		For Testing side*: Ensure that we have test scenarios mentioned from slides 22->25 Coding RTD_RunningInUserMode.pptx. Follow slide 23 to ensure we have one test suite to check all trusted functions able to call from outside RTD drivers.
		Refer to the implementation example on FLS:* ARTD-15610
		Requirement source:
		RTD implementation
		(e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...)
		Proposed solution optional:
		Follow Coding RTD_RunningInUserMode.pptx"

Release notes		

ID	Subtype	Headline and Description

ARTD-16466	New	New Feature
		
		[adc] All trusted functions should NOT defined as static or inline functions and should listed out in IM
		,,"NewWorkDescription:
		There are some points that need to be checked in each modules:
		1. All trusted functions should NOT defined as static or inline functions*, so OS Application can be able to call them from outside RTD drivers.
		Check in driver code all IP functions that needs to be called as trusted functions using macros OsIf_Trusted_Call[_Return][1-6params].
		Ensure these functions are defined without ""static"" or ""inline"" keywords, so OS Application can use ""extern"" keyword to declare and call them outside RTD drivers.
		For example:
		a. OsIf_Trusted_Call1param(*Adc_Sar_ClrUserAccessAllowed*, pBase);
		Adc_Sar_ClrUserAccessAllowed() function should be defined without ""static"" or ""inline"" as:
		void Adc_Sar_ClrUserAccessAllowed(const ADC_Type const pBase)
		{
		CLR_USER_ACCESS_ALLOWED((uint32)pBase, SAR_ADC_PROT_MEM_U32);
		}
		b. OsIf_Trusted_Call_Return1param(*C40_Ip_SetLockProtect*, Fls_VirtualSector);
		C40_Ip_SetLockProtect() function should be defined without ""static"" or ""inline"" as:
		C40_Ip_StatusType C40_Ip_SetLockProtect(C40_Ip_VirtualSectorsType Fls_VirtualSector)
		{
		}
		2. Create a new separate header file <IpName>_Ip_TrustedFunctions.h for each IPV has trusted functions, the AutosarOS just needs to include this new header file when user mode is used.
		In <IpName>_Ip_TrustedFunctions.h:
		Declare all trusted functions with ""extern"" keyword like:
		extern void C40_Ip_SetLockProtect(C40_Ip_VirtualSectorsType Fls_VirtualSector);
		Include all header files contain the definition of all types which are used by parameters or return type of those trusted functions.
		3. All these trusted functions need to be configured in OS, so they must be clearly listed in the driver IM (chapter 5.7 User Mode Support)
		List these functions follow guiding mentioned in slide 17 Coding RTD_RunningInUserMode.pptx
		All functions should be listed out in the table like:
		Function syntax||Description||Available via
		void C40_Ip_SetLockProtect(
		C40_Ip_VirtualSectorsType Fls_VirtualSector
		)|Set lock bit for flash sectors|C40_Ip_TrustedFunctions.h
		4. Subchapter ""*User Mode configuration in AutosarOS*"" needs to be added in IM:
		!image-2021-08-19-09-26-20-823.png|thumbnail!
		In order to add this subchapter, there are 2 files added in build_env: user_mode_support.dox, user_mode_config_in_autosar_os.dox (added on the ticket ARTD-15466).
		In module repository, each module needs to rename from user_mode_support*.dox to user_mode_config_in_module*.dox and also its title from ""*User Mode support*"" to ""*User Mode configuration in the module*"".
		Please refer the silde [Coding RTD_RunningInUserMode.pptx|https://nxp1.sharepoint.com/:p:/r/sites/Zebra/Shared%20Documents/General/Zebra%20Training/Coding%20-%20RTD_RunningInUserMode.pptx?d=w21c9578fff794ff387db07a106880274&csf=1&web=1&e=lpbnNC] to understand more about User mode implementation in RTD.
		For Testing side*: Ensure that we have test scenarios mentioned from slides 22->25 Coding RTD_RunningInUserMode.pptx. Follow slide 23 to ensure we have one test suite to check all trusted functions able to call from outside RTD drivers.
		Refer to the implementation example on FLS:* ARTD-15610
		Requirement source:
		RTD implementation
		(e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...)
		Proposed solution optional:
		Follow Coding RTD_RunningInUserMode.pptx"

Release notes		

ID	Subtype	Headline and Description

ARTD-16476	New	New Feature
		
		[icu] All trusted functions should NOT defined as static or inline functions and should listed out in IM
		,,"NewWorkDescription:
		There are some points that need to be checked in each modules:
		1. All trusted functions should NOT defined as static or inline functions*, so OS Application can be able to call them from outside RTD drivers.
		Check in driver code all IP functions that needs to be called as trusted functions using macros OsIf_Trusted_Call[_Return][1-6params].
		Ensure these functions are defined without ""static"" or ""inline"" keywords, so OS Application can use ""extern"" keyword to declare and call them outside RTD drivers.
		For example:
		a. OsIf_Trusted_Call1param(*Adc_Sar_ClrUserAccessAllowed*, pBase);
		Adc_Sar_ClrUserAccessAllowed() function should be defined without ""static"" or ""inline"" as:
		void Adc_Sar_ClrUserAccessAllowed(const ADC_Type const pBase)
		{
		CLR_USER_ACCESS_ALLOWED((uint32)pBase, SAR_ADC_PROT_MEM_U32);
		}
		b. OsIf_Trusted_Call_Return1param(*C40_Ip_SetLockProtect*, Fls_VirtualSector);
		C40_Ip_SetLockProtect() function should be defined without ""static"" or ""inline"" as:
		C40_Ip_StatusType C40_Ip_SetLockProtect(C40_Ip_VirtualSectorsType Fls_VirtualSector)
		{
		}
		2. Create a new separate header file <IpName>_Ip_TrustedFunctions.h for each IPV has trusted functions, the AutosarOS just needs to include this new header file when user mode is used.
		In <IpName>_Ip_TrustedFunctions.h:
		Declare all trusted functions with ""extern"" keyword like:
		extern void C40_Ip_SetLockProtect(C40_Ip_VirtualSectorsType Fls_VirtualSector);
		Include all header files contain the definition of all types which are used by parameters or return type of those trusted functions.
		3. All these trusted functions need to be configured in OS, so they must be clearly listed in the driver IM (chapter 5.7 User Mode Support)
		List these functions follow guiding mentioned in slide 17 Coding RTD_RunningInUserMode.pptx
		All functions should be listed out in the table like:
		Function syntax||Description||Available via
		void C40_Ip_SetLockProtect(
		C40_Ip_VirtualSectorsType Fls_VirtualSector
		)|Set lock bit for flash sectors|C40_Ip_TrustedFunctions.h
		4. Subchapter ""*User Mode configuration in AutosarOS*"" needs to be added in IM:
		!image-2021-08-19-09-26-20-823.png|thumbnail!
		In order to add this subchapter, there are 2 files added in build_env: user_mode_support.dox, user_mode_config_in_autosar_os.dox (added on the ticket ARTD-15466).
		In module repository, each module needs to rename from user_mode_support*.dox to user_mode_config_in_module*.dox and also its title from ""*User Mode support*"" to ""*User Mode configuration in the module*"".
		Please refer the silde [Coding RTD_RunningInUserMode.pptx|https://nxp1.sharepoint.com/:p:/r/sites/Zebra/Shared%20Documents/General/Zebra%20Training/Coding%20-%20RTD_RunningInUserMode.pptx?d=w21c9578fff794ff387db07a106880274&csf=1&web=1&e=lpbnNC] to understand more about User mode implementation in RTD.
		For Testing side*: Ensure that we have test scenarios mentioned from slides 22->25 Coding RTD_RunningInUserMode.pptx. Follow slide 23 to ensure we have one test suite to check all trusted functions able to call from outside RTD drivers.
		Refer to the implementation example on FLS:* ARTD-15610
		Requirement source:
		RTD implementation
		(e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...)
		Proposed solution optional:
		Follow Coding RTD_RunningInUserMode.pptx"

ID	Subtype	Headline and Description

ARTD-16477	New	New Feature
		
		[ocu] All trusted functions should NOT defined as static or inline functions and should listed out in IM
		,,"NewWorkDescription:
		There are some points that need to be checked in each modules:
		1. All trusted functions should NOT defined as static or inline functions*, so OS Application can be able to call them from outside RTD drivers.
		Check in driver code all IP functions that needs to be called as trusted functions using macros OsIf_Trusted_Call[_Return][1-6params].
		Ensure these functions are defined without ""static"" or ""inline"" keywords, so OS Application can use ""extern"" keyword to declare and call them outside RTD drivers.
		For example:
		a. OsIf_Trusted_Call1param(*Adc_Sar_ClrUserAccessAllowed*, pBase);
		Adc_Sar_ClrUserAccessAllowed() function should be defined without ""static"" or ""inline"" as:
		void Adc_Sar_ClrUserAccessAllowed(const ADC_Type const pBase)
		{
		CLR_USER_ACCESS_ALLOWED((uint32)pBase, SAR_ADC_PROT_MEM_U32);
		}
		b. OsIf_Trusted_Call_Return1param(*C40_Ip_SetLockProtect*, Fls_VirtualSector);
		C40_Ip_SetLockProtect() function should be defined without ""static"" or ""inline"" as:
		C40_Ip_StatusType C40_Ip_SetLockProtect(C40_Ip_VirtualSectorsType Fls_VirtualSector)
		{
		}
		2. Create a new separate header file <IpName>_Ip_TrustedFunctions.h for each IPV has trusted functions, the AutosarOS just needs to include this new header file when user mode is used.
		In <IpName>_Ip_TrustedFunctions.h:
		Declare all trusted functions with ""extern"" keyword like:
		extern void C40_Ip_SetLockProtect(C40_Ip_VirtualSectorsType Fls_VirtualSector);
		Include all header files contain the definition of all types which are used by parameters or return type of those trusted functions.
		3. All these trusted functions need to be configured in OS, so they must be clearly listed in the driver IM (chapter 5.7 User Mode Support)
		List these functions follow guiding mentioned in slide 17 Coding RTD_RunningInUserMode.pptx
		All functions should be listed out in the table like:
		Function syntax||Description||Available via
		void C40_Ip_SetLockProtect(
		C40_Ip_VirtualSectorsType Fls_VirtualSector
		)|Set lock bit for flash sectors|C40_Ip_TrustedFunctions.h
		4. Subchapter ""*User Mode configuration in AutosarOS*"" needs to be added in IM:
		!image-2021-08-19-09-26-20-823.png|thumbnail!
		In order to add this subchapter, there are 2 files added in build_env: user_mode_support.dox, user_mode_config_in_autosar_os.dox (added on the ticket ARTD-15466).
		In module repository, each module needs to rename from user_mode_support*.dox to user_mode_config_in_module*.dox and also its title from ""*User Mode support*"" to ""*User Mode configuration in the module*"".
		Please refer the silde [Coding RTD_RunningInUserMode.pptx|https://nxp1.sharepoint.com/:p:/r/sites/Zebra/Shared%20Documents/General/Zebra%20Training/Coding%20-%20RTD_RunningInUserMode.pptx?d=w21c9578fff794ff387db07a106880274&csf=1&web=1&e=lpbnNC] to understand more about User mode implementation in RTD.
		For Testing side*: Ensure that we have test scenarios mentioned from slides 22->25 Coding RTD_RunningInUserMode.pptx. Follow slide 23 to ensure we have one test suite to check all trusted functions able to call from outside RTD drivers.
		Refer to the implementation example on FLS:* ARTD-15610
		Requirement source:
		RTD implementation
		(e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...)
		Proposed solution optional:
		Follow Coding RTD_RunningInUserMode.pptx"

Release notes		

ID	Subtype	Headline and Description
ARTD-16417	Bug	[ICU] There are some issues in ICU module of RTD 1.0.0 CD01.<*> Detailed description (how to reproduce it): The ICU eMIOS channel cannot select bus counter except internal counter as its bus reference. It seems that only PWM eMIOS channel can select global bus counter. !image-2021-09-07-10-04-13-272.png! When ICU eMIOS channel selects internal counter as its bus reference, the IcuEmiosBusRef should be empty, but there will be a warning. !image-2021-09-07-10-08-16-135.png! The ICU module support WKPU NMI (non-Maskable Interrupt). However, if we add an ICU channel using WKPY NMI channel before an other type ICU channel, the declaration of notification function of latter one will not be generated. That will cause errors when compile the generated code. !image-2021-09-07-10-25-33-633.png! !image-2021-09-07-10-29-29-351.png! If the NMI channel is behind the ICU eMIOS channel, the declaration of notification function will be generated normally. !image-2021-09-07-10-37-16-575.png! !image-2021-09-07-10-38-35-320.png! In Icu.c*, the is a *Icu_GetPulseWidth*() API. However, it seems that it cannot be turn on in EB. !image-2021-09-07-10-43-24-862.png! !image-2021-09-07-10-48-08-751.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-16418	Bug	[FEE] Fee_DeserializeBlockHdr returns wrong block status<*> Detailed description (how to reproduce it): cannot recover all blocks Preconditions: virtual page size = 1, foreign feature is enabled Test Case ID (internal TC that caught the defect) optional: Fee_TS_502 Observed behavior: This function returns wrong block status Expected behavior: all blocks are recovered when invoking Fee_Init Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA

ID	Subtype	Headline and Description
ARTD-16448	Bug	[Platform] Investigate cache issues when running multi core tests<*> Detailed description (how to reproduce it): 2 cores will be trapped in Eunit due to cache issue. See more in a picture, !image-2021-09-07-13-02-11-989.png|thumbnail! Preconditions: Enable multi core feature Test Case ID (internal TC that caught the defect) optional: Rm_TC_MUL_0101 Observed behavior: trap in Eunit Expected behavior: N/A Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Check configuration of MPU in startup
ARTD-16480	Bug	[ETH] Wrong address of DMA channel control registers in Gmac_Ip_Device_Registers.h<*> Detailed description (how to reproduce it): Wrong address of DMA_CHx_CONTROL_ADDR16 in Gmac_Ip_Device_Registers.h Preconditions: NA Test Case ID (internal TC that caught the defect) optional: Eth_TC_FCT_0079 Eth_TC_FCT_0087 Observed behavior: NA Expected behavior: NA Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: The address of DMA control register should be: #define DMA_CH0_CONTROL_ADDR16 0x1100U #define DMA_CH1_CONTROL_ADDR16 0x1180U

ID	Subtype	Headline and Description
ARTD-16447	Bug	[ICU][CT] There are some text matching problems causing wrong configuration.<*> Detailed description (how to reproduce it): To reproduce this issue, please follow blow steps: Add two ICU eMIOS channels named as *Icu_Channel and *Icu_Channel_Alt* respectively in IcueMios tab. Other names are also possible, but please make sure that the beginning of the second name has the same string as the first name. !image-2021-09-07-13-06-25-911.png! Add two logic channels in IcuChannels tab. The first channel select Icu_Channel_Alt as its reference and work in Signal Measurement mode, and the second channel select Icu_Channel as its reference and work in Edge Detect mode. !image-2021-09-07-13-26-27-384.png! Then, we can generate the configuration code of eMIOS ICU by pushing Update Code. We will find that the second channel is wrongly configured to Signal Measurement mode, not Edge Detect mode. See following picture: !image-2021-09-07-13-32-29-434.png! I think this issue is caused by incorrect text matching. Due to the beginning string of configured channels' names are the same, the Icu_Channel_Alt* will be wrongly regarded as *Icu_Channel when ConfigTools generates code. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-16491	Bug	[Spi] On DS can generate LPSPI_TCR_CONT(1) even though SpiCsSelection is disabled<*> Detailed description (how to reproduce it): On DS can generate LPSPI_TCR_CONT(1) even though SpiCsSelection is disabled Preconditions: SpiCsContinous is True SpiCsSelection is disable Code generate LPSPI_TCR_CONT(1) Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: NA Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA

ID	Subtype	Headline and Description
ARTD-16487	New	New Feature [Rm] Remove unused variables in DS generated files ,,"- NewWorkDescription: Some variables get from resource are not use. see picture for more detail. !image-2021-09-07-15-00-06-182.png|width=844,height=289! Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Remove unused variable"
ARTD-16493	Bug	When PTE13 work as VRC_CTRL, it shouldn't work as other functions ,,"In S32CT, when external BJT is used, the base pin(LMBCTLEN) of the external BJT which generates 1.5V should be enabled in the power module. But when this pin works as VRC_CTRL, it should not be able to set to other function such as GPIO, but in Pins configuration it can still be set to other functions. I think the configuration of the pin PTE13 should be invalid when it works as VRC_CTRL.
ARTD-16623	New	New Feature [icu] Review changes according new Header files (S32K344, RM Rev.2)" ,,"Review changes according to new header files for S32K344 Update drivers (if needed) Remember to update on UM/ IM in quality documentation ticket Reference: Base: pull-request: [https://bitbucket.sw.nxp.com/projects/ARTD/repos/base/pull-requests/665/overview] / branch: [https://bitbucket.sw.nxp.com/projects/ARTD/repos/base/browse?at=refs%2Fheads%2Ffeature%2FARTD-16542-base-update-new-header-files-for-s32k344] Platform tag: PVT_S32K3XX_S32K3_ARTD_16571_V01 Reference Manual document: S32K3xx Reference Manual, Rev. 2, 08/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FS32K3xx%5FRM%5FRev2%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM] S32K3xx Data Sheet, Rev. 2 - 08/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FS32K3xx%5FDS%5FRev2%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS]

ID	Subtype	Headline and Description
ARTD-16499	Bug	[S32K3XX][S32K3XX][RTM 1.0.0] Build failed on K312 with GHS with Ip_Clock<*> Detailed description (how to reproduce it): During update test for Timeout test with Counter Type by SYystem_Timer (using CLock initialized by MCU) Build failed found on GHS (either ver 202114 or 202014), on K312 derivative. build failed log on ceram: http://ceram.ea.freescale.net/1/project/ar_int_fls_ghs/details Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Fls_TC_FCT_7000 Observed behavior: N/A Expected behavior: N/A Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-16502	Bug	[S32K3XX][i2C]master code of highspeed mode is not correct with i2c protocol<*> Detailed description (how to reproduce it): master code of highspeed mode is not correct with i2c protocol: driver need send 0b00001XXX instead 0b00000XXX. With XXX is high-speed master code Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: master code of highspeed mode is not correct with i2c protocol: driver send 0b00000XXX. Expected behavior: driver send 0b00001XXX Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) N/A Proposed solution optional: N/A

ID	Subtype	Headline and Description
ARTD-16509	Bug	[S32K3XX][S32K3XX_100] compiler warning<*> Detailed description (how to reproduce it): 1. Build project test for platform module by Gcc compiler some warning detect in system_lp.c Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Platform_TS_001 Observed behavior: N/A Expected behavior: Checking excel file got the station for k344barents.ea.freescale.net/0/project/custom_compilerwarning/details Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-16514	New	New Feature [ICU] Change Process Interrupt function to using "for" instead of using "while"" ,,"NewWorkDescription: ChangeProcess Interrupt function to using "for" instead of using "while" for Siul2 and Wkpu Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: NA

ID	Subtype	Headline and Description
ARTD-16516	Bug	[FLS][S32K3XX] Fls_CheckLoadAc condition-check is missing in case Multiple Sectors configured<*> Detailed description (how to reproduce it): During check ccov test hardfault , it showed: Due to LDRA build characteristic: It required to make an custom linker to build acc_code_rom to map to a sector at BLOCK_3, this make sure to test could run with access_code_load to Ram feature without Read-While_Write due to auxiliary files was generated (and mapped to code sectors of Block1) If configures Multiple sector (02 sectors in test case) in boundary location(from BLOCK2_SECTOR_383 the ending sector of Block2): driver shall check the next sector (BLOCK3_SECTOR_384) is satisfied CheckLoadAc() condition and implement load access-code to RAM section, but now, it doesn't. Preconditions: LDRA build run test. Test Case ID (internal TC that caught the defect) optional: Fls_TC_FCT_1000 Observed behavior: hardfault occur due to Read-While-Write condition. Expected behavior: CheckLoadAC shall be ensure such in case multiple sectors configured , especially in Boundary configured use-case (sector from Block1 to Block2, Block2 to Block3, ...) as long as sector to test stays on the same block of AccessCode. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-16506	Bug	[UART] Timeout error in function ABORT is raised same as DMA_ERROR<*> Detailed description (how to reproduce it): [Timeout Error in function ABORT is raised same as DMA_ERROR. This is not a clear status. It's confusing in the exact error detection] Preconditions: [N/A] Test Case ID (internal TC that caught the defect) optional: [Uart_TC_WBT_0016, Uart_TC_WBT_0017] Observed behavior: [N/A] Expected behavior: [N/A] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [N/A]

ID	Subtype	Headline and Description
ARTD-16522	Bug	[S32K3XX][PORT] Generate type Siul2_Port_Ip_PinSettingsConfig missing extern const not according driver<*> Detailed description (how to reproduce it): execute test with Plugin_792021.zip, run test IP_Port_Siul2_TS_002 in IAR compiler Preconditions: the result of this test need to be same IAR, GHS, GCC (GHS, GCC pass) Test Case ID (internal TC that caught the defect) optional: IP_Port_Siul2_TC_0004/IP_Port_Siul2_TS_002 Observed behavior: Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-16525	Bug	[ADC] Need to add constraint when AdcConvTimeOnce is enable and container AdcNormalConvTimings is disable<*> Detailed description (how to reproduce it): Need to add constraint when AdcConvTimeOnce is enable and container AdcNormalConvTimings is disable Preconditions: AdcConvTimeOnce is enable Tab Hw unit container AdcNormalConvTimings is disable More detail in attachment Test Case ID (internal TC that caught the defect) optional: Adc_TC_FCT_0001-Adc_TS_009 Observed behavior: AdcConvTimeOnce is enable container AdcNormalConvTimings is disable => Real status: generate pass Expected behavior: Generate fail beacause in this case users can not configure sample time value and what the values in sample time register after calling Adc_Init Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A

ID	Subtype	Headline and Description
ARTD-16526	Bug	[ADC] Hard fault error when calling Adc_SetClockMode(ADC_ALTERNATE) with AdcEnableDualClockMode is enable and AdcAlternateConvTimings is disable<*> Detailed description (how to reproduce it): Hard fault error when calling Adc_SetClockMode(ADC_ALTERNATE) with AdcEnableDualClockMode is enable and AdcAlternateConvTimings is disable Preconditions: AdcEnableDualClockMode is enable Tab hw unit container AdcAlternateConvTimings is disable Case 1: AdcConvTimeOnce is enable (Adc_TS_008) Case 2: AdcConvTimeOnce is disable (Adc_TS_009) More detail in attachment Test Case ID (internal TC that caught the defect) optional: Adc_TC_FCT_0002 Adc_TS_008 Adc_TC_FCT_0001 Adc_TS_009 Observed behavior: Calling Adc_SetClockMode(ADC_ALTERNATE) > Real status: Hard fault error in all 2 cases Expected behavior: no hard fault error Case 1: AdcConvTimeOnce is enable > calling Adc_SetClockMode(ADC_ALTERNATE) return e_not_ok or add constraint between AdcEnableDualClockMode and container AdcAlternateConvTimings (Adc_ts_008) Case 2: AdcConvTimeOnce is disable > calling Adc_SetClockMode(ADC_ALTERNATE) return ok because configure in group tab (Adc_ts_009) Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-16531	Bug	[CRC] The input data changed on IAR compiler is different from generated file<*> Detailed description (how to reproduce it): Initialize CRC module with multicore node is enabled and 2 channels CRC16ARC non-autosar for 2 cores(see Crc.xdm file) Call the Crc_SetChannelCalculate function with CRC16ARC for two cores VERIFICATION_POINT:Data as expected Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Crc_TC_FCT_0716 Observed behavior: The input data changed on IAR compiler is different from generated file(8.50.10 version) compiler(see IAR.png file). On GHS the input data is the same from generated file(see GHS.png file) Expected behavior: The input data is the same from generated file on IAR compiler Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A

ID	Subtype	Headline and Description
ARTD-16538	Bug	[SPI]Can not config Tx, Rx, Cs, Clk channel for Flexio, DMA ,,"Detailed description (how to reproduce it): [SPI]Can not config Tx, Rx, Cs, Clk channel for Flexio, DMA Preconditions: NA Test Case ID (internal TC that caught the defect) optional: Ip_Flexio_Spi_TS_001, Ip_Flexio_Spi_TS_002, Ip_Flexio_Spi_TS_003 Observed behavior: NA Expected behavior: NA Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-16544	Bug	[ICU][S32K3XX] Error relating to Emios reference in DS interface ip layer<*> The path to refer to master bus of Emios channel is not working. !image-2021-09-09-11-18-52-970.png!
ARTD-16542	New	New Feature [BASE] Update new header files for S32K344 ,,"NewWorkDescription: Update new header files for S32K344 Requirement source: RM Rev 2 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: N/A"

ID	Subtype	Headline and Description
ARTD-16549	Bug	[S32K312] I3C clock is not enabled on AIPS_0<*> Detailed description (how to reproduce it): [...] Run I3C test on K312 board Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] I3C clock is not enabled in sys_init function. Expected behavior: [...] I3C clock is enabled in sys_init function. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...] Change value of PRTN0_COFB1_CLKEN_REQ_MASK_U32 to 0x000137DFU
ARTD-16548	Bug	[ADC] "Adc Optimize DMA Streaming Groups" is still EDITABLE when "Adc Enable DMA support" is disabled ,,"Detailed description (how to reproduce it): This node ""AdcOptimizeDmaStreamingGroups"" is EDITABLE still when ""Adc Enable DMA support"" is disabled Preconditions: NA Test Case ID (internal TC that caught the defect) optional: Adc_TS_COT_001_cfg2 Observed behavior: This node ""AdcOptimizeDmaStreamingGroups"" is EDITABLE still when ""Adc Enable DMA support"" is disabled Expected behavior: This node is EDITABLE only if ""Adc Enable DMA support"" is enabled. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA

ID	Subtype	Headline and Description
ARTD-16569	Bug	[S32K3][S32DS][OCU] Incorrect behavior in OcuHWSpecificSettings<*> Detailed description (how to reproduce it): Create a project for S32K312 and add OCU (HL) or Emios_OCU(IP) component into the project, Add and configure channel 1 and channel 10 In OcuHWSpecificSettings, change channel 1's OcuEmiosBusSelect to each of the Counter Bus change channel 10's OcuEmiosBusSelect to each of the Counter Bus Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Ip_Emios_TS_001 Observed behavior: When both channel 1 and channel 10 are in the configuration, changing channel 1's OcuHWSpecificSettings does make any change to it's generated configuration, both in Code Preview and the generated file after updating code. See picture below !image-2021-09-09-15-36-25-337.png|thumbnail! However, changing channel 10's OcuHWSpecificSettings will make changes for both channel 1 and channel 10 !image-2021-09-09-15-40-56-461.png|thumbnail! !image-2021-09-09-15-42-52-049.png|thumbnail! This behavior will persist if settings for channel 1 and channel 10-19 exist in the same configuration. It will cease if there's only channel 1. This apply to channel 2 and channel 20-23 Expected behavior: Changing settings for a specific channel should not affect the other
ARTD-16571	New	New Feature [platform] Review changes according new Header files (S32K314/S32K324, RM Rev.2)" ,,"Review changes according to new header files for S32K314 and S32K324 Update drivers (if needed) Remember to update on UM/ IM in quality documentation ticket Reference: Base tag: *PVT_BASE_S32K3_1.0.0_V23 Base commit: [https://bitbucket.sw.nxp.com/projects/ARTD/repos/base/commits/91fb682863c2717eba1fc8e0135cbf9f7549a5f6] Reference Manual document: S32K3xx Reference Manual, Rev. 2, 08/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FS32K3xx%5FRM%5FRev2%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM] S32K3xx Data Sheet, Rev. 2 - 08/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FS32K3xx%5FDS%5FRev2%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS]

ID	Subtype	Headline and Description
ARTD-16574	Bug	[S32K3 RTM] OCU: EB generate code not corect<*> Detailed description (how to reproduce it): Tag: OCU_110 Branch: develop When code generate from EB, OcuPrescale_Alternate value generated is not correct Test Case ID (internal TC that caught the defect) optional: Ocu_TC_FCT_219 in Ocu_TS_101 Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)
ARTD-16572	New	New Feature [S32CT][ECPD] Create a "literals" option for enumerations represented by dynamic_enums" ,,"NewWorkDescription: Create a "literals" option for enumerations represented by dynamic_enums. If it exists, then the values for the ECUC-ENUMERATION-LITERAL-DEF nodes will be taken from this option. Otherwise, the values will be taken from the "items" expression of the dynamic_enum. This option represents a list of "fallback" values. Update the following presentation: https://nxp1.sharepoint.com/:p:/r/sites/Zebra/Shared%20Documents/Configuration%20(code,%20DS,%20EB,%20etc)/NXP_RTD_AUTOSAR_S32CT_V2.pptx?d=w28a51ba3c45240f5abb6a6933671dcd3&csf=1&web=1&e=s8y7Hc Requirement source: N/A (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Update generateEcpd.js to implement the described behaviour.

ID	Subtype	Headline and Description
ARTD-16573	Bug	[S32K3XX] Compilation failed on S32K314<*> Detailed description (how to reproduce it): Compilation failed on S32K314 due to undeclared variable. c:/Users/nxf47222/Documents/artd-repo/output/S32K3XX_S32K314_gcc/adc/../../eclipse/plugins/Platform_TS_T40D34M10I0R0/startup/src/system.c: In function 'SystemInit': c:/Users/nxf47222/Documents/artd-repo/output/S32K3XX_S32K314_gcc/adc/../../eclipse/plugins/Platform_TS_T40D34M10I0R0/startup/src/system.c:421:32: error: 'MSCM_IRSPRC_M7_1_SHIFT' undeclared (first use in this function); did you mean 'MSCM_IRSPRC_M7_0_SHIFT'? 421 coreMask = (1UL << MSCM_IRSPRC_M7_1_SHIFT); MSCM_IRSPRC_M7_0_SHIFT c:/Users/nxf47222/Documents/artd-repo/output/S32K3XX_S32K314_gcc/adc/../../eclipse/plugins/Platform_TS_T40D34M10I0R0/startup/src/system.c:421:32: note: each undeclared identifier is reported only once for each function it appears in Makefile:1041: recipe for target `system_c.o' failed Preconditions: Build a project. Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: Compilation error. Expected behavior: No compilation error. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-16638	Bug	[Uart] Callback for Dma transfer should be enable for using<*> Detailed description (how to reproduce it): [...] Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-16684	Bug	[CRYPTO] Key derivation service fills wrong descriptor parameter<*> Detailed description (how to reproduce it): Wrong descriptor parameter is used when X963 key derivation is requested. The bug is cosmetic because the descriptor parameter that is currently used has the same type as the descriptor parameter to be used. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: The derivation service is filling the descriptor for X963 with a hash used as pseudo random function in the {{hmacHash}} instead of hash}} parameter. Expected behavior: The X963 derivation function supports only hash as pseudo random function: !image-2021-09-10-16-08-16-808.png! Because a generic type ({{hseKdfCommonParams_t}}) is used for multiple KDFs, there are more parameters than needed for X963. !image-2021-09-10-16-11-47-908.png! Even if the current code works, because the prfAlgo}} is a union and hmacHash}} has the same type as hash}}, see picture below, the code should be updated to use the right parameter hash}}. !image-2021-09-10-16-13-54-928.png! Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Swap the parameter hmacHash}} with hash}}.
ARTD-16650	New	New Feature [ICU][S32K3XX] Add file version checking ,,"NewWorkDescription: Add file version checking. Attach file shown files version have not checked yet. Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]"
ARTD-16647	New	New Feature [RM] Update driver follow update from requirements ,,"NewWorkDescription: Some requirements are updated. code need to be updated as well Ticket: AAI-940 Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: NA"

ID	Subtype	Headline and Description
ARTD-16648	New	New Feature [FLS] Update code following to Rule 29 of Naming Convention ,,"NewWorkDescription: Update local variables, function parameters and struct members using only PascalCase naming, without any special prefix Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]"
ARTD-16659	Bug	[ICU][S32K3XX] Bug directive position wrong<*> Detailed description (how to reproduce it): #endif directive position is wrong in Icu_Ipw.h !image-2021-09-10-11-51-04-365.png|width=789,height=441! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-16667	Bug	[ICU] Update and Fix after review code / design checklist<*> Detailed description (how to reproduce it): Perform review UML design/ code review against checklist. The UML checklist/ code review template and guideline are enclosed in the attachment. Preconditions: Check and update code if have violation Test Case ID (internal TC that caught the defect) optional: N/a Observed behavior: N/a Expected behavior: all violation has update Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/a

ID	Subtype	Headline and Description
ARTD-16677	Bug	[ADC] Tresos identifier "New Data DMA enable mask(dynamic range)" can't be configured. ,,"Detailed description (how to reproduce it): [The Tresos identifier ""New Data DMA enable mask(dynamic range)"" in Adc component can't be configured, and I did not find any option to enable this configuration.] Preconditions: [Enable DMA operation when new data is available in ADCnDR register of BCTU module.] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [The Tresos identifier ""New Data DMA enable mask(dynamic range)"" in Adc component can't be configured] Expected behavior: [The Tresos identifier ""New Data DMA enable mask(dynamic range)"" in Adc component can be modified] !Capture.PNG! Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-16687	Bug	[PWM] Emios_Pwm_Ip_SyncUpdate does not sync the master buses<*> Detailed description (how to reproduce it): As part of the CPR_RTD_00511.mcl MCL requirement for synchronously updating the channels and master buses. The PWM is responsible for resetting the OUDIS bit for the master buses that it controls as well. Looking at the Emios_Pwm_Ip_SyncUpdate function code, the master buses are not cleared along with the channels. No specific section for master bus search is present and master buses are not added to Emios_Pwm_Ip_aCheckState to be able to appear in the final mask variable. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: Emios_Pwm_Ip_SyncUpdate at the end of the function both pwm channels and corresponding master busses OUDIS bits are cleared. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: At init add the master bus of channels that use it and have pwm exclusive access enabled as initialized in the Emios_Pwm_Ip_aCheckState Or when looping through all the channels of the instance, when encountering a channel type that uses the master buses, check the master bus also

ID	Subtype	Headline and Description
ARTD-16689	New	New Feature [MCL][Emios] Extend the requirement(s) for SyncUpdate ,,"NewWorkDescription: In order for the PWM to fully implement the synchronous update of the channels parameters an update needs to be done in MCL Emios. The problem is as follows. The user updates the master bus period using Mcl_Emios_SetCounterBusPeriod with syncUpdate=TRUE. After that updates the needed chanels dutyCycle as desired using syncUpdate=TRUE as well. At the end PWM_Sync is called and all the channels should update at the next reload point. This has a problem as the dutyCycle value is computed based on the master bus period, which is not yet updated in the register at the time. The MCL should add a new API in IPL to allow the PWM to read most updated master bus value. For this the master bus periods should be kept internal to the driver and updated every time a new value is written the register as well. Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Add a global variable for storing the master bus periods. At every point where the period register is written, the global variable should be updated as well. Add a new API uint16 Emios_Mcl_Ip_GetCounterBusPeriod(uint8 hwInstance, uint8 hwChannel) that will return the period of the master bus form the global variable."
ARTD-16691	New	New Feature [PWM][EMIOS] Update Emios_Pwm_Ip_GetCounterBusPeriod ,,"NewWorkDescription: As described in ARTD-16689 the MCL will add a new API to get the updated master bus period. Update all Emios_Pwm_Ip_GetCounterBusPeriod instances to the new MCL API to always get the updated period. Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: NA"

ID	Subtype	Headline and Description
ARTD-16696	Bug	[MCL] Compiler warning report has some warnings with Emios Ip<*> Detailed description (how to reproduce it): N/A Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Compiler warning report has some warnings(pls see attached file) Expected behavior: Compiler warning report no warning Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-16704	New	New Feature [GPT] Different declaration of functions in ReqExport and header files ,,"NewWorkDescription: List function in ""ReqExport.txt"" file but does not include in ""*.h"" files of driver code: void Gpt_SetMode(Gpt_ModeType Mode) void Gpt_Notification_(void) void Pit_Ip_Init(uint8 instance, const Pit_Ip_InstanceConfigType const config) Pit_Ip_StatusType Pit_Ip_InitChannel(uint8 instance, const Pit_Ip_ChannelConfigType chnlConfig) void Pit_Ip_StopChannel(uint8 instance, uint8 channel, uint32 countValue) uint64 Pit_Ip_GetLifetimeTimerCount(uint8 instance) void Rtc_Ip_Init(uint32 instance, const Rtc_Ip_ConfigType const initConfig) void Rtc_Ip_Deinit(uint32 instance) void Rtc_Ip_StartCounter(uint8 instance, uint32 value) Rtc_Ip_StatusType Rtc_Ip_SetTimeDate(uint8 instance, Rtc_Ip_TimedateType const timeDate) Rtc_Ip_StatusType Rtc_Ip_ConfigureAlarm(uint8 instance, Rtc_Ip_AlarmConfigType const alarmConfig) void Rtc_Ip_ConvertSecondsToTimeDate(uint32 const seconds, Rtc_Ip_TimedateType const timeDate) void Rtc_Ip_ConvertTimeDateToSeconds(Rtc_Ip_TimedateType const timeDate, uint32 const seconds) void Rtc_Ip_StopCounter(uint8 instance) void Stm_Ip_StartCounting(uint8 instance, uint32 channel, uint32 compareValue) void Stm_Ip_SetClockMode(uint8 instance, prescalerModeType prescalerMode) void Emios_Gpt_Ip_SetClockMode(uint8 instance, uint8 channel, prescalerModeType prescalerMode) Please see in attach file Requirement source: ReqExport.txt (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Check function in ""ReqExport.txt"" file but does not include in ""*.h"" files of driver code"

ID	Subtype	Headline and Description
ARTD-16707	Bug	[S32K3][CRYPTO] Fix findings after code review<*> Detailed description (how to reproduce it): Deviation from code guideline: Check attached excel, "Detailed_Findings" tab. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: Deviation from code guideline for rules: 6, 10, 19, 22, 23, 24, 29, 37, 43, 45, 46, 47, 85, 110 more detail check attached file, "Detailed_Findings" tab. Expected behavior: All findings are fixed. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-16709	Bug	[SENT] Generated code on S32CT and EBT are different<*> Detailed description (how to reproduce it): During comparation the generated code on EBT and S32CT, I saw that there are many differences between them. Please take a look the compare_output_files.docx and generated files in attached file for more detail. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: header files, src files generated by EBT and CT should be the same. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA

ID	Subtype	Headline and Description
ARTD-16724	Bug	[ADC] Not return warning error when DMA channel be shared among configurations<*> Detailed description (how to reproduce it): When using the same DMA channel for configurations, it does not give an error warning. Configure ADC module select DMA channel (node: AdcDmaChannelId): dmaLogicChannel_Type_0 Configure CTU FIFO select DMA channel (Node: BctuFifoDmaChannelId): dmaLogicChannel_Type_0 Preconditions: Use EB Tresos. Test Case ID (internal TC that caught the defect) optional: Adc_TC_FCT_0701 of Adc_TS_012_cfgdma Observed behavior: When using the same DMA channel for configurations, it does not give an error warning Expected behavior: When using the same DMA channel for configurations, it does give an error warning Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-16727	Bug	[RM] Fix Compiler Warning<*> Detailed description (how to reproduce it): Fix compiler warning > see more details in attachment Preconditions: Build all tests Test Case ID (internal TC that caught the defect) optional: all test cases Observed behavior: compiler warning Expected behavior: no compiler warning Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: fix compiler warning

ID	Subtype	Headline and Description
ARTD-16728	Bug	[ADC] There is some information that does not match EB and S32CT when comparing code generation<*> Detailed description (how to reproduce it): Step 1: clean generate Adc_TS_COT_001 for EB and Adc_TS_COT_101_CT for CT Step 2: Compare include folder and src folder of S32CT with EB Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: There is some information that does not match EB and S32CT when comparing code generation. Detail in share point link: [https://nxp1.sharepoint.com/sites/Zebra/Shared %20Documents/Forms/AllItems.aspx?RootFolder=%2Fsites%2FZebra%2FShared %20Documents%2FGroup%204%2FEBvsS32CT%2FADC] File: "Compare Config S32CT and EB Tresos_EPC_S32K3xx.xlsx" Expected behavior: EB and S32CT need to generate the same file. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-16731	Bug	[Uart] Uart_apConfig and Uart_Ipw_apChnConfig should'nt be NULL if driver is not de-initialized successfully<*> Detailed description (how to reproduce it): [Uart_apConfig and Uart_Ipw_apChnConfig should be kept values if driver is not de-initialized successfully. Driver should check status return by IPL layer !image-2021-09-13-17-56-03-969.png|width=303,height=130! !image-2021-09-13-17-57-26-625.png|width=305,height=112!] Preconditions: [N/A] Test Case ID (internal TC that caught the defect) optional: [N/A] Observed behavior: [N/A] Expected behavior: [Driver should check status return by IPL layer] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [N/A]

ID	Subtype	Headline and Description
ARTD-16733	Bug	[Uart] Lpuart_Uart_Ip_Deinit only check LPUART_UART_IP_TX_COMPLETE<*> Detailed description (how to reproduce it): [Currently function Lpuart_Uart_Ip_Deinit only check LPUART_UART_IP_TX_COMPLETE before implement de-initialize. Need to mention reception status. !image-2021-09-13-18-31-44-015.png|width=416,height=168!] Preconditions: [N/A] Test Case ID (internal TC that caught the defect) optional: [Review] Observed behavior: [N/A] Expected behavior: [Before de-initialization, driver should mention both Tx and Rx status] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [N/A]
ARTD-16735	Bug	[RM] Typo in macro definitions with XRDC GVLD bit<*> Detailed description (how to reproduce it): There is a typo in definition of XRDC GVLD bit macros (GLVD used instead of GVLD): #define XRDC_CR_GLVD_MASK ((uint32)0x00000001UL) #define XRDC_CR_GLVD_ENABLE ((uint32)0x00000001UL) #define XRDC_CR_GLVD_DISABLE ((uint32)0x00000000UL) Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: The name of GVLD bit is not the same as defined in reference manual. Expected behavior: The name of GVLD bit is the same as defined in reference manual. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Modify the above definitions to be as follows (GLVD replaced by GVLD in the macro names): #define XRDC_CR_GVLD_MASK ((uint32)0x00000001UL) #define XRDC_CR_GVLD_ENABLE ((uint32)0x00000001UL) #define XRDC_CR_GVLD_DISABLE ((uint32)0x00000000UL) Plus modify all these macros where used in code.

ID	Subtype	Headline and Description
ARTD-16758	Bug	[S32K3 RTM] OCU: Ocu_SetClockMode can't set for channel if channel used mater bus<*> Detailed description (how to reproduce it): Tag: OCU_112 Branch: develop When config channel in EB, we choose channel used materbus. But call Ocu_SetClockMode function driver intervened for channel register Test Case ID (internal TC that caught the defect) optional: OCU_TC_FCT_0219 in Ocu_TS_101 Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-16740	New	New Feature [SPI] Improve DMA mode to increase the performance ,,"NewWorkDescription: DMA mode is taking more CPU load so it should be improved as proposal in ticket: AAI-946 Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: 1. Add a new feature to support to configure 1 DMA channel (TX/RX) per transmit. 2. Move all TCD elements reconfigure which is constant to Init function. For detail: see AAI-946"
ARTD-16753	New	New Feature [ICU] verify test example ,,"NewWorkDescription: need to re-check generate, build for test example for release Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]"

ID	Subtype	Headline and Description
ARTD-16761	Bug	[S32K3XX][Crypro] Hse Ip generates the incorrect Hse.ecvd file<*> Detailed description (how to reproduce it): 1*. Modify line 512 in "mcu_data/components/PlatformSDK_S32K3_2021_09/system/codegenerator.js" as follows: !image-2021-09-14-11-35-09-510.png! This ensures that the ECPD is generated only for Hse Ip 2. Create a project in S32DS and add Hse Ip. Then generate Hse.ecvd file and Hse_s32k344_257bga.ecpd file. These files are attached. 3. This is generated Hse.ecvd file !image-2021-09-14-11-36-29-777.png! I see that SHORT-NAME is Crypto. This leads to import fail Hse.ecvd file to EB tresos if I don't enable path mapping and automatically caculated path mapping !image-2021-09-14-11-40-21-245.png! If I enable 2 these buttons, EB will automatic calculate path mapping and this file will be import successfully. But this leads to test fail automation with makefile. !image-2021-09-14-11-11-50-398.png! 4. I have try changing Crypto become Hse in Hse.ecvd file, and This is success for both manual and automatic test. Preconditions: tag CRYPTO_082 Test Case ID (internal TC that caught the defect) optional: Ip_Hse_TS_COT_001.mak Observed behavior: Importing fail Hse.ecvd file to EB tresos if we don't enable path mapping and automatically caculated path mapping buttons. Expected behavior: Importing success Hse.ecvd file to EB tresos if we don't enable path mapping and automatically caculated path mapping buttons. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: File generated Hse.ecvd file : Crypto > Hse in line 8
ARTD-16805	Bug	[LIN][LPUART] Report LIN_ERR_HEADER to LinIf when a frame error occurs in the header part of the frame<*> Detailed description (how to reproduce it): Driver is missing LIN_ERR_HEADER report to LinIf when a frame error occurs in the header part of the frame Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: NA Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA

ID	Subtype	Headline and Description
ARTD-16814	Bug	[UART] Remove duplicate callback name if user configured with same name<*> Detailed description (how to reproduce it): If user config 1 callback name for 2 or more channel of Uart, duplicate name will happen !image-2021-09-14-23-12-45-227.png|thumbnail! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: Remove duplicate callback name if user configured with same name Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-16817	Bug	[Wdg] There is some information that does not match EB and S32CT when comparing code generation<*> Detailed description (how to reproduce it): Step 1: clean generate Wdg_TS_COT_001 for EB and Wdg_TS_COT_101 for CT on S32K324 Step 2: Compare include folder and src folder of S32CT with EB Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: There is some information that does not match EB and S32CT when comparing code generation. There is issue at generate code on CT. When configuring Multicore node = ON but CORE ID is still 0xFFFF !image-2021-09-15-09-30-53-030.png! Detail in *share point link*: https://nxp1.sharepoint.com/:x:/r/sites/Zebra/_layouts/15/Doc.aspx?sourcedoc=%7BB20CD393-7B19-4F45-9E5A-CE2632F02AD3%7D&file=Wdg_Compare%20Config%20S32CT%20and%20EB%20Tresos.xlsx&action=default&mobileredirect=true Expected behavior: EB and S32CT need to generate the same file. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-16819	Bug	[RM] Update examples follow update from dependent drivers<*> Detailed description (how to reproduce it): Generate fail example on EB Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Generate fail example on EB Expected behavior: gen build run success example Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update configuration for dependent driver as Platform
ARTD-16831	Bug	[LIN] Failure at generating on S32DS<*> Detailed description (how to reproduce it): Open S32DS and error log(see attached file) !image-2021-09-15-15-15-00-517.png|thumbnail! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Can not generate code on S32DS due to LIN module Expected behavior: Can generate code on S32DS Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-16833	New	New Feature [RM][S32K3XX] Fix misra violations ,,"NewWorkDescription: Misra rule 10.8 violations appeared after updating header files and needed to be checked Reduce rule 2.5 violations Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]"

ID	Subtype	Headline and Description
ARTD-16838	Bug	[CRC] No error observed when CrcEnableUserModeSupport is enabled and undefined MCAL_ENABLE_USER_MODE_SUPPORT<*> Detailed description (how to reproduce it): N/A Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Crc_TC_COT_0001.c Observed behavior: No error observed when CrcEnableUserModeSupport is enabled and undefined MCAL_ENABLE_USER_MODE_SUPPORT Failure at building IAR compiler Missing Crc_Ip_CfgDefines.h in Crc_Ip_TrustedFunctions.h file Expected behavior: Error observe when CrcEnableUserModeSupport is enabled and undefined MCAL_ENABLE_USER_MODE_SUPPORT Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: 1. Include "Mcal.h" file into Crc_Ip_Types.h Swap "Mcal.h" position with "Crc_Ip_CfgDefines.h" 2. Add prototype for SpecificSetUserAccessAllowed function
ARTD-16841	Bug	[Rm] Rm_pConfig is allocated to wrong section<*> Detailed description (how to reproduce it): N/A Preconditions: Run with precompile option Test Case ID (internal TC that caught the defect) optional: Fee_TS_191 Observed behavior: This variable is not cleared before the init function is called Expected behavior: this is cleared to NULL_PTR Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: allocate to SEC_VAR_CLEARED_UNSPECIFIED

ID	Subtype	Headline and Description
ARTD-16843	Bug	[SAI] Generated code mismatch between EB and CT<*> Detailed description (how to reproduce it): Generate code with EBtresos Import EPC to S32DS and generate code Compare generated code between DS and EB Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: Sai_TS_200 Observed behavior: Different in *Sai_Ip_VS_0_PBcfg.c*: Missing type of member (See detail in below image) Different in *CDD_Sai_VS_0_PBcfg.c*: Still have ".member" in struct (See detail in below image) Expected behavior: Generated code between EB and CT should be mapping Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-16846	Bug	[ADC] Build fail: "implicit declaration of function 'Adc_ReportDetError'" when AdcHwTriggerApi is enable and AdcDevErrorDetect is disable ,,"Detailed description (how to reproduce it): Build fail: ""implicit declaration of function 'Adc_ReportDetError'"" when AdcHwTriggerApi is enable and AdcDevErrorDetect is disable Preconditions: AdcHwTriggerApi is enable and AdcDevErrorDetect is disable Test Case ID (internal TC that caught the defect) optional: Adc_TS_COT_011 cfg 10 Observed behavior: Build fail log: STDERR:e:/S32K3/output/S32K3XX_S32K344_gcc/adc/../../eclipse/plugins/Adc_TS_T40D34M10I0R0/src/Adc.c: In function 'Adc_CheckSetChannelCtuTriggers': STDERR:e:/S32K3/output/S32K3XX_S32K344_gcc/adc/../../eclipse/plugins/Adc_TS_T40D34M10I0R0/src/Adc.c:3466:13: error: implicit declaration of function 'Adc_ReportDetError'; did you mean 'Det_ReportError'? [-Werror=implicit-function-declaration] STDERR: 3466 Adc_ReportDetError(ADC_SETCHANNEL_ID, (uint8)ADC_E_PARAM_GROUP); Expected behavior: Build done Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA

ID	Subtype	Headline and Description
ARTD-16847	Bug	[BASE] Build failed with AutosarOs<*> Detailed description (how to reproduce it): [BASE] Build failed with AutosarOs OsIf_Cfg.c: OsCounter_0{color:#de350b}*U Os_cfg.h: OsCounter_0 Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: Observed behavior: Expected behavior: Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-16867	Bug	[SENT] Fix compiler warnings<*> Detailed description (how to reproduce it): compiler warning report is generated at here: [http://flores.ea.freescale.net/0/project/custom_compilerwarning/20210915111230923000/details] Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: NA Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-16871	Bug	[RM] Missing validate in configurating PFlash on DS<*> Detailed description (how to reproduce it): Enable Pflash but not configurate it => Generate an array with 0 element => Build fail. Please fix both HLD and IP. Preconditions: Enable Pflash in DS Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-16874	Bug	[UART] Specific header file wasn't included separatetly for S32K3xx derivatives<*> Detailed description (how to reproduce it): Specific header file wasn't included separatetly for S32K3xx derivative in generated files that lead to failed at build step. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: Header files should be added individually for each S32K3xx derivative. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-16887	New	New Feature [SENT] Change implementation of SENT when using DMA to improve the performance ,,"NewWorkDescription: Currently, Sent implementation needs interrupt for every frame (DMA interrupt with DMA mode), so it's not good performance Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Try to use interrupt once when at end of frame when using DMA mode"
ARTD-16880	Bug	[S32K3 RTM] FLS: Missing fls user mode check when defined MCAL_ENABLE_USER_MODE_SUPPORT<*> Detailed description (how to reproduce it): 1. enable fls user mode and not define MCAL_ENABLE_USER_MODE_SUPPORT 2. disable fls user mode and define MCAL_ENABLE_USER_MODE_SUPPORT No error generated in both case. Observed behavior: No error generated in both above case. Expected behavior: An error will generated in both above case. Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-16882	Bug	[Uart][FLEXIO] FlexIO missing enable error shifter when DMA using<*> Detailed description (how to reproduce it): [FlexIO missing enable error shifter when DMA using] Preconditions: [N/A] Test Case ID (internal TC that caught the defect) optional: [Uart_TS_0014] Observed behavior: [N/A] Expected behavior: [N/A] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [N/A]
ARTD-16891	New	New Feature [FLS][S32K3 1.0.0] Remove unused Qspi resources ,,"NewWorkDescription: There are some unused Qspi stuffs that should be removed from the driver code: QSPI_IP_READ_MODE_INTERNAL_DQS and QSPI_IP_READ_MODE_LOOPBACK_DQS FlsQspiSectorCh node configuration FlsHwUnitPageProgramBoundary* node configuration Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]"
ARTD-16930	Bug	[ADC]Content of example description is incorrect<*> Step: 1.Import all ADC example projects for S32K3: 2. Open description.txt then check content Observed behavior: Content of description isn't correctly, debugger not support for S32K3 Configuration Name Description $(example)_debug_ram_{color:red}s32debugger Debug the RAM configuration using{color:red} S32 Debugger $(example)_debug_flash_{color:red}s32debugger Debug the FLASH configuration using S32 Debugger Expected behavior: Content of description should be updated correctly with PE micro debugger

ID	Subtype	Headline and Description
ARTD-16932	Bug	[S32K3xx][Crypto] Content of description is incorrectly<*> Step: 1.Import all Crypto example projects for S32K3: 2. Open description.txt then check content Observed behavior: Content of description isn't correctly, debugger not support for S32K3 Configuration Name Description $(example)_debug_ram_{color:red}s32debugger Debug the RAM configuration using{color:red} S32 Debugger $(example)_debug_flash_{color:red}s32debugger Debug the FLASH configuration using S32 Debugger Expected behavior: Content of description should be updated correctly with PE micro debugger
ARTD-16926	Bug	[RTD_4.4_S32K3x_1.0.0] Warning "Invalid project path: Missing project folder or file: \...\include for Source path" displayed after detach RTD for NPW project ,," Install S32DS 3.4 SP2.EAR1 release and S32K3XX_RTD_4_4_RTM_1_0_0_DS_updatesite_2109_RC4.zip Test Case: # Create NPW for S32K3XX enable RTD 1.0.0 # Select project > SDKs > Detach RTD 1.0.0 # Check Problem view Observed behavior: There is a warning message displayed: ""_*Invalid project path: Missing project folder or file: \\{project_name}\include for Source path*_"" after detach RTD 1.0.0 Expected behavior: No warning message displayed
ARTD-16927	Bug	[I2c] Fix driver build fail with iar when use dma<*> Detailed description (how to reproduce it): [...] Fix driver build fail with iar when use dma for both lpi2c and flexio !image-2021-09-17-14-46-56-600.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-16941	Bug	[I2c] There isn't description with some example project I2C<*> Step: 1. File > New > S32DS project from example 2. Select all I2c example projects for S32K3> check description.txt I2c_IP_HLD_FLEXIO_Transfer_S32K312/S32K344 I2c_IP_HLD_LPI2C_Transfer_S32K312/S32K344 Observed behavior: There is no description Expected behavior: Should add description
ARTD-16947	New	New Feature [FLS][S32K3 1.0.0] Remove unused configurations ,,"NewWorkDescription: There are some unused configurations and macros that should be removed or hidden from the driver code: FlsAbortOwnedDomainsTimeout and its macro *FLS_ABT_DOMAINS_TIMEOUT FlsMCoreBusyWaitTimeout FlsProtection Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]"
ARTD-16949	Bug	[SENT] DMA buffer depth feature was not implemented<*> Detailed description (how to reproduce it): [...] Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-16952	Bug	[S32K3] CRYPTO DS examples cannot run with FLASH target<*> Detailed description (how to reproduce it): Crypto DS examples cannot run with FLASH target due to HSE disabled default configuration, while the user can select an alternative FLASH programming algorithm within Advanced Options dialog. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: Crypto DS examples cannot run with FLASH target. Expected behavior: Crypto DS examples can run with FLASH target. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-16974	Bug	[S32K3XX][I2C]fix warning - genfail - run fail on example of I2C<*> Detailed description (how to reproduce it): [...] Preconditions: [...] N/A Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] fix all warning of EBT example, and run fail on k312 Expected behavior: [...]alll examples run normally and have no warning Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) N/A Proposed solution optional: [...]N/A

ID	Subtype	Headline and Description
ARTD-16995	Bug	[LIN] [DS] Missing to set default for some node in template file<*> Detailed description (how to reproduce it): Some nodes in template file don't set to default value to NULL_PTR as: LinLpuartStartTimerNotification LinLpuartStopTimerNotification LinFlexioStartTimerNotification LinFlexioStopTimerNotification Update max value to 160MHz for LinClockRef node Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: NA Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-17012	New	New Feature [FLS] Update Fls_DataAddressType to fix Misra 11.6 ,,"NewWorkDescription: Fix Misra 11.6 ""A cast should not be performed between pointer to void and an arithmetic type."" Requirement source: Misra 2012 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Update Fls_DataAddressType to uint32 to avoid conversions from pointer to void to uint32."
ARTD-17018	Bug	[Uart] HLD Transmit and Receive functions need to check both receive and transmit status for reporting det error<*> Detailed description (how to reproduce it): [...] Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-17021	Bug	[ICU][S32K3XX] Fix warning of example and update add example for S32K312<*> Detailed description (how to reproduce it): Have a warning when build with EB example for S32K344, but it is related to Platform module. Update example for S32K312 and additional example with all IPV for S32K344. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-17023	Bug	[Uart] Compiler warning S32K3<*> Detailed description (how to reproduce it): [Compiler warning exists in driver] Preconditions: [N/A] Test Case ID (internal TC that caught the defect) optional: [None] Observed behavior: [None] Expected behavior: [No Compiler warning] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [None]
ARTD-17025	Bug	[RM] Mpu M7 : Wrong validation in calculating Region Size<*> Detailed description (how to reproduce it): Wrong calculated Region Size in Mpu M7 => Import or create new project which using Mpu M7 become fail. Please check both HLD and IP. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Check validation in Rm.component and Mpu_M7.component

ID	Subtype	Headline and Description
ARTD-17026	Bug	[SENT] Some requirements are not fully covered<*> Detailed description (how to reproduce it): There are some requirement have been added, some of them aren't fully covered by SENT driver. SWS_CDD_Sent_00057, SWS_CDD_Sent_00058, SWS_CDD_Sent_00059 Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: SWS_CDD_Sent_00057 and SWS_CDD_Sent_00059: only ignoring the entire message, not declaring to user that these errors have occurred. SWS_CDD_Sent_00059: Get all msg functions are using detecting timeout from each channel, so timeout expire case only occur when last channel has timeout error Expected behavior: Follow the requirement Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Using a user notification to inform to user when any above error occurred
ARTD-17031	Bug	[I2c] Ip Flexio can not transfer when use interrupt<*> Detailed description (how to reproduce it): [...] Ip Flexio can not transfer when use interrupt, the test is blocking in this funcition !image-2021-09-21-14-26-43-518.png! !image-2021-09-21-14-27-28-158.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Ip_Flexio_ts_200 Observed behavior: [...] Ip Flexio can not transfer when use interrupt Expected behavior: [...] Ip Flexio can transfer when use interrupt Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-17050	Bug	[UART] ECPD generate fail for HLD layer<*> Detailed description (how to reproduce it): ECPD generate fail for HLD layer NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: ECPD generate success for HLD layer Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-17055	Bug	[I2c] Fix build fail example after update template file on DS<*> Detailed description (how to reproduce it): [...] Fix build fail example after update template file on DS Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-17061	Bug	[S32K3XX 4.4] OCU: Clock prescale of internal counter incorrect<*> Detailed description (how to reproduce it): The channel divider uses an internal counter of DIV_1, but when debugging it is DIV_4 Preconditions: The channel using internal counter Test Case ID (internal TC that caught the defect) optional: Ocu_TS_101 Observed behavior: Prescale of internal counter is wrong when debugging Expected behavior: Prescale of internal counter is correct when debugging Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-17065	Bug	[S32K3XX][S32K3xx_100] import ecpd from CT to EB fail<*> Detailed description (how to reproduce it): follow ARTD-15711 ticket generate ecpd from s32ct. on s32ct create new project then add IntCtrl_Ip for project, after that export ecpd file and ecvd from s32ct. Open EB and create new project with plugin _*[^Ip_TS_T40D34M10I0R0.zip]*_ to project, then import ecvd gene rate from s32ct. Preconditions: follow ARTD-15711 ticket Test Case ID (internal TC that caught the defect) optional: Ip_Platform_TS_COT_001 Observed behavior: missing opption on eb !image-2021-09-22-17-35-06-172.png! 2. Compare file generate by EB on CT have some ! image-2021-09-22-17-38-18-269.png! Expected behavior: Add more opption on EB Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-17066	New	New Feature [PORT] Remove the PTA24 from S32K3x4_172mqfp package ,,"NewWorkDescription: !image-2021-09-23-10-43-46-373.png|width=827,height=406! From the latest request from customer, the PTA24 should not be existed from the Port configurations. Please refer to the email attachment for more details (Susan Sun) Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Remove the PTA24 from Port configuration."
ARTD-17073	Bug	[PORT] An error should be raised when configure the not available pins in CT HLD<*> Detailed description (how to reproduce it): There are some types of pins like this: !image-2021-09-23-11-11-49-494.png|width=606,height=333! There is an error should be raise when user configure those pins for the affected packages. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: There is no error was raised when user configure the not available pins Expected behavior: There is an error should be raised when user configure the not available pins Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA

ID	Subtype	Headline and Description
ARTD-17078	Bug	[S32K3 RTM][FEE] fix CMM MISRA violations<*> Detailed description (how to reproduce it): there is CCM MISRA violations in Fee_JobErrorNotification Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: there is CCM MISRA violations in Fee_JobErrorNotification Expected behavior: there is not CCM MISRA violations in Fee_JobErrorNotification Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-17079	Bug	[WDG][S32K3XX] Reset value of TO register is incorrect<*> Detailed description (how to reproduce it): Reset value of TO register isnt matching with S32k3xx_RM_Rev2 In Swt_Ip_FeatureDefines.h: #define SWT_IP_TO_RESET_VALUE_U32 (0x0073FDE0U) In RM (or check attached file) : !image-2021-09-23-13-13-45-777.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: Reset value of CS register isnt matching with S32k1xx_RM_Rev13 Expected behavior: update #define SWT_IP_TO_RESET_VALUE_U32 (0x00000320U) Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-17102	Bug	[ICU] Fix index of array node in ecpd<*> Detailed description (how to reproduce it): EPD ECU Parameter Definition (Schema) Used by EBT ECPD ECU Configuration Parameter Definition (Schema) Used by S32CT EPC ECU Parameter Configuration (Configuration File) Used by EBT ECVD ECU Configuration Value Description (Configuration File) Used by S32CT Index of array IcuHwConfiguration sort by name. attached 2 file epc and ecvd see the diffirent Preconditions: Index of array GptHwConfiguration sort by name. Test Case ID (internal TC that caught the defect) optional: Observed behavior: when import epc to DS .Index of array IcuHwConfiguration sort by name. Expected behavior: import epc file to DS the array same when import to EB. Can import export (EBT-DS) No violations VSMD. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: modify template file and xdm
ARTD-17109	New	New Feature [OCU] Different declaration of functions in ReqExport and header files ,,"NewWorkDescription: List function in ""ReqExport.txt"" file but does not include in ""*.h"" files of driver code: Ocu_ProcessChannelNotification(uint16 Channel) Emios_Ocu_Ip_ValueType Emios_Ocu_Ip_GetCounter(uint8 InstNum, uint8 ChNum) Emios_Ocu_Ip_ReturnType Emios_Ocu_Ip_SetAbsoluteThreshold(uint8 InstNum, uint8 ChNum, Emios_Ocu_Ip_ValueType ReferenceVal, Emios_Ocu_Ip_ValueType AbsoluteVal) Emios_Ocu_Ip_ReturnType Emios_Ocu_Ip_SetRelativeThreshold(uint8 InstNum, uint8 ChNum, Emios_Ocu_Ip_ValueType RelativeValue) Please see in attach file Requirement source: ReqExport.txt (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Check function in ""ReqExport.txt"" file but does not include in ""*.h"" files of driver code"

ID	Subtype	Headline and Description
ARTD-17116	Bug	[FLS] FlsCallCycle parameter is 0 and cannot be configured<*> Detailed description (how to reproduce it): FlsCallCycle parameter is 0 and cannot be configured. This parameter is used by Fls driver in bswmd file (eclipse\plugins\Fls_TS_T40D11M20I0R0\generate_swcd\swcd \Fls_Bswmd.arxml) as follows: <PERIOD>[!IF "node:exists(FlsConfigSet/FlsCallCycle)"![!"FlsConfigSet/FlsCallCycle"!] [!ELSE!]0[!ENDIF!]</PERIOD> As a result the generated value for Fls main function PERIOD in bswmd file is always 0 and this results in error in Autosar RTE as 0 is not a valid period of main function. Preconditions: FLS driver used together with Autosar RTE Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Not able to generate Autosar RTE because the Fls main function period in bswmd file is 0 Expected behavior: To be able to generate Autosar RTE (period is not 0 in bswmd file) Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Make the FlsCallCycle parameter configurable by these changes in Fls.xdm file: original FlsCallCycle definition: <v:var name="FlsCallCycle" type="FLOAT_LABEL"> <a:a name="LABEL" value="Fls Call Cycle"/> <a:a name="DESC"> .... Cycle time of calls of the flash driver main function Note: Not supported by the driver. .... </a:a> .... <a:da name="DEFAULT" value="0.0"/> .... <a:da name="READONLY" value="true"/> </v:var> Fixed definition (modified type of parameter from FLOAT_LABEL to FLOAT, modified DESC field to remove note that not supported by driver, modified default value from 0 to 0.01 and removed READONLY attribute): <v:var name="FlsCallCycle" type="FLOAT"> <a:a name="LABEL" value="Fls Call Cycle"/> <a:a name="DESC"> .... Cycle time of calls of the flash driver main function .... </a:a> .... <a:da name="DEFAULT" value="0.01"/> .... </v:var> Find attached the updated Fls.xdm file.

ID	Subtype	Headline and Description
ARTD-17128	Bug	[CAN] inital segments generated by auto calculation baudrate in FlexCAN_Ip_PbCfg.c is not same with the ones in HLD<*> Detailed description (how to reproduce it): with input paramaters: Can_CLK = 24Mhz and !image-2021-09-24-18-32-47-140.png! segments generated in IPL (FlexCAN_Ip_PbCfg.c) !image-2021-09-24-18-34-19-636.png! segments generated in HLD (Can_PbCfg.c) !image-2021-09-24-18-34-54-919.png! => NOT identical. so affter Can_Init called, segments generated by IP used => not works need to check for S32CT code also. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: segments generated by HLD and IP are not identical Expected behavior: segments generated by HLD and IP are identical Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-17130	Bug	[RM] Remove redundant characters<*> Detailed description (how to reproduce it): Some redundant character which make build fail CCOV test !image-2021-09-25-15-45-45-138.png|width=805,height=238! Preconditions: setup run CCOV test Test Case ID (internal TC that caught the defect) optional: Rm_TS_COV_001 Observed behavior: Build fail test: !image-2021-09-25-15-43-45-143.png|width=890,height=240! Expected behavior: build successful Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Remove the "\" character.

ID	Subtype	Headline and Description
ARTD-17137	Bug	[I2c] Driver can not link to channel Ecuc partition on EB 27.1<*> Detailed description (how to reproduce it): [...] Driver can not link to channel Ecuc partition on EB 27.1 !image-2021-09-27-10-29-05-288.png! Preconditions: [...] N/A Test Case ID (internal TC that caught the defect) optional: [...] I2c_TS_MUL_001 Observed behavior: [...] Driver can not link to channel Ecuc partition on EB 27.1 Expected behavior: [...] Driver can link to channel Ecuc partition on EB 27.1 Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-17140	Bug	[Mcl] Flexio_Ip_baIpIsInitialized was created of incorrect memory<*> Detailed description (how to reproduce it): Run IPV Flexio in core 1, driver don't go to function Flexio_Lin_Ip_IrqHandler Preconditions: Because module Mcl was init in core 0 => Flexio_Ip_baIpIsInitialized will equal TRUE in core 0. But Flexio run in core 1. Flexio_Ip_baIpIsInitialized allocated in MCL_START_SEC_VAR_CLEARED_BOOLEAN of memap. ! image-2021-09-27-11-30-35-458.png! => core 1 can't access to Flexio_Ip_baIpIsInitialized in core 0. Test Case ID (internal TC that caught the defect) optional: Lin_TC_WBT_0005 Observed behavior: Test fail Expected behavior: Test pass Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Change MCL_START_SEC_VAR_CLEARED_BOOLEAN to MCL_START_SEC_VAR_CLEARED_BOOLEAN_NO_CACHEABLE ! image-2021-09-27-15-12-10-063.png!

ID	Subtype	Headline and Description
ARTD-17142	New	New Feature [SPI] Add How to use half duplex mode in UM ,,"NewWorkDescription: Add How to use half duplex mode in UM Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: NA"
ARTD-17141	Bug	[Rm] Fix description and readme Example<*> Detailed description (how to reproduce it): 1. In description of all Example_S32K312, please modify to has only Debug Flash. (In picture attachment). 2. And Name in line 40-41 of Rm_Example_S32K312's description, should we change them into "Rm_Example_S32K312_Debug_FLASH_PNE" (in S32DS screen, using this name)? 3. In Mpu Example, in section1 Example Description, please fix "Xrdc" into "Mpu". Detail in attachment. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-17150	Bug	[S32K3XX] [PORT] Fix compiler warning<*> Detailed description (how to reproduce it): in file compiler warning report: [http://solomon.ea.freescale.net/1/project/custom_compilerwarning/details] Preconditions: all warning need to be run out Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: !image-2021-09-27-15-39-45-811.png! Expected behavior: driver need to be update to resolve this issue Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA

ID	Subtype	Headline and Description
ARTD-17200	Bug	[WDG] WDG_EXCLUSIVE_AREA_00 is missing in bswmd file<*> Detailed description (how to reproduce it): WDG_EXCLUSIVE_AREA_00 is not missing in bswmd file resulting in an issue that the exclusive area is not generate by Autosar RTE leading to compiler error. Preconditions: Wdg driver used with Autosar RTE Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Exclusive area 00 is not generated by Autosar RTE Expected behavior: Exclusive area 00 is generated by Autosar RTE Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update the exclusive_areas_to_be_defined_in_bsw_scheduler.dox file and NonASR_ServiceID.xml to map the exclusive area to a function which is generated into bswmd file by bswmd_creator script. Find attached updated files with one possible solution (adding Wdg_Cbk_GptNotification0/1/2/3/4/5/6 functions into NonASR_ServiceID.xml and then mapping the WDG_EXCLUSIVE_AREA_00 to Wdg_Cbk_GptNotification0/1/2/3/4/5/6 in exclusive_areas_to_be_defined_in_bsw_scheduler.dox).).
ARTD-17214	Bug	[LIN] Missing case LIN_DUAL_CLOCK_MODE with IPV FlexIO<*> Detailed description (how to reproduce it): Missing case LIN_DUAL_CLOCK_MODE with IPV FlexIO Preconditions: Missing case LIN_DUAL_CLOCK_MODE with IPV FlexIO Test Case ID (internal TC that caught the defect) optional: Lin_TC_FCT_0003 Observed behavior: NA Expected behavior: NA Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: add case LIN_DUAL_CLOCK_MODE with IPV FlexIO

ID	Subtype	Headline and Description
ARTD-17264	Bug	[S32K3 RTM] [I2C] Fixing HIS_CYCLE warning<*> Detailed description (how to reproduce it): There is are HIS_CYCLE appeared in report. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: Remove the HIS_CYCLE is required Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-17269	Bug	[WDG] Error in configuration of Example<*> Detailed description (how to reproduce it): The "max wdg timeout" is 2s in EB configuration , so the maximum value which we can push in the Wdg_43_Instance0_SetTriggerCondition is 2000. But the Wdg_43_Instance0_SetTriggerCondition(0xFD00) is called in the main.c Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: The example run to reset Expected behavior: The example do not run to reset Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A

ID	Subtype	Headline and Description
ARTD-17272	Bug	[I2c] [Example] Update description and rename example<*> Detailed description (how to reproduce it): [...] Update description example and correct name of example Edit connection description, update connector register !image-2021-09-28-17-18-53-878.png! !image-2021-09-28-17-23-12-469.png! !image-2021-09-28-17-20-07-624.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-17279	Bug	[BASE] No need to declare trusted functions in OsIf_Timer_Systick_TrustedFunctions.h when AutosarOS used<*> Detailed description (how to reproduce it): When AutosarOS used, the functions OsIf_GetCounter() and OsIf_GetElapsed() will call corresponding to GetCounterValue() and GetElapsedValue() in Os.h if enable OsIfUseSystemTimer. So, the functions OsIf_Timer_System_Internal_Init(), OsIf_Timer_System_Internal_GetCounter() and OsIf_Timer_System_Internal_GetElapsed() will only called when using OS_FREERTOS or OS_BAREMETAL. AutosarOS will not called these functions. So OsIf_Timer_Systick_TrustedFunctions.h file can be removed. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: In OsIf_Timer_System.c: the functions OsIf_Timer_System_Internal_Init(), OsIf_Timer_System_Internal_GetCounter() and OsIf_Timer_System_Internal_GetElapsed() are not called when AutosarOS is used(USING_OS_AUTOSAROS defined). Expected behavior: NA Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Remove OsIf_Timer_Systick_TrustedFunctions.h and update the subchapter User mode in IM

ID	Subtype	Headline and Description
ARTD-17276	Bug	[S32K3XX][S32k3xx_100] function in "ReqExport.txt" not mapping "*.h" files of driver code: ,,"Detailed description (how to reproduce it): checking for mapping between ReqExport.txt and "" .h "" files in driver code. Some functions not mapping. Checking S32K3XX_result.txt attached file Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Platform_TS_001 Observed behavior: !image-2021-09-28-18-47-12-970.png! Expected behavior: Modify Platform_GetIrqMonitorStatus function in driver code to mapping ReqExport Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-17294	Bug	[BASE] Fix compiler warning for S32K3XX RTM 1.0.0<*> Detailed description (how to reproduce it): Fix compiler warning for S32K3XX RTM 1.0.0. Please see the attachment for more detail. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: There is a compiler warning. Expected behavior: There is no compiler warning Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-17301	Bug	[S32K324] DS multicore project does not build<*> Detailed description (how to reproduce it): Create new multicore project in S32DS for S32K324 Build the project Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: Project does not build due the not updated multicore linker files Expected behavior: project builds, uploads to the board and executes on both cores Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-17352	Bug	[LIN] Driver and requirement are inconsistent<*> Detailed description (how to reproduce it): Driver and requirement are incompatible as below: No||Function name||Remark||_*Solution 1|void Flexio_Lin_Ip_GotoIdleState(const uint8 Channel);|Different name "Reqexport.txt" : "Flexio_Lin_Ip_GoToIdleState" " .h " file : "Flexio_Lin_Ip_GotoIdleState"|Change from Flexio_Lin_Ip_GotoIdleState to Flexio_Lin_Ip_GoToIdleState 2|void Lin_GetVersionInfo (Std_VersionInfoType VersionInfo);|Different name "Reqexport.txt" : "versioninfo" " .h " file : "VersionInfo"|The parameter in Lin_GetVersionInfo function need to be updated from VersionInfo to versioninfo. 3|void Lpuart_Lin_Ip_GotoIdleState(const uint8 Instance);|Different name "Reqexport.txt" : "Lpuart_Lin_Ip_GoToIdleState" " .h " file : "Lpuart_Lin_Ip_GotoIdleState"|Change from Lpuart_Lin_Ip_GotoIdleState to Lpuart_Lin_Ip_GoToIdleState 4|void Lpuart_Lin_Ip_TimerExpiredService(uint8 Instance);|Lacking const "Reqexport.txt" : "(const uint8 Instance);" " .h " file : "(uint8 Instance);"|The Instance parameter type in Lpuart_Lin_Ip_TimerExpiredService function should be changed to const. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Driver and requirement are inconsistent Expected behavior: Driver and requirement are consistent Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-17366	Bug	[RM] Fix Pin error and Clock warning in Example<*> Detailed description (how to reproduce it): 1. Pin Error : Pins initialization requires the PINS Driver in the project. Detail in attachment. 2. Clock Warning : Please check in Clock >Choose tab Code Preview > Double click in "Code generated with warnings". Detail warning in attachment. 3. Pin error is existed in all example of DS. Clock Warning is existed in example Rm HLD of DS. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: NA Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA

ID	Subtype	Headline and Description
ARTD-17421	Bug	[UART] [DS] S32K3XX Examples have some warning in Clock configuration<*> Detailed description (how to reproduce it): There is warning from Clock tab for DS Example Preconditions: Open the Clock tab > Click on the Code Preview tab > Double click on the Code generated with warnings Test Case ID (internal TC that caught the defect) optional: S32K3XX Examples Observed behavior: S32K3XX Example warning Expected behavior: Fix S32K3XX Example warning Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-17465	Bug	[S32K3][SENT] Incorrect SENT_MAX_PARTITIONS generation in Sent_Cfg.h<*> Detailed description (how to reproduce it): In Sent_Cfg.h, SENT_MAX_PARTITIONS is generated: [!VAR "maxCoreDefConfig" = "num:i(1)"!] [!IF "SentGeneral/SentMulticoreSupport = 'true'"!] [!IF "node:exists(as:modconf('EcuC')[1]/EcucPartitionCollection/*[1]/EcucPartition)"!] [!VAR "maxCoreDefConfig" = "num:i(count(as:modconf('EcuC')[1]/EcucPartitionCollection/*[1]/EcucPartition/*))"!] [!ENDIF!] [!ENDIF!] [!ENDNOCODE!] #define SENT_MAX_PARTITIONS[!WS "4"!][!"num:i($maxCoreDefConfig)"!]U But *SentMulticoreSupport doesn't exist in sent.xdm. So SENT_MAX_PARTITIONS always equal to 1. Preconditions: Enable multicore Test Case ID (internal TC that caught the defect) optional: Sent_TS_011 Observed behavior: NA Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Chane SentMulticoreSupport to *SentEnableMulticoreSupport* in Sent_Cfg.h

ID	Subtype	Headline and Description
ARTD-17470	Bug	[RM] Rm_Example_S32K312 fail<*> Detailed description (how to reproduce it): Rm_Example_S32K312 fail in gMpuErrorDetected with DS Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: NA Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-17515	New	New Feature [RESOURCE] Requirement CPR_RTD_00220.resource has changed to non-traceable ,,"NewWorkDescription: CPR_RTD_00220.resource has changed to non-traceable, so ""@implement ResourceSubderivative_Object"" in Resource.xdm should be removed. Requirement source: cPRT (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: NA"
ARTD-17530	Bug	[I2C] Add report review check list<*> Detailed description (how to reproduce it): NA Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: NA Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA

ID	Subtype	Headline and Description
ARTD-17597	Bug	[ICU][S32K3XX] Update test after code freeze<*> Detailed description (how to reproduce it): Update Req for Icu_TC_FCT_1302 Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:

4.7 0.9.0

ID	Subtype	Headline and Description
ARTD-990	New	New Feature [LIN][S32K3XX] - Add timeout checking for a frame reception ,,The LIN driver shall check if reception occurs in a limited period of time configured by user. A timeout checking shall be implemented in order to not wait forever for the frame reception
ARTD-1115	New	New Feature [ADC] Add support for streaming results reorder ,,"Details in CPR_RTD_00490.adc The adc driver shall support streaming access mode functionality with the possibility to arrange the adc results as multiple sets of group result buffer. E.g.: for a group with channels {CH1 Ch5 CH7} the resulting stream buffer shall be: {CH1, Ch5, CH7, CH1, Ch5, CH7, CH1, Ch5, CH7} instead of {CH1,CH1,CH1,CH5,CH5,CH5,CH7,CH7,CH7} like supported by autosar standard. This feature extension shall be enabled by using a parameter named Stream Result Grouping at group level. The default value of this parameter shall be False and shall only be editable when streaming access mode is selected for its group. Implement also in Tresos and S32CT"

ID	Subtype	Headline and Description
ARTD-1426	New	New Feature [ADC] Double buffering optimization - optimize DMA streaming ,,"Add dev test to validate double buffering optimization. Investigate and fix any eventual issue CPR_RTD_00384: The ADC driver shall provide an optional configuration parameter for reducing the number of interrupts required for processing the conversions of Adc Groups that consist of one or more channels (depending on HW capabilities) and which are configured as ADC_ACCESS_MODE_STREAMING. This parameter shall be available only when DMA transfer is used. When this feature is enabled, only one interrupt will be raised after the completion of all stream conversions (as configured by AdcStreamingNumSamples parameter). An additional interrupt to be raised after half of the stream is converted shall also be configurable. "
ARTD-1670	New	New Feature [CAN][FD/TDC] non-identical prescalers need to be supported ,,"Creating a simple testcase for sending an BRS frame with enabled TDC with bitrate 500Kbps 4000 Kbps. > after investigation, only a bitrate configuration (get from SDK) is working, others can work (but with many errors). This reflect that the TDC bitrate configuration is strictly depend on users environment > this raise the requirement for flexible bitrate configuration. CAN_TC_FCT_7590 can only send frame without errors with below bitrate configuration for 500Kbps-4Mbits: { (uint8)7U, (uint8)4U, (uint8)1U, (uint16)*9*, (uint8)1U } , /*values for CBT baudrate .bitrate_cbt*/ { (uint8)15U, (uint8)1U, (uint8)1U, (uint16)*0*, (uint8)1U } , The TDC offset exactly base on rm's expression: (proseg phase_seg1 2) == 15 1 2 == 18 => this relfect that identical prescalers does not help in this situation, instead limit the bitrate configuration! Expectation: non-identical prescalers should be support. and in this case, a warning can be raised for reflecting the recommendation in rm"
ARTD-1952	New	New Feature [S32K344] ICU_GET_PULSE_WIDTH_API is hardcoded as STD_OFF ,,Please see ticket AMNG-8589

ID	Subtype	Headline and Description
ARTD-1958	Bug	[PWM][IPV_EMIOS] Spike with PWM duty cycle 0% in OPWMB mode<*> Detailed description (how to reproduce it): An issue has been reported by Sumimoto when they're trying to generate PWM signal on S32K2. They observe a spike during Pwm_Init(), with PWM duty cycle 0% on OPWMB mode. Note: This is the cloned ticket from MCAL legacy, the code in Zebra has been changed. However, as it's an issue from IPV_EMIOS, which is available on K3, the ticket is created to avoid the similar issue. Preconditions: # PWM channel configuration EMIOS 0 channel 1, default duty cycle: 0, Polarity: PWM_HIGH, Idle state: PWM_LOW EMIOS 0 channel on OPWMB mode, BUS A selected. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Before entering OPWMB mode, PWM driver will set the EMIOS channel to GPDO mode with default Idle state => the output signal will be set to LOW When entering OPWMB mode, A and B registers are updated according to duty cycle and period, then EDPOL is set as polarity PWM_HIGH: REG_RMW32 (EMIOS_CCR_ADDR32(u8ModuleIdx, u8ChannelIdx), (CCR_MODE_MASK_U32 CCR_EDPOL_MASK_U32), ((u32CtrlRegVal & CCR_MODE_MASK_U32) (u32PolarityBit & CCR_EDPOL_MASK_U32)) => After that output signal will be set to HIGH Force match on the 1^st edge by writing to FORCEB bit: REG_BIT_SET32(EMIOS_CCR_ADDR32(u8ModuleIdx, u8ChannelIdx), CCR_FORCMB_MASK_U32); Because the duty cycle is 0 => the output signal will be set to LOW => A spike occurred. Expected behavior: This is a bug because Autosar requires not to have any spikes. It might impacts to other eMios platforms like Cobra, Rainier, Calypso, Mamba, Castor,... Also, we need to avoid spike in all APIs, so other PWM mode should be carefully tested. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Spike can be avoid by setting polarity after setting mode OPWMB entry, instead of setting both of them at same time.
ARTD-1966	New	New Feature [ADC] Implement ADC_BYPASS_CONSISTENCY_LOOP ,,"ADC: implement and rename ADC_BYPASS_CONSISTENCY_LOOP When enabled, Adc_Ipw_StopCurrentConversion does not wait for the actual conversion to finish. To support this, a new parameter should be added to Adc_Sar_Ip_AbortChain boolean Blocking. When set to false, this function should not wait until the conversion is actually completed. Update IPL requirement Consider renaming the feature. If renamed, update also in tresos, ct, and doc "

ID	Subtype	Headline and Description
ARTD-2020	Bug	[ADC] Adc_EnableHardwareTrigger set MODE to ONESHOT mode so sw continuous group can not run as expected<*> Test sequence: / Start ADC SW Normal continuous group conversion / Adc_StartGroupConversion(t_u8AdcSWNormalGroup); / Enable hardware trigger for ADC HW Injected group conversion / Adc_EnableHardwareTrigger(t_u8AdcHWInjectedGroup); / Verify: There is no DET error / EU_ASSERT(T_Adc_Det_TestNoError()); T_ADC_HWInjectedProcess(t_u8AdcHWInjectedGroup, t_u8HwUnitIndex); T_ADC_SWNormalProcess(t_u8AdcSWNormalGroup, t_u8HwUnitIndex); Adc_EnableHardwareTrigger set MODE to ONESHOT mode so t_u8AdcSWNormalGroup can not run as expected

ARTD-2039	Bug	[ADC] Adc_ReadGroup always resets user result buffer index<*>
		
		Detailed description (how to reproduce it):
		Adc_ReadGroup always resets user result buffer index
		Verify group conversion with normal group: hw, injected, oneshot, streaming circular
		Test sequence:
		1. Adc_Init with number of streaming sample = 10
		2. Adc_SetupResultBuffer: t_setupResultBuffer
		3. Adc_EnableHardwareTrigger
		4. Loop to generate ADC trigger several times that equals number of sample
		4.1 T_ADC_StartTrigger
		4.2 Wait until Adc_GetGroupStatus is ADC_COMPLETED, end of loop when status is ADC_STREAM_COMPLETED
		4.3 T_ADC_StopTrigger
		4.4 Adc_ReadGroup(group, t_readGroupBuffer) returns E_OK
		4.5 Verify conversion result in "t_readGroupBuffer"
		5. Verify conversion result in user result buffer: t_setupResultBuffer
		=> Fail at step 5: the "t_setupResultBuffer" has only 1 sample
		Observed behavior: After calling Adc_ReadGroup function, the user result buffer index always resets to 0
		Adc_ReadGroup
		{
		Adc_UpdateStatusReadGroupInt
		{
		if (ADC_COMPLETED == Adc_aGroupStatus[Group].eConversion){
		Adc_aGroupStatus[Group].ResultIndex = 0U;
		}
		}
		}
		=> The "t_setupResultBuffer" is overwritten at the first index
		Preconditions:
		[...]
		Test Case ID (internal TC that caught the defect) optional:
		Adc_TC_FCT_0107, refer: https://bitbucket.sw.nxp.com/projects/ARTD/repos/test_adc/browse/generic/src/Adc_TC_FCT_0107.c
		Observed behavior:
		After calling Adc_ReadGroup function, the user result buffer index always resets to 0
		Expected behavior:
		Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)
		Proposed solution optional:

ID	Subtype	Headline and Description
ARTD-2250	New	New Feature [SPI] Improvement data configuration structure for multicore should be split for each core ,,"The theory(and req) says: ""ALL the configuration data parsed by the Init() function is to be split into different configuration structures, allocat*able in different memory regions to ensure HW isolation. If you have common runtime data, that needs to stay into an array indexed by the core ID"". In practice, we did not fully implement the Memory Mapping support yet, and we decided still that we want to split the data completely if possible, into independent structures, to better cope with it when we will add the MemMap support. Currently, SPI has common structure configuration for all cores. To follow the problem mentioned above. The elements in arraysChannels, Jobs, Sequences, ExternalDevices, HWUnit which are not allocated to that core will be NULL pointer."
ARTD-2384	Bug	[ADC] Adc_ReadRawData need to have more Det checking<*> 1, Adc_ReadRawData does not raise Det error with condition "NumItems is greater than the maximum number of channels available"- CPR_RTD_00508.adc 2, ADC_SAR_CDR_COUNT (48u) in driver but in RM only have physical channel from 0 to 39

ID	Subtype	Headline and Description

ARTD-2534	New	New Feature
		
		[can] Handling timeout implementation using OsIf
		,,"Add a referenceable enum in Tresos for OsIf that can be used by other drivers to allow selection only of available osif counter types
		
		In each module configuration that needs to implement a timeout add the following field
		<v:var name=""<Module>TimeoutMethod"" type=""ENUMERATION"">
		<a:a name=""LABEL"" value=""<Module> Timeout Method""/>
		<a:a name=""DESC"">
		<a:v>
		<![CDATA[EN:
		<html>
		 <Module>TimeoutMethod
		 Configures the timeout method.
		 Based on this selection a certain timeout method from OsIf will be used in the driver.
		 Note: If SystemTimer or CustomTimer are selected make sure the corresponding timer is enabled in OsIf General configuration.
		Note: Implementation Specific Parameter.
		</html>
		]]>
		</a:v>
		</a:a>
		<a:a name=""IMPLEMENTATIONCONFIGCLASS""
		type=""IMPLEMENTATIONCONFIGCLASS"">
		<icc:v vclass=""PreCompile"">VariantPreCompile</icc:v>
		<icc:v vclass=""PostBuild"">VariantPreCompile</icc:v>
		</a:a>
		<a:a name=""ORIGIN"" value=""M4_XDM_AR_MODULE_ORIGIN""/>
		<a:a name=""SCOPE"" value=""LOCAL""/>
		<a:a name=""SYMBOLICNAMEVALUE"" value=""false""/>
		<a:a name=""UUID"" value=""ECUC:7228a335-4003-4639-8e1a-bb3d9f762a7b""/>
		<a:a name=""DEFAULT"" value=""DummyTimer""/>
		<a:da name=""INVALID"" type=""XPath"">
		<a:tst expr=""node:refs('ASPathDataOfSchema:/M4_XDM_AR_PKG_NAME/Base/OsIfGeneral/OsIfUseCustomTimer') = 'false' and node:fallback(.,'DummyTimer') = 'CustomTimer'"" true=""Custom Timer is not enabled in OsIf (OsIfGeneral/OsIfUseCustomTimer checkbox)""/>
		<a:tst expr=""node:refs('ASPathDataOfSchema:/M4_XDM_AR_PKG_NAME/Base/OsIfGeneral/OsIfUseSystemTimer') = 'false' and node:fallback(.,'DummyTimer') = 'SystemTimer'"" true=""System Timer is not enabled in OsIf (OsIfGeneral/OsIfUseSystemTimer checkbox)""/>
		</a:da>
		<a:da name=""RANGE"">
		<a:v>DummyTimer</a:v>
		<a:v>SystemTimer</a:v>
		<a:v>CustomTimer</a:v>
		</a:da>
		</v:var>
		Based on its configuration generate an enum field of the type OsIf_CounterType (which is defined in OsIf.h and described below)
		// This is defined in OsIf.h
		typedef enum
		{
		OSIF_COUNTER_DUMMY, /**< dummy counter /
		#if (OSIF_USE_SYSTEM_TIMER == STD_ON)
		OSIF_COUNTER_SYSTEM, /**< system counter /
		#endif / (OSIF_USE_SYSTEM_TIMER == STD_ON) /
		#if (OSIF_USE_CUSTOM_TIMER == STD_ON)
		OSIF_COUNTER_CUSTOM /**< custom counter /
		#endif / (OSIF_USE_CUSTOM_TIMER == STD_ON) /
		} OsIf_CounterType;
		Use the generated value of the type described above to use the OsIf APIs for

ID	Subtype	Headline and Description
ARTD-2569	New	New Feature [uart] How to handle Det files in DS+CT projects ,,"Det files need to be added in a DS+CT project when HLD components are used so the drivers can be compiled when the development errors detection is enabled. The Det stub already has a manifest associated to it, so each driver that needs Det for a successful build should add Det as a dependency in its manifest. Example from the Adc driver: <component id=""platform.driver.adc"" full_name=""Adc"" brief=""Adc Component"" dependency=""platform.driver.det"" name=""Adc"" type=""driver"" devices=""S32K314 S32K324 S32K344 S32G233A S32G234M S32G254A S32G274A S32G274A_Rev2""> <source path=""Adc_TS_$(AR_RELEASE_ID)/src"" type=""src"" target_path=""RTD/src""> <files mask=""*.c""/> <files mask=""Adc_Sar_Ip_HwAccess.h""/> </source> <source path=""Adc_TS_$(AR_RELEASE_ID)/include"" type=""c_include"" target_path=""RTD/include""> <files mask=""*.h""/> </source> </component> "
ARTD-2663	Bug	[ADC] Group sw trigger injected transfer by DMA can not stream complete<*> Group sw trigger injected transfer by DMA can not stream complete because of jumping to isr handler with IMR register configured Adc_TS_014

ID	Subtype	Headline and Description
ARTD-2799	Bug	[WDG] Example displays some warnings when generating code or building<*> Detailed description (how to reproduce it): Step 1: pull code from tag WDG_016 and compile wdg plugin Step 2: open cygwin command and cd to project example path in WDG plugin folder Step 3: make generate; make build Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: Display some warings when generating code or building Build warning ../../../..//EcuM_TS_T40D11M9I0R0/src/EcuM.c: In function 'EcuM_ValidateWakeupEvent': ../../../..//EcuM_TS_T40D11M9I0R0/src/EcuM.c:180:86: warning: unused parameter 'events' [-Wunused-parameter] 180 FUNC(void, ECUM_CODE) EcuM_ValidateWakeupEvent(VAR(EcuM_WakeupSourceType, AUTOMATIC) events) ../../../..//EcuM_TS_T40D11M9I0R0/src/EcuM.c: In function 'EcuM_CheckWakeup': ../../../..//EcuM_TS_T40D11M9I0R0/src/EcuM.c:193:78: warning: unused parameter 'wakeupSource' [-Wunused-parameter] 193 FUNC(void, ECUM_CODE) EcuM_CheckWakeup(VAR(EcuM_WakeupSourceType, AUTOMATIC) wakeupSource) ../../../..//Gpt_TS_T40D11M9I0R0/src/Gpt_Ipw.c:333:12: warning: unused variable 'tempValue' [-Wunused-variable] 333 uint32 tempValue = 0U; ../../../..//Gpt_TS_T40D11M9I0R0/src/Gpt_Ipw.c:332:12: warning: unused variable 'counterValue' [-Wunused-variable] 332 uint32 counterValue = 0U; ../../../..//Gpt_TS_T40D11M9I0R0/src/Gpt_Ipw.c:331:12: warning: unused variable 'compareValue' [-Wunused-variable] 331 uint32 compareValue = 0U; generate/src/Wdg_43_Instance0_VS_0_PBcfg.c:101:5: warning: initialization discards 'const' qualifier from pointer target type [-Wdiscarded-qualifiers] 101 &Wdg_Ipw_OffModeSettings_0_VS_0 generate/src/Wdg_43_Instance0_VS_0_PBcfg.c:109:5: warning: initialization discards 'const' qualifier from pointer target type [-Wdiscarded-qualifiers] 109 &Wdg_Ipw_SlowModeSettings_0_VS_0 generate/src/Wdg_43_Instance0_VS_0_PBcfg.c:117:5: warning: initialization discards 'const' qualifier from pointer target type [-Wdiscarded-qualifiers] 117 &Wdg_Ipw_FastModeSettings_0_VS_0 generate warning: WARNING 20-10-27,11:15:32 (1159) Node /TS_T40D11M9I0R0/Wdg/WdgGeneral/WdgEcucPartitionRef defines two attributes with the same name "EDITABLE" which could not be merged. Removing one of the attributes WARNING 20-10-27,11:15:32 (1159) Node /Wdg_43_Instance1_TS_T40D11M9I0R0/Wdg/WdgGeneral/WdgEcucPartitionRef defines two attributes with the same name "EDITABLE" which could not be merged. Removing one of the attributes WARNING 20-10-27,11:15:33 (1159) Node /Wdg_43_Instance2_TS_T40D11M9I0R0/Wdg/WdgGeneral/WdgEcucPartitionRef defines two attributes with the same name "EDITABLE" which could not be merged. Removing one of the attributes WARNING 20-10-27,11:15:33 (1159) Node /Wdg_43_Instance3_TS_T40D11M9I0R0/Wdg/WdgGeneral/WdgEcucPartitionRef defines two attributes with the same name "EDITABLE" which could not be merged. Removing one of the attributes WARNING 20-10-27,11:15:33 (1159) Node /Wdg_43_Instance4_TS_T40D11M9I0R0/Wdg/WdgGeneral/WdgEcucPartitionRef defines two attributes with the same name "EDITABLE" which could not be merged. Removing one of the attributes WARNING 20-10-27,11:15:33 (1159) Node /Wdg_43_Instance5_TS_T40D11M9I0R0/Wdg/WdgGeneral/WdgEcucPartitionRef defines two attributes with the same name "EDITABLE" which could not be merged. Removing one of the attributes WARNING 20-10-27,11:15:33 (1159) Node /Wdg_43_Instance6_TS_T40D11M9I0R0/Wdg/WdgGeneral/WdgEcucPartitionRef defines two attributes with the same name "EDITABLE" which could not be merged. Removing one of the attributes
Release notes		

ID	Subtype	Headline and Description
ARTD-2826	Bug	[ADC] DMA have wrong result value when using streaming group<*> DMA test have wrong result value when configuring streaming group-Adc_TS_014
ARTD-2827	Bug	[ADC] driver can not stop continuous group configured without interrupt<*> In Adc_TS_019 CFG_SETS=2, group 5 is continuous without interrupt group, when calling stop group, this group can not stop and raising error time out. More detail in attachment

ARTD-2935	Bug	[GPT] Problem with getting index of channel for each core used for channel initialization<*>
		
		When i config multicore in EB, for instance i config 2 channel (index 0, 1) with core 4 and 2 channel with core 5 (index 2,3). I found that channel 2,3 will not be initialized because:
		for (ChannelIndex = 0U; ChannelIndex < Gpt_pConfig[coreID]->channelCount; ChannelIndex++)
		{ channel = Gpt_ConvertChannelIndexToChannel(ChannelIndex, coreID); ...; Gpt_Ipw_Init(((*(Gpt_pConfig[coreID]->Gpt_pChannelConfig))[channel].Gpt_Ipw_HwChannelConfig)); }
		This section in Gpt_Init() function will init channel in order of each core. when init core 5 , if the ChannelIndex is 0 then channel is 2 , it needs the index 2 in channel configuration array generated in output. But the channel config in output just have 2 elements:
		Gpt_Ipw_HwChannelConfigType Gpt_Ipw_ChannelConfig_PB_VS_0_P_EcucPartition_Cinque[2U];
		So it cannot get the thirst element in this array.
		I think this function should return valid index for channel, it means when channel configuration of core 5 have 2 element, the channel index will be 0 or 1.
		channel = Gpt_ConvertChannelIndexToChannel();

ARTD-2945	Bug	S32K3 RTD SIUL PTC22 Input<*> When configure S32K344 pins in S32DS, there is an error reported when PTC22 is set as eMIOS input. But actually it can be configured as input according to S32K3 ref manual.

ID	Subtype	Headline and Description
ARTD-3015	Bug	[S32DS 3.3 Update 1] Two settings with the same ID defined, and one has a wrong type, "REFERENCE" ,,"Create a configuration for any S32G2 derivative, go to Peripherals Tool and check the log file. There will be a message related to some settings that couldn't be found: !ENTRY com.nxp.swtools.periphs.model.data 4 0 2020-10-27 12:48:51.333 !MESSAGE An instance of ArraySetting with ID DioEcucPartitionRef contains an unresolvable reference with ID DioEcucPartitionRef to a setting in component with ID Dio and config-set with ID Dio !MESSAGE An instance of ArraySetting with ID DioChannelEcucPartitionRef contains an unresolvable reference with ID DioChannelEcucPartitionRef to a setting in component with ID Dio and config-set with ID Dio !MESSAGE An instance of ArraySetting with ID DioChannelGroupEcucPartitionRef contains an unresolvable reference with ID DioChannelGroupEcucPartitionRef to a setting in component with ID Dio and config-set with ID Dio !MESSAGE An instance of ArraySetting with ID DioPortEcucPartitionRef contains an unresolvable reference with ID DioPortEcucPartitionRef to a setting in component with ID Dio and config-set with ID Dio Check in the component file the settings and there will be some structs and arrays defined like: <struct id=""DioEcucPartitionRef""> <array id=""DioEcucPartitionRef"" type=""REFERENCE""> <description></description> <!--Tressos XPath for REFERENCE: ASPathDataOfSchema:/AUTOSAR/EcucDefs/EcuC/EcucPartitionCollection/EcucPartition--> </array> </struct>

ID	Subtype	Headline and Description
ARTD-3038	Bug	[CRYPTO] uint32_t is redefined in std_type defs.h<*> Description: uint32_t is redefined in std_type defs.h Vector are using Crypto module of the MCAL SW32K3_RTD_4.4_0.8.0_P02 with IAR compiler. The Crypto needs the hse interface. And now they get the following error messages: "D:\usr\usage\Delivery\CBD20x\CBD2000733\DELIVERY41653\external \ThirdParty\Mcal_S32k\Supply\SW32K3_RTD_4.4_0.8.0_P02\eclipse\plugins \Base_TS_T40D34M8I0R0\include\BasicTypes.h",52 Error[Pe256]: invalid redeclaration of type name "uint32_t" (declared at line 80 of "D:\usr\usage\Delivery\CBD20x\CBD2000733\DELIVERY41653\external\Thir dParty\Mcal_S32k\Supply\SW32K3_RTD_4.4_0.8.0_P02\eclipse\plugins\Cry pto_TS_T40D34M8I0R0\examples\EBT\Crypto_Example_001\include\std_type defs.h") "D:\usr\usage\Delivery\CBD20x\CBD2000733\DELIVERY41653\external \ThirdParty\Mcal_S32k\Supply\SW32K3_RTD_4.4_0.8.0_P02\eclipse\plugins \Base_TS_T40D34M8I0R0\include\BasicTypes.h",100 Error[Pe256]: invalid redeclaration of type name "int32_t" (declared at line 79 of "D:\usr\usage\Delivery\CBD20x\CBD2000733\DELIVERY41653\external\Thir dParty\Mcal_S32k\Supply\SW32K3_RTD_4.4_0.8.0_P02\eclipse\plugins\Cry pto_TS_T40D34M8I0R0\examples\EBT\Crypto_Example_001\include\std_type defs.h") For explanation: they do not have the included #include <stdint.h> #include <stdbool.h> #include <stddef.h> Proposal solution*: Remove the define of int8_t, uint8_t , int16_t , uint16_t, int32_t, uint32_t, uint64_t in file "W32K3_RTD_4.4_0.8.0_P02\eclipse\plugins\Cry pto_TS_T40D34M8I0R0\examples\EBT\Crypto_Example_001\include\std_type defs.h"
ARTD-3506	New	New Feature [CRYPTO]Exclusive Area analysis and update ,,Perform in depth analysis of the necessity of exclusive areas for global variables that remained unanalyzed after S32G2 Beta 090 release.

ID	Subtype	Headline and Description
ARTD-3509	Bug	[CAN][S32DS/HLD] Initialize default valid configuration for CAN<*> To prepare for testing S32ds, please set high priority for this task. Expectation: simplest/default configuration on EB and S32DS should be the same Steps: on EB: add CAN from from scratch add only one rx hw object, fix all errors on DS: same as above step minimum the changes of default values at above steps generate codes and comparing output => ds generate many invalid default values some default values are different from EB's one Expected behaviors: default values of S32DS can be valid and be same as EB's one => same start point when using both tools attached .xdm, .mex and output of two tools.
ARTD-3552	Bug	[CAN][S32G2] Fix compiler warning<*> Please refer to the attached file for more detail about warnings. They should be fixed in next release !
ARTD-3581	Bug	[CAN] Improve Cyclomatic Complexity<*> Please reduce cyclomatic complexity below 20 level thread should for functions FlexCAN_Ip_Init_Privileged FlexCAN_IRQHandler Can_Ipw_InitRx Can_Ipw_MainFunction_Read
ARTD-3603	Bug	[uart] - Fix traceability warnings<*> The cprt requirements need to be analyzed and if they are not implemented they should be There are many warnings in traceability reports, so they should be checked and corrected.

ID	Subtype	Headline and Description
ARTD-3610	New	New Feature [IP_Flexcan] status will be retuned only if FLEXCAN_DEV_ERROR_DETECT is ON. ,,"""The major change that will impact the code is that the return status like BUFF_OUT_OF_RANGE and some times the ERROR need to be guarded by (FLEXCAN_DEV_ERROR_DETECT == STD_ON)*""" Many requirements relate to above were applied but the implementation is not in place Expectation: The implementation, review should be done List of APIs have same this srs: *FlexCAN_Ip_SetBitrate* FlexCAN_Ip_SetBitrateCbt FlexCAN_Ip_SetRxFifoGlobalMask FlexCAN_Ip_SetRxIndividualMask FlexCAN_Ip_Init FlexCAN_Ip_SendBlocking FlexCAN_Ip_Send FlexCAN_Ip_ConfigRxMb FlexCAN_Ip_Receive, FlexCAN_Ip_SetTxArbitrationStartDelay, FlexCAN_Ip_SetTDCOffset"
ARTD-3636	New	New Feature [SPI] Move SpiDataWidth, SpiTransferStart, SpiDefaultData nodes from SpiPhyUnit to SpiExternalDevice for IP driver" ,,"Each PCS in the same SPI unit can be used to control one external slave. They can be required to have different value of SpiDataWidth, SpiTransferStart or SpiDefaultDta. Currently, for IP driver, these nodes are pushed into SpiPhyUnit container in IP component file. So it is not supported to change these value for each external Slave device. So, these nodes should be moved to SpiExternalDevice container for IP driver.
ARTD-3673	Bug	[CAN] handle the Det_ReportError inside Can_Init<*> Please look at the case When Can_Ipw_Init/Can_Ipw_InitRx fail: Can_Init will return with: Can_eControllerState[u8ControllerID] = CAN_CS_STOPPED; Can_eDriverStatus[u32CoreId] = CAN_READY; => this cause the next call of Can_Init or Can_SetControllerMode alway fail TC_ID: CAN_TC_FCT_*2662

ID	Subtype	Headline and Description
ARTD-3696	New	New Feature [Ip_Flexcan][FLEXCAN_IP_014_001] Implementation for FlexCAN_Ip_ReceiveBlocking ,,"FLEXCAN_IP_014_001 > FLEXCAN_IP_014_006 will be cover by FlexCAN_Ip_*ReceiveBlocking. The implementation for FlexCAN_Ip_ReceiveBlocking should be done FlexCAN_Ip_*SendBlocking* should note if this api does not support *Interrupt*. This api accepts TxInfo type"
ARTD-3698	New	New Feature [Ip_Flexcan] implementation for FlexCAN_Ip_RxFifoBlocking ,,"FLEXCAN_IP_017_001 => FLEXCAN_IP_017_009 relate to FlexCAN_Ip_RxFifoBlocking. Implementation for *FlexCAN_Ip_RxFifoBlocking should be done. Blocking method APIs now support POLL only?. This should be considered to add to doc/srs "
ARTD-3705	New	New Feature [ADC] Exclusive areas on ADC SAR and BCTU. Avoid multiple use also for CTU ,,"Implement exclusive areas https://nxp1.sharepoint.com/:p:/s/Zebra/EehFcYqIlpVJkmyNp8pcae4BNyizwm47eVxbN_s7u30Tzg?e=gTPmi7 Analyze and try to move in IPL, to have exclusive areas as small as possible. See details in presentation and recording"
ARTD-3722	Bug	[CAN][SWS_Can_00273] Bus-off handler need to cancel pending Tx<*> Can_Init Can_Write PduInfo0 with bus-off Recover from bus-off Can_Write PduInfo1 => PduInfo0 was not canceled, instead going to MAF Can_Write PduInfo1 always return BUSY interrupt should be checked also SWS_Can_*00273*:After bus-off detection, the Can module shall cancel still pending messages TC_ID: CAN_TC_FCT_*1681* [POLLing]

ID	Subtype	Headline and Description
ARTD-3731	New	New Feature [LIN][S32K3XX] Add synchronization transmission and reception ,,"Follow requirement # SyncSendData LPUART_LIN_008_001: Service name: Lpuart_Lin_Ip_SyncSendData Syntax: Lpuart_Lin_Ip_statusType Lpuart_Lin_Ip_SyncSendFrameData (uint32 u32Instance, const uint8 pTxBuff, uint8 u8TxSize); Sync/Async: Sync Reentrancy: Non Reentrant Parameters: [in] u32Instance LIN Hardware Interface u32u32Instance number [in] pTxBuff source buffer containing 8-bit data chars to send [in] u8TxSize the number of bytes to send Return value: STATUS_SUCCESS The transmission is successful STATUS_TIMEOUT The transmission has timeout Description: This function sends a frame using a synchronous method LPUART_LIN_008_002: his function shall send frame data out through the LIN Hardware Interface module using a blocking method. The function does not return until the transmission is completed. LPUART_LIN_008_003: This function shall return STATUS_SUCCESS, if the transmission is complete successfully. LPUART_LIN_008_004: This function shall return STATUS_TIMEOUT, if timeout has occurred. # SyncReceive LPUART_LIN_011_001: Service name: Lpuart_Lin_Ip_SyncReceiveFrameData Syntax: Lpuart_Lin_Ip_statusType Lpuart_Lin_Ip_SyncReceiveFrameDatas(uint32 u32Instance, uint8 pRxBuff, uint8 u8RxSize); Sync/Async: Sync Reentrancy: Non Reentrant Parameters: [in] u32Instance LIN Hardware Interface u32Instance number [out] u8RxBuff A pointer to the buffer containing 8-bit received data [in] u8RxSize The number of bytes to receive Return value: STATUS_SUCCESS The receives frame data is successful. STATUS_TIMEOUT The checksum is incorrect. STATUS_BUSY Bus busy flag is true. STATUS_ERROR Operation failed due is equal to 0 or greater than 8 or node's current state is in SLEEP mode Description: This function receives a frame in a synchronous manner. LPUART_LIN_011_002: This function shall get (receive) data from the LIN Hardware Interface module using a blocking method (This function shall not return until the receive is completed) LPUART_LIN_011_003: This function shall return STATUS_SUCCESS, if the transmission is complete successfully. LPUART_LIN_011_004: This function shall return STATUS_TIMEOUT, if timeout has occurred. "

ID	Subtype	Headline and Description
ARTD-3750	Bug	[UART] Fix compiler warnings<*> Fix compiler warnings
ARTD-3755	New	New Feature [LIN] Fix MISRA and CW ,,Fix MISRA and CW
ARTD-3767	Bug	[CAN][SWS_Can_00373] Can_Mainfunction_Mode shall call the function CanIf_ControllerModeIndication<*> A> Look inside Can_Ipw_MainFunction_Mode, obviously see that no call of CanIf_ControllerModeIndication is in place! => Need to be implemented as the srs: SWS_Can_*00373*: The function Can_Mainfunction_Mode shall call the function CanIf_ControllerModeIndication to notify the upper layer about a successful state transition of the corresponding CAN controller referred by abstract CanIf ControllerId, in case the state transition was triggered by function Can_SetControllerMode. B>* Can_SetControllerMode(Controller, CAN_CS_STARTED*); always return E_OK (see the implementation of FlexCAN_Ip_SetStartMode for detail) TC_ID: CAN_TC_FCT_*1685
ARTD-3770	New	New Feature [ADC] Add support for TempSense ,,Add support for TempSense functions as mentioned by requirements available in CPRT
ARTD-3777	New	New Feature [LIN][S32K3XX] Add exclusive areas ,,Add exclusive area

ID	Subtype	Headline and Description
ARTD-3780	Bug	[SPI] Make sure total frames in TX FIFO and RX FIFO lower than FIFO size<*> 1. For Ip_SyncTransmit(): After driver code read all frames in RX FIFO, if there are still some frames in TX FIFO, at the time before driver code check number of frames available in TX FIFO to prepare to fill TX FIFO. At that time, interrupt occurred, and the time to process interrupt is longer than the time to transfer all frames in TX FIFO. So TX FIFO will be empty and some frames received in RX FIFO, then the program is returned from interrupt and fill TX FIFO until full. And there is a interrupt occurred after that before read all frames in RX FIFO, and the time to process interrupt is longer than the time to transfer all frames in TX FIFO. So, RX FIFO can be overflow. 2. For Ip_AsyncTransmit(): The same situation with Ip_SyncTransmit() can be occurred. In SPI interrupt function Ip_TransferProcess(), after driver code read all frames in RX FIFO, if there are still some frames in TX FIFO, at the time before driver code check number of frames available in TX FIFO to prepare to fill TX FIFO. At that time, another interrupt occurred and preemptive current interrupt, and the time to process that interrupt is longer than the time to transfer all frames in TX FIFO. So TX FIFO will be empty and some frames received in RX FIFO, then the program is returned from that interrupt and fill TX FIFO until full and exist SPI interrupt function. And if there is a interrupt occurred with higher priority of SPI interrupt and the time to process that interrupt is longer than the time to transfer all frames in TX FIFO. So, RX FIFO can be overflow due to SPI interrupt function is not serviced to read RX FIFO.
ARTD-3787	Bug	[CAN] Driver does not prevent CanControllerDefaultBaudrate from being referenced to another controller's baud-rate configuration on tresos<*> Test configuration: Controller 0: The baud rate is configured to enable FD mode. (_ctrl0_bdr_cfg0_) Controller 1: The baud rate is configured to disable FD mode. (_ctrl1_bdr_cfg0_) Can Controller Default Baudrate (in controller 1) is referred to ctrl0_bdr_cfg0 Code generated successfully. This results in even if ctrl1_bdr_cfg0 is configured in normal-mode, but ram-block configuration is allowed and leading to some other undesired action. !image-2020-11-09-15-23-15-419.png!

ID	Subtype	Headline and Description
ARTD-3815	Bug	[Adc] Group conversions started after a Self-Test will have ADC_BUSY as group status<*> Detailed description (how to reproduce it): Adc group status can not change to ADC_STREAM_COMPLETED after implement self test because: Set up voltage: AN_2: 1V AN_5: 2V After group convert completely in ISR, AN_2 cdr register don't have valid bit and value is 0 as in attachment Preconditions: Enable self test feature Test Case ID (internal TC that caught the defect) optional: Adc_TC_FCT_301 Observed behavior: / Execute self-test function / t_u8SelfRet = Adc_SelfTest(t_u8HwUnitIndex); / Start ADC group conversion / Adc_StartGroupConversion(t_u16AdcGroupType); / Expected STREAM_COMPLETE group / EU_ASSERT(ADC_STREAM_COMPLETED == Adc_GetGroupStatus(t_u16AdcGroupType)); Real status: ADC_BUSY Expected behavior: Group status is ADC_STREAM_COMPLETED Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA

ID	Subtype	Headline and Description
ARTD-3821	Bug	[WDG] Configurator does not display any warning when Wdg_au32Timeout [Wdg_Instance] is overflowed<*> Detailed description (how to reproduce it): Step 1: Config ' Wdg configuration: AutosarExt: Wdg Enable Direct Service: FALSE Wdg Disable Allowed: TRUE Wdg Initial Timeout [s]: 0, 0.001, 32.0, 64.534, 65.535 Default mode setting: Wdg Timeout Period[s]: 1.0) Other mode WdgTimeoutPeriod: 10.0 Step 2: Call Gpt_Init function Step 3: Call Wdg_Init function Step 4: Delay-> Verification Point: The program is not reset Step 5: De-Initialize WDG Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: Wdg_TC_FCT_1006 Observed behavior: When Wdg_au32Timeout [Wdg_Instance] is overflowed but doesn't have any warning display for user: with Wdg_au16CfgInitialTimeout = 64.534 or 65.535 and Wdg_u32TriggerSourceClock = 80000 Detail was attached. Expected behavior: Displays warning to user when the Wdg_au32Timeout [Wdg_Instance] is overflowed Check also S32CT component
ARTD-3825	New	New Feature [S32K344] OCU: Align eMIOS IRQ code with MCL ,,"Align driver code with MCL eMIOS common interrupt handler implementation. MCL code will treat the common handler interrupt point and will route to driver that uses the corresponding channel."

ID	Subtype	Headline and Description
ARTD-3838	New	New Feature [PORT] Add support for touch senses feature for S32K3XX ,,"TSPC_PORT_001_001*: ""A function, named Siul2_Port_Ip_EnableOBEGroup shall enable the specified group whose pads are participating in simultaneous transition"" TSPC_PORT_001_002: The specifications for the Siul2_Port_Ip_EnableOBEGroup function shall be: Service name: Siul2_Port_Ip_EnableOBEGroup Syntax: void Siul2_Port_Ip_EnableOBEGroup(uint8 group); Sync/Async: Synchronous Reentrancy: Non Reentrant Parameters (in): group->number of the OBE group that has to be enabled Parameters (inout): None Parameters (out): None Return value: None Description: This function enables the specified group whose pads are participating in simultaneous transition. Available via: Tspc_Port_Ip.h TSPC_PORT_002_001*: ""A function, named Siul2_Port_Ip_ConfigureOBEGroup shall configure which channels participate in the OBE group."" TSPC_PORT_002_002: The specifications for the Siul2_Port_Ip_ConfigureOBEGroup function shall be: Service name: Siul2_Port_Ip_ConfigureOBEGroup Syntax: void Siul2_Port_Ip_ConfigureOBEGroup(uint8 group, uint32 groupValue_p); Sync/Async: Synchronous Reentrancy: Non Reentrant Parameters (in): group->number of the OBE group that has to be enabled Parameters (in): groupValue_p->Pointer to the first word of the OBE group configuration Parameters (inout): None Parameters (out): None Return value: None Description: This function enables the specified group whose pads are participating in simultaneous transition. Available via: Tspc_Port_Ip.h CPR_RTD_00439.port*: ""The Touch Sensing Pin Coupling support shall be enabled/ disabled using a parameter named TSPC Support Implemented in the PortGeneral container. The default value of this Parameter shall be FALSE"" CPR_RTD_00440.port*: ""The Group Output Buffer Select functionality shall be configurable for each Port Pin that supports this feature. For this, a parameter named OBE Group Select shall be implemented in the PortPin container. The OBE Group Select parameter can have the following values NO_OBE_GROUP, OBE_GROUP1, OBE_GROUP2 ... . The default value for the OBE Group Select shall be NO_OBE_GROUP (no simultaneous OBE transition). This parameter shall be editable only when TSPC Support is configured as TRUE"""

ID	Subtype	Headline and Description
ARTD-3930	Bug	[ADC] The notification field is not defined for use in the Adc_CtuEnableNotification, Adc_CtuDisableNotification function. ,,"Detailed description (how to reproduce it): The notification field is not defined for use in the Adc_CtuEnableNotification, Adc_CtuDisableNotification function. Preconditions: Check ADC use BCTU mode. Observed behavior: The notification field is not defined for use in the Adc_CtuEnableNotification, Adc_CtuDisableNotification function. Expected behavior: The notification field is defined for use in the Adc_CtuEnableNotification, Adc_CtuDisableNotification function. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ARTD-3935	Bug	[SPI] Do nothing and return E_NOT_OK when set LSB and Frame size fail<*>
		
		in Spi_Ipw_SyncTransmit :
		Before call IP_Sync function to perform transmission for the channel, LSB and Framesize setup function were called but after that, it call Ip_Sycn function without check the status return of those fucntion. it should be like:
		Status = Lpspi_Ip_UpdateFrameSize();
		if(Status = OK)
		{
		Status = Lpspi_Ip_UpdateLsb();
		if(Status = OK)
		{
		status = Lpspi_Ip_SyncTransmit();
		}
		}

ARTD-3938	Bug	[SPI] The number of bytes transfer of channel should be configured corresponding to frame size of channel<*> Currently, SPI driver is supporting transfer with frame size is 4 to 32 bits. The design of driver now will lose some bytes of each channel if it don't have the compatible configuration: Details: If framesize is 16, number of bytes transfer is not divisible by 4 then all surplus bytes (%4) will be lost and missed. the same for 32 bits mode Solving: IB: In configuration, update a invalid expression to prevent user configure wrong number of bytes transfer for each channel. (example on EB tresos: SpiIbNBuffers and SpiDataWidth must be compatible) EB: Should be added a detect error for this case in Spi_SetupEB() function. Take a note in UM document to mention user can has valid channel configuration

ID	Subtype	Headline and Description
ARTD-4000	Bug	[uart] Update the used schema for all the .component files to 8.0 version<*> The used version for the component file from the header should be updated to 8.0 to be compatible with the S32CT framework version. If it is not updated, when the .component validation is done, will fail and the component file will not be loaded with success. xsi:schemaLocation="http://swtools.freescale.net/XSD/component/1.0 http://swtools.freescale.net/XSD/component/1.0/component.xsd" should be updated to: xsi:schemaLocation="http://swtools.freescale.net/XSD/component/1.0 http://swtools.freescale.net/XSD/component/1.0/component-8.0.xsd"
ARTD-4008	Bug	[qd] Update the used schema for all the .component files to 8.0 version<*> The used version for the component file from the header should be updated to 8.0 to be compatible with the S32CT framework version. If it is not updated, when the .component validation is done, will fail and the component file will not be loaded with success. xsi:schemaLocation="http://swtools.freescale.net/XSD/component/1.0 http://swtools.freescale.net/XSD/component/1.0/component.xsd" should be updated to: xsi:schemaLocation="http://swtools.freescale.net/XSD/component/1.0 http://swtools.freescale.net/XSD/component/1.0/component-8.0.xsd"

ID	Subtype	Headline and Description
ARTD-4027	Bug	[ICU] Review attached reported errors images and correct<*> Review attached images on the parent ticket and conclude if fixes are done. <<Follow up for issues reported on EAR phase and update code and configuration see attachement and <[test team link https://nxp1-my.sharepoint.com/personal/viet_nguyen_nxp_com/_layouts/15/onedrive.aspx?id=%2fpersonal%2fviet_nguyen_nxp_com%2fDocuments%2fNotebooks]>> # [[FIXED] BUG_ICU_010: Some functions have no prototype|#BUG_ICU_010%20Some%20functions%20have%20no%20&section-id=612f7f9c-f779-4595-a0f6-1e81015370f8&page-id=6086406f-bef7-49a1-ad89-194e6e25e07d&end] ([Web view|https://nxp1-my.sharepoint.com/personal/viet_nguyen_nxp_com/_layouts/15/Doc.aspx?sourcedoc=\{d858b9ba-6641-4816-9d4a-2223dcea36f5}&action=edit&wd=target%28ICU.one%7C612f7f9c-f779-4595-a0f6-1e81015370f8%2FBUG_ICU_010%20Some%20functions%20have%20no%20%7C6086406f-bef7-49a1-ad89-194e6e25e07d%2F%29&wdorigin=703&wdpreservelink=1]) > For this bug we have to eliminate Emios_Icu_Ip_EnableChannel() an Emios_Icu_Ip_DisableChannel() from ICU EMIOS IP code and use functions from MCL: Emios_Mcl_Ip_EnableChannel() and Emios_Mcl_Ip_DisableChannel(). # [[FIXED] [DevReview]BUG_ICU_009: The Masterbus counter is turned off when transmitting the Icu_DeInit () function.|#%5BDevReview%5DBUG_ICU_009%20The%20&section-id=612f7f9c-f779-4595-a0f6-1e81015370f8&page-id=f6a0bc77-192c-46d4-82ff-5fdf37d3d3ef&end] ([Web view|https://nxp1-my.sharepoint.com/personal/viet_nguyen_nxp_com/_layouts/15/Doc.aspx?sourcedoc=\{d858b9ba-6641-4816-9d4a-2223dcea36f5}&action=edit&wd=target%28ICU.one%7C612f7f9c-f779-4595-a0f6-1e81015370f8%2F%5BDevReview%5DBUG_ICU_009%20The%20%7Cf6a0bc77-192c-46d4-82ff-5fdf37d3d3ef%2F%29&wdorigin=703&wdpreservelink=1]): No driver should change global configuration of EMIOS without assuring it using all the instance or all the channels for a specific MusterBus, for this we have MCL functions to change the global configuration. # [[FIXED] BUG_ICU_011: Max counter is not set in Edge count function|#BUG_ICU_011%20Max%20counter%20is%20not%20&section-id=612f7f9c-f779-4595-a0f6-1e81015370f8&page-id=088f5935-19df-48df-89a2-e8745fb3e9ab&end] ([Web view|https://nxp1-my.sharepoint.com/personal/viet_nguyen_nxp_com/_layouts/15/Doc.aspx?sourcedoc=\{d858b9ba-6641-4816-9d4a-2223dcea36f5}&action=edit&wd=target%28ICU.one%7C612f7f9c-f779-4595-a0f6-1e81015370f8%2FBUG_ICU_011%20Max%20counter%20is%20not%20%7C088f5935-19df-48df-89a2-e8745fb3e9ab%2F%29&wdorigin=703&wdpreservelink=1]) Spoke again with tester about this BUG. VERIFY THAT ALL FUNCTIONS CAN BE USED IN BOTH MODES: AUTOSAR AND IPL standalone.

ID	Subtype	Headline and Description
ARTD-4054	Bug	[ADC] Adc group status can not change to ADC_STREAM_COMPLETED when using Module clock frequency / 8<*> Detailed description (how to reproduce it): Adc group status can not change to ADC_STREAM_COMPLETED when using Module clock frequency / 8 because: Set up voltage: AN_48: presampling, by pass pre sampling 0V AN_95: presampling, by pass pre sampling 3.3V After group convert completely in ISR, AN_48 cdr register don't have valid bit and value is 0 as in attachment In RM there are some conflicts: MCR_ADCLKSEL select Module clock frequency / 8 is valid but in chapter 23 clock source for div8 is not valid as attachment Preconditions: Using ADCLKSEL = 0x3 (Module clock frequency / 8) Test Case ID (internal TC that caught the defect) optional: Adc_TC_FCT_0301 Observed behavior: / Start ADC group conversion / Adc_StartGroupConversion(t_u16AdcGroupType); / Expected STREAM_COMPLETE group / EU_ASSERT(ADC_STREAM_COMPLETED == Adc_GetGroupStatus(t_u16AdcGroupType)); Real status: ADC_BUSY Expected behavior: Group status is ADC_STREAM_COMPLETED Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-4370	Bug	[S32K3][EMIOS][MCL] Enabling EmiosMclLowPowerMode will prevent user from creating config channels in Emios Master Buses tab<*> Enabling EmiosMclLowPowerMode will prevent user from creating config channels in Emios Master Buses tab !MicrosoftTeams-image.png|thumbnail!
ARTD-4393	Bug	[S32K3][MCL] Cannot use the IRQ function in Emios_Mcl_Ip_Irq.c file<*> There's MCL_EMIOS_0_CH_X_ISR_USED(Emios_Mcl_Ip_Irq.c file). But i don't see it generated or defined anywhere, user cannot use the IRQ function

ID	Subtype	Headline and Description
ARTD-4397	Bug	[CAN] Can_SetControllerMode shall cancel pending msg in case of Rx mailbox/ POLL<*> !image-2020-11-19-11-01-47-182.png! IIn case of POLL Rx processing type, abort will not work because FLEXCAN_MB_RX_BUSY == state->mbs[mb_idx].state only be satified if main_function_read was called All flags should be cleared before module enter stop mode, if not, Main_function API that can be called after that and executing processing in stop-mode can cause unexpected behavior IC_ID: CAN_TC_FCT_*1584 CAN_TC_FCT_5552 => for FIFO
ARTD-4401	Bug	[GPT] The Standby wakeup feature of Gpt does not work correctly according to the requirement<*> After calling Gpt_Init function, I found that the counter bit and interrupt bit of RTC IPW is cleared. So this does not match with the requirement as following: The Gpt driver shall provide an optional configuration parameter to support wakeup IP operation across STANDBY. Per default this optional functionality and configuration parameters shall be disabled. If the configuration parameter is enabled, the following shall be respected: The driver shall NOT CLEAR the interrupt flag, the interrupt enable bit and also should not disable the counter, during init, after a wakeup event. Please refer to the image attached to see error.
ARTD-4418	Bug	[SPI] Expression to check maximum "instance" is not correct ,,"if (instance > LPSPI_INSTANCE_COUNT) Should be replaced by if (instance >= LPSPI_INSTANCE_COUNT)
ARTD-4427	Bug	[BASE] OsIf_Internal.h may not found the macro USING_OS_AUTOSAROS<*> OsIf_Internal.h has the follwoing section: #if defined(USING_OS_AUTOSAROS) #include "Os.h" #endif / defined(USING_OS_AUTOSAROS) / But OsIf_Cfg.h is not included so that USING_OS_AUTOSAROS is never defined.
ARTD-4439	Bug	[SPI] SPI module use wrong function name for exclusive area<*> Spi uses defines like SchM_Enter_Spi_EXCLUSIVE_AREA_00(); It should be SchM_Enter_Spi*_SPI*_EXCLUSIVE_AREA_00()
ARTD-4446	Bug	[S32K3][EMIOS_MCL] Refactor EMIOS functions with respect to requirements<*> The following APIs should be merged in one to respect for the ZTH arhitecture: Emios_Mcl_Ip_InitChannel Emios_Mcl_Ip_InitInstance => Emios_Mcl_Ip_Init() which will respect the next requirement: EMIOS_MCL_IP_001_001 Emios_Mcl_Ip_DinitChannel Emios_Mcl_Ip_DeinitInstance => Emios_Mcl_Ip_Deinit() which will respect the next requirement: EMIOS_MCL_IP_002_001

ID	Subtype	Headline and Description
ARTD-4457	Bug	[S32K3XX][GPT] The return value of PIT RTI Timer is wrong after starting timer<*> After starting timer PIT RTI by calling function Gpt_StartTimer with the target timer value as a parameter, in term of requirement, the value of elapsed time must to be 0 because Timer just start to running. But when i debug this, the real elapsed value of timer equals the target timer value. I saw in debug interface that the counter of PIT RTI Timer after calling Gpt_StartTimer function, the counter of RTI has not yet started because some issue related to the delay of counter. I think this problem maybe is referred to some information in RM but i am not sure. I attached an image when i debugged this, please refer to it to see the problem more details.
ARTD-4468	Bug	[WDG] The S32CT example project has warnings<*> Detailed description (how to reproduce it): Step 1: Import example project into S32DS Step 2: Open Peripherals tab and Update code Step 3: Build code Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: The example project issues warnings at generation and build stage Actually, only one of these warning caused by swt_ip component which's "WDG_RAM undefined" Detail was attached. Expected behavior: The project no warnings, errors after generate and build code Fix typos in description.txt: *application, through
ARTD-4470	Bug	[S32K3XX][I2C] I2c baudrate at I2cHighSpeedModeConfiguration container always check I2c prescaler<*> I2c baudrate at I2cHighSpeedModeConfiguration container always check I2c prescaler in Master Mode
ARTD-4472	Bug	[PORT] Not all GPI mode were defined as Only input mode in Port driver for S32K3XX<*> The GPI mode are configuring as Only Input mode in csv files. It is incorrect
ARTD-4485	New	New Feature [S32K3XX][I2C] Should add Det to avoid the StartListening is called when SlaveListening is true ,,Should add Det to avoid the StartListening is called when SlaveListening is true
ARTD-4498	New	New Feature [UART] - Fix memory sections ,,The memory sections shall be added/fixed in the lpuart and flexio drivers.

ID	Subtype	Headline and Description
ARTD-4502	Bug	[S32K3XX][MCU][S32CT][EXAMPLE] Compiler warning on S32CT when build for gcc<*> Detailed description (how to reproduce it): Step 1: Import example project into S32DS Step 2: Open Peripherals tab and Update code Step 3: Build code Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: All examples use MCU when build code is warning after updating the code. Detail was attached. Expected behavior: The project no warnings, errors after build code. Readme for clock and power is incorrect
ARTD-4505	Bug	[Uart] First byte is wrong when transmit data after using Abort function<*> First byte is wrong when transmit data after using Abort function: Expect sending data : 0x01; 0x02;0x03;0x4;0x05;0x06;0x07;0x08 Reception data : 0xff; 0x01; 0x02;0x03;0x4;0x05;0x06;0x07
ARTD-4510	Bug	[PWM] Cannot update duty cycle value at runtime when newDutyCycle is greater than old period value<*> In Emios_Pwm_Ip_SetDutyCycle function, Register B not update intermediate at runtime, so when we gets the value from reg B , it still return old period value. It cause EMIOS_PWM_STATUS_ERROR when newDutyCycle value is greater than old period value.
ARTD-4520	Bug	[PWM] Check DevAssert is not correct in Emios_Pwm_Ip_InitEdgePlacementMode function<*> in OPWMB mode, selected counter bus should be MCB Up counter. So, condition: DevAssert(EMIOS_IP_MCB_UP_DOWN_COUNTER == Emios_Pwm_Ip_GetCounterBusMode(instance, userChCfg->channelId, userChCfg->timebase)); is not correct. It should be compare with EMIOS_IP_MCB_UP_COUNTER In Emios_Pwm_Ip_GetCounterBusPeriod function, you are using Emios_Mcl_Ip_GetCounterBusMode, and input channel parameter is eMios channel that configured in PWM. It will get counter bus mode = 0, because we haven't configured it yet. So, it is always equal to the BUS_A value. it is not correct. it should be channel that configured by MCL to check using counter bus
ARTD-4522	Bug	[PWM] Pwm_SetPeriodAndDuty function cannot run with input period value = 0<*> When use Pwm_SetPeriodAndDuty function with eMios ipv Emios_Pwm_Ip_SetPeriod function, we cannot pass condition: DevAssert(EMIOS_PWM_MIN_CNT_VAL <= newPeriod); when EMIOS_PWM_MIN_CNT_VAL =1; Please follow requirement: SWS_Pwm_00150: If the period is set to zero the setting of the duty-cycle is not relevant. In this case the output shall be zero (zero percent duty-cycle) for Pwm_SetPeriodAndDuty function

ID	Subtype	Headline and Description
ARTD-4526	Bug	[WDG] The Tresos example project issue warnings at generation stage<*> Detailed description (how to reproduce it): Step 1: Compile plugin Step 2: Use cmd command to "E:\Zebra\Repo\S32K3XX\output\eclipse\plugins \Wdg_TS_T40D34M8I1R0\examples\EBT\Wdg_Example" Step 3: make clean generate Step 4: make build Step 5: make run Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: The project generate code display some warnings Fix typos in wdg_example_readme.txt* (EB) and description.txt (S32CT): aplication, throguh, instalation Detail was attached. Expected behavior: The project generate code no warnings, errors Fix typos in description.txt: *application, through, installation
ARTD-4533	Bug	[I2c][S32K3XX] Interrupt flag should be cleared for spurious interrupts<*> Interrupt flag should be cleared for spurious interrupts.
ARTD-4535	Bug	[S32K3XX] FLS Missing declare variable ProgrammedData in C40_Ip.c<*> the 'pProgrammedData' variable is undefine at line 1064 of C40_Ip.c when :below nodes to be set such as: (STD_ON == C40_ATERNATE_INTERFACE_ENABLED) and (C40_ERASE_VERIFICATION_ENABLED = STD_ON) and (STD_OFF == C40_PROGRAM_VERIFICATION_ENABLED) and (STD_OFF == C40_IP_SYNCRONIZE_CACHE)
ARTD-4540	Bug	[CAN] Multicore issue with K3 platform, with enabled cache ,,"Multicore can not be executed See attached file for details. if put global array to non-cache region. issue can be solved TC_ID: CAN_TC_MC_0560
ARTD-4550	Bug	[SPI] Fix misra violation on DSPI and FLEXIO<*> Fix misra violation

ID	Subtype	Headline and Description
ARTD-4555	Bug	[ADC] Fix remaining static analysis violations (MISRA + HIS + CERT-C)<*> All static analysis need to be fixed for the BETA release. Everything needs to be fixed in the code or commented in Coverity if it cannot be fixed. The following wiki is work in progress, but it will be updated with all needed information: [https://confluence.sw.nxp.com/pages/viewpage.action?pageId=133734230]
ARTD-4558	New	New Feature [SENT] Fix VSMD warnings ,,"The following warnings from the VSMD reports must be fixed : Rule A205: Reference 'Sent/SentConfigSet/SentControllerConfig/SentControllerEcucPartitionRef' has no 'ECUC-VALUE-CONFIGURATION-CLASS' elements. Rule A205: Parameter 'Sent/SentConfigSet/SentControllerConfig/SentChannelConfig/SentFastCRCErrorNotification' has no 'ECUC-MULTIPLICITY-CONFIGURATION-CLASS' elements. Rule A205: Parameter 'Sent/SentConfigSet/SentControllerConfig/SentChannelConfig/SentSlowCRCErrorNotification' has no 'ECUC-MULTIPLICITY-CONFIGURATION-CLASS' elements. Rule A205: Parameter 'Sent/SentConfigSet/SentControllerConfig/SentChannelConfig/SentFastNotification' has no 'ECUC-MULTIPLICITY-CONFIGURATION-CLASS' elements. Rule A205: Parameter 'Sent/SentConfigSet/SentControllerConfig/SentChannelConfig/SentSlowNotification' has no 'ECUC-MULTIPLICITY-CONFIGURATION-CLASS' elements. Rule A207: 'Empty string' should not be used as default value of parameter 'Sent/CommonPublishedInformation/VendorApiInfix'. Rule A220: UUID 'ECUC:4e05c426-67f4-4e47-b644-7749e78ec98d' is not unique for 'SentTimeout'"
ARTD-4560	Bug	[CAN] implement Dma Error notification for enhance fifo & Missing 'ECUC-MULTIPLICITY-CONFIGURATION-CLASS' for optional Node (TpsEcuc_08037)<*> CanEnhanceFiFoDmaRef is an optional node, => need to have ECUC-MULTIPLICITY-CONFIGURATION-CLASS. need to update: <a:a name="IMPLEMENTATIONCONFIGCLASS" type="IMPLEMENTATIONCONFIGCLASS"> <icc:v vclass="PreCompile">VariantPreCompile</icc:v> <icc:v vclass="PreCompile">VariantPostBuild</icc:v> </a:a> to: <a:a name="IMPLEMENTATIONCONFIGCLASS" type="IMPLEMENTATIONCONFIGCLASS"> <icc:v vclass="PreCompile">VariantPreCompile</icc:v> <icc:v vclass="PreCompile">VariantPostBuild</icc:v> <icc:v mclass="PreCompile">VariantPreCompile</icc:v> <icc:v mclass="PreCompile">VariantPostBuild</icc:v> </a:a>

ID	Subtype	Headline and Description
ARTD-4599	New	New Feature [ADC] ADC_SAR IPL S32CT add a more user-friendly method for enabling the channels in each chain ,,"If my assumption is correct, for now, in order to enable ADC channels in either Normal or INJECTED chain, user must compute an type the masks for the desired channels. This forces the user to read the ADC chapter from the Reference Manual, to get the channels mapping, identify the correct registers and compute the values. This complicates too much the process for the end user. !image-2020-11-25-17-15-15-003.png! This process can be simplified for the end user by replacing the above fields with some checkboxes for each channel. My suggestion is to have a look on the S32SD for Power Architecture PEX options for the ADC, because the MPC5744P has a very similar ADC peripheral. More than that, why the Channel configuration array should have at leas one element if, for example I don't want to have the below notifications enabled for none of the channels enabled in the above fields, only the end of chain notification? !image-2020-11-25-17-41-06-410.png|width=545,height=133! To have an idea on why we request this, let me explain the following scenario: In Model-Based Design Toolbox, we create blocks for Simulink that will generate C code automatically. If a user needs an ADC conversion, he/she will add an ADC block. The block will open Config Tools. Now the user must read the RM, understand how the ADC works, compute registers values and then set the other proper settings. While he could just open the Config Tools, enable every channel with one click, and that's it."
ARTD-4600	Bug	[I2C][S32K3XX] Fix MISRA violations for I2c driver<*> All MISRA errors should be fixed/motivated for I2c driver.
ARTD-4601	New	New Feature [ICU] Provide API for reading the comparator status ,,"NewWorkDescription: The Icu driver shall provide an API for reading the comparator status It shall allow the user to pool for the status on selected comparator and return a value for distinguishing if comparator was triggered or not. Icu_GetInputState(logic_channel); Considered that this ticket should not add new HLD requirement at this point. The API should be implemented and requested on IP level as Cmp_Ip_TriggerStateType Cmp_Ip_GetStatus(cmp_channel); Requirement source: Customer Request (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Provide an API as in NW Description. The API will return if the current selected CMP resource was triggered or not and will clear the status after reading."
ARTD-4602	Bug	[ICU] Align eMios icu CT component generation to ebt ip generation<*> Update and correct emios generation in ct for icu. Perform a check with DS example and build emios icu with new mcl.

ID	Subtype	Headline and Description
ARTD-4605	Bug	[SAI] Fix remaining static analysis violations (MISRA + HIS + CERT-C)<*> All static analysis need to be fixed for the BETA release. Everything needs to be fixed in the code or commented in Coverity if it cannot be fixed. The following wiki is work in progress, but it will be updated with all needed information: https://confluence.sw.nxp.com/pages/viewpage.action?pageId=133734230

ARTD-4618	Bug	[WDG] Does not return error status when the unlock sequence is not successful after a timeout loop<*>
		
		Should return status error when software unlock is not successful after timeout loop.
		/* Soft lock */
		if ((base->CR & SWT_CR_SLK_MASK) != 0U)
		{
		/* Unlocks sequence */
		base->SR = SWT_SR_WSC(SWT_IP_UNLOCK_VALUE1);
		base->SR = SWT_SR_WSC(SWT_IP_UNLOCK_VALUE2);
		/* Waits unlock complete */
		while (((base->CR & SWT_CR_SLK_MASK) != 0U) && (timeout-- > 0))
		{
		/* Do nothing */
		}
		}

ARTD-4625	Bug	[SPI][LPSPI] IER register was clearing twice in Lpspi_Ip_AsyncTransmit function<*> in Lpspi_Ip_AsyncTransmit, if current master mode is Polling, it is clearing IER register twice.

ARTD-4626	Bug	[PWM]Emios_Pwm_Ip_GetCounterBusPeriod confused with Emios_Ip_GetCounterBusMode<*>
		
		The function "Emios_Pwm_Ip_GetCounterBusPeriod" called "Emios_Ip_GetCounterBusMode" because it needs to know the counter bus type.
		The following line of code is of problem:
		chBusMode = Emios_Ip_GetCounterBusMode(instance, channel);
		chBusMode is "Emios_Pwm_Ip_CounterBusSourceType";
		But function "Emios_Ip_GetCounterBusMode" returns "Emios_Ip_MasterBusModeType". They are different.
		
		Maybe we should add another API function as following:
		Emios_Pwm_Ip_CounterBusSourceType Emios_Ip_GetCounterBusSource(uint32 instance, uint8 channel)
		{
		eMIOS_Type base = Emios_Ip_Bases[instance];
		return (base->CH.UC[channel].C & eMIOS_C_BSL_MASK) >> eMIOS_C_BSL_SHIFT;
		}

ID	Subtype	Headline and Description
ARTD-4639	Bug	[ADC] The value config class of node "BctuFifoDmaBuffer", "BctuFifoDmaChannelId" is invalid ,,"Detailed description (how to reproduce it): Use EB Tresos config with case variant = 3. The nodes BctuFifoDmaBuffer"", ""BctuFifoDmaChannelId"" have the value config class is Precompile but when configuring, the values in other variants will not change. Preconditions: NA Observed behavior: when configuring, the values in other variants will not change. Expected behavior: when configuring, the values in other variants will change. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-4641	Bug	[S32K344 BETA] GPT compiler warnings<*> Please refer to the attached file to see the detail error
ARTD-4648	Bug	[ADC] The function "Adc_ReportDetError" declared implicitly when configuration AdcEnableReadRawDataApi is true and AdcDevErrorDetect is false ,,"Detailed description (how to reproduce it): when configuration AdcEnableReadRawDataApi is true and AdcDevErrorDetect is false => the build fails Adc_TS_COT_003 CFG_SETS=81. Preconditions: N/A Observed behavior: ...\output\eclipse\plugins\Adc_TS_T40D34M8I1R0\src\Adc.c"",4519 Error[Pe223]: function ""Adc_ReportDetError"" declared implicitly Expected behavior: In this case, it will build success. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-4652	New	New Feature [S32K3XX][PWM] Fix and comment static analysis violations (MISRA + HIS + CERT-C) ,,"All static analysis need to be fixed for the BETA release. Everything needs to be fixed in the code or commented in Coverity if it cannot be fixed. The following wiki is work in progress, but it will be updated with all needed information: [https://confluence.sw.nxp.com/pages/viewpage.action?pageId=133734230] "

ID	Subtype	Headline and Description
ARTD-4653	Bug	[PWM] Pwm_Notification has no prototype<*> STDERR:"C:\vv_tools\eb\EB_tresos_Studio_27.1.0_b200625-0900_02\plugins\Pwm_TS_T40D34M8I1R0\src\Pwm.c",2253 Error[Pa045]: function "Pwm_Notification".mcal_text"" has no prototype. It causes a build error with IAR compiler.
ARTD-4667	New	New Feature [FLS] Remove all redundant code relate to IRQ mode ,,"Since Fls driver no longer supports IRQ mode, all redundant code should be removed"
ARTD-4669	Bug	[PWM] Fix Compiler warning for S32K3XX EAR 0.8.1<*> Fix Compiler warning for PWM S32K3XX EAR 0.8.1. Please see in attach file.
ARTD-4679	Bug	[PWM] Pwm_SetOutputToIdle function is not working as expected<*> Pwm_SetOutputToIdle function is not working as expected. It just sets the required PWM pin state for current cycle and continues with normal PWM operation from next cycle. Due Force Match bit is always automatically returned the field to 0.
ARTD-4682	New	New Feature [SPI] Change SpiPhyUnitAsyncMethod to boolean node SpiPhyUnitAsyncUseDma ,,"Meaning of SpiPhyUnitAsyncMethod node is to select Asynchronous mechanism with DMA or not. So, that node can operate as an boolean node SpiPhyUnitAsyncUseDma. if SpiPhyUnitAsyncUseDma = false, the AsyncTransmit can be operated with interrupt or polling of SPI transfer flags. if SpiPhyUnitAsyncUseDma = true, the AsyncTransmit can be operated with interrupt or polling of DMA done flag."
ARTD-4715	Bug	[SPI] CS will be cleared during continues transfer<*> 1, CS will be cleared during continues transfer if second command with CONT =1 and CONTC =1 is written immediately after first command with CONT =1 and CONTC =0. Seem second command will be delayed to updated. =>So, In continuous CS, only set new command with CONTC=1 for next channel in Job(first command for first channel in Job should have CONTC = 0). 2, In slave mode, if data is filled into TX FIFO then reset TX FIFO by CR[RTF]=1 will not clear shifter. => So, Ip_Cancel() function must use software reset bit CR[RST] to clear old data in shifter. 3, In Master mode and under debug mode, CR[DBGEN] = 0, CS will be cleared automatically when CPU halt at breakpoint regardless of TCR[CONT]=1 or TCR[CONTC]=1. => CR[]BGEN] should be enabled to ensure CS will be kept when CPU halts at breakpoint.

ID	Subtype	Headline and Description
ARTD-4773	Bug	[ADC] Data conversion should not be recorded for disabled channels<*> Data conversion should not be recorded for disabled channels Limit check is still checked even for channels that are disabled via ADC_ENABLE_CH_DISABLE_CH_NONAUTO_API
ARTD-4836	Bug	[Uart] Macro in driver does not observed description in requirement<*> Driver is using naming macro "UART_E_INVALID_COREID" But in requirement, this macro must be UART_E_PARAM_CONFIG CPR_RTD_00420.uart|If DET error reporting is enabled, the UART will check upon each API call if the requested resource is configured to be available on the current core, and in case of error will return UART_E_PARAM_CONFIG.
ARTD-4833	New	New Feature [PORT] Add Port_SetAsUnusedPin and Port_SetAsUsedPin functionality for S32K3XX ,,"NewWorkDescription: Implement requirements: CPR_RTD_00425.port: The function void Port_SetAsUnusedPin(Port_PinType Pin) shall configure the referenced pin with all the properties specified in the NotUsedPortPin container. CPR_RTD_00426.port: If Det is enabled, the function Port_SetAsUnusedPin shall report PORT_E_MODE_UNCHANGEABLE error and return without any other action, if the parameter PortPinModeChangeable is set to FALSE CPR_RTD_00427.port: The function void Port_SetAsUsedPin(Port_PinType Pin) shall configure the referenced pin with all the properties that where set during the Port_Init operation. CPR_RTD_00428.port: If Det is enabled, the function Port_SetAsUsedPin shall report PORT_E_MODE_UNCHANGEABLE error and return without any other action, if the parameter PortPinModeChangeable is set to FALSE. CPR_RTD_00429.port: Port_SetAsUnusedPin and Port_SetAsUsedPin functionalities will be enabled/disabled by using a boolean precompile parameter named ""Port Set As Unused Pin API"" Requirement source: CPR_RTD_00425.port, CPR_RTD_00426.port, CPR_RTD_00427.port, CPR_RTD_00428.port, CPR_RTD_00429.port (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional:"
ARTD-4844	Bug	[GPT] The channel number checking of PIT in driver is wrong result to hardfault error<*> With resource of S32G274, The number channel of PIT 0 is not equal to PIT 1. So the number channel checked in interrupt function must to be diferrent each other between PIT 0 and PIT1. In addition, in case the PIT instance contains RTI channel, it should be checked to differentiate between some chip. Please refer to attached image to see the issue.

ID	Subtype	Headline and Description
ARTD-4849	New	New Feature [ADC]: CTU Trigger Mode support with HW triggered groups on multiple cores ,,"Multicore support for CTU Trigger Mode (CTU HW triggered groups must be configured and used only on a single core) Implemented on Tresos and S32CT."
ARTD-4850	Bug	[S32K3][MCL][EMIOS] Add EMIOS support in MCL HLD CT configuration<*> Need to add EMIOS files generation in CT.
ARTD-4872	Bug	[ADC] (ITG) Generate fail when configuring AdcLogicalUnitId at first place<*> Detailed description (how to reproduce it): Generate fail when configuring AdcLogicalUnitId at first place Preconditions: NA Test Case ID (internal TC that caught the defect) optional: Adc_TC_FCT_0101 Observed behavior: Generate fail: [e:\gitwork_rt\output\eclipse\plugins\Adc_TS_T40D11M10I0R0/generate_PB/Adc_RegOperations.m:2026]: Logical IDs must mach the element number in the HwUnit List container (node) Expected behavior: generate pass Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-4886	New	New Feature [PORT] Add support for UntouchedIMCR for S32K3XX ,,"Add support for UntouchedIMCR. Two things need to be checked: Check in Tresos configuration: out of range, configure one IMCR in both PortPin list and UntouchedIMCR list then Tresos should raise 1 error. Check in runtime: for example: Configure UntouchedIMCR 147 > call Port_Init() > then the IMCR147 should be keep its value "

ID	Subtype	Headline and Description
ARTD-4891	New	New Feature [PORT] Add Port_ResetPinMode functionality for S32K3XX ,,"NewWorkDescription: Implement Port_ResetPinMode functionality CPR_RTD_00422.port: The Port driver shall provide a autosar extension API with the prototype: void Port_ResetPinMode(Port_PinType Pin) . The function Port_ResetPinMode shall revert the port pin mode of the referenced pin to the value that was set by Port_Init operation. CPR_RTD_00423.port: If Det is enabled, the function Port_ResetPinMode shall report PORT_E_MODE_UNCHANGEABLE error and return without any other action, if the parameter PortPinModeChangeable is set to FALSE CPR_RTD_00424.port: Port_ResetPinMode functionality will be enabled/disabled by using a boolean precompile parameter named ""Port Reset Pin Mode API Per default this optional functionality and the configuration parameters shall be disabled Requirement source: CPR_RTD_00422.port, CPR_RTD_00423.port, CPR_RTD_00424.port (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional:"
ARTD-4916	Bug	[S32DS3.4] Add dependencies between development package and SDK package for S32K3<*> Detailed description (how to reproduce it): 1. Help > S32DS Extensions and Updates 2. Click Go Preferences > Add update site for S32K3 3. Wait until package are loaded. Select SDKs package S32K3 4.4 RTD 0.8.1 then press "Next" button 4. Observe dependencies package in the next page 5. Finish Observed behavior: 4. Development packages do not show 5. Only SDK pack is installed Expected behavior: 4. Development packages should show as dependencies package 5. Dev pack & SDK pack are installed
ARTD-4915	Bug	[S32DS3.4] Uninstall SW32 S32K3 RTD package should also remove SDK & all relevant<*> # Install SW32 S32K3 RTD package via MI # Uninstall SW32 S32K3 RTD package via MI # Go to the layout: <install_dir>\S32DS\integration <install_dir>\S32DS\software # Open S32DS on new workspace > SDK Management Observed behavior: 3. All relevant of S32K3 RTD still exist 4. SDK for S32K3 still exist Expected behavior:* Uninstall SW32 S32K3 RTD package should also remove SDK & all relevant Note: This issue also occurs with RTD for SW32G2 version 1.0.0, & RTD for S32R45 version 2.0.0

ID	Subtype	Headline and Description
ARTD-4902	New	New Feature [S32DS 3.4] Should update detail description for RTD for S32K3 0.8.1 ,,"Steps: # Open S32DS, add update site for S32K3 dev package & S32K3 SDK package (com.nxp.s32ds.dev.packages.internal_3.4.0.20201203234449.zip) # Open S32DS Extension and Updates > Select S32K3 SDK package then observes overview # Install S32K3 SDK then open Installation Details > Installed software , select RTD S32K3 Observed behavior: 2. RTD for S32K3 version 0.8.1 3. RTD for S32K3 0.8.1 Expected behavior: 2 . Should update detail description for S32K3 SDK ex:** _ **_ The S32 Software Development Kit (S32 SDK) is an extensive suite of peripheral drivers, RTOS, stacks and middleware designed to simplify and accelerate application development on NXP S32K3 ARM based microcontrollers. This S32 SDK supports development with the following devices: S32K314 S32K324 S32K334 3. Should update more detail, ex: ""S32 RTD SDK for S32K3xx Version 0.8.1"" "
ARTD-4920	Bug	[PWM] Invalid type of generated code in PWM_DRIVER_STATE_INITIALIZATION<*> Vector got this error when compiling PWM code: CC Pwm.o "../../../external/ThirdParty/Mcal_S32k/Supply/SW32K3_RTD_4.4_0.8.1/eclipse/plugins/Pwm_TS_T40D34M8I1R0/src/Pwm.c", line 197: error #144: a value of type "void " cannot be used to initialize an entity of type "boolean" static Pwm_DriverStateType Pwm_aState[1U] = PWM_DRIVER_STATE_INITIALIZATION; As the pwmChannelIdleState[PWM_CONFIG_LOGIC_CHANNELS] has type as boolean, but generated code is "NULL_PTR".
ARTD-4931	New	New Feature [SPI] Update driver according to requirements ,,Update driver according to requirements added to the ticket AAI-650

ID	Subtype	Headline and Description
ARTD-4932	New	New Feature [SPI][FLEXIO_SPI] Move SpiDataWidth, SpiTransferStart, SpiDefaultData nodes from SpiPhyUnit to SpiExternalDevice for IP driver" ,,"Each PCS in the same SPI unit can be used to control one external slave. They can be required to have different value of SpiDataWidth, SpiTransferStart or SpiDefaultDta. Currently, for IP driver, these nodes are pushed into SpiPhyUnit container in IP component file. So it is not supported to change these value for each external Slave device. So, these nodes should be moved to SpiExternalDevice container for IP driver.
ARTD-4933	Bug	[GPT] The number of PIT channel deinitialized in ip layer is not exactly for PIT 1<*> I found an problem with debugging, when i call function Gpt_DeInit to reset module, then it will call the ip layer and i checked the number channel deinitialized of PIT instance. I found that the number channel deinitialized of PIT 1 excess the actual channel number is 1 channel, it might lead to some error when access this non-existed channel. I found the issue with this code section in file Pit_Ip.c: !image-2020-12-06-19-23-06-449.png! In this code, the number channel of PIT 0 and PIT 1 is equal, it should be differrent.
ARTD-4954	New	New Feature [SPI] Improve LPSPI IP driver code on S32K3 ,,"S32K3XX is using new version of LPSPI IP. This new LPSPI IP version has difference behavior with old version on S32K1XX: For S32K1XX, In the case CS continue, last frame can be only pushed into RX FIFO if another frame is initialized or CONT bit is cleared. But this behavior is not appeared on S32K3XX, It means last frames received will be pushed immediately into RX FIFO and no need to initialized another frame or CONT bit is cleared. Currently, LPSPI IP driver code on S32K3XX is implemented according to old LPSPI IP version behavior. The information of next channel in Job is always gave to IP driver when IPW initializes to transfer a channel in Job. And IP driver code is implemented complex more due to next channel must be initialized at the end of previous channel to have last received frame in RX FIFO. So, LPSPI IP driver on S32K3XX can be improved to reduce complexity."
ARTD-4958	New	New Feature [SPI][FLEXIO] Update driver according to requirements ,,Update driver according to requirements added to the ticket AAI-650
ARTD-4959	New	New Feature [SPI] Use reference node to get frequency value from MCU for CT ,,Use reference node to get frequency value from MCU for CT.

ID	Subtype	Headline and Description
ARTD-5008	Bug	[gpt] DS Examples should use description.txt instead of readme.txt for readme details<*> Test Case : 1. Open S32DS 2. Open S32DS Project from Example wizard 3. Select example then observes description FlexCAN_example_CT Crc_Example_DS Dio_example_DS Eth_Example_DS_001 FLS_IP_QSPI_Example_001 Gpt_example_DS Icu_example_DS Lpuart_Lin_example_CT Mcl_Example_CT Clock_Ip_Example_CT Power_Ip_Example_CT Port_example_DS Pwm_example_DS Ip_Lpspi_example_DS Lpuart_Uart_Ip_example_UCT Observed behavior: 3. Description is empty, could not loaded (If I rename file readme.txt to description.txt, Description can be loaded success) Expected behavior: 3. Load success
ARTD-5011	Bug	[mcu] DS Examples should use description.txt instead of readme.txt for readme details<*> Test Case : 1. Open S32DS 2. Open S32DS Project from Example wizard 3. Select example then observes description FlexCAN_example_CT Crc_Example_DS Dio_example_DS Eth_Example_DS_001 FLS_IP_QSPI_Example_001 Gpt_example_DS Icu_example_DS Lpuart_Lin_example_CT Mcl_Example_CT Clock_Ip_Example_CT Power_Ip_Example_CT Port_example_DS Pwm_example_DS Ip_Lpspi_example_DS Lpuart_Uart_Ip_example_UCT Observed behavior: 3. Description is empty, could not loaded (If I rename file readme.txt to description.txt, Description can be loaded success) Expected behavior: 3. Load success

ID	Subtype	Headline and Description
ARTD-4997	Bug	[SPI][S32CC] Function Spi_SetupEB have an issue with length param<*> When frame size is 8 and length is 1, function Spi_SetupEB was dev error
ARTD-5024	Bug	[FLS] Slow access on nodes using // from xdm<*> The XDM schema file (_i.e. plugins\Icu_TS_T2D35M10I0R0\config\Icu.xdm_) contains several XPath expressions for INVALID attributes which start with '//...'. This kills the performance of the model verification in bigger projects, as such expressions do a lookup in the whole model tree. For example, this expression: _<a:da name="INVALID" type="XPath"> <a:tst expr="((.='ICU_MODE_EDGE_COUNTER') and (//IcuEdgeCountApi='false'))" true="If IcuMeasurementMode = 'ICU_MODE_EDGE_COUNTER', IcuEdgeCountApi switch should be set to ON"/> will take a search for IcuEdgeCountApi in the whole project, as described in Tresos development guide. Also, there is a note to warn that using double slash can lead to performance problems: !image-2020-12-08-17-32-44-359.png|width=419,height=182! Therefore the complete system model will be verified independent of the module. Depending at the ECU project, this will lead to many minutes of additional, unnecessary verification time. Changes the pattern to absolute or relative expressions, in order to reduce the performance problem, where possible.
ARTD-5092	New	New Feature [ICU] [S32CT] Implement EPD/EPC support for HLD and IPLD ,,"Implement EPD/EPC support for HLD and IPLD. Please refer to [this post on Teams https://teams.microsoft.com/l/message/19:e451c595d3ba410c8f9c1f5efc19a8a3@thread.tacv2/1606904026692?tenantId=686ea1d3-bc2b-4c6f-a92c-d99c5c301635&groupId=f9decd68-7b74-4101-a4d2-ad54e86f727f&parentMessageId=1606904026692&teamName=Zebra&channelName=Configuration%20(code%2C%20DS%2C%20EB%2C%20etc)&createdTime=1606904026692] for additional details. From the presentation, the main focus should be on the following sections: Mapping XDM to Component EPD Importer EPD Generation EPC Importer EPC Generation "

ID	Subtype	Headline and Description
ARTD-5093	New	New Feature [lin] [S32CT] Implement EPD/EPC support for HLD and IPLD ,,"Implement EPD/EPC support for HLD and IPLD. Please refer to [this post on Teams https://teams.microsoft.com/l/message/19:e451c595d3ba410c8f9c1f5efc19a8a3@thread.tacv2/1606904026692?tenantId=686ea1d3-bc2b-4c6f-a92c-d99c5c301635&groupId=f9decd68-7b74-4101-a4d2-ad54e86f727f&parentMessageId=1606904026692&teamName=Zebra&channelName=Configuration%20(code%2C%20DS%2C%20EB%2C%20etc)&createdTime=1606904026692] for additional details. From the presentation, the main focus should be on the following sections: Mapping XDM to Component EPD Importer EPD Generation EPC Importer EPC Generation "
ARTD-5050	New	New Feature [GPT] Add support for Predefined Timers in S32DS ,,Add support for Predef functionality in DS as it is in EBT
ARTD-5065	Bug	[Ip_Flexcan] FlexCAN_Ip_GetBitrateFD return empty value in case of enabled enhanced bit-time<*> FlexCAN_Ip_GetBitrateFD need to support when enabled enhanced bitrate Similar as FlexCAN_Ip_GetBitrate API See attached file for detail behavior TC_ID: Ip_FlexCAN_TC_*FCT_2200
ARTD-5068	Bug	[S32K3] Build fails for S32K314 and S32K324 when PIT component is used<*> # Create a new S32DS S32K314/S32K324 project. # Add PIT component, add GptPit and GptPitChannels configuration, and select Pit Channel CH_0 !image-2020-12-09-13-37-42-169.png! # Press the Update code button. # Build the project. The build will fail. I attached pit_log.txt file with the output of the build. This build fails because S32K344_PIT.h header file is not added in Pit_Ip_Cfg_Defines.h. !image-2020-12-09-13-47-40-543.png! It seems that config tool will add this include only for S32K344. This condition is used in other files too, so I expect the build to fail when those components are used: Emios_Gpt_Ip_Cfg_Defines.h Emios_Pwm_Ip_Cfg.h Rtc_Ip_Cfg_Defines.h Stm_Ip_Cfg_Defines.h

ID	Subtype	Headline and Description
ARTD-5070	Bug	[S32K3] Build fails when PIT channel CH_RTI is used<*> # Create a new S32DS S32K314/S32K324 project. # Add PIT component, add GptPit and GptPitChannels configuration, and select Pit Channel CH_RTI. !image-2020-12-09-15-05-05-845.png! # Press the Update code button. # Build the project. The build will fail. I attached pit_rti_log.txt file with the output of the build.
ARTD-5130	New	New Feature [CAN] FlexCAN_Ip_Send should take no action/or return error when it is called while module is not in ready/normal mode ,,"Situation: From HLD, users can call Can_Write cyclically. And the controller mode can be changed in the meantime. (by bus-off handling, or set_controler_to_stop, ...) => i think users would not want to check the controller_mode before they call Can_Write => Can_Write can be accidentally call in stop mode, from HLD, a Tx sw state will be changed to TX_BUSY permanently without notification (users can not see this behavior from HLD due to a HTH can includes many HW objects, if this issue happen with some of them, Can_Write can still work but with some resources was locked with TX_BUSY state) Expectation: A boolean (e.g isReady*) static variable can be created to store operation mode information then FlexCAN_StartSendData will check it "

ID	Subtype	Headline and Description
ARTD-5137	New	New Feature [MCL] Implement CPR_RTD_00521 support for synchronous start of Emios Counter Buses ,,"NewWorkDescription: CPR_RTD_00521*: The Mcl driver shall allow configuration of eMIOS Counter Buses that have hardware support and can be shared. The static configuration for eMIOS Counter Buses shall allow, if hardware supports, setting up a value for counter as starting point (that can be considered an offset shift between Counter Buses). Requirement source: Customer Request (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Requirement text} The Mcl driver shall allow configuration of Emios Counter Buses that have hardware support and can be shared. The static configuration shall allow, if hardware supports, setting up a value for counter as starting point (that can be considered an offset shift between Counter Buses) The Counter Buses shall be started all at once. For the motor control use case, Counter Buses with offset and PWM channels driven by Counter Buses, the following sequence may apply: Mcl_Init() Pwm_Init() / with 0% or 100% Duty Cycle / Pwm_SetDutyCycleNoUpdate() / for each channel used this will assure that on next cycle all channels will start synchronous using the CBes; / Pwm_SyncUpdate()"
ARTD-5143	Bug	[CAN]Add Enanced FIFO generation + others for HLD CT component<*> Please add generation of Enhaced Fifo for FlexCAN Ip Pbcfg.c in the Can UCT component. this need to be synced with the component from EBT. Now is added a dummy version only for compilation. Refer to the build log files for CT to fix some warnings also.
ARTD-5145	New	New Feature [ICU][OCU][MCL] Implement CPR_RTD_00522 restrictions and updates in CPR_RTD_00511 ,,"NewWorkDescription: Updates according to the updates in the requirement: *CPR_RTD_00511 CPR_RTD_00522*: Drivers capable of using Counter Buses shall not allow selection of an Counter Bus with exclusive access granted to PWM. The check will be performed at configuration time. Applicable only for Icu, Ocu, on eMIOS Requirement source: Customer Request CPR_RTD_00511 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Provide an API that will update (buffered change expected) the match/reload value for the counter selected."

ID	Subtype	Headline and Description
ARTD-5150	Bug	[GPT] The RTC IP Layer lacks the overflow interrupt<*> The user need to check when overflow interrupt is going to occur, but in driver has not supported this feature in RTC ip , so the user cannot check overflow interrupt. I find some issue related to this as following: RTC, in high layer, does not need callback function for overflow interrupt. In ip layer for RTC , it currently does not have some function enable interrupt overflow and in the interrupt function, it does not check overflow condition Some requirement in ip layer need to check over flow interrupt for RTC. So driver should support this feature.
ARTD-5162	Bug	[S32K3]PWM example not working, counter register is not incremented ,,"I tried to run the Pwm_example_DS project in S32DS 3.3 but was unable to get any PWM signal on output pin. Since the example configures the Emios0_Ch0 I used the PTD15 but the pin remains in low state. While investigating the issue, found following problems with example and peripheral: # [PWM] Emios_Pwm_Ip headers and sources are copied in the project under ""SDK"" folder, not ""RTD"" !1.JPG! # [PWM] The bus selector register remains on Select counter bus A, even the structure timebase in set on EMIOS_PWM_BUS_Internal. !2.JPG! # [PWM] The counter remains 0, see the register settings below. !3.JPG! # [Example] no physical pin used for the actual PWM signal output. # [Example] No clock initialization found and a typo line 88 and bad description !4.JPG! # [Example]The test passes even if the functionality is not working. Example runs until one of the count variables reaches the MAX_COUNT_PULSE. The issue is that the test is successful in both cases because the actual pin remains in low state over the entire run period. !5.JPG! # [Example]Readme has no indication on how to validate the example. The installation steps refers to some S32K2 boards.
ARTD-5163	New	New Feature [ADC] S32ConfigurationTool Multicore support for HLD ,,"Multicore support for S32CT HLD (SW triggered groups and HW Triggered groups in Trigger Mode) Generation must be identical as for Tresos for TS_001"
ARTD-5165	New	New Feature [ADC] S32ConfigurationTool DMA support for HLD (Triggered and Control Mode) and IPL ,,Generation must be identical as for Tresos for TS_002

ID	Subtype	Headline and Description
ARTD-5167	New	New Feature [PORT] Add the "Add required elements" in Tresos for UnTouchedPortPin" ,,"There should be a way to help the user add all required elements for UnTouchedPortPin container by !image-2020-12-11-09-30-44-174.png! After this improvement was implemented and user clicked on that button, does user can be add more pins into UnTouchedPortPin? If not, this improvement should not be applied.
ARTD-5169	Bug	[Platform] The functions get/clear pending interrupt do not work correctly with interrupt related to MSI<*> The purpose of the function IntCtrl_Ip_GetPending is to retrieve pending interrupt from external. It should not get status bit related to MSI. Another API should be supported to return status of interrupt of MSI. The function GetPending should return status of ISPR bit in NVIC. When there is a request interrupt from other cores, the corresponding bit in ISRPR is also raised if it has not yet served. !image-2020-12-11-09-31-51-907.png!
ARTD-5184	Bug	[ICU] Redesign IPL side for Timestamp measurement and Signal Measurement<*> Current design makes almost impossible for IPL user application to access all data provided by signal measurement and timestamp measurement. Proposal of design should be first described on: [OneNote page|https://nxp1.sharepoint.com/sites/Zebra/_layouts/OneNote.aspx?id=%2Fsites%2FZebra%2FSiteAssets%2FZebra%20Notebook&wd=target%28Group6.one%7C580E1A51-92D1-406A-ADA2-8FE4F6905B40%2FSIGNAL%20measurement%20for%20IPL%20case%7C386DB79B-D571-445D-B336-ABF25FB591A0%2F%29] Implementation should fit both eMIOS and FTM IPs as supported for actual platforms and allow extending for other new ones.
ARTD-5197	Bug	[S32K3][ICU][EMIOS] Emios specific configuration bugs<*> # If we have an instance of EMIOS on ICU which use a master bus not configured in MCL we don't receive an error(be aware of the MCL configuration). [NOT REPRODUCTIBLE] # When Signal Measurement API is checked on K3 on EMIOS IP we got an error. [NOT REPRODUCTIBLE] # If we start Timestamp Measurement without enabling the notification container we got an error when we are trying to generate. [RESOLVED] # Master bus must be configured exclusive in MCL when is used by this driver, ICU should not modify any CHs configured by MCL as master buses.(see generation for EMIOS on ICU) [NOT REPRODUCTIBLE] # Verify this attached email thread. [THIS EMAIL IS FOR MCL, FOLLOW UP IN ANOTHER TICKET]

ID	Subtype	Headline and Description
ARTD-5199	Bug	[ICU] Code implementation generates 'MISRA C-2012 Rule 11.5'<*> Implementation for IPW layer uses cast through void for different structure types mapping on each IP emios, ftm, wkpu, siul2 Re-factor the code for not triggering the MISRA rule violation.
ARTD-5214	Bug	[Platform][IntCtrl] Can not configure System Handler Priority Register (SHPR) with function IntCtrl_Ip_SetPriorityPrivileged<*> With the current implementation in driver for two function *IntCtrl_Ip_SetPriorityPrivileged, IntCtrl_Ip_GetPriorityPrivileged, There is no way for user can get/set System Handler Priority. As in below picture, the value of parameter eIrqNumber is always checked with value must greater than 1, so the highlight code can not be executed when DET is ON. !image-2020-12-13-17-27-26-277.png! !image-2020-12-13-17-34-22-388.png!
ARTD-5202	Bug	[Ip_Flexcan] ConfigEnhancedRxFifo and ConfigRxFifo and dev_assert<*> A>* FlexCAN_Ip_ConfigEnhancedRxFifo can work in normal mode (internally enter_freeze mode) B> FlexCAN_Ip_ConfigRxFifo (do nothing in case of normal mode), no error reporting C>* FlexCAN_Ip_ConfigEnhancedRxFifo can not work in normal mode when disableing dev_error_detect but still work when enabled dev_error_detect (because freeze mode is entered when turn of dev_detect) => enabled/disable dev_error_detect should impact to error reporting, should not change flow of code/functionality Expectation: FlexCAN_Ip_ConfigRxFifo and FlexCAN_Ip_ConfigEnhancedRxFifo should return ERROR while module is in normal mode and does not force module to freeze mode in this case => same approach as other api (e.g FlexCAN_Ip_SetRxFifoGlobalMask_Privileged)
ARTD-5211	Bug	[Ip_Flexcan] Rx FIFO Poll should have same mb_idx approach as interrupt/dma<*> Expect to move to next release, the fix can impact to HLD! Ip_FlexCAN_TC_FCT_*3055 Init flexcan with Legacy rx fifo, POLLing transfer type. FlexCAN_Ip_MainFunctionRead with mb_idx=0 will not work Expectation: same approach for poll/interrupt/dma (same hw abstraction mb_idx=0 value for legacy rxfifo), same mb_idx value when using set of APIs (FlexCAN_Ip_MainFunctionRead and FlexCAN_Ip_GetTransferStatus) Additionally: overflow/fifo_warning should be reported automatically (user should not need manually poll event with hw-dependency number as mb_idx=6 and mb_idx=7*) => hw abstraction need to be implemented for IP player. Documentation in this case will cause hard to use/error prone for application layer!)

ID	Subtype	Headline and Description
ARTD-5217	Bug	[s32k3][Ip_Flexcan] Stuck in error irq loop when enabling only FLEXCAN_IP_INT_RX_WARNING<*> Init Flexcan with Installed error callback FlexCAN_Ip_SetErrorInt(u8Inst, FLEXCAN_IP_INT_RX_WARNING, TRUE); => producing Rx warning interrupt => stuck in error irq due to Rx warning is not handled by driver !image-2020-12-08-19-13-24-289.png!
ARTD-5233	Bug	[S32DS 3.4] Warning: Invalid project path: Include path not found when attach SDK RTD for S32G2xx, S32K3xx, S32R4xx ,,"STEPS: # Create project S32G2xx/S32K3xx SDK RTD # Check problem view # Create project S32R4xx S32R4xx RTD # Check problem view Observed behavior: 2. There is warning displayed: Invalid project path: Include path not found (C:\Users\loandt \workspaceS32DS.3.4\B201211_2\g234\g234_M7_0\include) Invalid project path: Include path not found (C:\Users\loandt \workspaceS32DS.3.4\B201211_2\k3\include). 4. There is warning: Invalid project path: Include path not found (C: \NXP\S32DS.3.4\B201211_RC2\S32DS\software \PlatformSDK_S32R_2020_12\SW32_RTD_4_4_1_0_0_D2012\Platform_TS_T40D11M10I0R0\startu Expected behavior: No warning
ARTD-5247	Bug	[GPT][S32DS] Build fail with ghs compiler<*> S32ct Build fail with ghs compiler: !image-2020-12-14-15-41-31-619.png!
ARTD-5318	New	New Feature [CRYPTO] Fix compiler warnings ,,Fix reported compiler warnings.
ARTD-5319	Bug	[SPI][S32CC] Change node type of SpiBaudrate in S32CT<*> Change node type of SpiBaudrate from integer to float

ID	Subtype	Headline and Description
ARTD-5329	Bug	[S32DS 3.3 Update 1] Wrong id used in the component files for component_id attribute<*> Also, all the used ids are case sensitive. Check the attached log file for more details. Also, a similar message is caused because the name and Csub attributes doesn't match with the .component id, in the sdk_components.xml file: !MESSAGE Could not find any matching component for type Gpt representation in the sdk_components.xml file: <sdk_component Cbundle="RTD" name="gpt" id="platform.driver.gpt" Cvendor="NXP" Cclass="Device" Cgroup="RTD Driver" Csub="gpt" version="1.0.0" prj_file="Gpt.c" version_prj_files="Gpt.h" />
ARTD-5334	New	New Feature [SPI] Support for SpiSequence with multiple jobs without CPU intervention ,,"NewWorkDescription: Customer has the following SPI use case: SPI: Assume 4 slaves, all configured with same data phase and clock polarity, say with a 4MHz clockrate, each slave with 8 channels, each slave with their own chip select. At initialization, configure high side driver (transmit 2 individual 1-byte commands, no reply expected from slave) On demand, set driver outputs (transmit a single 1-byte command, no reply expected from slave) Once initialized, poll at a fixed interval to read feedback from driver IC (transmit 2 bytes per slave, receive 2 bytes from slave). Ideally we'd be able to group these reads, issue them in a sequence and let the SPI controller do the work, dumping the received data into a per-channel fixed offset in a buffer and notifying the software when the batch read is done. As a summary customer wants to send multiple transmissions to different slaves without SW intervention and get only one interrupt at the end to notify that all slave communications are finished. Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]"
ARTD-5337	Bug	[Crypto][S32G-RTM] CT component cannot configuration for CryptoEcucPartitionRef node<*> 1. Create a project on S32DS.3.4. 2. Add Crypto and EcUc component config all nodes for EcUc component. 3. Configuration for Crypto component node: CryptoEcucPartitionRef => Errors will appear, detail: attach file => Crypto configuration cannot generated config code.
ARTD-5339	New	New Feature [CRYPTO] Reduce cyclomatic complexity larger than 20 for driver functions ,,The cyclomatic complexity of the Crypto_ProcessJob() is over 20.

ID	Subtype	Headline and Description
ARTD-5356	Bug	[SPI][S32CC] Error with SpiEcucPartitionRef on S32CT<*> If node Spi Multicore Support is TRUE, error will raise as below although it had used by SpiExternalDevice : Issue: The partition referred in SpiEcucPartitionRef is not used by any SpiExternalDevice. Level: Error Type: Tool problem Tool: Peripherals Origin: Peripherals:BOARD_InitPeripherals Resource: Spi_1 Information: The partition referred in SpiEcucPartitionRef is not used by any SpiExternalDevice.
ARTD-5359	Bug	[CAN] enhanced rx fifo dma with underflow event<*> Init can with enhanced rx fifo, enabled dma Maf send two frames Call FlexCAN_Ip_RxFifoBlocking => the second frame loss due to underflow event TC_ID: Ip_FlexCAN_TC_FCT_5202 Investigation: Run any test case (for example CAN_TS_614), i check in debug that underflow event always happen. for example you can try below sequence: Init can with enhanced rx fifo, enabled dma call rx_fifo to start dma for receiving one frame maf send only one frame, aslo => see that underflow event will always manifest expectation: we should not let underflow event happen else this will cause un-determined bahavior, very hard to investigate if users encounter this issue Note: happen on S32G, not happen on S32K ! !image-2020-12-16-11-50-28-609.png!
ARTD-5468	New	New Feature [S32K344 BETA] Update and review driver for ICU ,,"IPs list: eMIOS, SIUL2, WKPU "
ARTD-5479	New	New Feature [S32K344 BETA] Update and review driver for OCU ,,"IPs list: eMIOS "

ID	Subtype	Headline and Description
ARTD-5490	New	New Feature [S32K344 BETA] Update and review driver for GPT ,,"IPs list: eMIOS, PIT, STM, RTC "
ARTD-5501	New	New Feature [S32K344 BETA] Update and review driver for PWM ,,"IPs list: eMIOS, Flexio_PWM "
ARTD-5679	New	New Feature [ETH]Fix HIS violations ,,"Fix HIS violations This ticket will be resolved in the ticket ARTD-5921"
ARTD-5680	New	New Feature [S32K344] OCU: Create EBT and DS Examples ,,"IPs list: Ftm and eMIOS Create EBT abd DS examples for available EVB boards. See [here|https://confluence.sw.nxp.com/display/AUTORD/Examples] how to create an example; the second method is recommended to create the examples automatically together with the plugins"
ARTD-5683	Bug	[ADC] Adc_Sar_Ip_GetConvData always returns 0 when called from EndOfConversion notification<*> Adc_Sar_Ip_GetConvData always returns 0 when called from EndOfConversion notification Environment: Board : S32G-VNP-EVB (Rev 2) S32 Design Studio version v.3.3 S32G2_S32DS_3.3.1_D2009 SW32G2_RTD_4.4_0.9.0_D2011_updatesite Customer configured ADC using S32DS Configuration Tool. After they configured Callback_EndOfConversionNotification function for end of channel conversion notification, they tried to read AD result in the function but all they can read is 0. I also reproduced this issue in my S32DS3.3, then I found a workaround as red box below. It means not clear the ECO_CHn of CEOCFR0 before read CDATA of PCDRa. Otherwise it can not enter the first if in Adc_Sar_Ip_GetConvData function. And you can see after read CDATA of PCDRa, it will clear the ECO_CHn of CEOCFR0. Finally, attached is the sample project provided by customer.
ARTD-5689	Bug	[SPI]Old frames will be included on next synctransmit session<*> When timeout occur, old frame will include on next synctransmit

ID	Subtype	Headline and Description
ARTD-5703	Bug	[CAN] remove multiple definition of FlexCAN_Ip_ExitFreezeMode<*> Remove double definition of the function macro FlexCAN_Ip_ExitFreezeMode from FlexCAN_Ip.h
ARTD-5721	Bug	[GPT][S32DS] Stm_Ip_u32NextTargetValue undefined when config GPT change next timeout<*> When config GPT HLD on s32ct, enable GPT change next time out without enable ISR i got the build fail: !image-2020-12-18-15-09-38-225.png! [^Gpt.mex]
ARTD-5724	Bug	[GPT] The RTC calculates wrong number of tick per seconds<*> The number of tick in case user need to use low frequency clock is currently wrong. For instance, user config clock with frequency equal 32 Khz, clock divider factor div32 = 1 and div 512 = 1. So the number of ticks per second is calculated have to be 1.953125 ticks. But in output configuration, this value is rounded to 1 ticks. So the time application will not operate accurately. I think this value should be freeze, not rounded, to create a time per second exactly. !image-2020-12-18-15-49-51-351.png!
ARTD-5730	Bug	[S32K3][ICU] IcuDmaNotification.c file is not generated for DS<*> IcuDmaNotification.c file should be generated with respect to the existing generation from EBT.
ARTD-5731	New	New Feature [ADC] Implement Adc_Sar_Ip_DisableChannelDmaAll ,,"Implement Adc_Sar_Ip_DisableChannelDmaAll and use from HLD if required Remove from requirement and code comments Adc_Sar_Ip_DisableChannelDmaAll, ONLY if it is not required to be called from Ipw function mentioned in ADC_SAR IP ZEBRA sheet from https://teams.microsoft.com/l/file/C97A8AE3-1D29-46CB-838A-B277B6FA1DD3?tenantId=686ea1d3-bc2b-4c6f-a92c-d99c5c301635&fileType=xlsx&objectUrl=https%3A%2F%2Fnxp1.sharepoint.com%2Fsites%2FZebra%2FShared%20Documents%2FGroup%204%2FADC_Requirements%2FADC_API_Analysis.xlsx&baseUrl=https%3A%2F%2Fnxp1.sharepoint.com%2Fsites%2FZebra&serviceName=teams&threadId=19:dea2a7f1858a42deaa0c3362b0318b93@thread.tacv2 a4d2-ad54e86f727f"
ARTD-5746	Bug	[PWM] Issue with float casting goes to Hardfault<*> Accessing float statement goes to HardFault. emiosChDuty = (uint16)(emiosChPeriod ((float)dutyCycle / 0x8000U));

ID	Subtype	Headline and Description
ARTD-5748	Bug	[DS] There's an issue related to indexer on S32DS<*> There are some errors and warning appeared before compilation when click any file on the DS project to open on S32DS. But it will not presented at compilation.
ARTD-5749	New	New Feature [ADC] DMA without interrupts ,,"CPR_RTD_00488.adc:The adc driver shall support dma transfer for groups that have the ""Without Interrupt"" optimization enabled. For these types of groups a dedicated DMA channel shall be used. Activities: Implement Add dev test add short description in UM remove limitation from UM that it was not supported Mark fulfilled in in Doors "
ARTD-5751	New	New Feature [WDG] Add restriction for Dem configuration and DisableDemErrorReports ,,Add restriction for the Wdg module so that all wdg instances will need to have the same settings applied for Dem Events and WdgDisableDemErrorReport. (same as for the multicore option).
ARTD-5753	Bug	[PORT] Incorrect placement of Port_pConfig structure pointer<*> The pointer to structure Port_pConfig in Port.c is defined in section: PORT_START_SEC_VAR_NO_INIT_UNSPECIFIED_NO_CACHEABLE I believe it should be as it was for S32K1 and S32K2 MCAL in section: PORT_START_SEC_VAR_INIT_UNSPECIFIED The placement as it is right now causes an IAR linker error for customer Magna as next: Error[Lp005]: placement includes a mix of sections with content (example "rw data section .mcal_bss_no_cacheable in Port.o") [suitable for placement in ROM] and sections without content (example "zi section .mcal_bss_no_cacheable C:\Projects\SAM_K3_Test\linker_flash.icf 153 Please confirm and fix in next release.
ARTD-5771	New	New Feature [ICU] integrate cmp IPL files into ICU driver ,,"Integrate ICU IPL driver into ICU driver. include in xdm for EB Tresos; include in .component for S32DS; generate ipl code for both worlds; map functionality ASR-IPL; review IPL DOORs requirements; Last known state of IPL is found on : feature/ARTD-419-icu-cmp commit id: d0a64491d4a2723fef92d4aa009ba2184c44e7bf"

ID	Subtype	Headline and Description
ARTD-5779	New	New Feature [CRYPTO] Multiple definition of a macro ,,"CRYPTO_JOB_QUEUE_NONE_U32 is defined in Crypto_Util.h and Crypto_Hse.c. The define from Crypto_Hse.c. should be remved."
ARTD-5825	Bug	[RTD][MCL]De-init function shall clear logic channel status<*> Detailed description (how to reproduce it): Init Mcl module(with no IRQ error) Set a error to dma channel Call De-init function Check value of CH error register > CH error register is not be clear Try to set again the transfer list with some commands All commands return DMA_IP_STATUS_ERROR > De-init function should support to clear HW error of channel Observed behavior: All HW error status of channel is not be cleared after de-init called Expected behavior: De-init function should support to clear all error status of channel
ARTD-5839	New	New Feature [SPI] Dem error can be reported in AsyncTransmit when HW errors occur ,,"Dem error can be reported in AsyncTransmit when HW errors occur. This can be implemented in Ipw_Callback function. And some requirements below can be also applied for AsyncTransmit, not only SyncTransmit as current implementation. SWS_Spi_00267 SWS_Spi_00383 SWS_Spi_00385 SWS_Spi_00386 SWS_Spi_00293"
ARTD-5853	Bug	[GPT] Rtc_Ip_IsCounterSync API can not be used because Rtc_Ip_ModeType is not defined<*> Rtc_Ip_IsCounterSync API can not be used by the user because the Rtc_Ip_ModeType is not defined in Rtc_Ip_Types.h proposal: Rtc_Ip_ModeType should be added in driver
ARTD-5879	New	New Feature [SAI] DMA support ,,"DMA support in tresos and s32ct. Add dev test"

ID	Subtype	Headline and Description
ARTD-5911	Bug	[platform] Checking the number of configured interrupt is not correct for the function Platform_Ipw_InitIntCtrl<*> 1. I'm trying to improve code coverage for the function Platform_Ipw_InitIntCtrl. I see that the pointer *pIntCtrlCtrlConfig which is a parameter of the function is passed from HDL, that was generate by configuration tool. So there is no way to create invalid configuration by configuration then check in this function. However, in the case there is error in generation configuration, the checking in this function maybe reasonable. But the checking seem to be incorrect. !image-2020-12-24-16-00-48-354.png! Suppose that there are 183 interrupt vector but the maximum interrupt number is 225. So if the value *pIntCtrlCtrlConfig->u32ConfigIrqCount (line 62) is 184, its is still valid. But indexing to the array aIrqConfig[irqIdx] at the line 71 is out of boundary, then probably cause hardfault.* 2. With assumption about there probably error in generating configuration causes incorrect generated code. There is a lack of checking for the function Platform_Ipw_InitNonCore !image-2020-12-24-16-18-06-869.png! Please check this issue.
ARTD-5904	Bug	[S32K3 BETA][SENT] Undefine value in Sent_VS_0_PBcfg.c and Flexio_Ip_VS_0_PBcfg.c<*> Issue When SentControllerActivation = false, Controller HW offset is (uint8)SENT_NULL_OFFSET_U8 in Sent_VS_0_PBcfg.c and Flexio_Ip_VS_0_PBcfg.c. [!IF "SentControllerActivation = 'true'"!] (uint8)[!"num:i(text:split(SentHwController,'_')[2])"!]U, [!ELSE!] (uint8)SENT_NULL_OFFSET_U8, [!ENDIF!] But this value has not been defined: STDERR:"e:/gitwork/Zerba/S32K3XX_4.4_noSASW/output/S32K3XX_S32K344/sent/Sent_TS_COT_007_cfg1/generate_tresos/src/Flexio_Ip_VS_0_PBcfg.c", line 216: error #20: STDERR: identifier "SENT_NULL_OFFSET_U8" is undefined STDERR: (uint8)SENT_NULL_OFFSET_U8,

ID	Subtype	Headline and Description
ARTD-5917	New	New Feature [SPI] Add a note in UM about limitation in Slave mode ,,"There is an note in RM sub-chapter "" 49.5.4.5 Continuous selection format "": !image-2020-12-24-17-13-27-965.png! In Slave mode and continuous CS, TFUF bit will be set when previous frame sent out but TX FIFO empty and CS signal was not de-asserted. In this situation, if external master still send next frame then previous frame was still sent out 1 time regardless of new frames filled into TX FIFO after that immediately. And TFUF bit is still set for each frame initialized by external master from that time until CS de-asserted. So the note should be added in UM sub-chapter ""Driver Limitations"" like: # In Slave mode and continuous CS, to avoid underflow error, the maximum number of byte to be sent is 32767 if DMA used and SpiDataWidth <= 8. Rationale: the maximum of BITER(Major Iteration Count) is 32767 and DMA major interrupt is processing when last entry in the TX FIFO is completely transmitted. # In Slave mode and use interrupt mode without DMA, the application needs to make sure Slave's interrupt service is not delayed to avoid errors underflow and overflow occur. Note (2) can be applied for platforms use LPSPI."
ARTD-5921	Bug	[S32R45-ETH] Generate failed when configure two controllers<*> Can not configure two controllers for S32R45 as the image attached
ARTD-5922	New	New Feature [SPI][FLEXIO] Support slave mode ,,Support slave mode
ARTD-5925	Bug	[ADC] There is a typo for Adc_sar component<*> Test Case ID (internal TC that caught the defect) optional: 1. Create project enable RTD for S32G274_Rev2 2. Open Peripherals tool-> Add Adc_Sar_Ip component 3. Open Adc_Sar component in Editor view > Channel configurations array > Enable "Threshold Enable" > Error shows in "Watchdog Threshold Register Index" (see pic 1) 4. In Watchdog threshold configurations array-> add one Register Observed behavior: The error in "Watchdog Threshold Register Index" is not resolved because there is a typo of default name missing "h": *AdcTresholdControl_0 It should be "**AdcThresholdControl_0**"
ARTD-5926	Bug	[SPI][FLEXIO] Add FLEXIO support macro to reduce code expose when FLEXIO is not selected<*> Add FLEXIO support macro to reduce code expose when FLEXIO is not selected

ID	Subtype	Headline and Description
ARTD-5930	Bug	[S32K3 BETA][SENT] Wrong type and description with SentTimeout in Flexio.component<*> Issue 1. In Flexio.component, id SentTimeout has wrong type and information <integer id="SentTimeout" label="Sent Timeout (0->65535)" type="uint8_t"> <description>Defines the depth of the DMA buffer</description> </integer> 2. In CDD_Sent.component, it has no SentTimeout node.

ARTD-5933	Bug	[S32K3 BETA][SENT] Duplicate and wrong some definitions in Sent_BOARD_INITPERIPHERALS_PBcfg.h<*>
		
		Issue 1
		build fail as below:
		C:/Users/trungdm1/workspaceS32DS.3.4/test_sent_01/generate/include/Sent_BOARD_INITPERIPHERALS_PBcfg.h:26: error: unterminated #ifndef
		26 #ifndef SENT_BOARD_INITPERIPHERALS_PBCFG_H
		> Issue comes from duplicating:
		#ifdef cplusplus
		extern "C"{
		#endif
		and in Sent_PBcfg.h on S32DS
		#ifndef SENT_[!<code>$variantName$</code>!]_PBCFG_H
		#define SENT_[!<code>$variantName$</code>!]_PBCFG_H
		Issue 2
		In Sent_Cfg.h has wrong definition:
		/ On/Off PreCompile switches /
		#define SENT_CONFIG_EXT
		SENT_CONFIG_BOARD_INITPERIPHERALS_PB
		> Sent_Cfg.h should update:
		<code>
		/ On/Off PreCompile switches /
		</code>
		<code>#define SENT_CONFIG_EXT \\\n</code>
		if(variantName)
		{
		<code>
		SENT_CONFIG_$variantName$_PB \\\n
		</code>
		}
		else
		{
		<code>
		SENT_CONFIG_PB \\\n
		</code>
		}

ID	Subtype	Headline and Description
ARTD-5947	Bug	[ADC] Missing constraints for S32CT component<*> Add constraints for found issues on ADC CT all constraints <constraint cond_expr="(($this.getValue() == ``) isCIdentifier($this.getValue()))" must remove ($this.getValue() == ``) condition adcGroupdefineitionArray must raise error if no channel is configured for that group Hw trigger source should not be available when ADC_HW_TRIGGER_API = OFF
ARTD-5995	Bug	[CRYPTO] Crypto_Hse.c: u32StreamId should be converted from uint32 to uint8<*> Crypto_Hse.c: u32StreamId should be converted from uint32 to uint8
ARTD-6018	Bug	[S32K3 BETA][SENT] Redefine Channel Id macros on Sent_Cfg.h<*> Issue Sent_Cfg.h and Flexio_Ip_Cfg.h define Channel ID macros, this one causes redefine error. Solution Remove channel ID macros in Sent_Cfg.h
ARTD-6019	Bug	[S32K3 BETA][SENT] Wrong Fast notification declaration in Flexio_Ip_PBCfg. c and Sent_PBcfg.c<*> Issue: STDERR:"e:/gitwork/Zebra/S32K3XX_4.4_noSASW/output/S32K3XX_S32K344/sent/Ip_Sent_TS_COT_001_cfgs32k314_mqfp100/generate_s32ct/generate/src/Flexio_Ip_BOARD_InitPeripherals_PBcfg.c", line 162: error #144:STDERR:"e:/gitwork/Zebra/S32K3XX_4.4_noSASW/output/S32K3XX_S32K344/sent/Ip_Sent_TS_COT_001_cfgs32k314_mqfp100/generate_s32ct/generate/src/Flexio_Ip_BOARD_InitPeripherals_PBcfg.c", line 162: error #144:STDERR: a value of typeSTDERR: "void (Flexio_Sent_Ip_StatusType, Flexio_Sent_SerialMsgType)"STDERR: cannot be used to initialize an entity of typeSTDERR: "const Sent_pFastNotificationType"STDERR: &FlexSent_FastNotif, Solution: Update in Sent_PBcfg.c and Flexio_Ip_PBCfg.c <code> extern void $sent_chConfigChildren[idx2].getChildById("SentFastNotification").getValue()$ (Flexio_Sent_Ip_StatusType status, Flexio_Sent_FastMsgType pSent_FastMsg); </code>
ARTD-6026	New	New Feature [SPI][FLEXIO] CS continuous mode only support with CPHA=1 with SLAVE mode ,,"RM said that: For CPHA=1, the select can remain asserted for multiple transfers and the timer status flag can be used to indicate the end of the transfer. So, Driver will not allow user configure CS continuous mode with CPHA is 1 with SLAVE mode "

ID	Subtype	Headline and Description
ARTD-6029	New	New Feature [SPI][FLEXIO] CS non-continuous mode only is supported when TIMCFG[TIMDIS] is 0 ,,"Currently, FLEXIO driver Master mode is supporting to configure SPI baudrate by 3 mode in TIMCFG[TIMDIS] field bits but only TIMCFG[TIMDIS] is 0 then CS non-continuous can be supported. So, The configuration file should be updated like: Add the condition expression like ""SpiCsContinous is FALSE only SpiBaudrateFlexio1 is selected"" a ticket to add the limitation of FLEXIO SPI in UM document will be created."
ARTD-6030	New	New Feature [SPI][FLEXIO] The delay value which will be configured by EB/CT tools is not used by FLEXIO ,,"FLEXIO don't have any registers to configure the delay timing. So the delay field configuration (SpiTimeClk2Cs, SpiTimeCs2Clk, SpiTimeCs2Cs) in Externaldevice should be disabled when FLEXIO is selected. That will not make user feel confuse when they setup their config"
ARTD-6049	Bug	[Ip_Flexcan] Timestamp for K3 build fail<*> A> build fail at IPL when enabling timestamp !image-2021-01-06-14-44-35-185.png! B>* timestamp is not available on EB / HLD => *CPR_RTD_00529.can, CPR_RTD_00528.can can not be tested now S1 (priority) because this need to be fixed and to be tested soon TC_ID: in-process
ARTD-6050	Bug	[BASE] The inter-module disable version check in "Devassert.h" is missed ,,"Devassert.h includes ""PlatformTypes.h"", however the DISABLE_MCAL_INTERMODULE_ASR_CHECK guard defined encapsulation is missed, leads to the compile error in VECTOR integrator.
ARTD-6052	Bug	[S32K3 BETA][SENT] SentDmaChannelReference and SentCpuClockRef need to refer to MCL and MCU in HL<*> Issue*: In CDD_Sent.component, SentCpuClockRef and SentDmaChannelReference are not refering to MCL and MCU. Solution*: Update 2 node SentCpuClockRef and SentDmaChannelReference. Update code generation. Add new node SentControllerActivation to synchronize with EBtresos.

ID	Subtype	Headline and Description
ARTD-6056	New	New Feature [SPI][FLEXIO] Add the limitation of SPI FLEXIO to UM document ,,"FLEXIO Limitation CS continous mode only supports with CPHA=1 CS non-continous mode of master mode only support with TIMCFG[TIMDEC] = 000 (SpiBaudrateFlexio1 is selected) FLEXIO don't support to configure the timing delay on master mode. "
ARTD-6059	Bug	[MCl][Emios] Build fail because the EMIOS_MCL_IP_DEV_ERROR_DETECT variable is undefined<*> Initializes the MCL module with configurations on EB tresos The bug: Build fail because the error appeared: Please, see the attached Bug_emios.PNG file for more detail. The root cause: The EMIOS_MCL_IP_DEV_ERROR_DETECT variable is defined in Emios_Mcl_Ip_CfgDefines.h file, but this file is not called anywhere in drive. I tried to include "Emios_Mcl_Ip_CfgDefines.h" in Emios_Mcl_Ip_Types.h file, the test build passed. Also, EMIOS_MCL_IP_DEV_ERROR_DETECT variable in Emios_Mcl_Ip_CfgDefines.h file is missing a space !MicrosoftTeams-image.png|thumbnail! Test Case ID (internal TC that caught the defect) optional: Test case: Mcl_TC_FCT_0201 Test suite: Mcl_TS_CC01 Observed behavior:*_ N/A Expected behavior:*_ N/A Note:* in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-6060	Bug	[S32K3][MCU]Mcu_ResetType did not folow req SWS_Mcu_00252<*> According requirement SWS_Mcu_00252: !image-2021-01-06-17-04-40-018.png|width=793,height=269! But in driver code declared: typedef Power_Ip_ResetType Mcu_ResetType; so we must update Mcu_ResetType follow req
ARTD-6062	Bug	[ICU][S32K3XX] The ICU_START_SEC_CODE and ICU_STOP_SEC_CODE macros are defined in wrong file.<*> The ICU_START_SEC_CODE and ICU_STOP_SEC_CODE macros are defined in src file. They should be defined in header file. pls see attach file.

ID	Subtype	Headline and Description
ARTD-6072	Bug	[S32K3]IAR linking issues<*> There has been linker errors with having the placement of sections with mixed content errors, I have the two that I am aware of below. The solution has been to change the section names in the cfg C files to correct the linker error: a. Error[Lp005]: placement includes a mix of sections with content (example "rw data section .mcal_bss in Adc_PBcfg.o") [suitable for placement in ROM] and sections without content (example "rw code section .ramcode in C:\Projects\SAM_K3_Test \linker_flash.icf 150 b. Error[Lp005]: placement includes a mix of sections with content (example "rw data section .mcal_bss_no_cacheable in Port.o") [suitable for placement in ROM] and sections without content (example "zi section .mcal_bss_no_cacheable C:\Projects \SAM_K3_Test\linker_flash.icf 153
ARTD-6077	Bug	[GPT][S32DS] Gpt got undefined error<*> Gpt got undefined error in PBcfg.c file for Pit, Stm and Emios, file generate is empty: See more detail in log file as in attachment !image-2021-01-07-13-33-18-812.png!
ARTD-6080	Bug	[S32K3xx_Beta][Port] EB tresos still config PortPin Slew Rate bit when driver not support by hardware<*> Detailed description (how to reproduce it): Configuration some pins by pins tool in S32DS. Slew Rate is Slowest setting. Some pins with config PortPin Slew Rate is Slowest setting, bit MSCR[SRC] not set to 1 (Slowest setting). Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Some pins has bit MSCR[SRC] default is not available by hardware.
ARTD-6082	Bug	[ICU] IcuDMAChannelRef has to be configured even if DMA is not used<*> In ICU driver, the parameter IcuDMAChannelRef has a multiplicity of 1:1 in the epd file. Thus, it has to be configured even if DMA is not used. The issue can be resolved, by adding OPTIONAL attribute for these parameters (refer to the attachment)
ARTD-6089	Bug	[S32K344 BETA][SENT] Some nodes need to refer from resource table in CDD_Sent/ Flexio.component<*> Issue*: 1. There are some node are hard code in CDD_Sent/Flexio.component files. flexio_sent_cfg_channelHwOffset items="toArray(`CHANNEL_0`,`CHANNEL_1`,`CHANNEL_2`,`CHANNEL_3`,`CHANNEL_4`,`CHANN flexio_sent_cfg_sentPinSelection items="toArray(`PIN_0`,`PIN_1`,`PIN_2`,`PIN_3`,`PIN_4`,`PIN_5`,`PIN_6`,`PIN_7`,`PIN_8`,`PIN_9`,`P flexio_sent_cfg_ControllerHwOffset items="toArray(`FLEXIO_0`,`FLEXIO_1`) 2. Disable node which does not support in K3: SentDmaBufferDepth 3. SentDmaChannelReference need to be enabled when SentDmaActivation=true.

ID	Subtype	Headline and Description
ARTD-6092	Bug	[MCL][CACHE] Cache_Ip_InvalidateByAddr(CACHE_IP_INSTRUCTION) doesn't invalidate entire length<*> Detailed description (how to reproduce it): Configure for Mcl drive with EB tool: The bug : The funtion Mcl_CacheCleanByAddr and Mcl_CacheInvalidateByAddr function can not invalidate or clean correct when the buffer is unalign with 32 byte. Please, see the attached Bug_cache1.PNG and Bug_cache file for more detail. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Mcl_TC_FCT_0802.c Mcl_TC_FCT_0804.c Observed behavior: N/A Expected behavior: N/A Note:* in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-6098	Bug	[S32K3XX] [PORT] Issue about IBE register value of Port_Init with Analog mode<*> Detailed description (how to reproduce it): When Port_Init pin analog mode, value IBE=1, but after that, declare function Port_ResetPinMode, ==>value IBE=0 Test Case ID (internal TC that caught the defect) optional: Port_TC_FCT_0033 Observed behavior: Call Port_Init: !image-2021-01-08-14-13-48-554.png! After Port_ResetPinMode: !image-2021-01-08-14-15-09-961.png! Expected behavior: Port_Init pins need to fix value IBE = 0, we declare function Port_ResetPinMode, register IBE need to be keep same value with init

ID	Subtype	Headline and Description
ARTD-6100	Bug	Pins not configurable as Input/Output<*> When setting the direction of a pin as Input, in the Routed Pins table, included in the Pins Tool (S32 Configuration Tools), the following input options are set in the configuration structure (input.png). When changing the direction of the pin as Output, the .mux field changes, but the previously shown input settings are not kept (output.png). The Siul2 component should offer the functionality of keeping both Input and Output settings when configuring a pin (e.g: inputMux[0] = PORT_INPUT_MUX_ALT1, inputMuxReg[0] = 217u and also .mux = PORT_MUX_ALT4). Currently, one selection cancels the settings made for the other. This functionality has an application inside the LPI2C example. There, the LPI2C pins must have both Input and Output settings. Currently, to ensure the example functionality, these settings are made by using an additional function Init_Pins, where the corresponding values are written inside MSCR and IMCR registers. (lpi2c_example.png) However, this approach does not use the Siul2_Port_Ip_Init function, since the pins configurations are not available from the Pins tool in Configuration Tools, as previously shown. To avoid writing values into specific registers, the workaround for the encountered issue is to configure the pins as an Input using the Pins Tool from CT (configuration.png), and then to add the output settings using the SetOutputBuffer API (code.png). However, we would like to be able to use the API functions for Pins initialization since this workaround assumes that the Pins initialization must be done every time the user wants to modify a pin of a specific functionality. Moreover, the IO Signal Table must be opened to find the appropriate MUX_ALT option, instead of just simply calling the Siul2_Port_Ip_Init function.
ARTD-6101	Bug	Siul2 PORT defines<*> The PORT[A-G] defines, in Siul2_Port_Ip_Defines.h (siul2_defines.png) assume that each PORT has 16 pins, instead of 32, as specified in the Reference Manual of S32K3 (ports_definition.png). Thus, for configuring for example the pin PTC6, the specified port must be PORTE (since PORTA covers the first 16 pins of the first port, PORTB the next 16 bits of the first port, PORTC the first 16 bits of the second port and so on). Moreover, for configuring for example PTF20, no define comes in hand (considering the same logic as previously described), and the address of the port needs to be computed as (PORT_Type)(SIUL2_MSCR_BASE 0xB0). Attached is an example (example.png) of using the Siul2_Port_Ip_SetOutputBuffer function for configuring output settings for the PTF20, PTF21, PTC6 and PTC7 pins. If the first argument is replaced to the appropriate defines (PORTF for the first 2 functions and PORTC for the next ones), hard faults will occur when these functions are executed.
ARTD-6102	Bug	[ADC] Naming convention: generated files <MSN>_PBCfg.h/c must change to <MSN>_PBcfg.h/c<*> Naming of generated files <MSN>_PBCfg.h/c should change to <MSN>_PBcfg.h/c in order to correctly generate the files for each variant within the list of functional groups.

ID	Subtype	Headline and Description
ARTD-6112	Bug	[GPT][S32CT] Cannot refer to the GptModuleRef node, and after workaround the project, the build code fails in GHS and IAR compiler ,,"Detailed description (how to reproduce it): Step 1: Pull code from tag PVT_GPT_ARTD_5492_V04, compile plugin and generate layout Step 2: Config for GPT and dependent module Step 3: Run command: make clean generate and make build Preconditions: [...] Observed behavior: Cannot refer to the GptModuleRef node, and after workaround the project, the build code fails in GHS and IAR compiler. Detail was attached. Expected behavior: The project no warnings, errors after generate and build code
ARTD-6116	Bug	[ICU][S32K3XX] Some macros are not generated at the IPL in eMios module<*> The EMIOS_ICU_DEINIT_API macro and some macros about feature are generated at the IPL in eMios module (eg: EMIOS_ICU_EDGE_COUNT_API). And in the DS interface there is no nodes to select these features. pls see attach file.
ARTD-6109	Bug	[S32K3XX][PWM] Emios_Pwm_Ip_ChannelConfigType type is undefined in Emios_Pwm_Ip_VS_0_PBcfg.h file<*> Build error: Emios_Pwm_Ip_ChannelConfigType type is undefined in Emios_Pwm_Ip_VS_0_PBcfg.h file. Emios_Pwm_Ip_ChannelConfigType type is defined in Emios_Pwm_Ip_Types file. But if you include Emios_Pwm_Ip_Types.h in this file, it will be included repeatedly (Emios_Pwm_Ip_Cfg.h > Emios_Pwm_Ip_VS_0_PBcfg.h > Emios_Pwm_Ip_Types.h-> Emios_Pwm_Ip_Cfg.h). I think you should create a new file to define this structure and include this file.
ARTD-6110	Bug	[S32K3XX][PWM] Define Emios_Pwm_Ip_DeInitChannel function do not match the requirement<*> Define function in driver code: void Emios_Pwm_Ip_DeInitChannel(uint8 instance, uint8 channel, Emios_Pwm_Ip_OutputStateType safeState) And in the requirement: void Emios_Pwm_Ip_DeInitChannel(uint8 instance, uint8 channel) Please update one of the 2 so they are in sync.
ARTD-6115	Bug	[S32K3XX][MCL] Missing line break when config Emios_Mcl_Ip with S32CT<*> When config Emios_Mcl_Ip and enable interrupt in S32CT, 3 define ISR_USED in Emios_Mcl_Ip_CfgDefines.h file do not have line break. It cause fail at build. Please see in attach file.

ID	Subtype	Headline and Description
ARTD-6123	Bug	[S32K3XX BETA] DMA Transfer using Channel Link doesn't work for the second transfer<*> Behavior: there are some bit fields are depended on DONE flag (MAJORELINK, ESG in TCDn_CSR). So for the next transfer if this register is updated while DONE=1; MAJORELINK and ESG will be forced to 0. !image-2021-01-08-18-31-42-227.png|thumbnail! Solution: DMA DONE flag should be cleared each time transfer complete in IRQHandler to avoid unexpected behavior
ARTD-6125	New	New Feature [CRYPTO]AES key generation improvement ,,"The AES key length can be taken from CryptoKeyElementSize(xdm configuration) filled in Tresos configurator, which translates to u32CryptoKeyElementMaxSize(Crypto_Cfg.c) instead of pu32CryptoElementActualSize(Crypto_Cfg.c) which must be set by calling Crypto_KeyElementSet(). The change in code: u32KeyLength = Crypto_aKeyElementList[u32KeyMaterialKeyElemIdx].pu32CryptoElementActualSize; to u32KeyLength = Crypto_aKeyElementList[u32KeyMaterialKeyElemIdx].u32CryptoKeyElementMaxSize;"
ARTD-6126	Bug	[GPT] Code generation error "config class PostBuild which is not allowed in this context" ,,"Detailed description (how to reproduce it): GPT has consistent error when using Post Build Variants (even with generic XDM). GPT module complains that PostBuild is not allowed in this context, but there is no post build configuration set up here. I have verified that there is no post build variants in the GPT.xdm file. Error message: Invalid XPath-expression for Attribute ""INVALID"" of node ""/AUTOSAR/TOP-LEVEL-PACKAGES/Gpt/ELEMENTS/Gpt/GptChannelConfigSet/GptPit/GptPit_Ecu_Sync_Timer_Device/GptPitChannels"": (1822) Attempt to read value of node /AUTOSAR/TOP-LEVEL-PACKAGES/Gpt/ELEMENTS/Gpt/GptChannelConfigSet/GptPit/GptPit_Ecu_Sync_Timer_Device/GptPitChannels/GptPitChannel_0/GptPitChannel with config class PostBuild which is not allowed in this context It seems the error is reported because the configuration parameter of config class precompile is referencing in INVALID tag a parameter which is postbuild. As a workaround the checkbox ""Enable Config Time support"" in properties of Tresos project can be disabled. Preconditions: Checkbox "Enable Config Time support" is enabled in properties of Tresos project. Observed behavior: Code generation error. Expected behavior: No code generation error. Proposed solution*: Modify the configuration class of configuration parameter in xdm file so that both parameters are of the same configuration class.

ID	Subtype	Headline and Description
ARTD-6127	Bug	[SPI] Code generation error "config class PostBuild which is not allowed in this context" ,,"Detailed description (how to reproduce it): SPI has consistent errors when using Post Build Variants (even with generic XDM). SPI module complains that PostBuild is not allowed in this context, but there is no post build configuration set up here. I have verified that there is no post build variants in the SPI.xdm file. Error messages: Invalid XPath-expression for Attribute ""RANGE"" of node ""/AUTOSAR/TOP-LEVEL-PACKAGES/Spi/ELEMENTS/Spi/SpiDriver/SpiExternalDevice/MMIC_1_SPI_40_MHz_Device/SpiCsIdentifier"": (1822) Attempt to read value of node /AUTOSAR/TOP-LEVEL-PACKAGES/Spi/ELEMENTS/Spi/SpiDriver/SpiExternalDevice/MMIC_1_SPI_40_MHz_Device/SpiHwUnit with config class PostBuild which is not allowed in this context Invalid XPath-expression for Attribute ""INVALID"" of node ""/AUTOSAR/TOP-LEVEL-PACKAGES/Spi/ELEMENTS/Spi/SpiDriver/SpiJob/MMIC_1_40MHz_Job/SpiChannelList"": (1822) Attempt to read value of node /AUTOSAR/TOP-LEVEL-PACKAGES/Spi/ELEMENTS/Spi/SpiDriver/SpiExternalDevice/MMIC_1_SPI_40_MHz_Device/SpiHwUnit with config class PostBuild which is not allowed in this context It seems the error is reported because the configuration parameter of config class precompile is referencing (in INVALID, or in RANGE tag) a parameter which is postbuild. As a workaround the checkbox ""Enable Config Time support"" in properties of Tresos project can be disabled. Preconditions: Checkbox "Enable Config Time support" is enabled in properties of Tresos project. Observed behavior: Code generation error. Expected behavior: No code generation error. Proposed solution*: Modify the configuration class of configuration parameter in xdm file so that both parameters are of the same configuration class.

ID	Subtype	Headline and Description
ARTD-6155	Bug	[gpt] Fix all M4, TABs, duplicated UUIDs ,,"Coding convention implies that no TAB is to be used in the code source files we deliver. (to avoid inconsistent displays of code alignment if TAB size is defined differently) Replace all duplicated UUIDs, to avoid generation crashes on customer side. Proposed solution: # Replace all TABs with 4 spaces. # Update your text editor settings to always use 4 spaces instead of a TAB # Replace duplicated UUIDs. Summary: Plugin*|*No. of duplicated UUIDs Eth.xdm | 1 Gpt.xdm | 2 Lin.xdm | 2 Platform.xdm | 17 Port.xdm | 1 Rm.xdm | 158 Rm_s32k314_mapbga257.xdm | 23 Rm_s32k314_mqfp100.xdm | 79 Rm_s32k314_mqfp172.xdm | 79 Rm_s32k324_mapbga257.xdm | 79 Rm_s32k324_mqfp172.xdm | 79 Rm_s32k344_mapbga257.xdm | 79 Rm_s32k344_mqfp172.xdm | 79 Sai.xdm | 22 Uart.xdm | 8 Wdg.xdm | 197 *Keyword* | *Hits* \t | 2330 M4_ | 54 *File* | *Hits* Dma_Ip_Hw_Access.c | 293 main.c | 192 Lpi2c_Ip.c | 176 Dma_Ip_Hw_AccessInline.h | 175 Uart_Ipw.c | 130 FlexCAN_Ip.c | 126 Dma_Ip.h | 112 Cache_Ip_HwAcc_ArmCoreMx.h | 97 Cache_Ip.c | 78 Dem_stub.c | 71 I2c_Ipw.c | 57 Dma_Ip_Irq.c | 53 FlexCAN_Ip_HwAccess.h | 49 Clock_Ip_Private.h | 48 Dma_Ip_Cfg_Defines.h | 40 FlexCAN_Ip_Types.h | 40 Det_stub.c | 39 Uart_Ipw.h | 38 FlexCAN_Ip_HwAccess.c | 35 Lpuart_Lin_Ip_Irq.c | 32 sys_init.c | 29 S32K344_AXBS_LITE.h | 28 Dma_Ip_Driver_State.c | 28 Clock_Ip_Monitor.c | 27 FlexCAN_Ip.h | 27 Mpu_M7_Ip.c | 23 Lpi2c_Ip_Types.h | 21 system.c | 19
Release notes		

ID	Subtype	Headline and Description
ARTD-6157	Bug	[sai] Fix all M4, TABs, duplicated UUIDs ,,"Coding convention implies that no TAB is to be used in the code source files we deliver. (to avoid inconsistent displays of code alignment if TAB size is defined differently) Replace all duplicated UUIDs, to avoid generation crashes on customer side. Proposed solution: # Replace all TABs with 4 spaces. # Update your text editor settings to always use 4 spaces instead of a TAB # Replace duplicated UUIDs. Summary: Plugin*|*No. of duplicated UUIDs Eth.xdm | 1 Gpt.xdm | 2 Lin.xdm | 2 Platform.xdm | 17 Port.xdm | 1 Rm.xdm | 158 Rm_s32k314_mapbga257.xdm | 23 Rm_s32k314_mqfp100.xdm | 79 Rm_s32k314_mqfp172.xdm | 79 Rm_s32k324_mapbga257.xdm | 79 Rm_s32k324_mqfp172.xdm | 79 Rm_s32k344_mapbga257.xdm | 79 Rm_s32k344_mqfp172.xdm | 79 Sai.xdm | 22 Uart.xdm | 8 Wdg.xdm | 197 *Keyword* | *Hits* \t | 2330 M4_ | 54 *File* | *Hits* Dma_Ip_Hw_Access.c | 293 main.c | 192 Lpi2c_Ip.c | 176 Dma_Ip_Hw_AccessInline.h | 175 Uart_Ipw.c | 130 FlexCAN_Ip.c | 126 Dma_Ip.h | 112 Cache_Ip_HwAcc_ArmCoreMx.h | 97 Cache_Ip.c | 78 Dem_stub.c | 71 I2c_Ipw.c | 57 Dma_Ip_Irq.c | 53 FlexCAN_Ip_HwAccess.h | 49 Clock_Ip_Private.h | 48 Dma_Ip_Cfg_Defines.h | 40 FlexCAN_Ip_Types.h | 40 Det_stub.c | 39 Uart_Ipw.h | 38 FlexCAN_Ip_HwAccess.c | 35 Lpuart_Lin_Ip_Irq.c | 32 sys_init.c | 29 S32K344_AXBS_LITE.h | 28 Dma_Ip_Driver_State.c | 28 Clock_Ip_Monitor.c | 27 FlexCAN_Ip.h | 27 Mpu_M7_Ip.c | 23 Lpi2c_Ip_Types.h | 21
Release notes		

ID	Subtype	Headline and Description
ARTD-6158	Bug	[wdg] Fix all M4, TABs, duplicated UUIDs ,,"Coding convention implies that no TAB is to be used in the code source files we deliver. (to avoid inconsistent displays of code alignment if TAB size is defined differently) Replace all duplicated UUIDs, to avoid generation crashes on customer side. Proposed solution: # Replace all TABs with 4 spaces. # Update your text editor settings to always use 4 spaces instead of a TAB # Replace duplicated UUIDs. Summary: Plugin*|*No. of duplicated UUIDs Eth.xdm | 1 Gpt.xdm | 2 Lin.xdm | 2 Platform.xdm | 17 Port.xdm | 1 Rm.xdm | 158 Rm_s32k314_mapbga257.xdm | 23 Rm_s32k314_mqfp100.xdm | 79 Rm_s32k314_mqfp172.xdm | 79 Rm_s32k324_mapbga257.xdm | 79 Rm_s32k324_mqfp172.xdm | 79 Rm_s32k344_mapbga257.xdm | 79 Rm_s32k344_mqfp172.xdm | 79 Sai.xdm | 22 Uart.xdm | 8 Wdg.xdm | 197 *Keyword* | *Hits* \t | 2330 M4_ | 54 *File* | *Hits* Dma_Ip_Hw_Access.c | 293 main.c | 192 Lpi2c_Ip.c | 176 Dma_Ip_Hw_AccessInline.h | 175 Uart_Ipw.c | 130 FlexCAN_Ip.c | 126 Dma_Ip.h | 112 Cache_Ip_HwAcc_ArmCoreMx.h | 97 Cache_Ip.c | 78 Dem_stub.c | 71 I2c_Ipw.c | 57 Dma_Ip_Irq.c | 53 FlexCAN_Ip_HwAccess.h | 49 Clock_Ip_Private.h | 48 Dma_Ip_Cfg_Defines.h | 40 FlexCAN_Ip_Types.h | 40 Det_stub.c | 39 Uart_Ipw.h | 38 FlexCAN_Ip_HwAccess.c | 35 Lpuart_Lin_Ip_Irq.c | 32 sys_init.c | 29 S32K344_AXBS_LITE.h | 28 Dma_Ip_Driver_State.c | 28 Clock_Ip_Monitor.c | 27 FlexCAN_Ip.h | 27 Mpu_M7_Ip.c | 23 Lpi2c_Ip_Types.h | 21
Release notes		

ID	Subtype	Headline and Description
ARTD-6129	Bug	S32K3 RTD CT Pins Config ADC Standard Input<*> When I select more than one ADC standard channels within on ADC module in S32DS Configuration Tool Pins configure, there are be errors reported. It looks like the Pins configure support only one standard input for one ADC module. But there are actually 16 standard channels within one ADC module.
ARTD-6130	Bug	S32K3 CT Pins Initial Values<*> We are not able to configure a pin's initial value if we configure it as SIUL GPIO output. We can manually add .initValue in the generated file "Siul2_Port_Ip_Cfg.c". Is it possible to add this feature into the configuration tool?
ARTD-6163	Bug	[S32K3XX]icu: Missing Emios instance 3 in S32DS<*> Missing Emios instance 3 in S32DS !image-2021-01-11-14-45-58-237.png|thumbnail!
ARTD-6165	Bug	[ETH] Hard fault happened with function Eth_GetCurrentTime<*> a hard fault happens Eth_GetCurrentTime with parameter timeQualPtr = NULL_PTR The cause from code line: return ((ETH_VALID == timeQualPtr*) ? (Std_ReturnType)E_OK : (Std_ReturnType)E_NOT_OK);
ARTD-6167	Bug	[S32XX][SENT] Wrong convert value from integer to hex for u8SentPin in Flexio_Ip_PBcfg.c<*> When test for S32CT, Flexio_Ip_PBCfg.c generate wrong u8SentPin value / Flexio pin to use as SENT Pin / / Flexio pin to use as SENT Pin / (uint8)0x $pinSelection$U, pinSelection is integer type, so can not put 0x before $pinSelection$U, Solution Delete "0x" in both Flexio_Ip_PBcfg.c and Sent_PBcfg.c for S32CT
ARTD-6168	Bug	[S32XX][SENT] Missing generating FXIO_ISR_PROCESS_TIMER_CTRL0 definition when driver is in POLLING mode<*> When test S32CT with Serial message with POLLING mode, driver will use interrupt to handle compare value by using interrupt with FXIO_ISR_PROCESS_TIMER_CTRL0. But Flexio_Ip_Cfg.h did not generate FXIO_ISR_PROCESS_TIMER_CTRL0 to use Flexio_Sent_Ip_IRQTimerHandler function. It causes Serial message did not work. Solution: FXIO_ISR_PROCESS_TIMER_CTRL0 need to defined incase driver is in POLLING mode

ID	Subtype	Headline and Description
ARTD-6172	Bug	[S32XX][SENT] Build fail when run test on IP for S32CT<*> There are some build fail errors when compile test for S32CT on IP. 1. Flexio_Ip_Irq.c and Flexio_Sent_Ip_Types.h include Sent_Cfg.h 2. Flexio_Sent_Ip_Types.h used some definition from HL. #if(STD_ON == SENT_DMA_FEATURE_ENABLE) const uint8 u8SentDmaChannel; /*!< Reference to the DMA Channel configure for the Request / #endif #if(STD_ON == SENT_DMA_FEATURE_ENABLE) uint8 sentDmaChannel; /*!< Reference to the DMA Channel configure for the Request / #endif
ARTD-6174	New	New Feature [ADC] Port DMA for CTU Control Mode ,,"# DMA for Control Mode to be moved in IPL # only for FIFOs, not also for result regs # use DMA IPL # use same configuration members in FIFO config as from BCTU mcal configuration dma channel as input. Buffer allocated by user # use code from Adc_Bctu_SetupDma and Adc_Ipw_BctuFifoXDmaComplete # Support Transferring FIFO RAW DATA and only result DATA (Full FIFO and only CDATA field) for K3. Similar with S32G RTM 1.0.0 Update Tresos and S32CT components Create dev test for basic validation Refer to S32G RTM 1.0.0"
ARTD-6194	Bug	[S32K3XX]icu: Missing Emios_Icu_Ip_GetCaptureRegValue function in driver code<*> Missing Emios_Icu_Ip_GetCaptureRegValue in driver code. On the other hand, Emios_Icu_Ip_EnableInterrupt and Emios_Icu_Ip_DisableInterrupt must not in static inline return type.
ARTD-6195	Bug	[GPT][S32DS] RTC Ip got undefined error in code generate with s32ct<*> RTC Ip got undefined error as below: !image-2021-01-12-09-45-12-470.png! In code generated with s32ct, Rtc_Ip_BOARD_InitPeripherals_PBcfg.c file is empty !image-2021-01-12-09-47-23-609.png! See more detail in attachment files.
ARTD-6193	New	New Feature [S32K344 BETA] [UART] - Fix memory sections for FlexIO ,,The memory sections shall be added/fixed in the lpuart and flexio drivers.
ARTD-6208	Bug	[ICU][S32K3XX] macro EMIOS_ICU_CONFIG_VS_0_PB was created incorrectly<*> macro EMIOS_ICU_CONFIG_VS_0_PB was created incorrectly. If configuration is not used eMios channel then the generation file still has EMIOS_ICU_CONFIG_VS_0_PB macro and WKPU channel (channel is used) is not generated.

ID	Subtype	Headline and Description
ARTD-6215	Bug	[S32K3][Crypto][CT] An error has occurred when adding new 'CryptoKeyElement' and then disable 'Use HSE Key'<*> Detailed description (how to reproduce it): # Open S32DS3.4 # Add Crypto component # Add KeyCatalogs # Add CryptoKeyElements # Click on the 'Authenticated Key Export' tab # In General tab, disable 'Use HSE Key' Test Case ID (internal TC that caught the defect): Crypto_TS_Eq_Cot_01 Observed behavior: When user adding new 'CryptoKeyElement' and then disable 'Use HSE Key', an error has occurred Expected behavior: No error has occurred, when adding CryptoKeyElement
ARTD-6222	Bug	[GPT][S32CT] Build code error in IAR compiler<*> Detailed description (how to reproduce it): Step 1: Pull code from tag GPT_012, compile plugin and generate layout Step 2: Config for GPT and dependent module Step 3: Run command: make clean generate and make build Preconditions: [...] Observed behavior: Build code error in IAR compiler. Detail was attached. Expected behavior: The project no warnings, errors after generate and build code
ARTD-6224	Bug	[Ip_FlexCAN][FLEXCAN_IP_014_002] FlexCAN_Ip_ReceiveBlocking can not return FLEXCAN_STATUS_BUSY<*> Call FlexCAN_Ip_Receive Call FlexCAN_Ip_ReceiveBlocking => Verification point: FlexCAN_Ip_ReceiveBlocking return BUSY => fail due to it return TIMEOUT !image-2021-01-12-17-32-41-604.png!
ARTD-6231	New	New Feature [ADC] CTU Hardware Trigger Optimization ,,"Implement feature Add dev test for basic validation CPRT requirement: ""It shall be possible to configure the CTU/BCTU channel lists only once at initialization in order to reduce cpu load when calling the Adc_EnableHardwareTrigger and Adc_EnableCtuTrigger APIs. When enabling this optimization the Adc_SetChannel service cannot be used, and the maximum size of groups cannot exceed the size of the entire command list divided by the number of adc hardware units triggered by the CTU/BCTU. This optimization can be enabled or disabled using a Boolean configuration parameter named CTU Enable Hardware Trigger Optimization. Per default this optional optimization shall be disabled."" "

ID	Subtype	Headline and Description

ARTD-6239	Bug	[S32K3XX][GPT] [EB_S32DS]The total number of channel of PIT instance 0 is extra without enable PIT RTI channel<*>
		
		I find that when user want to use PIT_RTI channel, this section is declared in file Pit_Ip_Types.h:
		#if (defined (PIT_IP_RTI_USED) && (PIT_IP_RTI_USED == STD_ON))
		#define RTI ((uint8)4)
		#endif
		So in case user does not enable RTI channel, the macro PIT_IP_RTI_USED will be STD_OFF, the RTI macro is not generated, so the total number of channel of PIT 0 is checked in interrupt function(PIT_0_CHANNELS_NUMBER) must not to be included RTI channel :
		ISR(PIT_0_ISR)
		{
		uint8 instance = 0U;
		uint8 channel;
		uint32 temp = 0;
		for (channel = 0U; channel < PIT_0_CHANNELS_NUMBER{color}; channel++)
		{
		temp = Pit_Ip_GetInterruptFlags(instance, channel);
		if (1U == temp)
		{
		Pit_Ip_ProcessCommonInterrupt(instance, channel);
		}
		}
		}
		The matter is PIT_0_CHANNELS_NUMBER is always defined is 5 channel. So this results hardfault when checking index channel 4 (RTI)

ARTD-6240	Bug	[GPT] Add missing PIT_2 AND STM_1 instance from resource on S32K314<*> when configuring pit and stm channels I saw a lack of resources for s32k314 This RM has described very clearly
ARTD-6243	Bug	[S32K3][SENT] Missing Usemode, DevErrorDetect in IPL for S32DS ,,"In IPL for S32DS, flexio.component is missing Usermode, DevErrorDetect node. 2 nodes should be added to Flexio.component file.

ID	Subtype	Headline and Description
ARTD-6250	Bug	[ADC] Hard fault error when calling Adc_EnableCTUTrigger, Adc_DisableCTUTrigger before Adc_Init ,,"Detailed description (how to reproduce it): Hard fault error when calling Adc_EnableCTUTrigger, Adc_DisableCTUTrigger before Adc_Init Preconditions: Calling Adc_EnableCTUTrigger, Adc_DisableCTUTrigger before Adc_Init Test Case ID (internal TC that caught the defect) optional: Adc_TC_FCT_0120 Adc_TS_045 Observed behavior: Calling Adc_EnableCTUTrigger before Adc_Init Expected det error uninit (requirement: CPR_RTD_00038.adc) Real status: Hard fault because calling const Adc_GroupConfigurationType const pGroupConfig = &(Adc_pCfgPtr[u32CoreId]->pGroups[Group]); before init Expected behavior: det error uninit Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-6251	Bug	[ADC] Adc_EnableCTUTrigger, Adc_DisableCTUTrigger need to validate if TriggerSource is not configured ,,"Detailed description (how to reproduce it): Adc_EnableCTUTrigger, Adc_DisableCTUTrigger need to validate if TriggerSource is not configured for the group Preconditions: Adc_EnableCTUTrigger, Adc_DisableCTUTrigger with trigger source out of trigger source configured Test Case ID (internal TC that caught the defect) optional: Adc_TC_FCT_0120 Adc_TS_045 Observed behavior: Calling Adc_Init Calling Adc_EnableCTUTrigger with trigger source is 95 (out of configuration 12) Expected det error (requirement: CPR_RTD_00038.adc) Real status: Hard fault error because implement with wrong trigger source Expected behavior: det error wrong bctu trigger source (requirement: CPR_RTD_00038.adc) Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA

ID	Subtype	Headline and Description
ARTD-6263	Bug	[ADC] Adc_DisableCTUTrigger report wrong det error Api ID<*> Detailed description (how to reproduce it): Adc_DisableCTUTrigger report wrong det error Api ID Preconditions: Adc_DisableCTUTrigger with sw trigger group Test Case ID (internal TC that caught the defect) optional: Adc_TC_FCT_0120 Adc_TS_045 Observed behavior: Invoke Adc_DisableCTUTrigger() but the Group is sw trigger group Verification point: Det error ADC_E_WRONG_TRIGG_SRC Real status: Det error with api id ADC_ENABLECTUTRIGGER_ID Expected behavior: EU_ASSERT_FATAL(Det_TestLastReportError(ADC_MODULE_ID, 0U, ADC_DISABLECTUTRIGGER_ID, ADC_E_WRONG_TRIGG_SRC)); Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-6300	Bug	[WDG][CT] EB supports multicore for 1 instance, but CT doesn't support ,,"Detailed description (how to reproduce it): Step 1: Pull code from tag WDG_045_V02, compile plugin and generate layout Step 2: Config S32CT and dependent modules Step 3: make clean generate and make build Preconditions: [...] Observed behavior: EB supports multi-core for 1 instance, but CT doesn't support. Expected behavior: Update CT support for 1 instance to users still can configure multicore in 1 instance

ID	Subtype	Headline and Description
ARTD-6310	Bug	[ADC] Hard fault error when starting group using dma by fixing hard code DMA_LOGIC_CH_0_NOF_CFG_SGA_ELEMENTS<*> Detailed description (how to reproduce it): Hard fault error when starting group using dma by fixing hard code DMA_LOGIC_CH_0_NOF_CFG_SGA_ELEMENTS Preconditions: Starting group using DMA transfer Test Case ID (internal TC that caught the defect) optional: Adc_TC_FCT_0101 Adc_TS_014 Observed behavior: Starting sw trigger group using DMA Verify conversion result Real status: Hard fault error as attachment because generated array by mcl driver only have 2 elements but adc driver access to the third element Expected behavior: No Hard fault error Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-6313	Bug	[platform] Pending interrupts are not clear after invoking Platform_Init in multicore context<*> Pending interrupt on all cores are not cleared except the one setting MSCM. For example: Config routing interrupt is responsible by core 0, so the pointer for core 1 is NUL, so pending interrupts will not be cleared on core 0. !image-2021-01-14-16-26-21-549.png!
ARTD-6320	Bug	[S32K3XX]icu: Difference between header and generated file in S32DS<*> !screenshot-1.png|thumbnail! Difference of eMios_Icu_Ip_ConfigType; between generated file and header file by missing #if (EMIOS_ICU_OVERFLOW_NOTIFICATION_API == STD_ON) as attached picture
ARTD-6321	New	New Feature [SAI] File version checks ,,File version checks
ARTD-6322	New	New Feature [SAI] Multicore support ,,Multicore support in EBT and S32CT
ARTD-6323	New	New Feature [SAI] Exclusive areas ,,Exclusive areas

ID	Subtype	Headline and Description
ARTD-6324	New	New Feature [SAI] Variant and pre-compile support for Tresos configurator ,,"Add dev test, fix any issues Check/add also precompile support (allowing calls to Init(NULL_PTR))"
ARTD-6325	New	New Feature [SAI] S32ConfigurationTool use functional group name as variant ,,S32ConfigurationTool use functional group name as variant (workaround instead of actual variant support)
ARTD-6344	Bug	[SAI] Wrong register reset value after using Sai_DeInit service<*> Detailed description (how to reproduce it): Wrong register reset value after using Sai_DeInit service After using Sai_DeInit service the TCSR register has wrong reset value, see the yellow highlight below: Wrong reset value 'SR' field in TCSR register Wrong RX register in Sai_Ip_RxDeInit function !image-2021-01-15-11-03-11-377.png! !image-2021-01-15-13-28-13-425.png! The Sai_DeInit service will disable the SAI module and configure the registers to their reset values. ID: 5 Req ID: SWS_SAI_00201 Master Req ID: Remarks: Comments (not visible in TM): Functionality / Item: Sai_DeInit Req Type: Functional Product: S32K3XX Fulfilled In: S32K3XX Req State: Approved Verification Criteria: Test Case Preconditions: [...] Observed behavior: Wrong register reset value after using Sai_DeInit service Expected behavior: Correct register reset value after using Sai_DeInit service Proposed solution optional:
ARTD-6351	Bug	[ICU] Update version checking for driver<*> Update version checking based on the attached violation report.
ARTD-6352	Bug	[PWM] Update version checking for driver<*> Update version checking based on the attached violation report.
ARTD-6354	Bug	[OCU] Update version checking for driver<*> Update version checking based on the attached violation report.

ID	Subtype	Headline and Description
ARTD-6355	Bug	[GPT] Update version checking for driver<*> Update version checking based on the attached violation report.
ARTD-6358	Bug	[platform] Compile error when installing NULL_PTR to interrupt handler.<*> There is error in compiling when config interrupt handler is NULL_PTR. !image-2021-01-15-15-13-26-929.png! !image-2021-01-15-15-14-22-419.png! The driver should add checking to not allow config NULL_PTR or NULL. However this limit ability to setting interrupt handler to NULL pointer.
ARTD-6364	Bug	[GPT] the macro EMIOS_GPT_IP_ENABLE_DISABLE_NOTIFICATION_API should not be guarded for using interrupt of EMIOS<*> If user does not enable notification function in autosar, the macro EMIOS_GPT_IP_ENABLE_DISABLE_NOTIFICATION_API = STD_OFF, so the interrupt function will not be declared. This results to error when user enable Emios hardware. !image-2021-01-15-17-06-50-414.png!
ARTD-6367	New	New Feature [SAI] Configurable BIT_CLK_SWAP and PACK_MODE ,,"Implement BIT_CLK_SWAP and PACK_MODE Add dev test for validation"
ARTD-6378	New	New Feature [SAI] Masking support ,,"Implement masking support preferably add as member in Sai_RequestType (and call Sai_Ip_SetNextMaskWords set Master Req ID in Doors Sai IP) or add new function at HLD layer to wrap Sai_Ip_SetNextMaskWords "
ARTD-6381	Bug	[S32K3xx][MCL] Array configuration is always NULL_PTR on S32DS<*> S32CT: Enable EMIOS common support is enabled in general tab but MCL array configuration is always NULL_PTR !image-2021-01-17-10-08-40-737.png|thumbnail! Two configs created with the same name !image-2021-01-17-11-17-22-821.png|thumbnail! Default period should be updated to be greater than offset at start value when user adds a new configuration Need to add a warning when user configuration is incorrect: Two configs with the same EMIOS instance Default period is greater than 65535 EB tresos: Add description for EmiosMclMasterBusModeType on EB !screenshot-1.png|thumbnail! Need to add a warning when user configuration is incorrect: Default period is less than or equal to offset at start value !screenshot-2.png|thumbnail!

ID	Subtype	Headline and Description
ARTD-6383	Bug	[S32K344][S32CT] Wrong maximum number of ADC channels in the BCTU command list<*> Detailed description (how to reproduce it): Use S32DS config for BCTU. In List command: The value maximum for list is 24. However, in RM is 32 Preconditions: Use S32DS config for BCTU. Observed behavior: !image-2021-01-18-08-37-20-120.png! Expected behavior: The value maximum of List command is 32. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-6393	Bug	[ICU][S32K3XX] SIUL2 and WKPU couldn't test Edge Detection with DS.<*> SIUL2 and WKPU don't have Notice, so Edge Detection can't be tested using DS.
ARTD-6425	Bug	[GPT] The prescaler of Emios channel is not changed accurately<*> When i change the prescaler of emios channel from value 2 to 3, the value of prescaler register need to be changed from 1 to 2. In fact in debug interface, I see the register change from 1 to 3. !image-2021-01-18-15-49-18-977.png! And configuration in EB as below : !image-2021-01-18-15-51-00-528.png! The reason for this is the old prescaler value in register is not cleared before writing the new value. !image-2021-01-18-15-55-07-552.png!
ARTD-6446	Bug	[S32K344 BETA][SENT] Timer Compare Register can not be updated when run on CORE_1<*> Issue*: When run test Sent_TS_100, Sent_TS_101 on CORE_1 or Multicore testing, Timer Compare Register can not be updated in both POLLING and INTERRUPT mode. Solution: Issue comes from Debug Enable bit (FlexIO Control Register). Timer Compare Register can be updated only when set Debug Enable bit.
ARTD-6458	Bug	[S32K344 BETA][SENT] Improve CYCLOMATIC COMPLEXITY<*> Issue: Sent has a function which CYCLOMATIC COMPLEXITY > 20. It comes from Flexio_Sent_Ip_GetSerialMsgData (with CYCLOMATIC COMPLEXITY = 22) Please improve Flexio_Sent_Ip_GetSerialMsgData to have CYCLOMATIC COMPLEXITY < 20.

ID	Subtype	Headline and Description
ARTD-6457	New	New Feature [ETH]Fix misra(continue) ,,"Fix misra rule 10.4, 5.6"
ARTD-6460	Bug	[SPI] Update driver code to reduce CYCLOMATIC COMPLEXITY and HIS metrics<*> Please update the driver to reduce CYCLOMATIC COMPLEXITY and HIS metrics for some functions: Event Description|Function Measured value of LEVEL metric 7.00 is higher than maximum value 4.00 allowed by the HIS metrics policy.|Lpspi_Ip_TransferProcess Measured value of LEVEL metric 5.00 is higher than maximum value 4.00 allowed by the HIS metrics policy.|Spi_Ipw_EndChannelCallback Measured value of LEVEL metric 7.00 is higher than maximum value 4.00 allowed by the HIS metrics policy.|Lpspi_Ip_SyncTransmit Measured value of CCM metric 25.00 is higher than maximum value 10.00 allowed by the HIS metrics policy.|Lpspi_Ip_SyncTransmit Measured value of CCM metric 27.00 is higher than maximum value 10.00 allowed by the HIS metrics policy.|Lpspi_Ip_TransferProcess
ARTD-6468	Bug	[S32K3XX][PWM] Cyclomatic complexity of Emios_Pwm_Ip_SetDutyCyclefunction higher than 20<*> Emios_Pwm_Ip_SetDutyCycle functions have complexity higher than 20, need to update to less than 20
ARTD-6464	Bug	[S32K3XX][ETH] The Gmac_Ip_ProvideRxBuff function does not work as expected with GCC compiler<*> The Gmac_Ip_ProvideRxBuff function does not work as expected with GCC compiler. Steps to reproduce: Initialize the GMAC module with reception ring size is 4, MAC loopback mode Send and Read the 4 prepared Ethernet frames => all frames are received successfully (and all the buffers in the receive ring are full) Provide the a new buffer pointing to a new memory area, then it will be used by the driver for further reception because all the buffers in the receive ring are full (call Gmac_Ip_ProvideRxBuff) Send and Read the fifth Ethernet frame Expected behavior:* When all the buffers in the receive ring are full, reading new frames will not work anymore; thus, by calling this function to provide a new buffer which is not used anymore pointing to a new memory area, the new frame will be received Actual behavior:* The frame is not received in run mode (it only received when run debug step by step for Gmac_Ip_ProvideRxBuff function)

ID	Subtype	Headline and Description
ARTD-6475	Bug	[SAI] Warnings in compiler warning report<*> Detailed description (how to reproduce it): There are some warnings in the Compiler Warnings report. For more details, please refer the report.[^RTD_SAI_Compiler_Warnings.xlsx] Preconditions: [...] Observed behavior: warnings in the Compiler Warnings report Expected behavior: No warnings in the Compiler Warnings report Proposed solution optional:
ARTD-6478	Bug	[S32K3XX][PWM] Missing extern call back function in Emios PBcfg.c file and define Emios ISR_USED<*> Missing extern call back function in Emios PBcfg.c file. It cause fail at build. If call back function is NULL_PTR, we can not pass dev essert: DevAssert(NULL_PTR != userChCfg->userCallback.cbFunction) and fail at run. Missing define EMIOS ISR_USED. It is used in process the interrupt function in Emios_Mcl_Ip_Irq.c file. If not defined, the function will not execute anything
ARTD-6491	Bug	[ICU] Code generation error "config class PostBuild which is not allowed in this context" ,,"Detailed description (how to reproduce it): For GPT I received this ticket I think you should check in your driver too. GPT's issue: GPT has consistent error when using Post Build Variants (even with generic XDM). GPT module complains that PostBuild is not allowed in this context, but there is no post build configuration set up here. I have verified that there is no post build variants in the GPT.xdm file. Error message: Invalid XPath-expression for Attribute ""INVALID"" of node ""/AUTOSAR/TOP-LEVEL-PACKAGES/Gpt/ELEMENTS/Gpt/GptChannelConfigSet/GptPit/GptPit_Ecu_Sync_Timer_Device/GptPitChannels"": (1822) Attempt to read value of node /AUTOSAR/TOP-LEVEL-PACKAGES/Gpt/ELEMENTS/Gpt/GptChannelConfigSet/GptPit/GptPit_Ecu_Sync_Timer_Device/GptPitChannels/GptPitChannel_0/GptPitChannel with config class PostBuild which is not allowed in this context It seems the error is reported because the configuration parameter of config class precompile is referencing in INVALID tag a parameter which is postbuild. As a workaround the checkbox ""Enable Config Time support"" in properties of Tresos project can be disabled. !image-2021-01-20-10-21-42-289.png|width=564,height=385! Preconditions: Checkbox "Enable Config Time support" is enabled in properties of Tresos project. Observed behavior: Code generation error. Expected behavior: No code generation error. Proposed solution*: Modify the configuration class of configuration parameter in xdm file so that both parameters are of the same configuration class.

ID	Subtype	Headline and Description
ARTD-6494	Bug	[S32K3XX][S32XX] OCU: Code generation error "config class PostBuild which is not allowed in this context" ,,"Detailed description (how to reproduce it): For GPT I received this ticket I think you should check in your driver too. GPT's issue: GPT has consistent error when using Post Build Variants (even with generic XDM). GPT module complains that PostBuild is not allowed in this context, but there is no post build configuration set up here. I have verified that there is no post build variants in the GPT.xdm file. Error message: Invalid XPath-expression for Attribute ""INVALID"" of node ""/AUTOSAR/TOP-LEVEL-PACKAGES/Gpt/ELEMENTS/Gpt/GptChannelConfigSet/GptPit/GptPit_Ecu_Sync_Timer_Device/GptPitChannels"": (1822) Attempt to read value of node /AUTOSAR/TOP-LEVEL-PACKAGES/Gpt/ELEMENTS/Gpt/GptChannelConfigSet/GptPit/GptPit_Ecu_Sync_Timer_Device/GptPitChannels/GptPitChannel_0/GptPitChannel with config class PostBuild which is not allowed in this context It seems the error is reported because the configuration parameter of config class precompile is referencing in INVALID tag a parameter which is postbuild. As a workaround the checkbox ""Enable Config Time support"" in properties of Tresos project can be disabled. !image-2021-01-20-10-21-42-289.png|width=564,height=385! Preconditions: Checkbox "Enable Config Time support" is enabled in properties of Tresos project. Observed behavior: Code generation error. Expected behavior: No code generation error. Proposed solution*: Modify the configuration class of configuration parameter in xdm file so that both parameters are of the same configuration class.
ARTD-6506	Bug	[CRYPTO] Spelling error<*> There is a spelling error in CRYPTO module. CYRPTO*_KE_KEYEXCHANGE_SHAREDVALUE CRYPTO spelling needs to be corrected to get the build through with the definition as expected by CSM upper module.
ARTD-6523	Bug	[SIUL2][ICU]:config tools generate "0" numChannel in configuration struct ,," Siul2_ICU initial process didn't work: In Siul2_Icu_Ip_Config_BOARD_INITPERIPHERALS the numChannels always be 0, didn't change by the config tools, and resulting SIUL_ICU initial failed without return any error. Location : Siul2_Icu_Ip_StA_BOARD_InitPeripherals_PBcfg.c !image-2021-01-21-16-27-35-791.png!

ID	Subtype	Headline and Description
ARTD-6526	Bug	[ICU][S32DS] Correct version checking added on DS generated files<*> Newly added version check of files does not take into account that for \ in DS generator we need to put \\\. All lines are generated without line concatenation so we have build error in DS. Also remove not used file Cmp_Ip_Defines.h from git repo
ARTD-6528	Bug	[port] Fix MISRA violations<*> Detailed description (how to reproduce it): There are some misra violation which need to be fixed or comment. Please refer the attachment for more detail Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: There are some misra violation Expected behavior: There is no misra violation Proposed solution optional:
ARTD-6525	Bug	[SIUL2][ICU]:ICU ISR is blocked<*> The SIUL2 ISR is always blocked, the config tools didn't generate the correct DEFINES AND MACROS. Location : Siul2_Icu_Ip_Irq.c !image-2021-01-21-16-38-05-697.png! !image-2021-01-21-16-46-02-068.png! Location : Siul2_Icu_Ip_Cfg.h !image-2021-01-21-16-38-48-782.png!
ARTD-6538	Bug	[CRYPTO]Crypto_Hse_ExportCipherScheme() called with NULL pointer parameter<*> If the configured CryptoKeyElement is used for symmetric key export without enabling the export, not ticking _HSE Key Export_, the configuration structure will generate with `pHseExportCipherScheme` as null pointer and the export request done via Crypto_KeyElementGet() API will call Crypto_Hse_ExportCipherScheme() with null pointer.
ARTD-6541	Bug	Number of LPSPI External Devices<*> When configuring LPSPI for S32K344 in s32ds3.4 CT, I can add 5 external devices at the most. If add one more external device in the LPSPI configuration, there are errors reported. See attached figure. And the mex file is with errors even after removing the LPSPI module in CT.

ID	Subtype	Headline and Description

ARTD-6542	Bug	s32k344 emios icu module issue<*>
		
		When configuring s32k344 in s32ds3.4, after adding Emios_Icu_Ip module into the project, the generated code is with problem. The Emios_Icu_Ip_ChannelConfigType structure generated in "Emios_Icu_Ip_StA_BOARD_InitPeripherals_PBcfg.c" doens't match this structure type definition in "Emios_Icu_Ip_Types.h"
		const Emios_Icu_Ip_ChannelConfigType
		Emios_Icu_Ip_0_ChannelConfig_PB_BOARD_INITPERIPHERALS[1U] =
		{
		/ brief IcueMios_0_Channel_0 /
		{
		/ brief Emios HW Module and Channel used by the Icu channel /
		0U,
		/ brief Emios Channel Freeze bit /
		FALSE,
		/ brief Emios Prescaler value /
		EMIOS_PRESCALER_DIVIDE_1,
		/ brief Emios Alternate Prescaler value /
		EMIOS_PRESCALER_DIVIDE_1,
		/ brief Emios IcuEmiosDigitalFilter value /
		EMIOS_DIGITAL_FILTER_BYPASSED,
		/ brief Emios IcuEmiosBusSelect value /
		EMIOS_BUS_INTERNAL_COUNTER,
		/ brief Emios IcuUserModeForDutycycle value /
		SAIC,
		/ brief Emios IcuSignalMeasureWithoutInterrupt bit /
		FALSE,
		/ brief Callback Pointer /
		NULL_PTR,
		/ brief Callback Param1*/
		0U
		}
		};
		
		typedef struct
		{
		uint8 hwChannel; /*!< Channel Id /
		eMios_Icu_Ip_UCModeType ucMode; /*!< eMios UC mode of operation /
		eMios_Icu_Ip_ModeType chMode; /*!< eMios module mode of operation /
		eMios_Icu_Ip_SubModeType chSubMode; /*!< eMios specific name of operation to execute /
		eMios_Icu_Ip_MeasType measurementMode; /*!< Measurement Mode for signal measurement*/
		eMios_Icu_Ip_EdgeType edgeAlignement; /*!< Edge alignment Mode for signal measurement*/
		boolean FreezeEn; /*!< Freeze enable /
		eMios_Icu_Ip_PrescalerType Prescaler; /*!< Channel Prescaler /
		eMios_Icu_Ip_PrescalerType AltPrescaler; /*!< Channel Alternate Prescaler /
		eMios_Icu_Ip_FilterType Filter; /*!< Channel Digital Input Filter /
		eMios_Icu_Ip_BusType CntBus; /*!< Channel Counter bus selection /
		boolean bWithoutInterrupt; /*!< Measurement of ICU signal property without using interrupt /
		CallbackFunctionTimestamp callbackTimestamp; /*!< The callback function for timestamp events /
		eMios_Icu_Ip_SignalMeasurementCallbackType callbackSM; /*!< The callback function for channels signal measurement /
		eMios_Icu_Ip_CallbackType callback; /*!< The callback function for channels edge detect events /
		uint8 callbackParams; /*!< The parameters of callback functions for channels events /
		} eMios_Icu_Ip_ChannelConfigType;

ID	Subtype	Headline and Description
ARTD-6543	Bug	[Wdg] Wdg_ChannelClearResetRequest must raise det instead of return code<*> Swt_Ip_RequestedReset must return SWT_IP_STATUS_TIMEOUT (instead of ERROR) if timeout occurred. Update also in SWT IP req in doors Wdg_ChannelClearResetRequest must raise det instead of return code: raise WDG_E_PARAM_TIMEOUT for SWT_IP_STATUS_TIMEOUT raise WDG_E_DRIVER_STATE when Swt_Ip_RequestedReset returns SWT_IP_STATUS_ERROR
ARTD-6545	Bug	[ADC] Adc_SetPowerState does not power down/up also BCTU when configured<*> [ADC] Adc_SetPowerState must power down/up also BCTU if configured
ARTD-6551	Bug	[S32K3XX] icu: Build fail due to some Define names are not correct with DS<*> !image-2021-01-22-11-27-27-906.png|thumbnail! Build fail due to some Define names are not correct with DS as picture
ARTD-6566	Bug	[S32K3xx][MCL] DEV_ASSERT should be added in driver code<*> EMIOS module on S32K344 only supports 3 instances and 24 channels so DEV_ASSERT should be added in driver code to check invalid input parameter for all functions as below: Emios_Mcl_Ip_Init Emios_Mcl_Ip_EnableChannel Emios_Mcl_Ip_DisableChannel Emios_Mcl_Ip_ComparatorTransferEnable Emios_Mcl_Ip_ComparatorTransferDisable Emios_Mcl_Ip_GetInstanceStatus Emios_Mcl_Ip_GetDebugMode Emios_Mcl_Ip_GetCounterBusMode Emios_Mcl_Ip_GetCounterBusPeriod
ARTD-6563	Bug	[ADC] Hard fault error when calling Adc_GetStreamLastPointer before Adc_Init<*> Detailed description (how to reproduce it): Hard fault error when calling Adc_GetStreamLastPointer before Adc_Init Preconditions: Calling Adc_GetStreamLastPointer before Adc_Init Test Case ID (internal TC that caught the defect) optional: Adc_TC_FCT_1201 Adc_TS_018 Observed behavior: Calling Adc_GetStreamLastPointer before Adc_Init Expected det error uninit (requirement: CPR_RTD_00038.adc) Real status: Hard fault because calling const Adc_GroupConfigurationType pGroupPtr = &(Adc_pCfgPtr[u32CoreId]->pGroups[GroupIndex]); Expected behavior: det error uninit Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA

ID	Subtype	Headline and Description
ARTD-6570	Bug	[GPT][RTC] Hardfault error when change the variable in output config as placing it in flash memory sector<*> When user use the Alarm feature. First user need to call function Rtc_Ip_ConfigureAlarm In this function, the pointer alarmConfig inside Rtc_Ip_u32ChState is pointed to the value of output alarm configuration . So the value of alarmConfig is not able to changed, because it is allocating in the flash memory. !image-2021-01-22-17-05-45-660.png! And in the interrupt funtion, a ointer variable is declared again and it is pointed to the alarm config pointer inside Rtc_Ip_u32ChState. So it means the variable alarmConfiguration in interrupt function is pointing to the address of the output alarm configuration. !image-2021-01-22-17-10-28-489.png! When have a change in value of pointer variable alarmConfiguration, it will result to a hardfault error as below: !image-2021-01-22-17-11-49-982.png! Because the alarm configuration generated is in a memory that is not changeable. !image-2021-01-22-17-13-09-405.png!
ARTD-6571	Bug	[GPT] Build fail when enable Gpt Timeout Dem Error<*> When I used the PIT_0_CH_RTI channel and turned on the GPT_E_TIMEOUT feature, the test encountered a build error. (uint16)DemConf_DemEventParameter_DemEventParameter_0}; "d:\cc_work\zebra\S32K3XX_4.4\output\S32K3XX_S32K344\gpt\Gpt_TS_301_cfg2\generate_tresos\src\Gpt_Cfg.c",72 Error[Pe020]: identifier "DemConf_DemEventParameter_DemEventParameter_0" is undefined Errors: 1 Warnings: none make: [Makefile:1041: Gpt_Cfg_c.o] Error 1

ID	Subtype	Headline and Description
ARTD-6578	New	New Feature [S32K3XX][PWM][FLEXIO] Implement PWM over FLEXIO ip ,,"EBT 3-7d xdm user interface generation templates vsmd check only check existing example to not have issues Resource files to be used on EBT and DS as well. 1d DS 3-5d component user interface generation templates and manifest updates/addition epd/epc compliance check only check existing example to not have issues Requirements definition in separate xls file 1d IPL static code create/update/review 5d Update plugin makefile IPW code update/review 1d Dev test create/update to contain FLEXIO channels 1d Review xls of requirements for DOORS upload 1d Design update for flexio requirements Sharing strategy and implementation into MCL Example code for IPL and HLD as a separate branch from the code branch 2d Very rough estimatation: 2.5w 4w"

ARTD-6588	Bug	[S32K3XX][PWM] Pwm_GetChannelState function can not work in IDLE state<*>
		
		In the IDLE state, the channel mode will be changed to the GPO mode.
		If call Pwm_GetChannelState function then and this function call Emios_Pwm_Ip_GetDutyCycle function, It cannot check the correct mode in use and go to DevAssert(FALSE);
		And if using recalculate duty based on period and duty of Emios.
		emiosChDuty = Emios_Pwm_Ip_GetDutyCycle(ipConfig->channelInstanceId, ((Emios_Pwm_Ip_ChannelConfigType)ipConfig->channelConfig)->channelId);
		/ Get the period of the chanel /
		emiosChPeriod = Emios_Pwm_Ip_GetPeriod(ipConfig->channelInstanceId, ((Emios_Pwm_Ip_ChannelConfigType)ipConfig->channelConfig)->channelId);
		/ Calculate new duty value in ticks /
		dutyCycle = (uint16)(0x8000U ((float)emiosChDuty / emiosChPeriod));
		it will cause the error. This is not correct for tick units

ARTD-6592	Bug	[GPT] The function Pit_Ip_ChainMode does not work correctly<*> !image-2021-01-25-13-29-22-065.png! The chainmode channel need to count from 1.
ARTD-6595	Bug	[SAI] DBGE not configurable<*> DBGE not configurable Check if other bits/functionalities are not added in configuration (except one for which ticket is already raised)

ID	Subtype	Headline and Description
ARTD-6599	New	New Feature [ETH]Fix HIS LEVEL ,,Some functions have nesting level > 4.
ARTD-6590	Bug	[GPT] Fix compiler warning S32K3XX<*> Fix compiler warning for S32K3xx

ID	Subtype	Headline and Description

ARTD-6600	Bug	[SAI] CPR_RTD_00011 ISR function did not fully check the initialization status<*>
		
		Detailed description (how to reproduce it):
		
		CPR_RTD_00011 ISR function did not check initialization status.
		ISR shall check whether its respective driver is initialized. If the driver is not initialized, the ISR shall only clear interrupt status flag and return immediately.ISR shall check whether its respective driver is initialized. If the driver is not initialized, the ISR shall only clear interrupt status flag and return immediately. ID: 11 Req ID: CPR_RTD_00011
		
		Currently, the ISR function only check callback field, there may be a case when the default initialization value is not NULL_PTR.
		
		Preconditions:
		[...]
		Observed behavior:
		Expected behavior:
		Proposed solution optional:
		Refer to LPI2C driver
		static Lpi2c_Ip_SlaveStateType g_lpi2cSlaveStatePtr[LPI2C_INSTANCE_COUNT] = \{
		
		NULL_PTR}
		
		;
		Lpi2c_Init()
		{
		
		g_lpi2cSlaveStatePtr[instance] = userConfigPtr->slaveState;
		}

ID	Subtype	Headline and Description
ARTD-6607	Bug	[ADC] The Adc_CtuSetListPointer() API does not keep value of other bits in BCTU.MCR Register<*> Detailed description (how to reproduce it): When use the Adc_CtuSetListPointer() function reconfigure position of the first channel of the command list, it affect some bit in register BCTU_TRGCFG Preconditions: Details review test case Adc_TC_FCT_0708 Observed behavior: When use the Adc_CtuSetListPointer() function reconfigure affect some bit in BCTU_TRGCFG register. In test case Adc_TC_FCT_0708, when calling the Adc_CtuSetListPointer() the bits TRGCFG_DATA_DEST, ADC_SEL0 are affected. Expected behavior: When using the Adc_CtuSetListPointer () function, reconfiguration does not affect some of the bits in the previously configured BCTU_TRGCFG register. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-6610	Bug	[platform] S32DS Compile error when installing NULL_PTR to interrupt handler.<*> There is error in compiling when config interrupt handler is NULL_PTR. !image-2021-01-15-15-13-26-929.png! !image-2021-01-15-15-14-22-419.png! The driver should add checking to not allow config NULL_PTR or NULL. However this limit ability to setting interrupt handler to NULL pointer.
ARTD-6604	Bug	[SAI] Wrong mapping data type between EBT and S32CT<*> Detailed description (how to reproduce it): There are some fields on S32CT that are not mapping the data type between EBT and S32CT [^SAI_NodeToM4.xlsx] Refer link: [https://nxp1.sharepoint.com/:p:/s/Zebra/EaMbpShSxPVAq7amkzZx3NMB1LWDlRvDlnrzP1m0TZ9elQ?e=TJtb0O] Slide 19 Preconditions: [...] Observed behavior: warnings in the Compiler Warnings report Expected behavior: No warnings in the Compiler Warnings report Proposed solution optional:
ARTD-6631	Bug	[GPT] Example EBT cannot generate due to MCU<*> Gpt EBT Example cannot generate due to Mcu error: !image-2021-01-26-09-37-18-619.png!

ID	Subtype	Headline and Description
ARTD-6675	Bug	PIT RTI support<*> The S32_CT cannot generate correct PIT configuration for PIT_RTI after enable PIT_RTI feature(PIT_IP_RTI_USED = STD_ON): typedef struct { uint8 hwChannel; /**< brief Timer channel number / Pit_Ip_UnitModeType periodUnit; /**< brief Period value unit / #if (defined (PIT_IP_RTI_USED) && (PIT_IP_RTI_USED == STD_ON)) errorReportCallBackType errorReportCallBack; /**< brief errorReportCallBack / #endif boolean enableInterrupt; /**< brief Enable interrupt generation / Pit_Ip_CallbackType callback; /**< brief callback / uint8 callbackParam; /**< brief callbackParam / } Pit_Ip_ChannelConfigType_; typedef struct { boolean chInit; /**< brief chInit / #if (defined (PIT_IP_RTI_USED) && (PIT_IP_RTI_USED == STD_ON)) errorReportCallBackType errorReportCallBack; /**< brief errorReportCallBack / #endif Pit_Ip_CallbackType callback; /**< brief callback / uint8 callbackParam; /**< brief callbackParam / } Pit_Ip_State; No configuration of *errorReportCallBack* for the above two structures.
ARTD-6678	New	New Feature [PORT] Update the name of Touch Sense function to follow the requirements ,,"There are 2 functions which need to be renamed in the driver to follow the requirements: From: Tspc_Port_Ip_Enable*OBE*Group Tspc_Port_Ip_Configure*OBE*Group To: Tspc_Port_Ip_Enable*Obe*Group Tspc_Port_Ip_Configure*Obe*Group"
ARTD-6682	Bug	[wdg] CR->STP allowed for configuration even if not supported on SWT_1<*> CR->STP not supported on SWT_1 Make readonly in configurators (EBT and CT) using a new resource variable
ARTD-6688	Bug	[S32K344] MCL: TC build fail with multi-variant on CT<*> TC build fail with multi-variant on CT !image-2021-01-26-15-43-59-696.png!

ID	Subtype	Headline and Description
ARTD-6690	New	New Feature [S32K344 BETA] OCU: Implement CPR_RTD_00522 restrictions and updates in CPR_RTD_00511 ,,"NewWorkDescription: Updates according to the updates in the requirement: *CPR_RTD_00511 CPR_RTD_00522*: Drivers capable of using Counter Buses shall not allow selection of an Counter Bus with exclusive access granted to PWM. The check will be performed at configuration time. Applicable only for Icu, Ocu, on eMIOS Requirement source: Customer Request CPR_RTD_00511 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Provide an API that will update (buffered change expected) the match/reload value for the counter selected."
ARTD-6698	Bug	[S32K3XX][PWM] Fix the compiler warning and failed building in DS examples<*> The DS example has compiler warning and failed building with Pwm_Example_Ds
ARTD-6695	Bug	[S32K344][LIN] When header transmit and have a error occurred, driver doesn't return LIN_TX_HEADER_ERROR. ,,"When header transmit and have a error occurred, IRQ function will return linCurrentState->currentEventId = LPUART_LIN_IP_READBACK_ERROR and in callback function will return Lin_Ipw_au8LinChFrameErrorStatus[u8Channel] = LIN_TX_ERROR_U8. When function Lin_GetStatus called funciton Lin_Ipw_ErrorGetStatus will check and return LIN_TX_HEADER_ERROR if *Lin_Ipw_au8LinChFrameErrorStatus[u8Channel] = LIN_TX_HEADER_ERROR_U8* but it equal *LIN_TX_ERROR_U8* then driver doesn't return LIN_TX_HEADER_ERROR
ARTD-6707	Bug	[SAI] State structures allocated for all instances even if not used<*> State structures allocated for all instances even if not used Update also EBT and S32CT

ID	Subtype	Headline and Description
ARTD-6710	Bug	[DIO] Fix MISRA violations<*> Detailed description (how to reproduce it): There are some misra violation which need to be fixed or comment. Please refer the attachment for more detail Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: There are some misra violation Expected behavior: There is no misra violation Proposed solution optional:
ARTD-6716	Bug	[ETH] Fix compiler warning for S32K3XX BETA 0.9.0 release<*> There are 2 warning when compile the driver code with GCC and IAR compiler. Please check the attached file.
ARTD-6725	Bug	[BASE] UM missing stub file information<*> The Base UM should include the information about the stub files, to be clear which file can be changed or not by an integrator, customer. For Reference, check the attached manual and screenshot. !image-2021-01-27-11-47-11-574.png!

ID	Subtype	Headline and Description

ARTD-6728	Bug	[ADC][EXAMPLE] Some example description should be updated<*>
		
		Detailed description (how to reproduce it):
		In EBT example description*, I think you should add the expected output like this:
		If the result is correct, the program will go through to the end of code without stuck in loop with bStatus variable is set as "True"
		In Adc_example_DS_IP description*, the expected output is :
		If all conditions are correct, the code goes to the end of program without stuck in loop
		In the main.c of Adc_example_DS_IP
		for(;;)
		{
		if(exit_code != 0)
		{
		break;
		}
		}
		When debug example, the program is stuck in this for loop, although that means example works normally but I think there is a conflict with description "the code goes to the end of program without stuck in loop"
		Preconditions:
		[...]
		Observed behavior:
		Some description are missing and not matching with code.
		Expected behavior:
		Right example description.
		Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)
		Proposed solution optional:

ARTD-6751	Bug	[CAN] Driver may call CanIf_TxConfirmation with wrong swhandler with TxProcessing is INTERRUPT<*> Driver may call CanIf_TxConfirmation with wrong swhandler with TxProcessing is INTERRUPT In Can_Write, PduInfo->swPduHandle should be saved before FlexCAN_Ip_Send is triggered, else in case of the transmission was complete sooner (before PduInfo->swPduHandle is saved), the unexpected value will be reported to CanIf_TxIndication. !image-2021-01-28-08-44-07-176.png! Expectation:
ARTD-7080	Bug	[STM]:config tools can't generate source code<*> Config tools "problems" found errors !image-2021-01-28-14-35-02-418.png! The file "Stm_Ip_BOARD_InitPeripherals_PBcfg.c" didn't generated any contents. !image-2021-01-28-14-35-09-563.png!

ID	Subtype	Headline and Description
ARTD-7083	Bug	[CRYPTO] Missing MU instance parameter in Hse_Ip_GetHseStatus function<*> Function "*Hse_Ip_GetHseStatus*" can't get status from other MU instance except "0U" Is "*Hse_Ip_GetHseStatus*" could have a parameter like "*_u8MuInstance_*" to get status of other MU instances? !image-2021-01-28-14-39-47-562.png!
ARTD-7084	Bug	[S32DS 3.4] Has an error "Path to collateral manifest does not exist ${eclipse_home}../S32DS/software/PlatformSDK_S32K3_2021_02/itm.s32k3.rtd.collateral.PlatformSDK_S32K3_2021_02.xml" after finishing the installation ,,"Detailed description (how to reproduce it): Step 1: Install package: S32DS: S32DS.3.4_b201217_win32.x86_64.exe Development package: SW32K3_S32DS_3.4.0_D2012.zip and com.nxp.s32ds.s32r45.update_3.4.1.20210115121654.zip Update site: S32K3XX_RTD_4_4_BETA_0_9_0_DS_updatesite_2101.zip Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: Has an error ""*Path to collateral manifest does not exist ${eclipse_home}../S32DS/software/PlatformSDK_S32K3_2021_02/itm.s32k3.rtd.collateral.PlatformSDK_S32K3_2021_02.xml*"" after finishing the installation Detail was attached. Expected behavior: After finishing the installation there was no warning or error
ARTD-7088	Bug	[PINS][S32CT] Cannot configure direction Input_Output for for PTD16 (EMAC_MDIO)<*> When I test example for ETH module (Eth_Example_DS_001 for IPL) on S32CT (([S32K3XX_RTD_4_4_BETA_0_9_0_DS_updatesite_2101.zip| http://transgateway.nxp.com/cgi-bin/trans/index.pl?path=/Transcend_Gateway/RTD/S32K3XX/4_4/BETA_0_9_0/S32K3XX_RTD_4_4_BETA_0_9_0_DS_updatesite_2101.zip] Wed Jan 27 19:22:31 2021), There is an issue for PTD16: it cannot be configured direction as Input_Output. Please check the attached screen-shot.

ID	Subtype	Headline and Description
ARTD-7097	Bug	[ADC] Build fail when not configuring anything in BctuHwUnit tab<*> Detailed description (how to reproduce it): Build fail when not configuring anything in BctuHwUnit tab Preconditions: AdcEnableCtuControlModeApi is enable Add BctuHwUnit_0 by default (click on add icon in tab BctuHwUnit) Test Case ID (internal TC that caught the defect) optional: Adc_TS_COT_011 cfg 45 Observed behavior: Generate step was passed but build step was failed Build fail log: STDERR:"e:/S32K3/output/S32K3XX_S32K344/adc/Adc_TS_COT_011_cfg45/generate_tresos/src/Bctu_lp_VS_0_PBcfg.c", line 157: error #1981-D: STDERR: empty initializer is non-standard STDERR: }; STDERR: STDERR: More detail in attachment report Expected behavior: Build done Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-7093	Bug	[BASE] Some compiler options are not the same between SOW and S32CT<*> Detailed description (how to reproduce it): Step 1: Create new project. Step 2: Select project > right click > Properties > C/C Build > Settings Step 3: Check compiler options and compare with SOW file Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: Some compiler options are not the same between SOW and S32CT : Compiler: Missing : fno-zero-initialized-in-bss Linker: Duplicate: mcpu=cortex-m7 In file SOW*: Map=<map_file_name> and -mfloat-abi=soft but CT is: Map and -mfloat-abi=softfp Expected behavior: Update compiler option for CT the same with compiler option in SOW file.

ID	Subtype	Headline and Description

ARTD-7099	Bug	[ADC] Adc_Ipw_StopCurrentConversion uses incorrect channel index resulting in hardfault<*>
		
		Adc_Ipw_StopCurrentConversion uses incorrect channel index resulting in hardfault (for example for ChIndex=18)
		#if (ADC_SETCHANNEL_API == STD_ON)
		ChIndexTemp = Adc_aRuntimeGroupChannel[Group].pChannel[ChTemp];
		#else
		ChIndexTemp = Adc_pCfgPtr[u32CoreId]->pGroups[GroupIndex].pAssignment[ChTemp];
		#endif
		(void)Adc_Sar_Ip_GetConvData(Unit, ChIndexTemp);
		Must be:
		(void) Adc_Sar_Ip_GetConvData(Unit, (uint32)Adc_pCfgPtr[u32CoreId]->pAdcIpwConfig->apAdcConfig[LogicalHwUnitId]->pChannelConfigs[ChIndexTemp].u8ChannelIndex);
		Like in Adc_Ipw_ClearValidBit. Consider using this function

ARTD-7123	Bug	[I2C][S32K3XX] Fix some function which has HIS violation<*> Some functions have HIS_LEVEL above 4.00 Refer to attached file to see detail and fix all of them

ID	Subtype	Headline and Description
ARTD-7192	Bug	[ADC] Build fail: "implicit declaration of function 'Adc_Ipw_IsChannelEnable and 'ChannelExist' undeclared" in Adc_Ipw.c ,,"Detailed description (how to reproduce it): Build fail: ""identifier ""ChannelExist"" is undefined"" Preconditions: Compiler gcc Using function Adc_Ipw_HwResultReadGroup (ADC_ENABLE_CTUTRIG_NONAUTO_API = ON) ADC_ENABLE_CH_DISABLE_CH_NONAUTO_API = ON ADC_READ_GROUP_API = OFF Test Case ID (internal TC that caught the defect) optional: Adc_TS_COT_011 cfg 05 Observed behavior: Generate step was passed but build step was failed Build fail log: STDERR:e:/S32K3/output/S32K3XX_S32K344_gcc/adc/../../eclipse/plugins/ Adc_TS_T40D34M9I0R0/src/Adc_Ipw.c: In function 'Adc_Ipw_HwResultReadGroup': STDERR:e:/S32K3/output/S32K3XX_S32K344_gcc/adc/../../eclipse/plugins/ Adc_TS_T40D34M9I0R0/src/Adc_Ipw.c:2147:29: error: implicit declaration of function 'Adc_Ipw_IsChannelEnable' [-Werror=implicit-function-declaration] STDERR: 2147 ChannelEnable = Adc_Ipw_IsChannelEnable(LogicalHwUnitId, GroupId, ChIndex, u32CoreId); STDERR: STDERR:e:/S32K3/output/S32K3XX_S32K344_gcc/adc/../../eclipse/plugins/ Adc_TS_T40D34M9I0R0/src/Adc_Ipw.c:2150:49: error: 'ChannelExist' undeclared (first use in this function); did you mean 'ChannelCount'? More detail in attachment report Expected behavior: Build done Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA

ID	Subtype	Headline and Description
ARTD-7193	Bug	[ADC] Tresos Build fail: "identifier "Dma_Ip_LogicChannelTransferListType" is undefined in Bctu_Ip.c with PreCompile enabled and Variant Size <= 1 ,,"Detailed description (how to reproduce it): Build fail: ""identifier ""Dma_Ip_LogicChannelTransferListType"" is undefined in Bctu_Ip.c Preconditions: CtuEnableDmaTrasferMode is enable Using VariantPreCompile Test Case ID (internal TC that caught the defect) optional: Adc_TS_COT_011 cfg 03 Observed behavior: Generate step was passed but build step was failed Build fail log: STDERR:""e:/S32K3/output/S32K3XX_S32K344_ghs/adc/../../eclipse/plugins/Adc_TS_T40D34M9I0R0/src/Bctu_Ip.c"", line 1318: error #20: STDERR: identifier ""Dma_Ip_LogicChannelTransferListType"" is undefined STDERR: Dma_Ip_LogicChannelTransferListType LocTransferList[12U]; More detail in attachment report Expected behavior: Build done Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-7213	Bug	[WDG] SWT_1 must not be accessed by customers on S32K344 and S32K314<*> [WDG] SWT_1 must not be accessed by customers on S32K344 and S32K314 According to RM rev2Draft A supported for 0.9.0 release !image-2021-01-29-13-06-37-271.png|thumbnail!
ARTD-7215	Bug	[ETH]Fix build failed<*> Used \\\ instead of cause failure.
ARTD-7218	New	New Feature [ADC] Add support for XSTRGEN external start feature ,,"Add support for XSTRTEN external start feature Integrate in IPL and HLD configurator. No new API is required. !screenshot-1.png|thumbnail! !screenshot-2.png|thumbnail! This must be used via TRGMUX"
ARTD-7219	Bug	[SAI] Wrong memory section<*> Wrong memory section for callback functions in Sai_Ip_PBcfg.h Functions should be in SAI_START_SEC_CODE / SAI_STOP_SEC_CODE.

ID	Subtype	Headline and Description
ARTD-7225	Bug	[ADC] Build fail: implicit declaration of function 'Adc_ValidateQueueNotFull' in Adc.c<*> Detailed description (how to reproduce it): Build fail: implicit declaration of function 'Adc_ValidateQueueNotFull' in Adc.c Preconditions: Compiler gcc ADC_ENABLE_START_STOP_GROUP_API = OFF ADC_HW_TRIGGER_API = ON Test Case ID (internal TC that caught the defect) optional: Adc_TS_COT_010 cfg 4 Observed behavior: Generate step was passed but build step was failed Build fail log: STDERR:e:/S32K3/output/S32K3XX_S32K344_gcc/adc/../../eclipse/plugins/ Adc_TS_T40D34M9I0R0/src/Adc.c: In function 'Adc_ValidateExtraParams': STDERR:e:/S32K3/output/S32K3XX_S32K344_gcc/adc/../../eclipse/plugins/ Adc_TS_T40D34M9I0R0/src/Adc.c:1244:9: error: implicit declaration of function 'Adc_ValidateQueueNotFull'; did you mean 'Adc_ValidateStateNotIdle'? [- Werror=implicit-function-declaration] STDERR: 1244 Adc_ValidateQueueNotFull(&ValidationStatus, u8ServiceId, Group, u32CoreId); STDERR: STDERR: Adc_ValidateStateNotIdle More detail in attachment report Expected behavior: Build done Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-7234	New	New Feature [S32K344 BETA] OCU: Implement CPR_RTD_00522 restrictions and updates in CPR_RTD_00511 on S32DS ,,"NewWorkDescription: Updates according to the updates in the requirement: *CPR_RTD_00511 CPR_RTD_00522*: Drivers capable of using Counter Buses shall not allow selection of an Counter Bus with exclusive access granted to PWM. The check will be performed at configuration time. Applicable only for Icu, Ocu, on eMIOS Requirement source: Customer Request CPR_RTD_00511 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Provide an API that will update (buffered change expected) the match/reload value for the counter selected."

ID	Subtype	Headline and Description
ARTD-7237	Bug	[SPI]Struct "<unnamed>" has no field "pCmdDmaFast" ,,"The errors occurred in the case of SpiEnableDmaFastTransferSupport = true and SpiGlobalDmaEnable = false: 1. Struct ""<unnamed>"" has no field ""pCmdDmaFast"", ""rxDmaChannel"", ""txDmaChannel"". 2. Lpspi_Ip.c Function ""Lpspi_Ip_TxDmaTcdSGConfig"" was referenced but not defined static void Lpspi_Ip_TxDmaTcdSGConfig(uint8 u8Instance, uint8 u8TCDSGIndex, uint8 u8DisHwReq);
ARTD-7240	Bug	[S32K3XX] port: Cannot use pin PTC6 for Wakeup Input mode in DS<*> Open Icu_example_DS_eMios_Siul_Wkpu project, Configure pin PTC6 to Wakeup Input mode, Update code. Observed: Pin PTC6 was not generated and IBE was not enable in register. Propose: Update PTC6 as default value when enter Wakeup Input mode according to RM.
ARTD-7311	New	New Feature [gpt] Create CERT-C report and fix violations ,,"Create CERT-C report Fix all violations if any are found Guideline following: [https://confluence.sw.nxp.com/pages/viewpage.action?pageId=133734230]"
ARTD-7318	New	New Feature [crypto] Create CERT-C report and fix violations ,,"Create CERT-C report Fix all violations if any are found Guideline following: [https://confluence.sw.nxp.com/pages/viewpage.action?pageId=133734230]"
ARTD-7276	Bug	[crypto][S32DS][S32G]Missing component description for Gmac, Hse,Suil2_Dio, Suil2_Port in select component window ,,"Test Case ID (internal TC that caught the defect) optional: 1. Create project enable RTD for S32G274_Rev2 2. Open Peripherals tool-> Click to add component Observed behavior: Missing Component description for some components in Select component window: Gmac, Hse,Suil2_Dio, Suil2_Port Expected behavior: There should have component description for these components: Gmac, Hse,Suil2_Dio, Suil2_Port

ID	Subtype	Headline and Description
ARTD-7282	Bug	[S32K3xx][MCL] Failure at building on S32CT<*> Failure at building on S32CT, because Emios_Mcl_Ip_BOARD_InitPeripherals_PBcfg.c file included Emios_Mcl_Ip_PBcfg.h file, compiler cannot find this file !image-2021-02-03-10-50-27-006.png|thumbnail!
ARTD-7287	Bug	[S32K3XX][SENT][EXAMPLE] S32CT example not be display in S32DS project from Example box<*> Issue*: Can not find Sent example when create new project from example om S32DS Solution*: for each example, It needs to register to Base module, in this file: https://bitbucket.sw.nxp.com/projects/ARTD/repos/base/browse/specific/S32K3XX/integration/swm.rtd.s32k3.release_id.xml
ARTD-7284	Bug	[GPT][S32K3XX] Stm_Ip_u32InstanceState is undefined when set clock mode = OFF<*> I got build fail with STM as in attachment files, please help me check
ARTD-7332	Bug	[MCL] Store Destination Address overwrites Source Signed Last Address Adjustment<*> 1. At initialization, Store Destination Address overwrites the Source Signed Last Address Adjustment. 2. Update C termination "At the end of the CDD_MCL header file the ifdef cplusplus is missing and always needs to be added manually."

ID	Subtype	Headline and Description
ARTD-7595	Bug	[SAI] Code generation error "config class PostBuild which is not allowed in this context" ,,"Detailed description (how to reproduce it): Error when generating project with SAI project: INFO 21-02-04,10:32:41 (11136) Project ""TestProject"" was created with different version of the tool. Migrating project. ERROR 21-02-04,10:32:47 (1803) Code generation (mode: ""generate"") Invalid XPath-expression for Attribute ""INVALID"" of node ""/AUTOSAR/TOP-LEVEL-PACKAGES/Sai/ELEMENTS/Sai/SaiConfiguration"": (1822) Attempt to read value of node /AUTOSAR/TOP-LEVEL-PACKAGES/Sai/ELEMENTS/Sai/SaiConfiguration/SaiConfiguration_0/SaiTxRxConfiguration with config class PostBuild which is not allowed in this context ERROR 21-02-04,10:32:47 (13028) Code generation (mode: ""generate"") Project ""TestProject"" has errors, see Problems View ERROR 21-02-04,10:32:47 (1803) Code generation (mode: ""generate"") Invalid XPath-expression for Attribute ""INVALID"" of node ""/AUTOSAR/TOP-LEVEL-PACKAGES/Sai/ELEMENTS/Sai/SaiConfiguration"": (1822) Attempt to read value of node /AUTOSAR/TOP-LEVEL-PACKAGES/Sai/ELEMENTS/Sai/SaiConfiguration/SaiConfiguration_0/SaiTxRxConfiguration with config class PostBuild which is not allowed in this context ERROR 21-02-04,10:32:47 (13028) Code generation (mode: ""generate"") Project ""TestProject"" has errors, see Problems View Unattended wizard ""Execute multiple tasks(GenerateAllVariants) (GenerateAllVariants)"" exited with errors. WARNING 21-02-04,10:32:41 (1648) Created required node ""/AUTOSAR/TOP-LEVEL-PACKAGES/Sai/ELEMENTS/Sai/GeneralConfiguration/SaiEnableUserModeSupport"" in container ""/Sai/Sai/GeneralConfiguration""Errors ""4"" Warnings ""1"" Makefile:658: recipe for target `/cygdrive/d/zebra/repo_s32k3/output/S32K3XX_S32K344/sai/Sai_TS_WIR_001_cfgCORE0/generate_tresos/generate_timestamp' failed make: [/cygdrive/d/zebra/repo_s32k3/output/S32K3XX_S32K344/sai/Sai_TS_WIR_001_cfgCORE0/generate_tresos/generate_timestamp] Error 1 !image-2021-02-04-11-09-19-670.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: Observed behavior: Generate project failed Expected behavior: Generate project successfully Proposed solution optional: Refer the fix from ARTD-6494
ARTD-7598	Bug	[GPT] Code generation error "config class PostBuild which is not allowed in this context" ,,"Invalid XPath-expression for Attribute ""INVALID"" of node ""ASPath:/Gpt/Gpt/GptChannelConfigSet/GptChannelConfiguration_0/GptWakeupConfiguration"": (1822) Attempt to read value of node /AUTOSAR/TOP-LEVEL-PACKAGES/Gpt/ELEMENTS/Gpt/GptChannelConfigSet/GptChannelConfiguration/GptChannelConfiguration_0/GptEnableWakeup with config class PostBuild which is not allowed in this context

ID	Subtype	Headline and Description
ARTD-7606	Bug	[platform]The platform driver build faild when system interrupt not initialized<*> The platform driver build faild when system interrupt not initialized !image-2021-02-04-18-19-53-026.png!
ARTD-7607	Bug	[ETH]Fix generate failed when Config Time enabled<*> When config time enabled, some nodes are precompile but refer to post build node will generate failed.
ARTD-7612	New	New Feature [CRYPTO]Update code to follow HSE_IP_014_001 requirement ,,"HSE_IP_014_001 states the following: ""The type Hse_Ip_StatusType shall be an enumeration that describes the status of the execution of the Hse Ip driver's APIs"". The IP implementation is done using _status_hse_ip_t structure instead of _Hse_Ip_StatusType_. Additionally the enum values can be updated: `STATUS_HSE_IP_SUCCESS` to `HSE_IP_STATUS_SUCCESS` `STATUS_HSE_IP_ERROR` to `HSE_IP_STATUS_ERROR`"
ARTD-7613	New	New Feature [ADC] Add configurable resolution ,,"Add configurable resolution: CALBISTREG->RESN Add in IPL and HLD configurators at group level Mask accordingly the read result operations Validate feature by checking if converted value for bandgap is correct for all supported resolutions (not required to add dev test) Add requirement for new IPL function"

ID	Subtype	Headline and Description
ARTD-7631	Bug	[ADC] Multicore should not be supported on S32K344 and S32K314 derivative<*> Detailed description (how to reproduce it): As new information (click the links for more information) [Single core on S32K344|https://teams.microsoft.com/l/message/19:0bd08d52409848849e868ba689b329c0@thread.tacv2/1612435813929?tenantId=686ea1d3-bc2b-4c6f-a92c-d99c5c301635&groupId=f9decd68-7b74-4101-a4d2-ad54e86f727f&parentMessageId=1612435813929&teamName=Zebra&channelName=00.%20S32K3XX_BETA_0.9.0%20(S32K3)&createdTime=1612435813929] Multicore on S32K314 and S32K344 derivative should be not supported, so driver should update follow this. Multicore is only available on S32K324 derivative Preconditions: Resource configured as S32K314 or S32K344 derivative Observed behavior: Multicore is enable for all derivative Expected behavior: Multicore should be not supported on S32K314 and S32K344, only available on S32K324 Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-7633	Bug	[BASE][OSIF] Multicore should be disabled on S32K344 derivative<*> Detailed description (how to reproduce it): As new information [Single core on S32K344|https://teams.microsoft.com/l/message/19:0bd08d52409848849e868ba689b329c0@thread.tacv2/1612435813929?tenantId=686ea1d3-bc2b-4c6f-a92c-d99c5c301635&groupId=f9decd68-7b74-4101-a4d2-ad54e86f727f&parentMessageId=1612435813929&teamName=Zebra&channelName=00.%20S32K3XX_BETA_0.9.0%20(S32K3)&createdTime=1612435813929] Multicore on S32K344 derivative is disabled, so driver should update follow this. Multicore is only available on S32K324 derivative Preconditions: [...] Observed behavior: Multicore is enable for all derivative Expected behavior: Multicore is disabled on S32K344, only available on S32K324 Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)
ARTD-7622	Bug	[S32K3XX][S32XX][GPT] Missing UM/IM path in the <Mdl>.mak file<*> Missing user manuals doc path in the <Module>.mak file SRC_FILES = $(MODULE_PATH)/specific/$(S32K3XX_NAME)/doc/user_manuals/RTD_GPT_IM.pdf@outdir=doc,bin=y \ $(MODULE_PATH)/specific/$(S32K3XX_NAME)/doc/user_manuals/RTD_GPT_UM.pdf@outdir=doc,bin=y

ID	Subtype	Headline and Description
ARTD-7626	Bug	[S32K3xx][MCL] Generate file is missing some variables<*> I see that generate file form S32CT is missing some variables(Pls see as below) !image-2021-02-05-12-40-26-548.png|thumbnail! Redundant config variant in configTimeSupport. I think it is not necessary at IP layer !screenshot-1.png|thumbnail!
ARTD-7647	Bug	[platform][S32DS]The platform driver build faild when system interrupt not initialized<*> The platform driver build faild when system interrupt not initialized !image-2021-02-04-18-19-53-026.png!
ARTD-7671	New	New Feature [GPT] S32K344 is selected on Tresos/CT, the multicore feature should be disabled" ,,"Please see the topic below : [Vlad Lionte: K344 single core |https://teams.microsoft.com/l/ message/19:0bd08d52409848849e868ba689b329c0@thread.tacv2/1612435813929? tenantId=686ea1d3-bc2b-4c6f-a92c-d99c5c301635&groupId=f9decd68-7b74-4101- a4d2- ad54e86f727f&parentMessageId=1612435813929&teamName=Zebra&channelName=00. %20S32K3XX_BETA_0.9.0%20(S32K3)&createdTime=1612435813929] posted in Zebra / 00. S32K3XX_BETA_0.9.0 (S32K3) at Feb 4, 2021 5:50 PM In the conclusion, when the chip K344 is selected on Tresos/CT, the multicore feature should be disabled in these tools For multicore testing, we should use the support for K324, tested on a K344 with lockstep disabled. P/s: Please check carefully if the multicore nodes were disabled but the value are still true. In this case, seems that the multicore can be run anyway.
ARTD-7675	Bug	[S32K3XX][CRYPTO] Missing array store value actual length of the key element has ID is 1 on array Crypto_au8VolatileKeyElemValues<*> Detailed description* (how to reproduce it): Problem when generate config file with S32DS,when config a Kelement have Id is 1 and referent it to RamKeyCatalog, but when generate array Crypto_au8VolatileKeyElemValues on file Crypto_Cfg.c don't have value of actual length of the key element has ID is 1. Observed behavior*: Missing array store value actual length of the key element has ID is 1 on array Crypto_au8VolatileKeyElemValues Expected behavior: if(KeyElement.getChildById("UseHseKey").getValue() == true && KeyElement.getChildById("HseKeyCatalogGroupRef").*getValue()*.contains*("/ RamKeyCatalog/*")) should be change : " else if(KeyElement.getChildById("UseHseKey").getValue() == true && deref*(KeyElement.getChildById("HseKeyCatalogGroupRef")).*getId()*.contains("*RamKeyCatalog*")

ID	Subtype	Headline and Description
ARTD-7678	New	New Feature [ADC] Hw Triggered Mode DMA with streaming, without interrupts and group streaming results reorder" ,,"DMA without interrupts, with streaming and with group streaming results reorder: after each group conversion is finished transfer results using SG in an internal buffer use counting DMA channel to copy from this internal buffer into buffer setup via Adc_SetupResultBuffer counting DMA channel must be configurable in ct and hld when ADC is configured for DMA, without interrupt and streaming Group streaming results reorder is required to allow using a single DMA channel without SG for transfering results into the result buffer. Otherwise, a single DMA without SG cannot move result from internal buffer into a circular result buffer arranged as per Autosar requirement: internal buffer Ch0,Ch1,Ch2 > result buffer Ch0,Ch0,Ch0;Ch1,Ch1,Ch1;Ch2,Ch2,Ch2 (because cannot be solved with DMA modulo feature, or minor loop destination/source offset would be required to support different values for destination and source) But this can be achieved: Ch0,Ch1,Ch2 > result buffer Ch0,Ch1,Ch2;Ch0,Ch1,Ch2;Ch0,Ch1,Ch2 Other updates: same implementation to be used also for double buffering optimization
ARTD-7684	Bug	[Wdg] cmm filename is wrong in example readme.txt<*> cmm filename is wrong in example readme.txt Please correct it, also check for other wrong information in example readme
ARTD-7695	New	New Feature [SPI][FLEXIO] Add support for FLEXIO common ,,"Add Mcl common code and configurator for FLEXIO IP to be used by drivers: PWM, I2C, LIN, UART, SENT, SPI See links of ticket for start-up."
ARTD-7706	New	New Feature [S32K3XX][PWM][FLEXIO] PWM over FLEXIO: EBT support ,,"EBT 3-7d xdm user interface generation templates vsmd check only check existing example to not have issues Resource files to be used on EBT and DS as well. 1d "

ID	Subtype	Headline and Description
ARTD-7707	Bug	[ARTD] _end symbol not properly defined for heap memory section<*> The heap section is not properly defined in linker file (linker_ram.ld) and the allocation of dynamic memory will fail. The '_end' symbol need to be inside the heap section. Steps: # create a Design Studio 3.4 project # Allocate memory using malloc (void p = (void)malloc(79);) immediately after the beginning of main() # Observe that it will jump into Hard_Fault (screenshots attached) Possible fix solution (I attached my new linker file): move the '_end symbol inside the heap section
ARTD-7708	New	New Feature [S32K3XX][PWM][FLEXIO] PWM over FLEXIO: DS configuration ,,"DS 3-5d component user interface generation templates and manifest updates/addition epd/epc compliance check only check existing example to not have issues Resource files to be used on EBT and DS as well. 1d"
ARTD-7709	New	New Feature [S32K3XX][PWM][FLEXIO] PWM over FLEXIO: Static code create/add ,,"Requirements definition in separate xls file 1d IPL static code create/update/review 5d Update plugin makefile IPW code update/review 1d Dev test create/update to contain FLEXIO channels 1d Review xls of requirements for DOORS upload 1d Design update for flexio requirements Sharing strategy and implementation into MCL "
ARTD-7714	Bug	[S32K3] Lin and Uart can't be used in the same application<*> It both Lpuart_Uart and Lpuart_Lin components are used in an application, the build will fail due to redeclarations of enums. Starting from the Lpuart_Lin_Example, which uses LPUART_IP_0 as the Lin Hardware Channel, we also added a Lpuart_Uart component. This component configures LPUART_1 as the UartHwChannel, therefore a different instance of the peripheral. The build of the application fails as some enumerators are declared both in the Lpuart_Uart_Ip_HwAccess and inside the Lpuart_Lin_Ip_Hw_Access header files. A screenshot of the S32 Design Studio build console is attached.
ARTD-7722	New	New Feature [S32K3XX][PWM][EMIOS] Add Exclusive Areas for Emios IPL ,,Exclusive Areas must be added in the Emios IPL.

ID	Subtype	Headline and Description
ARTD-7737	Bug	[ICU] Code generation error "config class PostBuild which is not allowed in this context" ,,"Detailed description (how to reproduce it): For GPT I received this ticket I think you should check in your driver too. GPT's issue: GPT has consistent error when using Post Build Variants (even with generic XDM). GPT module complains that PostBuild is not allowed in this context, but there is no post build configuration set up here. I have verified that there is no post build variants in the GPT.xdm file. Error message: Invalid XPath-expression for Attribute ""INVALID"" of node ""/AUTOSAR/TOP-LEVEL-PACKAGES/Gpt/ELEMENTS/Gpt/GptChannelConfigSet/GptPit/GptPit_Ecu_Sync_Timer_Device/GptPitChannels"": (1822) Attempt to read value of node /AUTOSAR/TOP-LEVEL-PACKAGES/Gpt/ELEMENTS/Gpt/GptChannelConfigSet/GptPit/GptPit_Ecu_Sync_Timer_Device/GptPitChannels/GptPitChannel_0/GptPitChannel with config class PostBuild which is not allowed in this context It seems the error is reported because the configuration parameter of config class precompile is referencing in INVALID tag a parameter which is postbuild. As a workaround the checkbox ""Enable Config Time support"" in properties of Tresos project can be disabled. !image-2021-01-20-10-21-42-289.png|width=564,height=385! Preconditions: Checkbox "Enable Config Time support" is enabled in properties of Tresos project. Observed behavior: Code generation error. Expected behavior: No code generation error. Proposed solution*: Modify the configuration class of configuration parameter in xdm file so that both parameters are of the same configuration class.
ARTD-7754	Bug	[S32K3][SENT] Flexio channel needs to be assigned follow by HW channel from configuration<*> Issue: Currently, Flexio channels were allocated automatically in SENT module. Driver will allocate Flexio channel to which one is free. > This implementation is incorrect. It needs to follow HW channel from configuration.
ARTD-7757	Bug	[S32K344][LIN] Driver can't receive data to buffer in case receive response<*> Driver can't receive data to buffer in case receive response. I predicted DATA register might be read 2 time continuous makes value in data buffer receive equal = 0. First time read in function Lpuart_Lin_Ip_FrameIrqHandler line 1928 make value in DATA register return 0 then second time in function Lpuart_Lin_Ip_GetBytetoBuffer called by function Lpuart_Lin_Ip_ProcessReceiveFrameData.

ID	Subtype	Headline and Description
ARTD-7758	Bug	[S32K344][LIN] Driver need check case fail when config node Multicore support = ON and resource different S32K324<*> Driver need check case fail when config node Multicore support = ON and resource different S32K324. Check topic: [Vlad Lionte: K344 single core |https://teams.microsoft.com/l/message/19:0bd08d52409848849e868ba689b329c0@thread.tacv2/1612435813929?tenantId=686ea1d3-bc2b-4c6f-a92c-d99c5c301635&groupId=f9decd68-7b74-4101-a4d2-ad54e86f727f&parentMessageId=1612435813929&teamName=Zebra&channelName=00.%20S32K3XX_BETA_0.9.0%20(S32K3)&createdTime=1612435813929] posted in Zebra / 00. S32K3XX_BETA_0.9.0 (S32K3) at Feb 4, 2021 5:50 PM
ARTD-7761	New	New Feature [ICU] [S32XX]][S32CT] Implement EPD/EPC support for HLD and IPLD ,,"<this is a follow up for solving build errors and re-check the epd epc script on CC platform> Implement EPD/EPC support for HLD and IPLD. Please refer to [this post on Teams https://teams.microsoft.com/l/message/19:e451c595d3ba410c8f9c1f5efc19a8a3@thread.tacv2/1606904026692?tenantId=686ea1d3-bc2b-4c6f-a92c-d99c5c301635&groupId=f9decd68-7b74-4101-a4d2-ad54e86f727f&parentMessageId=1606904026692&teamName=Zebra&channelName=Configuration%20(code%2C%20DS%2C%20EB%2C%20etc)&createdTime=1606904026692] for additional details. From the presentation, the main focus should be on the following sections: Mapping XDM to Component EPD Importer EPD Generation EPC Importer EPC Generation"
ARTD-7783	Bug	[S32K3][SENT] Multicore supports on S32K324 only<*> Since S32K3 has derivative S32K324 support multicore, S32K314 and S32K344 do not have multicore. Therefore, driver need to update in order to enable multicore support on S32K324 only, other ones need to disable. (S32K344 and S32K314)

ID	Subtype	Headline and Description
ARTD-7777	Bug	[ICU] Multicore should be disabled on S32K344 derivative<*> Detailed description (how to reproduce it): As new information (click the links for more information) [Single core on S32K344|https://teams.microsoft.com/l/message/19:0bd08d52409848849e868ba689b329c0@thread.tacv2/1612435813929?tenantId=686ea1d3-bc2b-4c6f-a92c-d99c5c301635&groupId=f9decd68-7b74-4101-a4d2-ad54e86f727f&parentMessageId=1612435813929&teamName=Zebra&channelName=00.%20S32K3XX_BETA_0.9.0%20(S32K3)&createdTime=1612435813929] [Multicore is disabled on S32K344|https://teams.microsoft.com/l/message/19:b5f29bf74fdc497491f31257ffdf916c@thread.tacv2/1612491947574?tenantId=686ea1d3-bc2b-4c6f-a92c-d99c5c301635&groupId=0c20671d-eae6-4fd5-8fd2-7cc683861979&parentMessageId=1605838003935&teamName=FPT%20Zebra%20Team&channelName=General&createdTime=1612491947574] Multicore on S32K344 derivative is disabled, so driver should update follow this. Multicore is only available on S32K324 derivative Preconditions: NA Observed behavior: Multicore is enable for all derivative Expected behavior: Multicore is disabled on S32K344, only available on S32K324 Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:
ARTD-7778	Bug	[PWM] Multicore should be disabled on S32K344 derivative<*> Detailed description (how to reproduce it): As new information (click the links for more information) [Single core on S32K344|https://teams.microsoft.com/l/message/19:0bd08d52409848849e868ba689b329c0@thread.tacv2/1612435813929?tenantId=686ea1d3-bc2b-4c6f-a92c-d99c5c301635&groupId=f9decd68-7b74-4101-a4d2-ad54e86f727f&parentMessageId=1612435813929&teamName=Zebra&channelName=00.%20S32K3XX_BETA_0.9.0%20(S32K3)&createdTime=1612435813929] [Multicore is disabled on S32K344|https://teams.microsoft.com/l/message/19:b5f29bf74fdc497491f31257ffdf916c@thread.tacv2/1612491947574?tenantId=686ea1d3-bc2b-4c6f-a92c-d99c5c301635&groupId=0c20671d-eae6-4fd5-8fd2-7cc683861979&parentMessageId=1605838003935&teamName=FPT%20Zebra%20Team&channelName=General&createdTime=1612491947574] Multicore on S32K344 derivative is disabled, so driver should update follow this. Multicore is only available on S32K324 derivative Preconditions: NA Observed behavior: Multicore is enable for all derivative Expected behavior: Multicore is disabled on S32K344, only available on S32K324 Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:

ID	Subtype	Headline and Description
ARTD-7779	Bug	[OCU] Multicore should be disabled on S32K344 derivative<*> Detailed description (how to reproduce it): As new information (click the links for more information) [Single core on S32K344|https://teams.microsoft.com/l/message/19:0bd08d52409848849e868ba689b329c0@thread.tacv2/1612435813929?tenantId=686ea1d3-bc2b-4c6f-a92c-d99c5c301635&groupId=f9decd68-7b74-4101-a4d2-ad54e86f727f&parentMessageId=1612435813929&teamName=Zebra&channelName=00.%20S32K3XX_BETA_0.9.0%20(S32K3)&createdTime=1612435813929] [Multicore is disabled on S32K344|https://teams.microsoft.com/l/message/19:b5f29bf74fdc497491f31257ffdf916c@thread.tacv2/1612491947574?tenantId=686ea1d3-bc2b-4c6f-a92c-d99c5c301635&groupId=0c20671d-eae6-4fd5-8fd2-7cc683861979&parentMessageId=1605838003935&teamName=FPT%20Zebra%20Team&channelName=General&createdTime=1612491947574] Multicore on S32K344 derivative is disabled, so driver should update follow this. Multicore is only available on S32K324 derivative Preconditions: NA Observed behavior: Multicore is enable for all derivative Expected behavior: Multicore is disabled on S32K344, only available on S32K324 Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:
ARTD-7780	Bug	[GPT] Multicore should be disabled on S32K344 and S32K314 derivative<*> Detailed description (how to reproduce it): As new information (click the links for more information) [Single core on S32K344|https://teams.microsoft.com/l/message/19:0bd08d52409848849e868ba689b329c0@thread.tacv2/1612435813929?tenantId=686ea1d3-bc2b-4c6f-a92c-d99c5c301635&groupId=f9decd68-7b74-4101-a4d2-ad54e86f727f&parentMessageId=1612435813929&teamName=Zebra&channelName=00.%20S32K3XX_BETA_0.9.0%20(S32K3)&createdTime=1612435813929] Multicore on S32K344 derivative is disabled, so driver should update follow this. Multicore is only available on S32K324 derivative Preconditions: NA Observed behavior: Multicore is enable for all derivative Expected behavior: Multicore is disabled on S32K344, only available on S32K324 Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:
ARTD-7792	Bug	[S32K3][SENT] Remove instance parameter from polling functions<*> The parameter 'instance' needs to be remove from the following HLD functions, since these functions will poll all the channels available: Std_ReturnType Sent_GetFastMsgData(uint8 instance) Std_ReturnType Sent_GetSerialMsgData(uint8 instance)

ID	Subtype	Headline and Description
ARTD-7795	Bug	[S32K3xx][EMIOS] Some functions in high layer should check coreID<*> Mcl_Emios_SetReloadInterval and Mcl_SetEmiosCounterBusPeriod functions should check for coreID before writing to register, because EB tresos is configuring that each instance will refer to Ecuc partition Ref. If condition is not met then the function will raise a DET error. !image-2021-02-18-17-27-35-072.png|thumbnail! Similar to IRQ in Emios_Mcl_Ip_Irq file
ARTD-7794	Bug	[platform][S32DS]The platform driver build faild when system interrupt not initialized<*> The platform driver build faild when system interrupt not initialized !image-2021-02-04-18-19-53-026.png!
ARTD-7807	Bug	[S32K3XX] Icu: Number of instance is not correct<*> Step to reproduce: 1: Create a project on S32DS 2: Add cmp module at IP level 3: Edit the field of IcuLpCmp > ICU CMP IP instance number => add value 3 but have no error here, Meanwhile max of instance of S32K344 is 2(0, 1, 2)
ARTD-7811	Bug	[ICU] WKPU_IP_64_CH_USED does not define for S32K3XX<*> S32K3XX have 64 channels for WKPU but WKPU_IP_64_CH_USED does not define for S32K3XX
ARTD-7812	Bug	[S32K3] Lin and Uart can't be used in the same application<*> It both Lpuart_Uart and Lpuart_Lin components are used in an application, the build will fail due to redeclarations of enums. Starting from the Lpuart_Lin_Example, which uses LPUART_IP_0 as the Lin Hardware Channel, we also added a Lpuart_Uart component. This component configures LPUART_1 as the UartHwChannel, therefore a different instance of the peripheral. The build of the application fails as some enumerators are declared both in the Lpuart_Uart_Ip_HwAccess and inside the Lpuart_Lin_Ip_Hw_Access header files. A screenshot of the S32 Design Studio build console is attached.
ARTD-7818	Bug	[S32K3][ICU] The EMIOS_ICU component in RTD0.8.1 cannot work correctly.<*> The configuration variables generated by CT are totally different from their definitions in Emios_Icu_Ip_Types.h_, including spelling mistakes. Besides, there are AutoSar version error, vendor error and Software version error in Emios_Icu_Ip.h_ and the _Icu_Types.h is missing. For more information see attachments.
ARTD-7856	Bug	[WDG] Plugin contains xdm file duplicated in EBT folder<*> Plugin contains xdm file duplicated in EBT folder Check also for other differences in plugin ouput folders/files vs another driver (e.g. eth)

ID	Subtype	Headline and Description
ARTD-7858	Bug	[SAI] Det_ReportRuntimeError is guarded by SAI_DEV_ERROR_DETECT<*> Det_ReportRuntimeError in Sai_SyncTransmit is guarded by #if(SAI_DEV_ERROR_DETECT == STD_ON) Also Sai_ValidateCore (added for 0.9.0 release) is used only when (SAI_DEV_ERROR_DETECT == STD_ON), so function definition must also be guarded
ARTD-7869	Bug	[ETH][S32T] The multicore should not be supported for IPL<*> The multicore should not be supported at IPL on S32CT when only the IPL was used for the project.
ARTD-7871	New	New Feature [LIN][LPUART] - Add a check in configuration for the Hw instance ,,Add a check in EBT and CT for LIN and UART components over LPUART which will signal a duplicated hw instance usage.
ARTD-7874	Bug	[SAI] Driver always busy in receiver mode when setting both transmitter and receiver<*> Detailed description (how to reproduce it): Driver always busy in receiver mode when setting both transmitter and receiver in EB SAI configuration, create 2 configuration, one for transmitter and one for receiver, both of them is master, interrupt, async mode. Init driver and start receiving data Call Sai_AsyncTransmit with receiver request wait until the driver status is completed => driver status is always busy Preconditions: [...] Observed behavior: Can not receive data successfully Expected behavior: Receive data successfully Proposed solution optional:
ARTD-7877	Bug	Missing define in generated file triggers compilation error<*> GPT_START_SEC_CONST_UNSPECIFIED is not defined in generated file Gpt_BOARD_InitPeripherals_PBcfg.c RTD version used: PlatformSDK_S32K3_2021_03 !image-2021-02-22-17-57-33-704.png|thumbnail!

ID	Subtype	Headline and Description
ARTD-7882	Bug	[ETH][S32CT] The multicore should be supported for ETH HLD on S32K324<*> On S32CT, the ETH module (HLD) should support Multicore feature on S32K324. Steps to reproduce: # Create a S32DS application project with S32K324 # Add Eth module (HLD) # Enable Multicore support for ETH module Observed behavior: When EthMulticoreSupport check box is selected, the Problems view shows: "This derivative doesn't support multicore" Expected behavior: There is not any error when EthMulticoreSupport check box is selected.
ARTD-7887	Bug	[S32K3XX][MCL] Cannot initialize EMIOS with Ecuc Partition ref is core 1<*> Sequence of test case: Initialize EMIOS module (core 0 with EMIOS instance 0 and core 1 with EMIOS instance 1) on core 0 Delay a period of time for the IRQ to occur Get ISR trigger Multicore of MCL module is type 3(Initialization is performed on a single, designated core), but I see that in driver code, condition at line 96(if (configCore == CoreId) of Emios_Mcl_Ip.c file cannot be satisfied.
ARTD-7888	Bug	[ETH][K3XX] Error when config Shaper<*> There is an error when configure Eth Shaper. Please check the attached screen-shot.
ARTD-7894	Bug	[ADC] Function Adc_Sar_Ip_SetExternalTrigger calling in Adc_Ipw_EnableCtuTrigger is redundant<*> Detailed description (how to reproduce it): Function Adc_Sar_Ip_SetExternalTrigger calling in Adc_Ipw_EnableCtuTrigger is redundant Preconditions: AdcEnableCtuTrigAutosarExtApi is enable Test Case ID (internal TC that caught the defect) optional: Adc_TC_FCT_0120 Observed behavior: Trigger sources passing to Adc_EnableCtuTrigger are always different from EXT_TRIG so Adc_Sar_Ip_SetExternalTrigger calling in Adc_Ipw_EnableCtuTrigger is redundant More detail in attachment report Expected behavior: No need to call this function Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA

ID	Subtype	Headline and Description
ARTD-7917	Bug	[S32K3XX][Dio][S32CT] The Multicore did not raise any error when the chip K314, K344 is selected ,,"Detailed description (how to reproduce it): 1. Creating project for S32DS (derivative S32K344 or S32K314) 2. Open Peripheral 3. Import .mex file with <setting name=""DioMulticoreSupport"" value=""true""/> (attach Dio_multicore_support.mex for S32K344) 4. Update code Test Case ID (internal TC that caught the defect):* NA Observed behavior:*_ generate code successfully, no Error Expected behavior: error occurred in ""Problem"" box or generate fail because multicore enable
ARTD-7953	Bug	[ADC] CT ADC_SAR_IP missing the generated struct for ADC_SAR_1<*> Detailed description (how to reproduce it): In CT, create the configuration for ADC0 and ADC1 then generate code => Missing the struct configuration for Adc_sar_1 !image-2021-02-26-15-37-57-027.png! Test Case ID (internal TC that caught the defect) optional: Adc_sar_TC_FCT_0001 Observed behavior: Missing the struct configuration for Adc_sar_1 Expected behavior: Can generate the struct configuration for Adc_sar_1 Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-7957	New	New Feature [SPI][FLEXIO] Update CT for FLEXIO following new approach ,,Update CT for FLEXIO following new approach
ARTD-7968	New	New Feature [RTD][LIN] Mark some requirements as External requirement ,,"NewWorkDescription: There is a standard requirements of LIN which need to be marked as External requirements because it was done by BASE module. !image-2021-02-26-20-34-40-367.png! Requirement source: ASR SWS (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]"

ID	Subtype	Headline and Description
ARTD-7971	New	New Feature [S32K3XX][PWM] Integrate FLEXIO IPL in PWM ASR Driver ,,"IPW code update/review 1d Dev test create/update to contain FLEXIO channels 1d Sharing strategy and implementation into MCL Update IPL Flexio to use MCL driver."
ARTD-7994	Bug	[CRYPTO] Function Crypto_Hse_Init always return E_OK<*> Detailed description (how to reproduce it): Function Crypto_Hse_Init always return E_OK.It ,must return E_NOT_OK when Hse_Ip_Init() != HSE_IP_STATUS_SUCCESS Observed behavior: Missing return E_NOT_OK when Hse_Ip_Init() != HSE_IP_STATUS_SUCCESS Expected behavior: Add return E_NOT_OK when Hse_Ip_Init() != HSE_IP_STATUS_SUCCESS
ARTD-8034	Bug	[S32K344] [PORT] Issue in INMUX when implement Virtual Wrapper feature<*> Detailed description (how to reproduce it): when delare Port_Init, the pin with config INPUT mode, turn on Virtual Wrapper, core 1 (PDAC1), the hard fault occur in step Write to Input Multiplexed Signal Configuration Register (IMCR) Test Case ID (internal TC that caught the defect): Port_TC_FCT_2001 Observed behavior:* !image-2021-03-02-18-02-23-244.png|width=1185,height=226!! image-2021-03-02-18-04-39-923.png! Expected behavior:* resolve hard fault in Port_Init
ARTD-8065	Bug	[Platform][S32K3xx_090] Platform_SystemIrqConfigType struct missing when config two McmConfig on S32CT<*> Detailed description (how to reproduce it): # Create new project with resource s32k324 # Enable multi core # Enable system setting with two instance Partition_0 and Partition_1 # Generate code # Checking Platform_Ipw_Cfg.c missing Platform_SystemIrqConfigType struct for Partition_1 Test Case ID (internal TC that caught the defect):* Platform_TS_MUL_002 Observed behavior:* Missing Platform_SystemIrqConfigType struct for Partition_1 when add some instance !image-2021-03-03-10-29-26-142.png! Expected behavior:* Add Platform_SystemIrqConfigType for Partition_1.

ID	Subtype	Headline and Description
ARTD-8085	Bug	[SPI] SPI DMA notification function is not called by DMA interrupt in DMA fast transfer mode<*> In DMA transfer fast mode, driver is configurated using sequence of DMA ScatterGather TCD. There is one fail case: To support to transfer a Spi SEQUENCE has number of Channels <= 3. The sequence of ScatterGather is configured for SpiPhyRxDmaChannel in MCL: TCDScatterGather0->TCDScatterGather1->TCDScatterGather2. TCDScatterGather0: ESG=1, DREQ=0, INTMAJOR=0 TCDScatterGather1: ESG=1, DREQ=1, INTMAJOR=1 TCDScatterGather2: ESG=0, DREQ=1, INTMAJOR=0 If the SEQUENCE has 2 Channels is used for transferring then Spi Dma notification function is not called by MCL. Because TCDScatterGather2 is loaded immediately by HW after TCDScatterGather1 Done. So INTMAJOR will be set back to 0. So, when CPU jump to DMA interrupt function, MCL understood it is spurious interrupt(Done flag = 1 but INTMAJOR = 0). This will lead to SPI Dma notification is not called after that.
ARTD-8082	Bug	[GPT] Pit_Ip_SetCounterValue sets the period of timer one tick more<*> Detailed description (how to reproduce it): We are using PIT timer to generate periodic interrupt and we need to set the period of the interrupt exactly 50ms. The PIT timer is clocked by 60MHz so the period in ticks is 50e-3/(1/60e6) = 3000000 = 0x2dc6c0. Then we call the function to start the timer with this period: Pit_Ip_SetCounterValue(uint8 instance, uint8 channel, uint32 countValue); The interrupt is generated periodically after 0x2dc6c0+1 ticks which is not correct (the period is one clock tick more than expected). As per reference manual the value written to PIT LDVAL register shall be computed as follows (with minus 1): LDVAL trigger = (period / clock period) 1 Preconditions: PIT timer used Test Case ID (internal TC that caught the defect) optional: Ip_Pit_TC_003 Observed behavior: Wrong period set by Pit_Ip_SetCounterValue() Expected behavior: Correct period is set by Pit_Ip_SetCounterValue() Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: The PIT LDVAL register must be written with period 1 to generate correctly the period (timeout). So the value passed to Gpt_StartTimer() shall be decremented by 1 before writing to LDVAL register.

ID	Subtype	Headline and Description
ARTD-8131	Bug	S32_CT cannot generate both Tx and Rx configuration for the same SAI instance<*> S32K344 SAI0 is used to connect with audio codec sgtl5000 via I2S mode. Thus we need to configurate SAI0 Tx and Rx param both, via the Configuration Tools. There is a "Hardware Unit" Param in the Sai component Configuration Array, which indicates the SAI instance. However, each SAI instance can only appear once in each configuration array. That means, if I configure SAI_0 for Rx, then I can't add another configuration for SAI_0 anymore, even though SAI_0 Tx should be accepted to configure meanwhile. It is interested that the "Hardware Unit", which the SAI instance, actually not generated in the Param structure after Update Code, so I can select SAI_1 temporarily for Tx configuration. But if I do, the SAI_1 instance configuration can not be added.
ARTD-8207	Bug	[ADC] Compilation error when using DMA without results reorder or dma stream optimization<*> The following compilation error occurs on Dev Test Suites 007 and 008: c:/Users/nxf47222/Documents/artd-repo/output/S32K3XX_S32K344_gcc/adc/../../eclipse/plugins/Adc_TS_T40D34M9I0R0/src/Adc_Ipw.c: In function 'Adc_Ipw_StartDmaOperation': c:/Users/nxf47222/Documents/artd-repo/output/S32K3XX_S32K344_gcc/adc/../../eclipse/plugins/Adc_TS_T40D34M9I0R0/src/Adc_Ipw.c:1012:49: error: 'u32AdcCountingDmaLogicChId' undeclared (first use in this function); did you mean 'u32AdcDmaLogicChId'? 1012 LocTransferList[13].Value = u32AdcCountingDmaLogicChId; u32AdcDmaLogicChId c:/Users/nxf47222/Documents/artd-repo/output/S32K3XX_S32K344_gcc/adc/../../eclipse/plugins/Adc_TS_T40D34M9I0R0/src/Adc_Ipw.c:1012:49: note: each undeclared identifier is reported only once for each function it appears in c:/Users/nxf47222/Documents/artd-repo/output/S32K3XX_S32K344_gcc/adc/../../eclipse/plugins/Adc_TS_T40D34M9I0R0/src/Adc_Ipw.c:1031:13: error: 'CountingDmaLocTransferList' undeclared (first use in this function) 1031 CountingDmaLocTransferList[0].Param = DMA_IP_CH_SET_SOURCE_ADDRESS;
ARTD-8218	Bug	SAI component can't generate the Bit Clock correctly when use External Master Clock.<*> When use S32DS 3.4 Configuration Tool to configure the SAI component of S32K3xx RTD version 0.9.0, if we choose Master Clock Source as EXTERNAL_CLKi1/4OEthen the Sai Sample Rate can not be edit anymore, however, the SAI driver only calculate the Clock Divider for Internal Master Clock, therefore, the SAI BCLK and Frame Sync are not works as our expected frequency.
ARTD-8219	Bug	[S32K3][CLOCK] Correct the number of elements generated when the under MCU control node is false<*> The number of elements generated is wrong when the under MCU control node is false
ARTD-8221	Bug	[GPT] Update Example DS/EB<*> Update example Add example HLD on DS Update MCU on EB

ID	Subtype	Headline and Description
ARTD-8224	Bug	[DIO]The address of MPGPDO works incorrectly<*> The address calculation of MPGPDO register works incorrectly when it is MPGPDO1->MPGPDOmax Expected behaviour: The address calculation of MPGPDO register will work correctly Step: Update the address calculation of MPGPDO
ARTD-8228	Bug	[S32K3-LIN] Wakeup feature issue with Flexio IP<*> LIN doesn't wake up when MAF sends wakeup signal
ARTD-8237	Bug	[S32K3][SENT] SENT refers to wrong DMA channel from MCL<*> CDD_Sent.component needs update as bellow: <dynamic_enum id="SentDmaChannelRef_t" label="Sent Dma Channel Reference name" items="system::makeRefs(system::getChildrenByASPath(`/AUTOSAR/EcucDefs/Mcl/MclConfig/dmaLogicChannel_Type`))"> <description><![CDATA[EN:<html>Reference to the DMA Channel configure for the Request. </html>]]></description> </dynamic_enum>
ARTD-8270	Bug	[PWM][S32K3XX] Update Pwm_SyncUpdate API for taking into account multiple channels<*> Implement SyncUpdate functionality to be able to apply the settings for multiple channels from same instance. Please also consider the corner cases that were identified on former MCAL and AMNG implementations. See Pwm_eMios_SyncUpdate in that codebase. !image-2021-03-05-18-54-41-572.png|width=381,height=170!
ARTD-8276	Bug	s32k3 RTD SDK SIUL2 ICU issue<*> When configuring SIUL2 ICU module in s32ds configuration tool, the callback function name always reports with error: "Name must be a valid C identifier." See attached figure. Please provide a workaround.

ID	Subtype	Headline and Description
ARTD-8279	Bug	[SAI] Incorrect name of variable types as coding guideline<*> We has met some issues, when they define NO_STDINT_H: Nomal test, Example, Compile only d:\s32_zebra\repo_k3xx_beta\output\eclipse\plugins\sai_ts_t40d34m9i0r0\src \Sai_Ip_HwAccess.h: In function 'Sai_Ip_IsTxChannelEnabled': d:\s32_zebra\repo_k3xx_beta\output\eclipse\plugins\sai_ts_t40d34m9i0r0\src \Sai_Ip_HwAccess.h:117:16: error: 'true' undeclared (first use in this function) 117 bRet = true; d:\s32_zebra\repo_k3xx_beta\output\eclipse\plugins\sai_ts_t40d34m9i0r0\src \Sai_Ip_HwAccess.h:117:16: note: each undeclared identifier is reported only once for each function it appears in d:\s32_zebra\repo_k3xx_beta\output\eclipse\plugins\sai_ts_t40d34m9i0r0\src \Sai_Ip_HwAccess.h:121:16: error: 'false' undeclared (first use in this function) 121|bRet = false; As our coding guideline, I supposed *NULL_PTR*, *boolean* and *TRUE* should be used, instead of *NULL*, *bool* and *true
ARTD-8280	Bug	[WDG] Incorrect name of variable types as coding guideline<*> Detailed description (how to reproduce it): Now, driver code has some errors about coding rules when define CCOPT+=-DNO_STDINT_H Build error log: "d:/Zebra/S32K3XX_BETA/output/S32K3XX_S32K344_ghs/wdg/../../eclipse/plugins/Wdg_TS_T40D34M9I0R0/src/Swt_Ip.c", line 411: error #20: identifier "NULL" is undefined DevAssert(Swt_Ip_pConfig != NULL); "d:/Zebra/S32K3XX_BETA/output/S32K3XX_S32K344_ghs/wdg/../../eclipse/plugins/Wdg_TS_T40D34M9I0R0/src/Swt_Ip.c", line 538: error #20: identifier "NULL" is undefined DevAssert(Swt_Ip_pConfig != NULL); Preconditions: [...] Observed behavior: Incorrect name of variable types as coding guideline Expected behavior: Correct name of variable types as coding guideline Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:
ARTD-8273	New	New Feature [Platform]Fix some warning errors ,,"Detailed description (how to reproduce it): # Build test platform on station # check compilerwarning # dowload RTD_S32K3XX_Compiler_Warnings and check log file Test Case ID (internal TC that caught the defect):* N/A Observed behavior:* still some warning errors in the [MISRA Reports XLSX|https://bamboo1.sw.nxp.com/browse/ARTD-CIP136-6/artifact/BUILDCOV/MISRA-Reports-XLSX/] Expected behavior:* fix all warning errors"

ID	Subtype	Headline and Description
ARTD-8294	Bug	[S32K3XX][PORT] Build fail when add -DNO_STDINT_H in makefile<*> Detailed description (how to reproduce it): When add CCOPT+=-DNO_STDINT_H we can not build test due to in Siul2_Port_Ip.c did not define NULL Test Case ID (internal TC that caught the defect): IP_Port_Siul2_TC_0001 Observed behavior:* !image-2021-03-08-15-35-14-211.png! Expected behavior:* can build successfully, we must use NULL_PTR instead of NULL
ARTD-8286	Bug	[S32K344][LIN] Function Lpuart_Lin_Ip_GetReceiveStatus return value pBytesRemaining incorrect.<*> Function Lpuart_Lin_Ip_GetReceiveStatus return value pBytesRemaining incorrect. After receiver response OK, Lpuart_Lin_Ip_GetReceiveStatus still return value pBytesRemaining equal 1.
ARTD-8299	Bug	[S32K3][MCU] Hardfault error when call Mcu_InitClock on Sent_example_DS<*> Issue In function Mcu_InitClock, I got hardfalut error when execute NOT_UNDER_MCU_CONTROL_A with clkState[PLL_CLK]: !image-2021-03-08-16-26-39-356.png|thumbnail!
ARTD-8303	Bug	[CRYPTO] Compiler warnings<*> Detailed description (how to reproduce it): Compiler warning report have waring on GCC sheet (attached file below) link station: http://somov.ea.freescale.net/2/project/custom_compilerwarning/details Test Case ID (internal TC that caught the defect)*: N/A Observed behavior: C:/vv_tools/eb/EB_tresos_Studio_27.1.0_b200625-0900_06/plugins/Crypto_TS_T40D34M9I0R0/include/Crypto_ASRExtension.h 130 "CRYPTO_ENABLE_TLS12_DERIVE_SUPPORT" is not defined, evaluates to 0 [-Wundef]@56 130 #if (STD_ON == CRYPTO_ENABLE_TLS12_DERIVE_SUPPORT) Expected behavior: No warning in compiler warning report
ARTD-8308	Bug	[S32XX][S32K3XX] Crypto: CT configuration does not check Max value of key slot and same key ID<*> Detailed description (how to reproduce it): # Can configure the maximum number of key slot for a groups key catalog is 256 but each group key have specific value maximum # When configure CryptoKelement for CryptoKeyType , user can configure 2 key same ID , need add condition a CryptoKeyTyppe doesn't configure 2 keyelement same ID Expected behavior: # Add check the maximum allowed number of configured groups in both Nvm and Ram key catalogs # Add check a CryptoKeyElement with the same CryptoKeyElementId already exists in the reference list when configure CryptoKelement for CryptoKeyType

ID	Subtype	Headline and Description

ARTD-8309	Bug	[S32K3][MCL][Design] Redesign requirement CPR_RTD_00511.mcl<*>
		
		Change of period should be supported for an active/initialized eMIOS counter bus assigned exclusively to PWM.
		The MCL driver shall provide an API for updating the period at run time for eMIOS counter bus channels exclusively assigned to PWM.
		The API name shall be:
		void Mcl_eMiosSetCounterBusPeriod(CounterBus, Period, SyncUpdate);
		The implementation should validate the API parameters channel range and period range.
		Per default this optional API and functionality shall be disabled.
		Drivers capable of using Counter Buses shall check on configuration time and not allow selection of an Counter Bus with exclusive access granted to PWM.
		
		Note:
		The runtime flow for sync update will be:
		
		void Mcl_eMiosSetCounterBusPeriod(CounterBus, Period, SyncUpdate=TRUE);
		clear OUDIS with specific MCL API;

ARTD-8328	Bug	[SAI] Can not continue receiving data after DMA receiver error<*> Detailed description (how to reproduce it): Can not continue receiving data after DMA receiver error Prepare SAI receiver buffer data, declare as const to make driver can not write to buffer data and generate DMA error event Setup MAF to send data Setup SAI is master, receiver mode Call Sai_AsyncTransmit and wait until the driver status is not BUSY Verification Point: Driver returns SAI_STATUS_ERROR Repeat step to setup MAF and SAI driver Verification Point: Driver returns SAI_STATUS_COMPLETED => FAIL{color}*, driver stucks in Dev_assert function. !SAI_DMA_ERROR.png! Preconditions: [...] Observed behavior: Can not receive data successfully Expected behavior: Receive data successfully Proposed solution optional:
ARTD-8331	Bug	[S32K3_0.9.0][Tresos] Compilation failed with both ICU and OCU in project<*> I am facing a compilation issue when using both ICU and OCU - Tresos plugins of RTD_S32K3_BETA_0.9.0 In Emios_Ocu_Ip_Types.h and Emios_Icu_Ip_Types.h, you are having same macros naming but with different types of definitions. For example: <Emios_Ocu_Ip_Types.h> #define EMIOS_BUS_A (0x0U) <Emios_Icu_Ip_Types.h> typdef enum \{EMIOS_BUS_A 0} Which causes the compilation issue when using both of them in Tresos project.

ID	Subtype	Headline and Description
ARTD-8340	Bug	[GPT] Compile_Only tests will fail because 'true' is used instead of 'TRUE'<*> !image-2021-03-09-10-37-33-788.png|thumbnail! usage of 'true' instead of 'TRUE' leads to a build failed
ARTD-8342	Bug	[MCU] Lack implement requirement RAM_IP_001_002<*> Follow requirement RAM_IP_001_002*: The function Ram_Ip_GetRamState shall be available to the user if the pre-compile parameter McuGetRamStateApi is set to TRUE. Instead, if the former parameter is set to FALSE, this function shall be disabled(e.g. the hardware does not support this functionality). Solution*: in Ip layer define a macro "RAM_IP_GET_RAM_STATE_API" and guard function Ram_Ip_GetRamState
ARTD-8347	Bug	[ADC] Incorrect name of variable types as coding guideline<*> Detailed description (how to reproduce it): Now, ADC example has some incorrect name of variable types as coding guideline (NULL) Platform_InstallIrqHandler(ADC0_IRQn, Adc_Sar_0_Isr, NULL); Platform_InstallIrqHandler(BCTU_IRQn, Bctu_0_Isr, NULL); Preconditions: [...] Observed behavior: Incorrect name of variable types as coding guideline Expected behavior: Correct name of variable types as coding guideline Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:
ARTD-8344	Bug	LCU output filter<*> The LCU_FILT_LUT_RISE_FILT_MASK should be removed. Otherwise, the filter value writes to LCx_FILTy will always keep zero.
ARTD-8366	Bug	s32k3 siul2 icu callback function type<*> When configuring siul2_icu, the callback funtion is declaration generated in "Siul2_Icu_Ip_SA_BOARD_InitPreipherals_PBcfg.c" is void (void) type. But actually this callback funtion type is "Siul2_Icu_Ip_CallbackType", that is void (uint16, boolean). So there will be compiling warnings here since the generated function type doesn't match the callback function type definition. Also, I don't know why the callback function has two parameters. The second boolean parameter is not used according to Siul2_Icu_Ip.c source code "Siul2_Icu_Ip_Callback()" function definition.
ARTD-8367	Bug	[S32K3XX][PWM] Fix and comment static analysis violations after adding FlexIO ipv (MISRA + HIS + CERT-C)<*> After adding FlexIO ipv in Pwm driver, it has some misra violation and HIS that need to be fixed or commented . Please see attached file below :

ID	Subtype	Headline and Description
ARTD-8381	Bug	[GPT] Lacking misra violation<*> !image-2021-03-10-15-11-14-772.png|thumbnail! please see the picture
ARTD-8386	Bug	[S32K][MCL-LCU] Correct Lcu_Ip_LogicInputInit function.<*> Update HwAcc_Lcu_AsyncSetInputSwSyncMode(HwLcu, LocHwLcInputId, (pConfig->SwSynMode & 1U) << LocHwLcInputId); to HwAcc_Lcu_AsyncSetInputSwSyncMode(HwLcu, LocHwLcInputId, (pConfig->SwSynMode & 1U));
ARTD-8393	Bug	[S32K3][MCL] TRGMUX Output Names for LCU need to be updated<*> Update the TRGMUX Output Names for: LCU_0_{color:#DE350B}-lc1-{color}_inp_i1 -> TRGMUX_IP_OUTPUT_LCU0_I0 LCU_0_{color:#DE350B}-lc1-{color}_inp_i2 -> TRGMUX_IP_OUTPUT_LCU0_I1 LCU_0_{color:#DE350B}-lc1-{color}_inp_i3 -> TRGMUX_IP_OUTPUT_LCU0_I2 LCU_0_{color:#DE350B}-lc1-{color}_inp_i4 -> TRGMUX_IP_OUTPUT_LCU0_I3 LCU_0_{color:#DE350B}-lc2-{color}_inp_i1 -> TRGMUX_IP_OUTPUT_LCU0_I4 LCU_0_{color:#DE350B}-lc2-{color}_inp_i2 -> TRGMUX_IP_OUTPUT_LCU0_I5 LCU_0_{color:#DE350B}-lc2-{color}_inp_i3 -> TRGMUX_IP_OUTPUT_LCU0_I6 LCU_0_{color:#DE350B}-lc2-{color}_inp_i4 -> TRGMUX_IP_OUTPUT_LCU0_I7 LCU_0_{color:#DE350B}-lc3-{color}_inp_i1 -> TRGMUX_IP_OUTPUT_LCU0_I{color:#57D9A3}8 LCU_0_{color:#DE350B}-lc3-{color}_inp_i2 -> TRGMUX_IP_OUTPUT_LCU0_I{color:#57D9A3}9 LCU_0_{color:#DE350B}-lc3-{color}_inp_i3 -> TRGMUX_IP_OUTPUT_LCU0_I{color:#57D9A3}10 LCU_0_{color:#DE350B}-lc3-{color}_inp_i4 -> TRGMUX_IP_OUTPUT_LCU0_I{color:#57D9A3}11 Same for LCU1.
ARTD-8402	New	New Feature [ETH]Revert Gmac_Cfg.h caused by merged Kinetis code ,,Gmac_Ip_Cfg.h changed when merged Kinetis driver. Have to revert.
ARTD-8406	New	New Feature [S32K3XX][VNV_CONFIG] Update wiring for PWM ,,"Update wiring for PWM as below: Test point MCU pin Jump MAF_TP_PWM0_1 PTC31 J181.1 MAF_TP_PWM0_5 PTD24 J184.11"

ID	Subtype	Headline and Description
ARTD-8416	Bug	[MCU] FXOSC bypass bit(FXOSC_CTL[OSC_BYP]) will not be generated appropriately<*> Description: SWS reported that FXOSC Bypass configuration in McuFXOSC will not be applied to generated source code. As you can see in the figure below, even when FXOSC Bypass's checkbox is cleared, XOSC bypass option in Clock_I_PBcfg.c will be 0. #if CLOCK_XOSCS_NO > 0U { FXOSC_CLK, / Clock name associated to xosc / 40000000U, / External oscillator frequency. / 1U, / Enable xosc. / 157U, / Startup stabilization time. / 0U, / XOSC bypass option / This value is always 0 0U, / Comparator enable / 12U, / Crystal overdrive protection / }, Proposal solution: Update the code(By*P*ass to By*p*ass) of in the file Clock_Ip_RegOperations.m from: [!MACRO "GetXoscBypass","Name"!][!// [!NOCODE!] [!VAR "capitalName" = "text:replace($Name,substring($Name,2),text:tolower(substring($Name,2)))"!] [!VAR "bypassPath" = "concat('Mcu',$Name,'/Mcu',$capitalName,'ByPass')"!] to: [!MACRO "GetXoscBypass","Name"!][!// [!NOCODE!] [!VAR "capitalName" = "text:replace($Name,substring($Name,2),text:tolower(substring($Name,2)))"!] [!VAR "bypassPath" = "concat('Mcu',$Name,'/Mcu',$capitalName,'Bypass')"!]
ARTD-8424	Bug	[SAI] Missing check in configurator for Element Size to be larger than Sai Word Width<*> Add check in configurator for this note from RM: 70.3.4.2 FIFO pointers When writing to a Transmit Data Register (TDRn), the Write FIFO Pointer (WFP) of the corresponding Transmit FIFO Register (TFRn) increments after each valid write. The SAI supports 8-bit, 16-bit, and 32-bit writes to the Transmit Data Register and the FIFO pointer increments after each individual write. Note that 8-bit writes should only be used when transmitting up to 8-bit data; 16-bit writes should only be used when transmitting up to 16-bit data. Also clarify description and node name: Sai_RequestType: /**< brief Buffer Size : The number of words for reading or writing of each channel. / uint32 bufferSize; The word size from here is actually defined by number of bytes in "Sai Element Size", not the SAI word width. I suggest renaming to "Sai Buffer Element Size" and adding a comment for bufferSize, to clarify this: "The number of words for reading or writing of each channel. The size of each buffer word element is "Sai Buffer Element Size" selected in configurator. /

ID	Subtype	Headline and Description
ARTD-8432	Bug	[S32K3XX][PWM] The name of the configuration structure for PB is not correct<*> Detailed description (how to reproduce it): Naming of the configuration structure for PB is not correct. If post-build variants exist, then the configuration structure used for initialization must be named as <Mip>_Config_<PredefinedVariant.shortName>. Otherwise, the name is <Mip>_Config. But now, the generated name of configuration structure is Pwm_Config[!"$postBuildVariantNameUnderscore"!]_PB; We need remove "_PB" there. Preconditions: IMPLEMENTATION_CONFIG_VARIANT = VariantPostBuild Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-8435	Bug	[ICU][S32K3XX] Generate failed in DS in Icu module about masterbus<*> Detailed description (how to reproduce it): Icu ASR component using EMIOS IP with CounterBus selection in Mcl issues error on generation. Preconditions: Create project in DS with emios using counter bus. Define the counterbus in Mcl component. Try to generate and build the project. Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Multiple issues reported in Problems View. Expected behavior: Code generation works and build of project can be done. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Generate failed in DS in Icu module about masterbus. pls see attach file

ARTD-8444	Bug	s32k3 rtd lpspi drv source code issue<*>
		
		In the source code "Lpspi_Ip.c", line 1254, the code is:
		if (state != NULL_PTR)
		while it should be like this:
		if (state == NULL_PTR)

ID	Subtype	Headline and Description
ARTD-8446	Bug	[S32DS] Generated file for S32DS high layer missing some parameter in config<*> Please refer to the attached image to see the error of the parameter. It is need to generate same as in EB Tresos. !image-2021-03-12-17-11-23-353.png!
ARTD-8459	Bug	[ICU][S32K3XX] Generate with ECUM string in DS in Icu<*> Detailed description (how to reproduce it): Icu ASR component using channels with wakeup is generating with fix string on wakeup source. Preconditions: Create project in DS with channels with wakeup capabilities. Try to generate and build the project. Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: !image-2021-03-12-17-48-22-090.png! Expected behavior: Code generation works and build of project can be done. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: correct wakeup source generation.
ARTD-8463	Bug	[S32K3XX] PWM: The failed building with CT when using the interrupt<*> Detailed description (how to reproduce it): Cannot generate the Prototypes of PWM channels User Notifications in HLD in CT Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-8465	New	New Feature [S32K344] [PORT] (ITG)Adding new req relate to execute test with supervisor mode and user mode ,,"NewWorkDescription: new reqs about run test with user mode and supervisor mode: CPR_RTD_00395.port: The RTD drivers shall be able to run in a privileged processor mode (e.g. Supervisor mode). All known related constraints shall be documented. CPR_RTD_00352.port: The Real Time Drivers shall be able to run in a non-privileged processor mode (e.g. User mode). All known related constraints shall be documented. A vendor specific pre-compile boolean configuration parameter PortEnableUserModeSupport \{PORT_ENABLE_USER_MODE_SUPPORT}shall be created for each driver to activate the specific implementation for non-privileged mode. By default, 'PortEnableUserModeSupport' field shall be disabled. Requirement source: CPR_RTD_00395.port, CPR_RTD_00352.port (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: add on Port_TC_WBT_0036"
ARTD-8472	Bug	[MCU][S32CT] Wrong condition of RAM DEFAULT VALUE<*> Condition of RAM DEFAULT VALUE is incorrect on S32CT. RAM DEFAULT VALUE have range is 0 > 255. But when i add 255 to McuRamDefaultValue, S32CT display error "The Ram base address must be 4 byte aligned" Detail in attached files
ARTD-8491	Bug	[GPT] Duplicate UUIDs<*> Coding convention implies that no TAB is to be used in the code source files we deliver. (to avoid inconsistent displays of code alignment if TAB size is defined differently) Replace all duplicated UUIDs, to avoid generation crashes on customer side. Proposed solution: Replace all TABs with 4 spaces. Update your text editor settings to always use 4 spaces instead of a TAB Replace duplicated UUIDs. Summary: Plugin No. of duplicated UUIDs Eth.xdm 1 Gpt.xdm 1 Lin.xdm 2 Rm.xdm 236 Rm_s32k314_mapbga257.xdm 2 Rm_s32k314_mqfp100.xdm 118 Rm_s32k314_mqfp172.xdm 118 Rm_s32k324_mapbga257.xdm 118 Rm_s32k324_mqfp172.xdm 118 Rm_s32k344_mapbga257.xdm 118 Rm_s32k344_mqfp172.xdm 118 Sai.xdm 1 Sent.xdm 2

ID	Subtype	Headline and Description
ARTD-8494	Bug	[GPT] Re-Align code for run TraceabilityMatrix<*> Some line of code not match with implement Do Not change line of code
ARTD-8498	Bug	[ADC] Adc_ConfigVariantPredefined placed in different memory section in .h vs .c<*> Detailed description (how to reproduce it): Adc_ConfigVariantPredefined placed in different memory section in .h vs .c .h: #ifdef ADC_PRECOMPILE_SUPPORT #define ADC_START_SEC_VAR_NO_INIT_UNSPECIFIED #include "Adc_MemMap.h" extern const Adc_ConfigType const Adc_ConfigVariantPredefined[ADC_MAX_PARTITIONS]; #define ADC_STOP_SEC_VAR_NO_INIT_UNSPECIFIED #include "Adc_MemMap.h" #else in .c is placed in ADC_START_SEC_CONFIG_DATA_UNSPECIFIED The variable ends up alocated in mcal_const_cfg with gcc and iar. So functionality is correct Expected behavior: same memory section used for function declaration and definition
ARTD-8543	New	New Feature [S32K344] [PORT] (ITG)Fix issue relate to StandardType ,,"NewWorkDescription: Build fail when execute test IPL relate to undefine some variables when have condition NO_STDINT_H Requirement source: NA Proposed solution optional: IP_Port_Siul2_TC_0001, ...-> IP_Port_Siul2_TC_0006"

ID	Subtype	Headline and Description
ARTD-8558	Bug	[ICU][S32K3XX] The array length for instance configuration is wrong<*> Detailed description (how to reproduce it): There are 2 items to address: in file Icu_Ipw_VS_0_PBcfg.c; array size for instance configuration is wrong (see picture attached) the generation for the case where the reference ECUM wakeup info is missing is rising error in tool even if the wakeup capability is not enabled for the channel this is a regression from previous TAG. Preconditions: use attached mex file for configuring an example in DS Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: with latest icu tag there are errors on generation and also if the errors are corrected in generation the size of instances array is wrong. The array length contains the instance configuration is error in file Icu_Ipw_VS_0_PBcfg.c. In the attach file, the configuration has 3 instances, but the length array is 5. Expected behavior: generation is not depending on wakeup capability and size of array should be correct. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:
ARTD-8566	Bug	[K3XX][ETH] Fix "true" -> "TRUE" in Eth_Ipw_SetCorrectionTime ,,"Detailed description (how to reproduce it): When the option CCOPT+=-DNO_STDINT_H is enabled on .mak file. The compile only tests for HLD failed at build. In Eth_Ipw.c, line 523, please fix: ""true"" > ""TRUE"" STDERR:C:/vv_tools/eb/EB_tresos_Studio_27.1.0_b200625-0900_06/plugins/Eth_TS_T40D34M9I0R0/src/Eth_Ipw.c:523:85: error: 'true' undeclared (first use in this function) Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: Eth_TS_035 Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-8572	New	New Feature [S32K344] [PORT] (ITG)Fix issue relate to StandardType ,,"NewWorkDescription: Build fail when execute test IPL relate to undefine some variables when have condition NO_STDINT_H Requirement source: NA Proposed solution optional: IP_Port_Siul2_TC_0004"
ARTD-8575	Bug	[Wkup]: The error of "selected core does not support NMI" has always existed in s32ds3.4+RTD0.9.0.<*> Detailed description (how to reproduce it): [No matter how you modify the Wkup configuration, the error of "selected core does not support NMI" has always existed in s32ds3.4+RTD0.9.0.] !RTD_Wkup_error.png! : [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-8582	New	New Feature [S32K344 BETA][CF3] GPT: Test code update ,,"IPs list: eMIOS, PIT, STM, RTC. Tests implementation. 100% requirements coverage. Update test code for Ip layer"

ID	Subtype	Headline and Description
ARTD-8595	Bug	[SAI] S32CT can not config data line when use interrupt and mux_mem mode<*> Detailed description (how to reproduce it): Create new SAI project with S32DS Select INTERRUPT and MUX_MEM mode Enable Sai Data Line 0, 1, 2 Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: Appear an error: "In memory mux mode and interrupt, enable at least two datalines." Expected behavior: Project have no error when enable at least 2 data line in memory mux mode and interrupt Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-8596	New	New Feature [S32K344 BETA] Crypto: Update driver FMEA ,,"NewWorkDescription: Update *Driver source code and *Driver requirements FMEA fields with the latest souce code tag and requirements. Requirement source: FMEA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Driver source code: *CRYPTO_043 Driver requirements:*10.0 BLNREQ_CRYPTO_RTD_4.4_S32K3XX_0.9.0"

ID	Subtype	Headline and Description

ARTD-8599	Bug	[ADC] Normal Software group cannot run in parallel with Injected HW group with DMA enable<*>
		
		Detailed description (how to reproduce it):
		Normal Software group cannot run in parallel with Injected HW group with DMA enable, because StartGroupConversion reprograms DMA channel.
		ExternalDma cannot be used as workaround for ADC Sw group, because in Adc_Ipw_StartNormalConversion all DMA channels are disabled before enabling again the DMA channel for Sw group:
		#ifdef ADC_DMA_SUPPORTED
		if (ADC_DMA == Adc_pCfgPtr[u32CoreId]->pAdcIpwConfig->Mapping.u8Adc_DmaInterruptSoftware[Unit])
		{
		Adc_Sar_Ip_DisableChannelDmaAll(Unit);
		Adc_Sar_Ip_EnableChannelDma(Unit,pGroupPtr->LastCh);
		Adc_Sar_Ip_EnableDma(Unit);
		if((uint8)STD_OFF == pGroupPtr->u8AdcExtDMAChanEnable)
		{
		/ Configure DMA in MCL module /
		Adc_Ipw_StartDmaOperation(Unit, Group, u32CoreId);
		}
		}
		else
		Preconditions:
		Adc_EnableHardwareTrigger for injected group with DMA must be called before calling SW group
		Test Case ID (internal TC that caught the defect) optional:
		N.A.
		Expected behavior:
		Sw Group can work in parallel with or without interrupt or with dma
		Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)

ARTD-8609	Bug	[GPT][S32K3XX] Add volatile keyword for variable testcase multicore to avoid hardfault error when compiler is optomized<*> Avoid compiler optimization with variable in testcase sometime lead to hardfault error.
ARTD-8621	Bug	[ADC] DMA streaming without interrupts is not working simultaneously on multiple ADCs because u32DmaNoIrqBuffer is shared between ADCs<*> Detailed description (how to reproduce it): DMA streaming without interrupts is not working simultaneously on multiple ADCs because u32DmaNoIrqBuffer is shared between ADCs Preconditions: N.A. Test Case ID (internal TC that caught the defect) optional: N.A> Observed behavior: DMA streaming without interrupts is not working simultaneously on multiple ADCs because u32DmaNoIrqBuffer is shared between ADCs Expected behavior: DMA streaming without interrupts works simultaneously on multiple ADCs Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)

ID	Subtype	Headline and Description
ARTD-8634	New	New Feature [GPT] [S32K3XX] Remove config Emios for test multicore external because of some unknown hardfault when running with GCC compiler ,,"When i run test configured for Emios with 2 parabell core at once, Error hardfault occurred but it is not clear. This error happen is random at any location while running test. But if turning off compiler optimization, this will not happen anymore. With other compiler GHS and IAR, test is good and stable, and also with internal test without running with MAF, for Emios hardware, running test wit Emios is absolutely stable. So i think this error maybe due to MAF or some issue with optimization of compiler. So i will remove config for Emios in test for testsuite Gpt_TS_300 to avoid this error effect to the result of test and document collection."

ID	Subtype	Headline and Description
ARTD-8651	Bug	[CRYPTO][CT Examples] Duplicate number of catalogue in description.txt of some example projects<*> Precondition:* Open S32SD3.4 update1 which installed package SW32_RTD_4.4_1.0.0_HF01_D2102_DS_Updatesite.zip! Step: 1.Import all example project for S32G: 2. Open description.txt then check content Observed behavior: Duplicate number of catalogue " 3.2 Compiling the application" and " 3.2 Running the application on the board" Wdg_Example_IPL_DS Wdg_Example_HLD_DS Uart_HLD_S32G_DS_Example Linflexd_Uart_Ip_S32G_DS Spi_IP_example_CT_S32G Spi_HLD_example_CT_S32G Qdec_Ip_example_DS Qdec_example_DS Port_example_DS Ocu_Ftm_example_DS Ocu_example_DS Ocotp_IP_Example Ocotp_AUTOSAR_Example Lin_example_IPV Lin_example_HLD Icu_Siul2_Wkpu_example Icu_Ftm_example Icu_ASR_example I2c_S32G274A_IP_DS I2c_S32G274A_HLD_DS Example_S32G2XX_DS_Qspi_Ip Example_S32G2XX_DS_Fls Fee_Example_S32G2 Eth_Example_DS_002 Eth_Example_DS_001 Example_S32G2XX_DS_Eep Dio_example_DS_S32G Hse_Ip_Read_Hse_Attr Hse_Ip_Aes_Enc_Async_Irq Crypto_Hash Crypto_Cmac_Gen_Ver Crypto_Aes_Enc_Dec FlexCAN_example_CT CAN_example_CT Adc_example_DS_IP Adc_example_DS Expected behavior:

4.8 EAR 0.8.1

ID	Subtype	Headline and Description
ARTD-952	Bug	[MCL] VSMD Report: Warnings and Errors<*> RTD_MCL_VSMDReport.html contains warnings and errors which need to be resolved/ commented.
ARTD-971	New	New Feature [CAN][S32G274 BETA] CAN Add support for Enhanced RxFIFO ,,"Add support for Enhanced RxFIFO Configuration, setup of Enhanced Rx Filters, support for read of messages(pooling, interrupt and DMA)"
ARTD-982	Bug	[OCU] Update EBT config files to remove warnings like "'macro' is not defined, evaluates to 0" ,,"Update EBT config files to remove warnings like ""_'macro' is not defined, evaluates to 0_""
ARTD-1052	New	New Feature [S32G274 BETA][S32K3 BETA] GPT: Update test specification to fix comments from STRX team ,,"When creating the TestCases and the Test Specification, please check attachment and fix comments from STRX team for below module: ADC, CAN, CRYPTO, DIO, ETH, FEE, FLS, GPT, I2C_CDD, ICU, MCL, MCU, OCU, PORT, PWM, SPI, WDG"
ARTD-1161	New	New Feature [SENT][S32K3XX BETA] Implementation for Serial Enhanced Messages ,,"Serial Enhanced support needs to be implemented: Implement algorithm to decode Serial message from FLEXIO timer to: Enhanced Short data. Create 2 functions Sent_GetSerialMsgData, Sent_GetSerialChannelMsgData to receive serial message."
ARTD-1176	Bug	[MCL] TRGMUX: S32CT Configuration of Logic Trigger Group is not limited<*> The TRGMUX S32CT Logic Group number of triggers is not limited to the number of possible triggers per group.

ID	Subtype	Headline and Description
ARTD-1464	New	New Feature [cdd_qd] [S32G274 BETA]Fix copyright violations ,,"Please refer to the attached ""copyright_violations.txt"" ([https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/General/Attachments/S32G%20RTD%204.4%200.9.0/ARTD-972/copyright_violations.txt]) to identify the files that need to be updated. The plugins of the following drivers contain at least a source file or header file without copyright notice: [adc|https://jira.sw.nxp.com/issues/?jql=project+%3D+ARTD+AND+component+%3D+adc], [base|https://jira.sw.nxp.com/issues/?jql=project+%3D+ARTD+AND+component+%3D+base], [can|https://jira.sw.nxp.com/issues/?jql=project+%3D+ARTD+AND+component+%3D+can], [canif|https://jira.sw.nxp.com/issues/?jql=project+%3D+ARTD+AND+component+%3D+canif], cryif, crypto, csm[, dem|https://jira.sw.nxp.com/issues/?jql=project+%3D+ARTD+AND+component+%3D+dem], [det|https://jira.sw.nxp.com/issues/?jql=project+%3D+ARTD+AND+component+%3D+det], [dio|https://jira.sw.nxp.com/issues/?jql=project+%3D+ARTD+AND+component+%3D+dio], [ecum|https://jira.sw.nxp.com/issues/?jql=project+%3D+ARTD+AND+component+%3D+ecum], eep, [eth|https://jira.sw.nxp.com/issues/?jql=project+%3D+ARTD+AND+component+%3D+eth], [fee|https://jira.sw.nxp.com/issues/?jql=project+%3D+ARTD+AND+component+%3D+fee], [fls|https://jira.sw.nxp.com/issues/?jql=project+%3D+ARTD+AND+component+%3D+fls], [gpt|https://jira.sw.nxp.com/issues/?jql=project+%3D+ARTD+AND+component+%3D+gpt], [i2c_cdd|https://jira.sw.nxp.com/issues/?jql=project+%3D+ARTD+AND+component+%3D+i2c_cdd], [icu|https://jira.sw.nxp.com/issues/?jql=project+%3D+ARTD+AND+component+%3D+icu], [linif|https://jira.sw.nxp.com/issues/?jql=project+%3D+ARTD+AND+component+%3D+linif], [mcl|https://jira.sw.nxp.com/issues/?jql=project+%3D+ARTD+AND+component+%3D+mcl], [mcu|https://jira.sw.nxp.com/issues/?jql=project+%3D+ARTD+AND+component+%3D+mcu], [memif|https://jira.sw.nxp.com/issues/?jql=project+%3D+ARTD+AND+component+%3D+memif], ocu, os, [port|https://jira.sw.nxp.com/issues/?jql=project+%3D+ARTD+AND+component+%3D+port], pwm, qdec, rm, sent, [spi|https://jira.sw.nxp.com/issues/?jql=project+%3D+ARTD+AND+component+%3D+spi], uart, [wdg|https://jira.sw.nxp.com/issues/?jql=project+%3D+ARTD+AND+component+%3D+wdg], [wdgif|https://jira.sw.nxp.com/issues/?jql=project+%3D+ARTD+AND+component+%3D+wdgif] Please refer to the following link to obtain the correct header comment (which contains the copyright notice): [https://confluence.sw.nxp.com/display/AUTORD/Module+C+source+files+templates]"
ARTD-1474	New	New Feature [ETH]Support time-aware shaper and Preemption ,,Support time-aware shapper along the credit base feature

ID	Subtype	Headline and Description
ARTD-1499	Bug	[MCL] Hard Fault is triggered when using Mcl_Init() to configure channels from 13 to 31<*> Detailed description (how to reproduce it): I have tried running a test but it not work because the program jump to hard fault when using Mcl_Init function to configure for channel 12 > 31. With configuration on EB as: Config all paramater for the logic channels 0 > 31. I investigated and saw that the address offset of channels 12 31, which the drive defined, is incorrect. it will result the program jump to hard fault in Dma_Ip_Features.h file in MCL drive #define DMA_IP_TCD_PTR_ARRAY ((Dma_Ip_HwChTcdRegType) ((uint32)DMA_IP_TCD_BASE (uint32)(0U 16384U))),\ ..... ((Dma_Ip_HwChTcdRegType)((uint32)DMA_IP_TCD_BASE (uint32)(11U 16384U))),\ ((Dma_Ip_HwChTcdRegType)((uint32)DMA_IP_TCD_BASE (uint32)(1916928U (0U 16384U)))),\ ((Dma_Ip_HwChTcdRegType)((uint32)DMA_IP_TCD_BASE (uint32)(1916928U (1U 16384U)))),\ .....} I have calculated and replaced 1916928U to 2097152U. it works well. Preconditions: Config all paramater for the logic channels 0 > 31 on EB tresos. Test Case ID (internal TC that caught the defect) optional: Mcl_TC_FCT_0201 Observed behavior: Got Hard Fault when using Mcl_init function to configure for channels 13 through 31 Expected behavior: Hard Fault no longer occur Note:* in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-1525	New	New Feature [SENT][S32K3XX BETA] Implementation for Fast Messages using polling ,,"Implement feature to receive Fast message using polling method (Synchronous reception using polling method) Sent_GetFastMsgData Sent_GetFastChannelMsgData"
ARTD-1550	Bug	[S32CC][DIO] Driver implement missing SIUL2 Parallel GPIO Pad Data In Register (PGPDI)<*> Test case Wiring for test_dio build fail. DIO driver missing SIUL2 Parallel GPIO Pad Data In Register (PGPDI)) TC : tse_bbx_wir_dio_00100 Expected behavior:* Dio driver add PGPDI feature Solution: Add the MACRO for PGPDI. Check all the other MACRO for other register and update.

ID	Subtype	Headline and Description
ARTD-1552	New	New Feature [CRYPTO] Add Tresos support for running on top of different HSE Firmware Types (Standard, Premium)" ,,"Add support for running on top of different HSE Firmware Types (Standard, Premium) add a new attribute in Tresos plugin called HseFwType allowing the user to choose the flavour of the HSE that runs under Crypto update resource.txt files to include distinct values for the supported Hse Fw types update the EBT Crypto,xdm file such that all ecu:get and ecu:list calls are made to the resource variables constructed based on the user chosen Hse Fw Type update the EBT Crypto_Cfg.c/h file such that all ecu:get and ecu:list calls are made to the resource variables constructed based on the user chosen Hse Fw Type
ARTD-1564	Bug	[MCL] Mcl_CacheDisable() triggers HardFault_Handler()<*> when use function Mcl_CacheDisable(Mcl_CacheAll); to disable cache for S32K3xx Function disable cache is not available and jump to HardFault_Handler() (Note: If call to funtion clean cache before disable cache, function Mcl_CacheDisable() is available) Detail on attached file
ARTD-1567	New	New Feature [SENT][S32K3XX BETA] Implementation for Fast Messages using interrupt ,,Implement feature to receive Fast message using interrupt method (Asynchronous reception using interrupt method)

ID	Subtype	Headline and Description
ARTD-1619	New	New Feature [ocu] Update target_path in manifest files ,,"The target folder name in DS has been changed to ""RTD"" from ""SDK"": !image-2020-09-16-17-01-39-986.png! As a result, all the target_path attributes in the driver's manifest files must be updated: Example: {code:xml|title=old_sdk_manifest_ethernet.xml|borderStyle=solid} <component id=""platform.driver.gmac"" full_name=""Gmac"" brief=""""" dependency="""" name=""Gmac"" type=""driver"" devices=""S32G233A S32G234M S32G254A S32G274A S32G274A_Rev2"">"> <source path=""Eth_TS_$(AR_RELEASE_ID)/src"" type=""src"" target_path=""SDK/ src"">"> <files mask=""Gmac*.c""/> </source> <source path=""Eth_TS_$(AR_RELEASE_ID)/include"" type=""c_include"" target_path=""SDK/include"">"> <files mask=""Gmac*.h""/> <files mask=""Emac_Ip_Wrapper.h""/> </source> </component> {code:xml|title=new_sdk_manifest_ethernet.xml|borderStyle=solid} <component id=""platform.driver.gmac"" full_name=""Gmac"" brief=""""" dependency="""" name=""Gmac"" type=""driver"" devices=""S32G233A S32G234M S32G254A S32G274A S32G274A_Rev2"">"> <source path=""Eth_TS_$(AR_RELEASE_ID)/src"" type=""src"" target_path=""RTD/ src"">"> <files mask=""Gmac*.c""/> </source> <source path=""Eth_TS_$(AR_RELEASE_ID)/include"" type=""c_include"" target_path=""RTD/include"">"> <files mask=""Gmac*.h""/> <files mask=""Emac_Ip_Wrapper.h""/> </source> </component> "
ARTD-1708	New	New Feature [I2C] Driver should support for precompile variant ,,Driver should support for precompile variant

ID	Subtype	Headline and Description
ARTD-1752	New	New Feature [ocu] Handle SchM files in a Design Studio project ,,"Each driver that has SchM files in the Rte driver needs to update its sdk manifest xml file to copy the .c and .h files from Rte when the component is added in the project. Reference implementation: [https://bitbucket.sw.nxp.com/projects/ARTD/repos/dem/pull-requests/10/diff#specific/S32CC/sdk_manifest_dem.xml] A new component will be added in the driver manifest: The name of the new component should be Rte_<module_name>. Ex: Rte_Spi, Rte_Can_43_LLCE (for vendor API infix extended module names) <component id=""platform.driver.rte_dem"" full_name=""Rte_Dem"" brief="""" dependency="""" name=""Rte_Dem"" type=""utilities"" devices=""S32G233A S32G234M S32G254A S32G274A S32G274A_Rev2""> <source path=""Rte_TS_$(AR_RELEASE_ID)/include"" type=""c_include"" target_path=""RTD/include""> <files mask=""Rte_Dem_Type.h""/> </source> </component> or <component id=""platform.driver.rte_eth"" full_name=""Rte_Eth"" brief="""" dependency="""" name=""Rte_Eth"" type=""utilities"" devices=""S32G233A S32G234M S32G254A S32G274A S32G274A_Rev2""> <source path=""Rte_TS_$(AR_RELEASE_ID)/src"" type=""src"" target_path=""RTD/src""> <files mask=""SchM_Eth.c""/> </source> <source path=""Rte_TS_$(AR_RELEASE_ID)/include"" type=""c_include"" target_path=""RTD/include""> <files mask=""SchM_Eth.h""/> </source> </component> The new component will be added as dependency for the other components that need it: Example: <component id=""platform.driver.dem"" full_name=""Dem"" brief="""" dependency=""platform.driver.rte_dem"" name=""Dem"" type=""driver"" devices=""S32G233A S32G234M S32G254A S32G274A S32G274A_Rev2""> <source path=""Dem_TS_$(AR_RELEASE_ID)/src"" type=""src"" target_path=""RTD/src""> <files mask=""*.c""/> </source> <source path=""Dem_TS_$(AR_RELEASE_ID)/include"" type=""c_include"" target_path=""RTD/include""> <files mask=""*.h""/> </source> </component> "

ID	Subtype	Headline and Description
ARTD-1862	Bug	[SENT] Fix bugs on Sent_Init and Flexio_Sent_Ip_Init<*> Flexio_apChnlConfig should be pointer to pointer in Flexio_CtrlConfigType structure Flexio_aChnlUserConfig's elements which are generated from EB are not matched with Flexio_Sent_Ip_UserConfigType. Re-struct Flexio_Sent_Ip_StateType, flexioCommon (rename to chnlCfg) should be array of channel configuration (instead of array of pointer). Flexio_Sent_Ip.c: global variables have no address when were initialized.
ARTD-2022	Bug	[SENT] Fix algorithm to receive fast message<*> List of issues: Flexio_Sent_Ip_Configure: TRGSEL bit need to be written with 2*N (Pin N input). Flexio_Sent_Ip_GetFastMsgFromRaw: wrong algorithm to extract nibble value from the RAW value. Flexio_Sent_Ip_StartTransfer: update code to prevent reduce error of calculation. Flexio_Sent_Ip_GetFastChannelMsgData: TIMSTAT need to be cleared only when this flag was raised
ARTD-2052	New	New Feature [CAN][CPR_RTD_00513.can] Can_ListenOnlyMode API ,,"Feature for CAN Listen-Only Mode need to be implemented disabling/enabling Can_ListenOnlyMode API on EB Std_ReturnType Can_ListenOnlyMode(uint8 Controller, Can_ListenOnlyType State) API in driver code TC_ID: CAN_TC_FCT_*11550"
ARTD-2056	Bug	[SENT] Fix algorithm to receive serial message<*> List of bugs: # Missing Sent_GetSerialChannelMsgData and +Sent_GetSerialMsgData on HLD and IPW layer. # Flexio_Sent_Ip_ProcessSerialMsg+: Missing extract startbit from status&communication nibble:_ startbit = ((data->aNibbleVal[0] & 0x08) >> 3); # Flexio_Sent_Ip_GetSerialChannelMsgData+: Wrong condition to check serial message processing done Fast message state is not reset after fast message processing done. TIMSTAT bit need to be cleared only when this flag was raised.

ID	Subtype	Headline and Description
ARTD-2092	New	New Feature [crypto] Fix XDM violations ,,"Please refer to the attached ""xdm_violations.txt"" ([https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/General/Attachments/S32G%20RTD%204.4%200.9.0/ARTD-2088/xdm_violations.txt]) to identify the xdm lines that need to be updated. There are 3 types of violations: # Violation 1: Nodes that have constant false editable conditions (exception being the nodes under <Mdl>_ModuleDescription) Solution 1: <a:a name=""EDITABLE"" value=""false""/> will change to <a:a name=""READONLY"" value=""true""/> # Violation 2: Nodes which have READONLY attributes with XPath Solution 2: <a:da name=""READONLY"" type=""XPath"" expr=""..."" /> will change to <a:da name=""EDITABLE"" type=""XPath"" expr=""..."" /> # Violation 3: Reference nodes which use READONLY instead of EDITABLE Solution 3: Reference nodes (type=""REFERENCE"") with <a:a name=""READONLY"" ... />will change to <a:a name=""EDITABLE"" ... />"
ARTD-2100	New	New Feature [ocu] Fix XDM violations ,,"Please refer to the attached ""xdm_violations.txt"" ([https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/General/Attachments/S32G%20RTD%204.4%200.9.0/ARTD-2088/xdm_violations.txt]) to identify the xdm lines that need to be updated. There are 3 types of violations: # Violation 1: Nodes that have constant false editable conditions (exception being the nodes under <Mdl>_ModuleDescription) Solution 1: <a:a name=""EDITABLE"" value=""false""/> will change to <a:a name=""READONLY"" value=""true""/> # Violation 2: Nodes which have READONLY attributes with XPath Solution 2: <a:da name=""READONLY"" type=""XPath"" expr=""..."" /> will change to <a:da name=""EDITABLE"" type=""XPath"" expr=""..."" /> # Violation 3: Reference nodes which use READONLY instead of EDITABLE Solution 3: Reference nodes (type=""REFERENCE"") with <a:a name=""READONLY"" ... />will change to <a:a name=""EDITABLE"" ... />"
ARTD-2145	Bug	[SENT] IRQ Handler functions need to be combined due to FLEXIO has only 1 interrupt vector<*> With the current implementation, a SENT channel (Flexio timer) has a processing type (interrupt/polling/dma) individually. This is incompatible with FLEXIO hardware. A FLEXIO controller has only 1 interrupt vector for all inside timer channel*. It causes that Fast/Serial message need to handle in a IRQ handler function. So driver needs change: Configuration file: merge Fast/Serial processing type to Sent processing (_SentProcessing_) type and move from the channel to the controller. Configuration file: SentProcessing is enabled only when InterruptCombination is enabled. Used FLEXIO_Ctrl0_SentMessageIRQHandler for IRQ handler in combinedIRQ and SENT has only Combined IRQ type when IPV = FLEXIO.

ID	Subtype	Headline and Description
ARTD-2177	Bug	[MCU] Fix compiling errors on PMC activation<*> When the POWER component is added, some errors appear by default. !pwr_errors.png! Fixed by removing "_U32" from some lines of the PMC.c file. There is also a missing parenthesis in line #214, causing issues. Working PMC_PrepareLowPowerEntry looks like this. !pwr_solved.png!
ARTD-2178	Bug	[MCU] Fix inconsistent naming problems in MC_ME<*> There are some inconsistent naming between MC_ME.c and MC_ME.h files. Fixed by changing MC_ME_GetPreviousMode MC_ME_SocStandbyEntry MC_ME_CoreStandbyEntry To Power_Ip_MC_ME_GetPreviousMode Power_Ip_MC_ME_SocStandbyEntry Power_Ip_MC_ME_CoreStandbyEntry in the MC_ME.c driver file.
ARTD-2180	Bug	[MCU] Fix incorrect MC_ME register access<*> Incorrect access to the following MCME registers. pMC_ME->MODE_CONF pMC_ME->MODE_UPD Fixed as follows in MC_ME.c file !conf.png! !upd.png!
ARTD-2181	Bug	[MCU] Fix Main Core Select generation issue in CT<*> The selection of the Main Core in the ConfigTool is not reflected in the generated code. !ct.png! !maincore.png!
ARTD-2200	Bug	[SENT] Sent_Config is generated incorrectly in some cases of ECUC and VariantPostBuild<*> Sent_Config is generated with unexpectation in case: Driver is in Precompile with both of existing SENT EcucPartition References and no ECUC partition referenced in SENT. The issue comes from Sent_PBcfg.c: Name of some nodes variables (SentControllerConfig, SentEcucPartitionName,) is wrong.
ARTD-2211	New	New Feature [PORT] Implement the CPR_RTD_00026: Adding HIGH_Z direction for Port driver ,,"Internal Requirement: CPR_RTD_00026: ""The type Port_PinDirectionType shall be of enumeration type having range as PORT_PIN_IN, PORT_PIN_OUT, PORT_PIN_INOUT, PORT_PIN_HIGH_Z. (extension of SWS_Port_00220 AUTOSAR requirement)"" The HIGH_Z direction need to be added in Port driver"

ID	Subtype	Headline and Description
ARTD-2228	New	New Feature [PORT] Implement SIUL2_PORT_007_001, SIUL2_PORT_007_002: Add Siul2_Port_Ip_SetPinDirection API" ,,"SIUL2_PORT_007_001, SIUL2_PORT_007_002+_: "A function, named Siul2_Port_Ip_SetPinDirection shall configure the IBE and OBE according to the direction parameter."
ARTD-2242	New	New Feature [SENT] Implement CRC checking for Fast and Serial message ,,"Current driver supports CRC Recommended Implementation with 256 Element Array for Fast message only. Therefore, driver need to update following by SAEJ2716 For Fast Short message: add more LEGACY Implementation: The CRC checksum can be implemented as a series of shift left by 4 (multiply by 16) followed by a 256 array lookup. RECOMMENDED implementation with 6 Element Array: The CRC checksum can be implemented as a bit-wise exclusive OR with a 16 element array lookup. For Enhanced message: Add new function to check CRC. The CRC checksum can be implemented via a bit-wise exclusive OR with a 64 array lookup"
ARTD-2498	Bug	[gpt] Fix attached findings for generation with S32DS<*> For details see one note page [GPT|#section-id=\{353E5BC1-7280-46C5-B130-090DAA3A19F8}&end] ([Web view|https://nxp1-my.sharepoint.com/personal/viet_nguyen_nxp_com/_layouts/OneNote.aspx?id=%2Fpersonal%2Fviet_nguyen_nxp_com%2FDocuments%2FNotebooks%2FLIST_BUG_G6_TEST&wd=target%28GPT.one%7C353E5BC1-7280-46C5-B130-090DAA3A19F8%2F%29]) attached pictures Also align templates from UCT with templates from EBT
ARTD-2503	Bug	PORT: PortPinMode Error of PTC6&PTC7<*> when I input 70/71(means PTC6&PTC7) in "PortPin Mscr"(dynamic range), these two pins' "PortPin Mode" do not have I2C related item. The chip is S32K344.
ARTD-2567	New	New Feature [eth] How to handle Det files in DS+CT projects ,,"Det files need to be added in a DS+CT project when HLD components are used so the drivers can be compiled when the development errors detection is enabled. The Det stub already has a manifest associated to it, so each driver that needs Det for a successful build should add Det as a dependency in its manifest. Example from the Adc driver: <component id=""platform.driver.adc"" full_name=""Adc"" brief=""Adc Component"" dependency=""platform.driver.det"" name=""Adc"" type=""driver"" devices=""S32K314 S32K324 S32K344 S32G233A S32G234M S32G254A S32G274A S32G274A_Rev2""> <source path=""Adc_TS_$(AR_RELEASE_ID)/src"" type=""src"" target_path=""RTD/src""> <files mask=""*.c""/> <files mask=""Adc_Sar_Ip_HwAccess.h""/> </source> <source path=""Adc_TS_$(AR_RELEASE_ID)/include"" type=""c_include"" target_path=""RTD/include""> <files mask=""*.h""/> </source> </component> "

ID	Subtype	Headline and Description
ARTD-2594	Bug	[S32K344] OCU: CT Config files - remove magic numbers or hard-coded values<*> Do not use magic numbers or hard-coded values; use resource values or defines from platform header files as much as possible

ARTD-2623	Bug	[IP_Flexcan][FLEXCAN_IP_001_003] FlexCAN_Ip_SetBitrate should remain in original mode after timeout<*>
		
		eResult = FlexCAN_Ip_SetStopMode(u8Inst);
		EU_ASSERT(FLEXCAN_STATUS_SUCCESS == eResult);
		
		eResult = FlexCAN_Ip_SetBitrate(u8Inst, &bitrate, false);
		EU_ASSERT(FLEXCAN_STATUS_TIMEOUT == eResult);
		
		Verification point: EU_ASSERT(TRUE == FlexCAN_Ip_GetStopMode(u8Inst));
		> fail due to after timeout, FlexCAN_Ip_SetBitrate did not return to original mode (stop/ disabled mode).
		TC_ID: *Ip_FlexCAN_TC_FCT_1054
		A:
		!image-2020-10-19-16-55-24-980.png!
		=> this snippet code should be considered to be updated
		
		B: FlexCAN_EnterFreezeMode does not enter freeze mode if module is being in stop/ disabled mode (this is another issue)
		=> below code should be considered !image-2020-10-19-16-52-45-500.png!

ARTD-2662	Bug	[CRYPTO] Crypto_Example_002 S32DS project not working properly<*> The S32DS example project called Crypto_Example_002 provided within RTD EAR 0.8.0 patch 02 is not working as expected. Please see attached picture and next observations: The output cipher text is not the same as the expected cipher text. Variable u32NumFailedApiCalls is 2, while it should be 0. Issue can be seen using Lauterbach or P&E interface. If using P&E, just build the project with D_CACHE_ENABLE macro removed, due to current bug of P&E while reading static/global variables when data cache enabled.
ARTD-2771	Bug	[CAN] IMASK must not be cleared by FlexCAN_Ip_AbortTransfer()<*> Requirement SWS_Can_00426 says that: !image-2020-10-22-19-53-35-664.png! Although interrupts have been disabled by Can_DisableControllerInterrupts() previously, the driver code always disables MB interrupt (IMAKS) by function FlexCAN_Ip_AbortTransfer() in Can_SetControllerMode(CAN_CS_STOPPED) In

ID	Subtype	Headline and Description
ARTD-2781	Bug	[S32CC][RM] Abnormal switch from secure to nonsecure module when PID value is greater than 0x20<*> Sequence of test case: Initialize RM module Call Rm_XrdcSetProcessID function with PID value is 0x3F PID bit #5 should not be touched, as it will decide the module will use secure or non-secure mode, user should be prohibited from affecting this bit. XRDC_PID_FIELD_MASK has the value of 0x3F if the user use u8Pid with a value of 3F then the whole PID will be affected and set to 1, which is non-secure mode.
ARTD-2806	Bug	[OsIf] Change OsIf_Init(void) to OsIf_Init(void* Config) to be called with NULL_PTR<*> Add param to OsIf_Init, always validate as being NULL_PTR
ARTD-2829	Bug	[FLS] S32CC_4.4 BETA 0.9.0 Lack of DET report FLS_E_TIMEOUT in case Timeout Occur<*> #1. For Sync Mode of FLS: During verify Timeout report for Fls Job(s), , in case configured to make time out occur on Write/Erase/ Read/DLL Lock. it's lake of DET report FLS_E_TIMEOUT. #2. For Async Mode : Timeout report not implemented yet, for 2 nodes: FlsQspiAsyncWriteTimeout and FlsQspiAsyncEraseTimeout. #3. Read Job , in Qspi_Ip_Read: it's missing "break" in case STATUS_QSPI_TIME_OUT == status (see snap shot for detail)
ARTD-2906	New	New Feature [ocu] Verify and fix all the MemMap violations ,,"Problem*: Driver variables (and functions) placed in default linker sections (.data, .bss, .text, .rodata) instead of RTD specific ones (.mcal_data, .mcal_bss, .mcal_const). Impact*: Memory partitioning impact; for safety reasons the customer does not want the RTD specific data to bleed into default or other linker sections. Higher impact in Autosar applications. Why could this problem appear*: # No or inconsistent MemMap sections placed around all definitions and declarations* +. # Incorrect MemMap sections, which do not match the variable type, like: ## Initialized variable placed in NO_INIT section ## Modifyable variable placed in CONST section ## Const variable, config data, placed in VAR sections ## Zero Initilized variable, or unintialized variables placed in incorrect sections, see the attached picture. Solution: Build a test, check in the output .map file that all driver specific variables and functions are allocated in .mcal sections, not the default ones (.data, .bss, .rodata, .text) Fix all the inconsistencies. !image-2020-10-23-14-57-28-805.png!"

ID	Subtype	Headline and Description
ARTD-2943	Bug	[CAN] Can Automatic Time Segments can not work<*> A>* Enable Can Automatic Time Segments Calculation as below: !image-2020-10-27-11-41-17-880.png! generated code reflects that the computed bitrate segments are correct but is not located on Flexcan_aCtrlConfigPB_VS_0 => Can_Init() will use unexpected bitrate configuration. [detail in attached file] TC_ID: CAN_TC_FCT_*2880 B>* Bitrate warning is not correct. It only notify when bitrate segments > computed segments. Expectation: warning should be notified incase: bitrate segments != computed segments. C> Bitrate warning *does not notify error when CanControllerPrescallerAlternate is used (due clock is enabled) && Can Automatic Time Segments Calculation is enabled-> invalid computed birate still be generated
ARTD-2967	Bug	[S32CC][RM] XrdcMasterMode is missing 1xb - Use the bus master's secure/nonsecure attribute directly mode<*> RM(S32G2_RM_Rev2_DraftF) has stated that !image-2020-10-23-10-28-18-886.png|thumbnail! However, when i assign a core for both domains, an error occur !EB_RM.png|thumbnail! When use select XRDC_NONCORE_MASTER mode then XrdcMasterInstance, XrdcMasterPID, XrdcMasterPIDMask options should be hidden, because MDA_Wr_m_DFMT1 does not have PID bit and XrdcMasterMode is missing 1xb Use the bus master's secure/nonsecure attribute directly XrdcMasterMode is missing 1xb Use the bus master's secure/nonsecure attribute directly mode
ARTD-3018	New	New Feature [S32K344] OCU: Align '.component' to '.xdm' nodes with epd attributes stored ,,"Update .component file used for Design Studio CT AUTOSAR/nonAUTOSAR version with: align the nodes and tree structure with xdm file used in EB Tresos use same names; run the epd2ct executable to add option attributes to .component file procedure desribed in Chapter 9 in [link|https://teams.microsoft.com/l/file/C3F9B9A6-C039-4BA5-AFC3-FE18D8BB7208?tenantId=686ea1d3-bc2b-4c6f-a92c-d99c5c301635&fileType=pptx&objectUrl=https%3A%2F%2Fnxp1.sharepoint.com%2Fsites%2FZebra%2FShared%20Documents%2FConfiguration%20(code%2C%20DS%2C%20EB%2C%20etc)%2FNXP_RTD_AUTOSAR_UCT.pptx&baseUrl=https%3A%2F%2Fnxp1.sharepoint.com%2Fsites%2FZebra&serviceName=teams&threadId=19:e451c595d3ba410c8f9c1f5efc19a8a3@thread.tacv2&a4d2-ad54e86f727f] The updated .component will be used afterwards for epd / epc generation for import / export actions."

ID	Subtype	Headline and Description
ARTD-3026	Bug	[S32DS 3.3 Update1] Error when enable the flexcan_43 component<*> Steps: # Enable flexcan_43 component # Add a new item to the FlexCAN configurations array # Check the log file. There is an error related to some expressions that couldn't be resolved: !ENTRY com.nxp.swtools.common.utils.expression 4 0 2020-10-27 14:59:15.245 !MESSAGE [DATA] Error resolving: (($configSet.flexcanCfg.pe_clock_frequency.getValue() / ((($parent.flexcan_cfg_preDivider.getValue() 1) (((4 $parent.flexcan_cfg_propSeg.getValue()) $parent.flexcan_cfg_phaseSeg1.getValue()) $parent.flexcan_cfg_phaseSeg2.getValue())) (0r1000))) < 1001), Value of: $configSet.flexcanCfg.pe_clock_frequency not found !ENTRY com.nxp.swtools.common.utils.expression 4 0 2020-10-27 14:59:15.551 !MESSAGE [DATA] Error resolving: $parent.pattern.getValue().toString().formatMessage(($configSet.flexcanCfg.pe_clock_frequency.getV ((($parent.flexcan_cfg_preDivider.getValue() 1) (((4 $parent.flexcan_cfg_propSeg.getValue()) $parent.flexcan_cfg_phaseSeg1.getValue()) $parent.flexcan_cfg_phaseSeg2.getValue())) (0r1000)))), Value of: $configSet.flexcanCfg.pe_clock_frequency not found!ENTRY com.nxp.swtools.common.utils.expression 4 0 2020-10-27 14:59:15.558 !MESSAGE [DATA] Error resolving: $parent.pattern.getValue().toString().formatMessage(($configSet.flexcanCfg.pe_clock_frequency.getV ((($parent.flexcan_cfg_preDivider.getValue() 1) (((3 $parent.flexcan_cfg_propSeg.getValue()) $parent.flexcan_cfg_phaseSeg1.getValue()) $parent.flexcan_cfg_phaseSeg2.getValue())) (0r1000)))), Value of: $configSet.flexcanCfg.pe_clock_frequency not found
ARTD-3049	Bug	[SENT] Flexio_Sent_Ip_GetSerialMsgData missed serial message on multiple of channel<*> When the number of channel which received serial message continuously is upper than 2 channels, Flexio_Sent_Ip_GetSerialMsgData always missed serial message on later channels. The issue comes from serial message handling on channels in sequentially.* In-while processing of the first channel, the sencond channel is in idle state, compare register of the timer can not update the timer value from SENT signal. This one causes missing serial message on the second channel. To solve this issue, I propose another way to handle serial message: Using interrupt of timer to trigger saving timer value to a virtual buffer on every channel (global variable: g_flexioTimerBuffer). Flexio_Sent_Ip_GetSerialMsgDaata calls enable/disable timer interrupt to use interrupt. the algorithm of serial message will apply on g_flexioTimerBuffer, instead of timer register as present driver.

ID	Subtype	Headline and Description

ARTD-3073	New	New Feature
		
		[Crypto] Handling timeout implementation using OsIf
		,,"Add a referenceable enum in Tresos for OsIf that can be used by other drivers to allow selection only of available osif counter types
		
		In each module configuration that needs to implement a timeout add the following field
		<v:var name=""<Module>TimeoutMethod"" type=""ENUMERATION"">
		<a:a name=""LABEL"" value=""<Module> Timeout Method""/>
		<a:a name=""DESC"">
		<a:v>
		<![CDATA[EN:
		<html>
		 <Module>TimeoutMethod
		 Configures the timeout method.
		 Based on this selection a certain timeout method from OsIf will be used in the driver.
		 Note: If SystemTimer or CustomTimer are selected make sure the corresponding timer is enabled in OsIf General configuration.
		Note: Implementation Specific Parameter.
		</html>
		]]>
		</a:v>
		</a:a>
		<a:a name=""IMPLEMENTATIONCONFIGCLASS""
		type=""IMPLEMENTATIONCONFIGCLASS"">
		<icc:v vclass=""PreCompile"">VariantPreCompile</icc:v>
		<icc:v vclass=""PostBuild"">VariantPreCompile</icc:v>
		</a:a>
		<a:a name=""ORIGIN"" value=""M4_XDM_AR_MODULE_ORIGIN""/>
		<a:a name=""SCOPE"" value=""LOCAL""/>
		<a:a name=""SYMBOLICNAMEVALUE"" value=""false""/>
		<a:a name=""UUID"" value=""ECUC:7228a335-4003-4639-8e1a-bb3d9f762a7b""/>
		<a:a name=""DEFAULT"" value=""DummyTimer""/>
		<a:da name=""INVALID"" type=""XPath"">
		<a:tst expr=""node:refs('ASPathDataOfSchema:/M4_XDM_AR_PKG_NAME/Base/OsIfGeneral/OsIfUseCustomTimer') = 'false' and node:fallback(.,'DummyTimer') = 'CustomTimer'"" true=""Custom Timer is not enabled in OsIf (OsIfGeneral/OsIfUseCustomTimer checkbox)""/>
		<a:tst expr=""node:refs('ASPathDataOfSchema:/M4_XDM_AR_PKG_NAME/Base/OsIfGeneral/OsIfUseSystemTimer') = 'false' and node:fallback(.,'DummyTimer') = 'SystemTimer'"" true=""System Timer is not enabled in OsIf (OsIfGeneral/OsIfUseSystemTimer checkbox)""/>
		</a:da>
		<a:da name=""RANGE"">
		<a:v>DummyTimer</a:v>
		<a:v>SystemTimer</a:v>
		<a:v>CustomTimer</a:v>
		</a:da>
		</v:var>
		Based on its configuration generate an enum field of the type OsIf_CounterType (which is defined in OsIf.h and described below)
		// This is defined in OsIf.h
		typedef enum
		{
		OSIF_COUNTER_DUMMY, /**< dummy counter /
		#if (OSIF_USE_SYSTEM_TIMER == STD_ON)
		OSIF_COUNTER_SYSTEM, /**< system counter /
		#endif / (OSIF_USE_SYSTEM_TIMER == STD_ON) /
		#if (OSIF_USE_CUSTOM_TIMER == STD_ON)
		OSIF_COUNTER_CUSTOM /**< custom counter /
		#endif / (OSIF_USE_CUSTOM_TIMER == STD_ON) /
		} OsIf_CounterType;
		Use the generated value of the type described above to use the OsIf APIs for

ID	Subtype	Headline and Description
ARTD-3091	Bug	[IP_FLEXCAN][FLEXCAN_IP_002_002] FlexCAN_Ip_SetBitrateCbt should return error in case disabled fd<*> TC_ID: *Ip_FlexCAN*_TC_FCT_*2063 init flexcan with disabled FD call FlexCAN_Ip_SetBitrateCbt > verification point: FlexCAN_Ip_SetBitrateCbt should return FLEXCAN_STATUS_ERROR => fail due to wrong condition expression: !image-2020-10-29-11-25-46-191.png! Additional: the call of FlexCAN_Ip_SetBitrateCbt on HLD should be updated also after above issue is fixed
ARTD-3092	Bug	[S32G274] OCU: remove all tabulators in source files<*> remove all tab characters in all file, follow the table below: *File*||*Hits Ftm_Ocu_Ip.c|774 Ftm_Ocu_Ip_Irq.c|69 Ocu.c|49 Ftm_Ocu_Ip_PBcfg.c|48 Ocu_PBcfg.c|40 Ftm_Ocu_Ip_Types.h|28 Ftm_Ocu_Ip_PBcfg.h|12 Ocu_Ipw_PBcfg.h|12 Ocu_Cfg.h|12 !image-2020-10-29-11-28-33-300.png!

ID	Subtype	Headline and Description

ARTD-3101	Bug	[LIN] LIN cannot transmit and receive frame correctly<*>
		
		Description:
		1.The current LinDriver cannot send frame with PID higher than 0x3F. The correct behavior should be LinDriver cannot send frame with ID higher than 0x3F.
		LIN driver need check invalid ID instead of PID and call Lpuart_Lin_Ip_MasterSendHeader() with parameter is ID (Lin_Ipw_SendResponse() and Lin_Ipw_SendHeader() in Lin_Ipw.c).
		2.The current LinDriver cannot return the correct recived data from frame via Lin_GetStatus() function if driver doesn't use LPUART0
		In Lin_Ipw_HardwareGetStatus() the code should be:
		
		for (u8Indx = 0U; u8Indx < Lin_Ipw_eCurrentDataLength[u8Channel]; u8Indx++)
		Instead of:
		for (u8Indx = 0U; u8Indx < Lin_Ipw_eCurrentDataLength[u8HwUnit]; u8Indx++)
		3. the function Lin_GetStatus() does not return LIN_RX_ERROR or LIN_TX_ERROR if framing error happens in bus
		In Lin_Ipw_HardwareGetStatus() the code should be:
		/ Frame error in transmission occured /
		else if ((LIN_FRAMING_ERROR == u8FrameError) &&
		(LIN_TX_MASTER_RES_COMMAND == u8TransmitHeaderCommand))
		{
		u8ReturnStatus = LIN_TX_ERROR;
		}
		/ Frame error in reception occured /
		else if ((LIN_FRAMING_ERROR == u8FrameError) &&
		(LIN_TX_SLAVE_RES_COMMAND == u8TransmitHeaderCommand))
		instead of:
		/ Frame error in transmission occured /
		else if ((LIN_FRAME_ERROR == u8FrameError) &&
		(LIN_TX_MASTER_RES_COMMAND == u8TransmitHeaderCommand))
		{
		u8ReturnStatus = LIN_TX_ERROR;
		}
		/ Frame error in reception occured /
		else if ((LIN_FRAME_ERROR == u8FrameError) &&
		(LIN_TX_SLAVE_RES_COMMAND == u8TransmitHeaderCommand))
		4. Driver cannot send frame which has ID 0x3F in bus.
		In Lin_Ipw_SendHeader() and Lin_Ipw_SendResponse() the checking code should be:
		0x3FU >= id
		Instead of:
		0x3FU > id
		
		Proposal solution:
		Please see attached file for more information.

ARTD-3480	New	New Feature [ETH]Fix trace ability warning ,,In trace ability report contains some warning uncovered.

ID	Subtype	Headline and Description
ARTD-3484	Bug	[SENT] Missing serial message in interrupt mode<*> 1. Interrupt mode, serial message missed. The problem comes from Flexio_Sent_Ip_IRQ_Dispatch implementation: interrupt enable and interrupt flags in for loop; timer value and clear interrupt are in Flexio_Sent_Ip_IRQHandler function > decrease speed of interrupt handler Solution: Read all interrupt flag at the same time (read TIMSTAT register). Read timer value and clear interrupt flag in Flexio_Sent_Ip_IRQ_Dispatch. 2. Remove hardcode for tick time value, and get this value from user configuration. 3. Improve *Flexio_Sent_Ip_IRQHandler:* Remove some serial message checking, the current code make serial message missed in some special case. 4. Fix spurious interrupt. 5. Implement returning fast message data when call Flexio_Sent_Ip_GetSerialMsgData, Flexio_Sent_Ip_GetSerialChannelMsgData 6. Fix CRC calculating for SENT_RECOMMENDED_IMPLEMENTATION_256_ELEMENT
ARTD-3486	New	New Feature [S32K3XX] update multicore int monitor in EB ,,"Update multicore, porting from S32CC"
ARTD-3490	New	New Feature [ETH]Fix cyclomatic complexity > 20 ,,The function Eth_MainFunction has cyclomatic complexity > 20.
ARTD-3500	Bug	[Ip_Flexcan][S32_DS] Can not choose flexcan channel in case of more than one Instances<*> Create new project Add first flexcan configuration, refer to FLEXCAN_*0*, input maxmb value is 95 Add second flexcan configuration, refer it to FLEXCAN_*1 > at this step error happen at *first flexcan configuration because it refer to FLEXCAN_*1* also Expected behavior: the implementation should be done as the HLD's one, so we can map each configuration to expected Flexcan channel. I set high priority for this task since DS update will impact much to testing activities this release.

ID	Subtype	Headline and Description
ARTD-3520	Bug	[CAN][EB] CanMainFunctionRWPeriodRef should be enabled in case of CanHardwareObjectUsesPolling/Mix<*> Two issues should be analysed A> Add Can Choose Tx/Rx Processing Type: MIXED Add one Tx or Rx hardware object Enable CanHardwareObjectUses*Polling* => CanMainFunctionRWPeriodRef need to be notified to be selected. (should have same behavior as case of Tx/Rx Processing Type is POLL*) B>* **Look at desciption of CanHwFilterMask: !image-2020-11-02-15-06-46-919.png! The highlight description (and related srs ids) is no longer applied with current implementation: CanFilterMaskRef is not be implemented now => users always need to configure mask with BASIC CanHandleType => FULL value of CanHandleType is not supported (have no meaning) anymore => the description should be updated.
ARTD-3522	Bug	[IP_Flexcan] FDCTRL_FDRATE should not be enabled by FlexCAN_Ip_Send<*> Init Flexcan with Config.bitRateSwitch = FALSE FlexCAN_Ip_Send with tx_info.enable_brs = TRUE => brs request should be ignored in this case, normal frames should be sent, because FDCTRL_FDRATE config is on Flexcan_Init now, and FlexCAN_Ip_Send should not change module configuration by itself (additionally, this cause an extra/redundant access exclusive area each time call FlexCAN_Ip_Send !) !image-2020-11-02-15-26-15-570.png! => Flexcan_send should control BRS bit in Tx Mb, instead of controlling FDRATE bit in FDCTRL Expectation: remove below code: !image-2020-11-02-15-28-47-513.png! Additionally*: Please add below typical development error detect for FlexCAN_Ip_Init_Privileged DEV_ASSERT(instance < CAN_INSTANCE_COUNT); DEV_ASSERT(state != NULL); DEV_ASSERT(*g_flexcanStatePtr[instance] == NULL); (re-init without de-init) TC_ID: *Ip_*FlexCAN_TC_FCT*_2060
ARTD-3564	Bug	[S32G][ETH] Fix conmpiler warning<*> Fix conmpiler warning

ID	Subtype	Headline and Description
ARTD-3579	Bug	[IP_Flexcan][FLEXCAN_IP_005_001] FlexCAN_Ip_SetRxFifoGlobalMask now set literal user's mask<*> A> FLEXCAN_IP_005_001: A function called FlexCAN_Ip_SetRxFifoGlobalMask shall Set Rx FIFO global mask as the 11-bit standard mask or the 29-bit extended mask*. > This description is no longer applied in Zebra due to the implementation was changed (see attached file) Expectation: update description in header file and requirement (should be similar as the description FlexCAN_Ip_SetRxIndividualMask) B>* For now: FlexCAN_Ip_Set*RxMb*GlobalMask: Set Rx Message Buffer global mask as the 11-bit standard mask or the 29-bit extended mask (calculated mask) FlexCAN_Ip_Set*RxFifo*GlobalMask: Sets FlexCAN Rx FIFO literal mask FlexCAN_Ip_Set*RxIndividual*Mask: Sets FlexCAN Rx individual literal mask FlexCAN_Ip_Set*RxIndividual*MaskCalc: Sets FlexCAN Rx individual calculated mask* => please see how the names of APIs can lead to confuses. and currently, Set*RxMb*GlobalMask is supported as calculated mask Set*RxFifo*GlobalMask is not supported as calculated mask! Expectation*: need to analysis and finalize the clear API showcase that will come to users
ARTD-3585	Bug	[S32K3]SIUL2 Config Tool PORT defines mismatch RTD Siul2_Dio_Ip_Cfg.h<*> Config Tool defines for the user pin and port configurations macros to be used further in the application development. However, the macro value for each PORT differs from the ones defined in RTD. For example, RTD defines port as PTB_H_HALF and PTB_L_HALB while the Config tools generates output port as simply PTB. Siul2_Port_Ip_Cfg.h #define RGBLED0_RED_PIN 13u #define RGBLED0_RED_PORT PTB Siul2_Dio_Ip_Cfg.h #define PTA_L_HALF ((GPIO_Type)(&(SIUL2->PGPDO0))) #define PTA_H_HALF ((GPIO_Type)(&(SIUL2->PGPDO1))) #define PTB_L_HALF ((GPIO_Type)(&(SIUL2->PGPDO2))) #define PTB_H_HALF ((GPIO_Type)(&(SIUL2->PGPDO3))) !image-2020-11-03-13-23-39-737.png!!image-2020-11-03-13-24-05-011.png!

ID	Subtype	Headline and Description
ARTD-3674	Bug	[SENT] Build fail relate to name of sent controller object's pointer structure in case variant_no > 1<*> In case varian_no > 1, SENT gets this error in build step: In file included from ../../../output/S32K3XX_S32K344/sent/Sent_TS_001_cfgPB/generate/src/Sent_VS_1_PBcfg.c:90: ../../../output/S32K3XX_S32K344/sent/Sent_TS_001_cfgPB/generate/include/Sent_Ipw_Cfg.h:98:5: error: unknown type name 'SENT_IPW_CONFIG_VS_1_PB'; did you mean 'SENT_IPW_CONFIG_VS_0_PB'? 98 SENT_IPW_CONFIG_VS_1_PB \ Solution: Need to change name of controller pointer structure following by postBuildVariant. Flexio_aCtrlConfig > Flexio_aCtrlConfigPB[!IF "var:defined('postBuildVariant')"!]_[!"$postBuildVariant"!][!ENDIF!] Sent_Ipw_aCtrlConfig > Sent_Ipw_aCtrlConfigPB[!IF "var:defined('postBuildVariant')"!]_[!"$postBuildVariant"!][!ENDIF!]
ARTD-3678	New	New Feature [SPI] Support FlexIO ,,Support FlexIO
ARTD-3691	New	New Feature [SENT] Update resource for SENT driver ,,"Update resource names. Sent_s32k314_mapbga257 Sent_s32k314_mqfp100 Sent_s32k314_mqfp172 Sent_s32k324_mapbga257 Sent_s32k324_mqfp172 Sent_s32k344_mapbga257 Sent_s32k344_mqfp172 Update resource content: Sent.SentConfigSet.SentControllerConfig:1 Sent.SentConfigSet.SupvAvailable:STD_ON Sent.SentConfigSet.SentHwUnderRegProtList:SENT_FLEXIO_0 Sent.SentConfigSet.SentControllerConfig.SentChannelConfig:8 Sent.SentConfigSet.SentControllerConfig.SentHwController:FLEXIO_0 Sent.SentConfigSet.SentControllerConfig.SentHwChannel:CHANNEL_0,CHANNEL_1,CHANNEL_2, Sent.SentConfigSet.SentControllerConfig.SentPinID:PIN_0,PIN_1,PIN_2,PIN_3,PIN_4,PIN_5,PIN_6,
ARTD-3704	New	New Feature [I2C][S32K3XX] Add SlaveListening function for K3 ,,SlaveListening functions should be available for S32K3XX platform.

ID	Subtype	Headline and Description
ARTD-3782	Bug	[build_env] The interrupt vector table can be overwriten when there is a variable define in no-cacheable section<*> !image-2020-11-09-13-30-28-402.png! As in the highlight picture, the size of .intc_vector_ram will be zero so it's address will be same as starting address of .mcal_data_no_cacheable. Currently the issue occur on gcc, please also check with iar.
ARTD-3790	Bug	[FEE]: Some variables are placed in different sections<*> Fee_ClrGrps and Fee_BlockConfig are placed in different section in generated files: are placed in FEE_START_SEC_CONFIG_DATA_UNSPECIFIED in Fee_Cfg.c in FEE_START_SEC_CONST_UNSPECIFIED in Fee_Cfg.h
ARTD-3819	New	New Feature [FLS][S32K3XX-4.4] Update Test List ,,Fls Update Test list
ARTD-3822	Bug	[MCU] There are no warnings/errors when system clock doesn't have the correct ratios<*> There are no warnings/errors when system clock is not respect follow ratio (the same issue for CORE and HSE clocks) !image-2020-11-10-14-30-24-471.png|width=689,height=456!
ARTD-3843	New	New Feature [PORT] Add support for USER MODE for S32K3 BETA 0.9.0 ,,Add support for USER MODE for S32K3 BETA 0.9.0. Refer the implementation from S32XX platform
ARTD-3897	Bug	[SENT][S32K344 BETA] The first FAST message which received from MAF always missed<*> The issue is that: The first SENT message which received from MAF always missed when the ticktime 10us and the FLEXIO's freq = 80Mhz. The root cause: The time counter start as soon as SENT initialized, this one causes the Time Compare gets a random value when detect a falling edge from MAF (calibration pulse). If this Time Compare value = SYNC_CAL_TICK 25% (this occurs when ticktime 10us and the FLEXIO's freq = 80Mhz in my test), the second Time Compare value (time for calibration pulse) will be rejected and it will be ignore the first Fast message and it mean the first Serial message will be missed also. Solution: To prevent this issue, the time counter must start only when detect a falling edge. It means TIMENA = 0x7 (Timer enabled on Trigger rising or falling edge) when configure TIMCFG register

ID	Subtype	Headline and Description
ARTD-3898	Bug	[ETH] Build failed related to names of interrupts<*> The name of interrupt should be changed to EMAC in stead of ENET
ARTD-3906	New	New Feature [FLS] Update eec feature for internal flash ,,Update ecc feature for internal flash
ARTD-3923	Bug	[S32K344][ADC] Wrong index range of list and can not select ADC channel for LIST conversion mode<*> Detailed description (how to reproduce it): Wrong index range of list and can not select ADC channel for LIST conversion mode. List Index range: 0-31 but config in EB 0-23. Details are in the attached file. Preconditions: Config ADC in BCTU mode. Select trigger conversion mode is LIST Can not select ADC channel. Observed behavior: Wrong index range of list and can not select ADC channel for LIST conversion mode. Expected behavior: Incorrect index range of list (0-31) and can select ADC channel for LIST conversion mode. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-3927	Bug	[SENT][S32K344 BETA] Fix build fail on GHS compiler<*> Fix all build fails on GHS compiler

ID	Subtype	Headline and Description
ARTD-3929	Bug	[S32K3XX] ADC: Adc_SetChannel calling before Adc_Init cause hard fault error<*> Detailed description (how to reproduce it): Adc_SetChannel calling before Adc_Init cause hard fault error (Adc_GroupType GroupIndex = Adc_pCfgPtr[u32CoreId]- >pGroupIdToIndexMap[Group]; out of checking StatusChecks == E_OK) Preconditions: Adc_SetChannel is enable Compiler IAR Test Case ID (internal TC that caught the defect) optional: Adc_TC_FCT_1103 Observed behavior: / Call the Adc_SetChannel before initial driver / Adc_SetChannel(t_u16AdcGroupType, t_g_pAdcChannel[t_u16AdcGroupType], T_ADC_MAX_CHANNEL_COUNT); / [CPR_RTD_00329.adc] Verification point: Det error ADC_E_UNINIT / EU_ASSERT_FATAL(Det_TestLastReportError(ADC_MODULE_ID, 0U, ADC_SETCHANNEL_ID, ADC_E_UNINIT)); > cause hard fault errors Expected behavior: Hard fault does not occur Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-3944	Bug	[SENT] Sent_Init gets build fail in case precompile+nopartition+variantno>1<*> Condition: Precompile No partition Variant no >=1 Issue: "e:/gitwork/Zerba/S32K3XX_4.4_noSASW/output/S32K3XX_S32K344_ghs/sent/../../ eclipse/plugins/Sent_TS_T40D34M8I1R0/src/CDD_Sent.c", line 293: error #142: expression must have pointer-to-object type if (NULL_PTR == Sent_Config[u32CoreId]) Root cause: In the mention case, the configuration variable is +const Sent_ConfigType Sent_Config +, so need to update Sent_Init function: +Sent_pConfig[u32CoreId] = pConfig;
ARTD-3945	Bug	[ETH] Multicast packages reception doesn't works<*> Controller doesn't work at multicast filtering modes

ID	Subtype	Headline and Description
ARTD-3953	Bug	[S32K344][ADC-BCTU] Faulty reading from FIFO result when using function Adc_CtuReadFifoResult() to read<*> Detailed description (how to reproduce it): Faulty reading from FIFO result when using function Adc_CtuReadFifoResult() to read. Step check: Step1: Config ADC in BCTU mode. With data conversions are saved in FIFO. Step2: Call Adc_CtuReadFifoResult(), read FIFO result. Step3: the reading result is false. Incorrect channel index. Preconditions: Follow the steps above. Observed behavior: Faulty reading from FIFO result when using function Adc_CtuReadFifoResult() to read. Expected behavior: Correct reading from FIFO result when using function Adc_CtuReadFifoResult() to read. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-3982	Bug	[RTD_S32K344][PORT] no prototype of Siul2_Port_Ip_SetUserAccessAllowed<*> build fail at IAR compiler, error log: no prototype of Siul2_Port_Ip_SetUserAccessAllowed
ARTD-3998	Bug	[eth] Update the used schema for all the .component files to 8.0 version<*> The used version for the component file from the header should be updated to 8.0 to be compatible with the S32CT framework version. If it is not updated, when the .component validation is done, will fail and the component file will not be loaded with success. xsi:schemaLocation="http://swtools.freescale.net/XSD/component/1.0 http://swtools.freescale.net/XSD/component/1.0/component.xsd" should be updated to: xsi:schemaLocation="http://swtools.freescale.net/XSD/component/1.0 http://swtools.freescale.net/XSD/component/1.0/component-8.0.xsd"
ARTD-4002	Bug	[spi] Update the used schema for all the .component files to 8.0 version<*> The used version for the component file from the header should be updated to 8.0 to be compatible with the S32CT framework version. If it is not updated, when the .component validation is done, will fail and the component file will not be loaded with success. xsi:schemaLocation="http://swtools.freescale.net/XSD/component/1.0 http://swtools.freescale.net/XSD/component/1.0/component.xsd" should be updated to: xsi:schemaLocation="http://swtools.freescale.net/XSD/component/1.0 http://swtools.freescale.net/XSD/component/1.0/component-8.0.xsd"
ARTD-4032	New	New Feature [S32K3XX] update list test ,,Update list test

ID	Subtype	Headline and Description
ARTD-4049	New	New Feature [SPI] Remove instance parameter of spi_Ip_Init, spi_Ip_SyncTransmit and spi_Ip_AsyncTransmit" ,,"Currently, some functions are declared as below: Lpspi_Ip_StatusType Lpspi_Ip_Init(uint32 instance, const Lpspi_Ip_ConfigType Configuration); Lpspi_Ip_StatusType Lpspi_Ip_SyncTransmit(uint32 instance, const Lpspi_Ip_ExternalDeviceType externalDevice, void txBuffer, void rxBuffer, uint16 numberOfFrames, uint32 timeout); Lpspi_Ip_StatusType Lpspi_Ip_AsyncTransmit(uint32 instance, const Lpspi_Ip_ExternalDeviceType externalDevice, void txBuffer, void rxBuffer, uint16 numberOfFrames, Lpspi_Ip_CallbackType callback); Each instance is allocated by SpiPhyUnitMapping node on configuration tools (EB or CT) for each SpiPhyUnit. And each external device configuration is also allocated to each SpiPhyUnit. So, to avoid confusing for choise wrong instance corresponds with SpiPhyUnit and External Device configuration: instance can be stored in structures Lpspi_Ip_ConfigType and Lpspi_Ip_ExternalDeviceType. So, instance parameter can be removed. To easy for remember structure name for each configuration. Structure name is generated by configuration tools should be added infix <Configuration Name of each configuration on EB or CT> like: const Lpspi_Ip_ConfigType Lpspi_Ip_PhyUnitConfig_<Name of Config>_<Variant name> const Lpspi_Ip_ExternalDeviceType Lpspi_Ip_DeviceAttributes_<Name of Config>_<Variant name>
ARTD-4053	New	New Feature [ETH] Workaround relative to LDRA's issue ,,"for checking define have multiple sub expressions, these sub expression always checked parawell. This lead to build failed if the first or second sub expression not defined. ex: #if ((STD_ON == GMAC_ENABLE_USER_MODE_SUPPORT) && defined(MCAL_GMAC_REG_PROT_AVAILABLE) && (STD_ON == MCAL_GMAC_REG_PROT_AVAILABLE)) will build failed if MCAL_GMAC_REG_PROT_AVAILABLE has not defined yet."
ARTD-4367	New	New Feature [ETH]Fix build failed on CT

5 Legal information

5.1 Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

5.2 Disclaimers

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Suitability for use in automotive applications — This NXP product has been qualified for use in automotive applications. If this product is used by customer in the development of, or for incorporation into, products or services (a) used in safety critical applications or (b) in which failure could lead to death, personal injury, or severe physical or environmental damage (such products and services hereinafter referred to as "Critical Applications"), then customer makes the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, safety, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP. As such, customer assumes all risk related to use of any products in Critical Applications and NXP and its suppliers shall not be liable for any such use by customer. Accordingly, customer will indemnify and hold NXP harmless from any claims, liabilities, damages and associated costs and expenses (including attorneys' fees) that NXP may incur related to customer's incorporation of any product in a Critical Application.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

5.3 Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 31 March 2023