1. Description

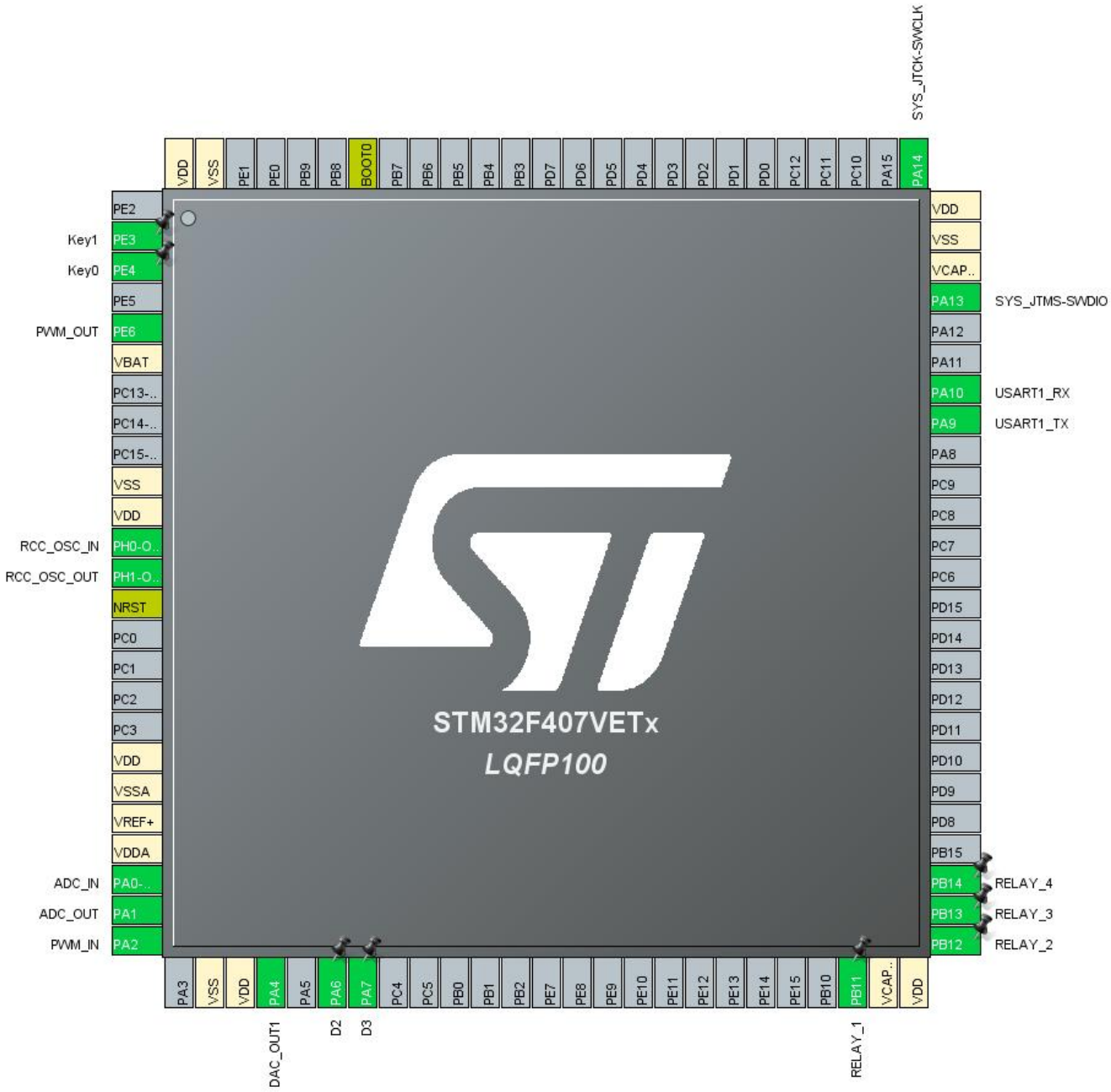
1.1. Project

Project Name	D_GuoSai2019VE
Board Name	custom
Generated with:	STM32CubeMX 5.3.0
Date	08/10/2019

1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F407/417
MCU name	STM32F407VETx
MCU Package	LQFP100
MCU Pin number	100

2. Pinout Configuration



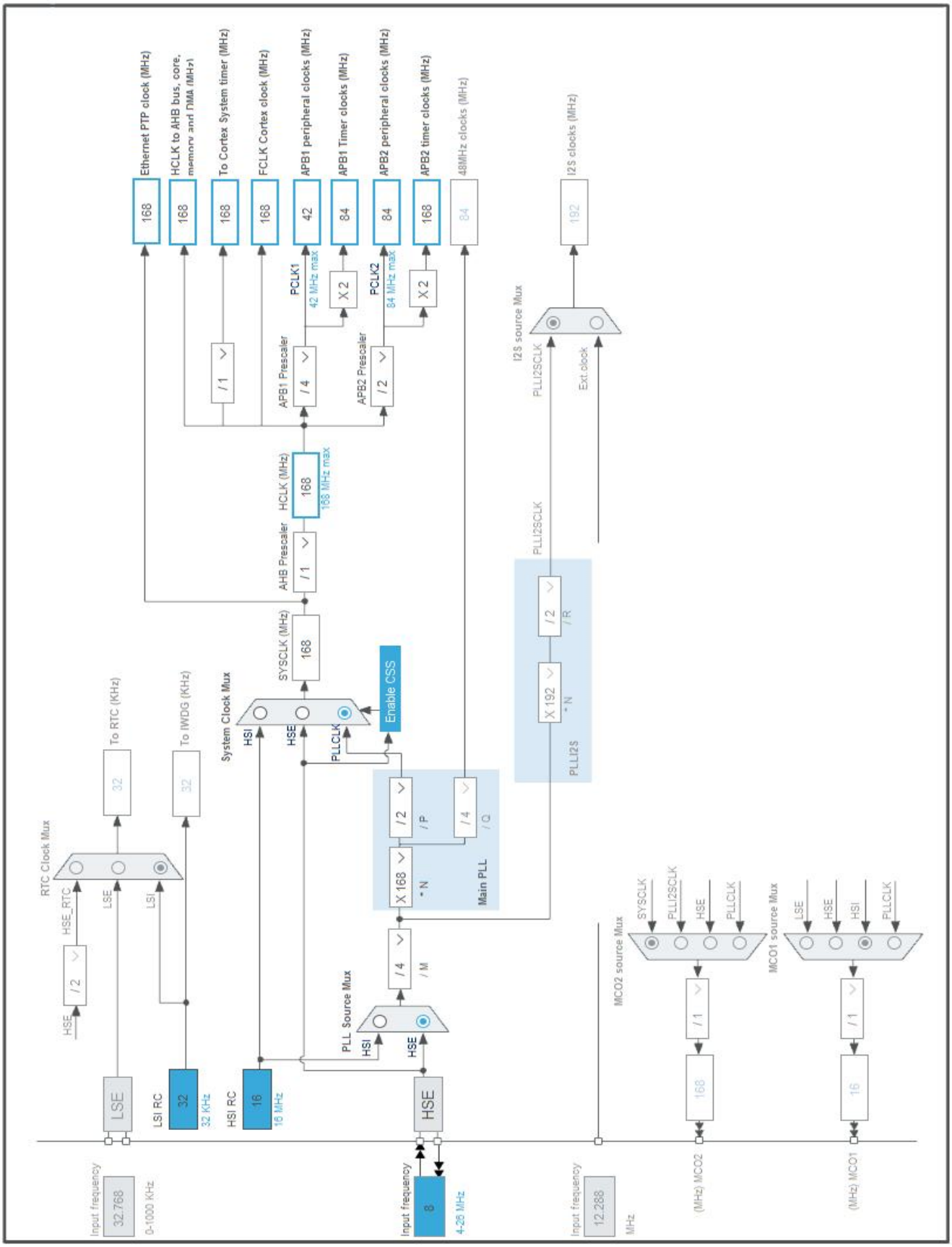
3. Pins Configuration

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
2	PE3 *	I/O	GPIO_Input	Key1
3	PE4 *	I/O	GPIO_Input	Key0
5	PE6	I/O	TIM9_CH2	PWM_OUT
6	VBAT	Power		
10	VSS	Power		
11	VDD	Power		
12	PH0-OSC_IN	I/O	RCC_OSC_IN	
13	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
14	NRST	Reset		
19	VDD	Power		
20	VSSA	Power		
21	VREF+	Power		
22	VDDA	Power		
23	PA0-WKUP	I/O	ADC1_IN0	ADC_IN
24	PA1	I/O	ADC2_IN1	ADC_OUT
25	PA2	I/O	TIM5_CH3	PWM_IN
27	VSS	Power		
28	VDD	Power		
29	PA4	I/O	DAC_OUT1	
31	PA6 *	I/O	GPIO_Output	D2
32	PA7 *	I/O	GPIO_Output	D3
48	PB11 *	I/O	GPIO_Output	RELAY_1
49	VCAP_1	Power		
50	VDD	Power		
51	PB12 *	I/O	GPIO_Output	RELAY_2
52	PB13 *	I/O	GPIO_Output	RELAY_3
53	PB14 *	I/O	GPIO_Output	RELAY_4
68	PA9	I/O	USART1_TX	
69	PA10	I/O	USART1_RX	
72	PA13	I/O	SYS_JTMS-SWDIO	
73	VCAP_2	Power		
74	VSS	Power		
75	VDD	Power		
76	PA14	I/O	SYS_JTCK-SWCLK	
94	BOOT0	Boot		
99	VSS	Power		

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
100	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	D_GuoSai2019VE
Project Folder	E:\MCU\stm32\STM32F407\D_GuoSai2019VE
Toolchain / IDE	MDK-ARM V5
Firmware Package Name and Version	STM32Cube FW_F4 V1.24.1

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	Yes

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F4
Line	STM32F407/417
MCU	STM32F407VETx
Datasheet	022152_Rev8

6.2. Parameter Selection

Temperature	25
Vdd	3.3

7. IPs and Middleware Configuration

7.1. ADC1

mode: IN0

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	**Enabled ***
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	**Enabled ***
Number Of Discontinuous Conversions	1
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	**EOC flag at the end of all conversions ***

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	**Timer 3 Trigger Out event ***
External Trigger Conversion Edge	Trigger detection on the rising edge
Rank	1
Channel	Channel 0
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

7.2. ADC2

mode: IN1

7.2.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	**Enabled ***
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	**Enabled ***
Number Of Discontinuous Conversions	1
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	**Timer 3 Trigger Out event ***
External Trigger Conversion Edge	Trigger detection on the rising edge
Rank	1
Channel	Channel 1
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

7.3. DAC

mode: OUT1 Configuration

7.3.1. Parameter Settings:

DAC Out1 Settings:

Output Buffer	**Disable ***
Trigger	**Timer 4 Trigger Out event ***
Wave generation mode	Disabled

7.4. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.4.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3

Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulatror Voltage Scale	Power Regulator Voltage Scale 1

7.5. SYS

Debug: Serial Wire

Timebase Source: SysTick

7.6. TIM3

Slave Mode: Trigger Mode

Trigger Source: ITR3

Channel1: PWM Generation No Output

7.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**4096 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable
Slave Mode Controller	Trigger Mode

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	**Enable (Trigger delayed for master/slaves simultaneous start) ***
Trigger Event Selection	**Update Event ***

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

7.7. TIM4

Clock Source : Internal Clock

7.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**11 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	**Update Event ***

7.8. TIM5

Channel3: Input Capture direct mode

7.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**84000000-1 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Input Capture Channel 3:

Polarity Selection	**Both Edges ***
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	**4 ***

7.9. TIM9

Channel2: PWM Generation CH2

7.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**168-1 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**2-1 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	**1 ***
Fast Mode	Disable
CH Polarity	High

7.10. USART1

Mode: Asynchronous

7.10.1. Parameter Settings:

Basic Parameters:

Baud Rate	**921600 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0-WKUP	ADC1_IN0	Analog mode	No pull-up and no pull-down	n/a	ADC_IN
ADC2	PA1	ADC2_IN1	Analog mode	No pull-up and no pull-down	n/a	ADC_OUT
DAC	PA4	DAC_OUT1	Analog mode	No pull-up and no pull-down	n/a	
RCC	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM5	PA2	TIM5_CH3	**Alternate Function Open Drain ***	No pull-up and no pull-down	**Very High ***	PWM_IN
TIM9	PE6	TIM9_CH2	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	PWM_OUT
USART1	PA9	USART1_TX	Alternate Function Push Pull	Pull-up	**Very High ***	
	PA10	USART1_RX	Alternate Function Push Pull	Pull-up	**Very High ***	
GPIO	PE3	GPIO_Input	Input mode	**Pull-up ***	n/a	Key1
	PE4	GPIO_Input	Input mode	**Pull-up ***	n/a	Key0
	PA6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	D2
	PA7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	D3
	PB11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Medium ***	RELAY_1
	PB12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Medium ***	RELAY_2
	PB13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Medium ***	RELAY_3
	PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Medium ***	RELAY_4

8.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA2_Stream0	Peripheral To Memory	**High ***
DAC1	DMA1_Stream5	Memory To Peripheral	**High ***
USART1_RX	DMA2_Stream5	Peripheral To Memory	**Medium ***
ADC2	DMA2_Stream2	Peripheral To Memory	**High ***

ADC1: DMA2_Stream0 DMA request Settings:

Mode:	Normal
Use fifo:	**Enable ***
FIFO Threshold:	Full
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word
Peripheral Burst Size:	Single
Memory Burst Size:	Single

DAC1: DMA1_Stream5 DMA request Settings:

Mode:	**Circular ***
Use fifo:	**Enable ***
FIFO Threshold:	Full
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word
Peripheral Burst Size:	Single
Memory Burst Size:	Single

USART1_RX: DMA2_Stream5 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***

Peripheral Data Width:	Byte
Memory Data Width:	Byte

ADC2: DMA2_Stream2 DMA request Settings:

Mode:	Normal
Use fifo:	**Enable ***
FIFO Threshold:	Full
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word
Peripheral Burst Size:	Single
Memory Burst Size:	Single

8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 stream5 global interrupt	true	0	0
ADC1, ADC2 and ADC3 global interrupts	true	1	0
USART1 global interrupt	true	0	0
TIM5 global interrupt	true	1	0
DMA2 stream0 global interrupt	true	0	0
DMA2 stream2 global interrupt	true	0	0
DMA2 stream5 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
TIM1 break interrupt and TIM9 global interrupt	unused		
TIM3 global interrupt	unused		
TIM4 global interrupt	unused		
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	unused		
FPU global interrupt	unused		

*** User modified value**

9. Software Pack Report