Enabling OpenCL and SYCL for RISC-V processors

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ABSTRACT

RISC-V is a non-profit, member managed organization and is gaining momentum in the processor space, with more than 900 members. One of the goals of the organization is to build an open software platform, providing software developers an easy way to harness the familiar benefits already available on CPUs and GPUs.

Today, system-on-chip manufacturers are building specialist accelerator processors based on the RISC-V architecture, taking advantage of the Vectorized extensions that match compute performance mostly seen on GPUs today. The availability of a familiar and well defined programming model is an absolute requirement if expecting to successfully bring these new processors to market.

This presentation will dive into the details of Codeplay's work in partnership with NSI-TEXE and Kyoto Microcomputer, describing the components needed to integrate OpenCL and SYCL onto RISC-V using multiple simulators. This project forms part of Japan's New Energy and Industrial Technology Development Organisation ("NEDO") project to build a powerful supercomputer.

While Codeplay has previously enabled OpenCL for a variety processor architectures, there are a number of technical challenges involved in delivering a generic integration that can be used by multiple RISC-V based systems, and the solution required a change in approach. By adding to the existing LLVM back-end for RISC-V, and creating an integration layer that plugs into OpenCL, we have built a common base architecture for a range of RISC-V processors from different companies. This presentation will explain how Codeplay's current driver interface works, and how it has been adapted to integrate with multiple RISC-V targets, in particular the riscvOVPsim and Spike RISC-V ISA simulators. We will also talk about some of the RISC-V extensions that are available, and how these can help to to expose features specific to the RISC-V architecture through OpenCL.

CCS CONCEPTS

• **Computing methodologies** → **Parallel programming languages**; • **Hardware** → **Hardware accelerators**.

KEYWORDS

SYCL, OpenCL, RISC-V

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