A Fully Integrated Chip-ID Tag Used in Chip Information Identification

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***ABSTRACT* — A fresh and creative passive UHF RFID tag, which can be referred to as "Chip-ID tag", has been proposed in this paper. The fully integrated Chip-ID tag, fabricated on the same substrate of the identified SOC, can be used for the SOC chip information identification, such as the chip manufacturer, function and series number identification, etc. The Chip-ID tag without OCA can be implemented as small as a PAD. OCA can be embedded in the periphery of the identified SOC chip or outside the ring of bonding pad. In order to guarantee the maximum power transmission between the reader antenna and the OCA tag, theoretical and experimental analysis between reader antenna and Chip-ID tag have been presented for verifying the feasibility of the proposed Chip-ID tag in this work. Finally, a Chip-ID tag with 4 mm x 4 mm single-turn square loop OCA, including the identified SOC chip, is successfully designed and taped out in 0.18-um CMOS technology. Measurement results demonstrate that the Chip-ID tag can be powered up and then transmit a unique Chip-ID data to the single-turn loop reader antenna with diameter of 1 cm by 110 KHz full-ASK clock signals modulation in complete contact circumstances, when reader transmit -9dBm RF input power at 915 MHz band. The maximum reading range of 1.3 cm can be achieved with 20dBm RF input power by the reader generated. It is worth emphasizing that, within all published papers, this paper is the first time to put forward a self-contained, CMOS-only Chip-ID tag for the SOC chip information identification.**

Keywords — Chip-ID tag, Chip-ID data, on-chip antenna, reader antenna, the identified SOC chip .

I. I. INTRODUCTION

In recent years, the electronic market followed electronics like a raging fire development situation has became one of the most potential and attractive market in the world. The security problem of electronic products, however, has also aroused more and more people to pay attention. Compared with the traditional anti-counterfeiting technology, radio frequency identification (RFID) technology would be the best choice to solve this severe challenge. Although many anti-counterfeit applications even in those rigorous research such as monetary anti-counterfeiting, pharmaceutical labeling, fine supply chain management, document tagging, military intelligence have adopted RFID technology, they have not integrated RFID tag with the identified objects in the same substrate and always need some extra post processing steps. Therefore, it is not desirable for the SOC chip in terms of lower cost and complexity, higher reliability and smaller area. Based on the above thinking, RFID tag is urgently needed to be integrated with the identified SOC chip in the same substrate to ensure the SOC chip safety. In addition, it is also worth emphasizing that rapid progress in semiconductor technology makes the militarization of RFID tag circuit possible. A 0.3 mm x 0.3 mm μ-chip has been implemented in an available 0.18μm CMOS fine standard process in 2003 [1] and then the other ultra-small RFID chip reported in 2007 is only 0.05 mm x 0.05 mm [2], but OCA is not included in both of them. So, it is greatly possible that a RFID tag can be made as small as a PAD. In order to reduce the packaging and the manufacturing cost of off-chip antenna and shrink the whole size of RFID tag, the integrated OCA of RFID tag has been put on the agenda and implemented in [4]. Therefore, based on these factors mentioned above, it would be imperative to design an ultra-small passive RFID tag with OCA, integrating with the identified SOC chip in one for the SOC chip information identification.

In this paper for the first time, we proposed a fully integrated Chip-ID tag with OCA for the SOC chip information identification such as the chip manufacturer, function and series number identification, etc. The Chip-ID tag, as small as a PAD, can be fabricated on the same substrate with the identified SOC chip. This means that the proposed Chip-ID tag, which also is a self-contained, CMOS-only system without any external components, cannot be damaged and erased, unless the identified SOC chip would be destroyed at the same time.

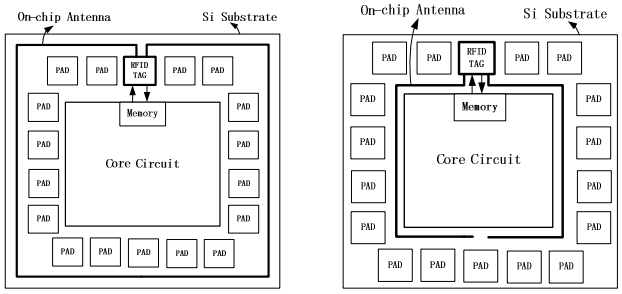
Furthermore, this paper gives a complete description of the Chip-ID tag from the general work principle and the system design to final verification. Section II displays the whole system and chip architecture of Chip-ID tag. Followed by Section III, reader antenna and OCA of this proposed Chip-ID tag have been designed and verified. Then, a transformer equivalent circuit is extracted from the inductive coupling system between reader antenna and the Chip-ID tag for discussing the maximum power transfer problem. Section IV presents a successful experiment applying an ultra-small Chip-ID tag with 4 mm x 4 mm single-turn square loop OCA to confirm the feasibility of Chip-ID tag. Finally, conclusions are displayed in Sections V.

II. SYSTEM AND CHIP ARCHITECTURE

Fig.1 including (a) and (b) shows the proposed fully integrated Chip-ID tag, which is fabricated on the same

substrate with the identified SOC chip for the SOC chip information identification, such as the chip manufacturer, function and series number identification, etc. Aiming at the different application requirements, OCA can be embedded in the periphery of the identified SOC chip or outside the ring of bonding pad. What is more, the shape, turns and size can be various for OCA. For example, single-turn OCA, multi-turns OCA, loop OCA, dipole antenna, etc. The total Chip-ID tag without OCA can be made as small as a PAD.

The whole system architecture of the proposed Chip-ID tag with different OCA is showed in Fig. 1. Fig.1 (a) displays the Chip-ID tag with single-turn square loop OCA and OCA is deposited on the outside the bonding pad ring, while Fig.1 (b) concerns the Chip-ID tag with dipole OCA and OCA is embedded in the periphery of the identified SOC chip.



(a) (b)

Fig. 1. The system architecture of the Chip-ID tag with different OCA.

As stated in the previous sections, to overcome the limitations of cost and area and expand the application scope, the core circuit of this Chip-ID tag usually only consist of a low power analog front end, digital baseband processor as well as OCA. Memory can be selected to use, or not. This means that the Chip-ID tag can share the memory with the identified SOC chip, when a memory is needed in the Chip-ID tag.

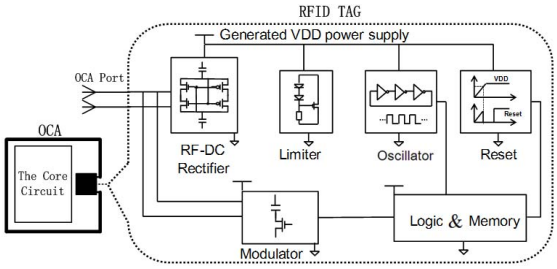


Fig. 2. The module diagram of Chip-ID tag architecture.

Detailed chip architecture for the proposed Chip-ID tag shows as Fig.2, the Chip-ID tag comprise a high efficiency RF-DC rectifier supplying the power for the whole system, a limiter for limiting the available voltage from the rectifier, a current controlled ring oscillator generating clock for data communication, reset block providing a reset pulse with 0.8 V supply voltage, as well as a signal modulator and logic & memory.

Moreover, the whole area of this Chip-ID tag system without OCA is just as small as the PAD size. Thus, the Chip-ID tag can be put in the position of a PAD or in any place where the size is larger than the area of PAD in the substrate. When the reader transmit enough RF input power, the Chip-ID tag can be powered up and then transmit Chip-ID data stored in memory to reader by captive load modulation.

III. Reader Antenna and The OCA Tag

This section, divided into three parts, is mainly devoted to the maximum power transfer problem between the reader antenna and the OCA tag at the specific frequency band. First, reader antenna is designed and modeled by electromagnetic simulation software in part A. Second, take the single-turn square loop OCA for example, part B occurs the related theoretical analysis and the simulation results of OCA to verify the feasibility of this proposed Chip-ID tag. Finally, an inductive coupling model is presented to analyze the maximum power transfer between the reader antenna and the OCA tag in part C.

A. Reader Antenna

In this paper vividly displayed in Fig. 3, a single-turn loop antenna with the diameter of 1 cm [4], which is manufactured by insulated copper wire, is used to wirelessly transport energy and data to OCA of the Chip-ID tag by inductive coupling. Thus, it is very important to focus on the electromagnetic field analysis of the single-turn loop reader antenna.

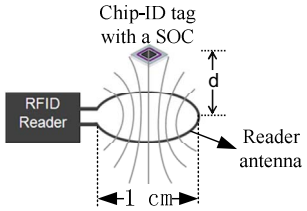


Fig. 3. Inductive coupling between reader antenna and the Chip-ID tag.

With the vertical distance (z-axis on behalf of the vertical direction in Fig. 4 (a)) changing from 0 to 1 cm, the magnetic field intensity of the reader antenna can be got by two ways, when 1A current is flowing around the reader antenna coil.

On the one hand, the vertical magnetic field intensity of this near field electrically small antenna can be calculated by the equation as follows

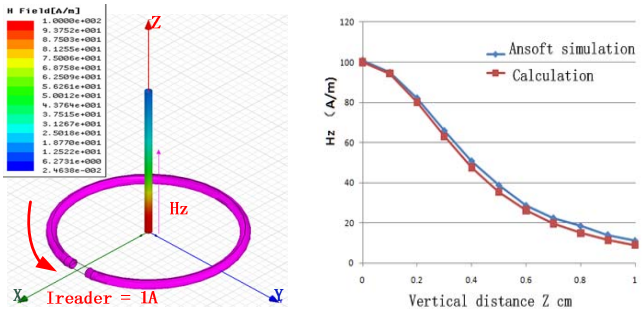
$$H_z = \frac{NIR^2}{2\sqrt{\left(R^2+Z^2\right)^3}} \tag{1}$$

Where R and Z is coil radius and vertical distances (z-axis on behalf of vertical direction in Fig. 4 (a)), respectively. N is the track turns and I represents the amount of current flowing in the coil [4].

On the other hand, the simulation results of the vertical magnetic field intensity for this near field electrically small single-loop reader antenna also can be obtained by electromagnetic simulation software.

Comparing the calculation results and the simulation results of the magnetic field intensity, we can not only receive a very

good agreement shown in Fig. 4 (b), but also further demonstrate the feasibility and effectivity of this design method.



(a) (b)

Fig. 4. Electromagnetic simulation result of single-turn loop reader antenna.

Besides, as we know, the intensity of magnetization is defined as

$$B = \mu \times H_z \tag{2}$$

Therefore, we can select H_z = 1A/m, and then the intensity of magnetization B can be concluded as 0.4 π x 10^{-6} T which would be used in the below analysis.

B. *OCA for the Chip-ID tag*

A lumped parameter model, which is a classical single-π model of the single-turn square loop OCA shows in Fig. 5 derived by electromagnetic simulation software at 915 MHz band, has been developed to analyze the OCA design process.

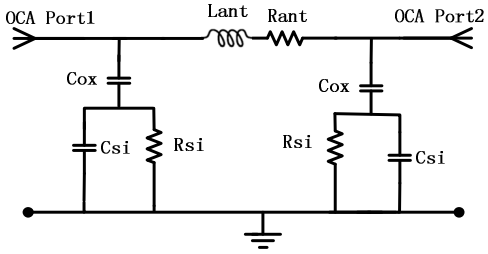


Fig. 5. A lumped-parameter model of single-turn square loop OCA.

In Fig. 5, L_{ant} and R_{ant} are the series inductance and conductor loss, respectively; C_{ox} represents the oxide capacitance, while R_{si} and C_{si} represent the silicon substrate parasitic resistance and capacitance, respectively.

When the inner diameter Din of OCA changes from 2 mm to 8 mm, along with other process parameters of OCA unchanged, we can conveniently plot the variation diagram (see Fig. 6) of resistance and inductance at 915 MHz, respectively.

Then, it becomes clear that the resistance and inductance of OCA both are increased with the increase of the inner diameter of OCA from 1mm to 8mm.

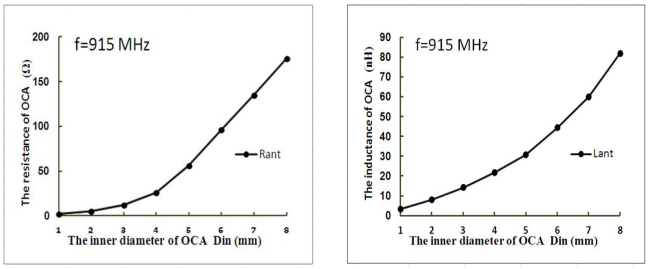


Fig. 6. The resistance and inductance of the single-turn square loop OCA influenced by its inner diameter.

C. *The maximum power transfer analysis between the reader antenna and the OCA tag*

From a design point of view, the tag antenna impedance must be the complex conjugate with the RFID tag impedance and at the same time reader antenna must be developed to be 50 Ω input impedances at the specific frequency [3]. Unfortunately, it is almost impossible that the OCA impedance, with the changed inner diameter of OCA, can be always matched with the fixed impedance parameters of this Chip-ID tag without any extra matching network. Facing this challenge, a transformer-type coupling between the primary coil in the reader and the secondary coil integrated in Chip-ID tag has been given to explain wirelessly transmit energy between reader antenna and the Chip-ID tag in Fig. 7.

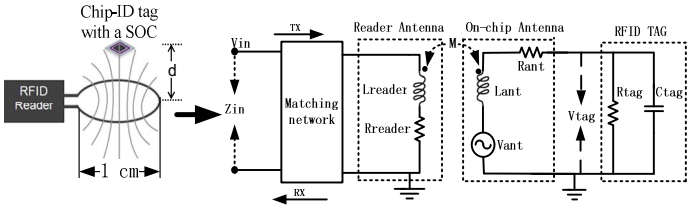


Fig. 7. Inductive coupling model between reader antenna and the OCA tag.

According to the scheme of Fig. 7, the induced voltage of OCA from reader antenna can be expressed by,

$$\left|V_{ant}\right| = \omega B_{reader} S_{OCA} \approx \omega B_{reader} D_{in}^2 \tag{3}$$

Where ω is the circular frequency; B is intensity of magnetization; S and Din are the equivalent area and the inner diameter of OCA, respectively.

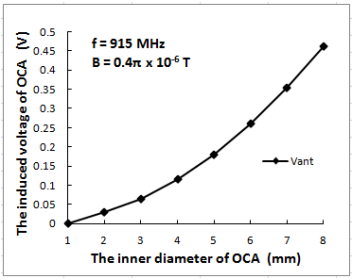


Fig. 8. The induced voltage of OCA from the reader antenna vs. the inner diameter of single-turn square loop OCA.

As equation (3) stated clearly, Fig. 8 shows a square relationship variation curve between the induced voltage of

OCA from reader antenna and the inner diameter of OCA at 915 MHz band and the fixed intensity of magnetization.

In addition, according to this inductive coupling model, transmission function of this Chip-ID tag is deduced as,

$$|H(\omega)| = \frac{1}{\sqrt{\left(\frac{\omega L_{ant}}{R_{tag}} + \omega R_{ant} C_{tag}\right)^2 + \left(1 - \omega^2 L_{ant} C_{tag} + \frac{R_{ant}}{R_{tag}}\right)^2}} \quad (4)$$

With Chip-ID tag impedance parameters fixed at 915 MHz, equation (4) indicates that the transmission function is controlled by the resistance and inductance of OCA (see in Fig.7). And also, according to the published literature [4] as well as Fig 6, we can conclude that the resistance and inductance of OCA is mainly determined by the inner diameter of single-turn square loop OCA under the other process parameters invariable.

Consequently, an explicit functional relation between the available voltage of Chip-ID tag from OCA and the inner diameter of single-turn square loop OCA was derived by,

$$V_{tag} = \frac{B\omega \times D_{in}^{\ 2}}{H(D_{in})} \quad (5)$$

Furthermore, we assume that the impedance for a existing tag is 20 - j 120 Ω at 915 MHz and the intensity of magnetization B is fixed. Thus, it is visually displayed in Fig. 9 that the obtainable voltage of Chip-ID tag from the single-turn square loop OCA is also increased with the increase of the inner diameter of OCA.

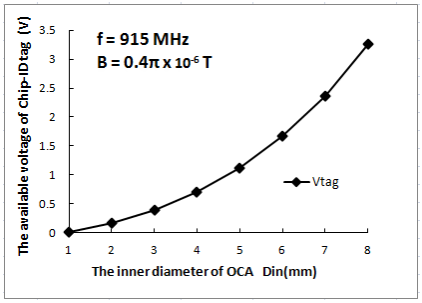


Fig. 9. The obtainable voltage of RFID tag transmitted by OCA influenced by the inner diameter of single-turn square loop OCA.

At the same time, Fig. 9 indicates that there is a critical limit for the maximum available voltage of Chip-ID tag transmited by OCA (0.8V is the critical limit in this work). This proposed system cannot work, unless the available voltage of Chip-ID tag from OCA exceeds the critical limit.

All in all, the electromagnetic simulation result of the single-turn square loop OCA shows a gradually increase relationship between the reachable voltage of Chip-ID tag and the inner diameter Din of OCA. It is worth noting that the Chip-ID tag can work normally even for the recognition of the maximum CPU, as long as the obtainable voltage of Chip-ID tag from the integrated single-turn square loop OCA can exceed the critical voltage.

IV. Experimental Results

A fully integrated passive UHF Chip-ID tag with single-turn square loop OCA, deposited on the same substrate with the identified SOC, has been designed and fabricated in 0.18-um CMOS technology. OCA is manufactured with the top layer metal to achieve high Q factor inductor. In order to minimize the chip area and fabrication costs, the identified SOC chip is surrounded by the OCA as Fig. 10. The whole size of OCA is 4 mm x 4 mm with 15 um line width.

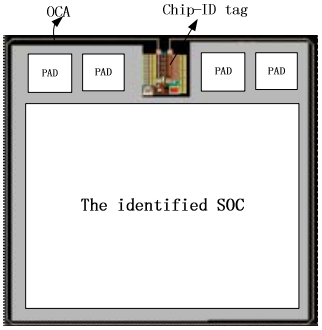


Fig. 10. A fully integrated Chip-ID with single-turn square loop OCA fabricated in 0.18-um CMOS technology.

The detail test plan is shown in Fig. 11. As is indicated that an automatic impedance tuner, instead of matching network in actual measurement, is fine controlled to develop the single-turn loop reader antenna to be 50 Ω - input impedances to guarantee the maximum energy-transmission between the reader and the proposed Chip-ID tag.

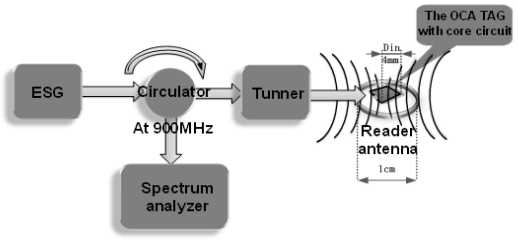


Fig. 11. Testing environment of this chip self-recognition

Measurement results demonstrate that the reader antenna can detect Chip-ID data by monitoring backscattered clock signals from this Chip-ID tag in complete contact, when the carrier power launched by signal generator reaches -9dBm at 915MHz. With the reader transmission power up to 20dBm, the maximum communication range achieved between the reader antenna and the OCA tag is 1.3 cm. And also, the digital logic circuit is just designed to verify the feasibility of this Chip-ID tag by outputting a frequency of 110 KHz pulse to modulate the impedance values of OCA ports. Finally, we can receive the response waveforms of this proposed Chip-ID tag by spectrum analyzer at 915 MHz as Fig.12.

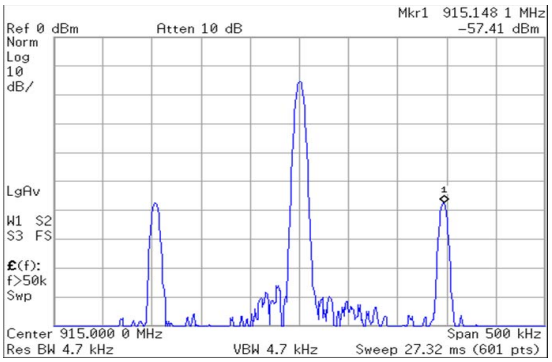


Fig.12. The response spectrum of this proposed Chip-ID tag.

V. CONCLUSION

This paper creatively advanced a fully integrated Chip-ID tag with OCA, which is fabricated on the same substrate with the identified SOC for the SOC chip information identification, such as the chip manufacturer, function and series number identification, etc. The Chip-ID tag without OCA can be made as small as a PAD. OCA can be placed in the periphery of the identified SOC chip or be deposited on the outside the bonding pad ring. It implies that this Chip-ID tag cannot be destroyed and erased, unless the identified SOC chip would be damaged at the same time. By using this self-contained, CMOS-only system, in other words, the security of the identified SOC chip can be guaranteed without any external components. When the reader emit enough RF input power in the near field, this Chip-ID tag can be powered up and then transmit unique Chip-ID data to reader by modulator. A lumped model of this proposed system has been presented to study the maximum power transmission between the reader antenna and the OCA tag, combined with the feasibility and applicability analysis of the integrated OCA. Based on the above thinking, a experimental validation exploiting an ultra-small Chip-ID tag with the integrated single-turn square loop OCA fabricated in standard 0.18-um CMOS technology is successfully provided and confirmed. Measurement results demonstrate that the maximum reading range of this system is 1.3 cm through generating 20dBm RF power by reader at 915-MHz band.

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