

Implementation of Energy and cost-efficient SRAM array with reversible logic gate in QCA.

Static Random-Access Memory (SRAM) is a type of volatile memory used in digital systems. SRAM supports read and write operations to retrieve data from memory location and to store data into those locations respectively. Power leakage in SRAM occurs due to sub-threshold leakage currents which accumulate in SRAM cells and can lead to increased power consumption, heat reduction and reduced battery life. The fundamental constructing block of an SRAM array is the SRAM cell. The SRAM cells in an array are arranged in rows and columns. Quantum-dot cellular automata is a paradigm for addressing issues of device density and interconnection and to overcome the drawbacks of CMOS technology. It can represent information based on spatial distribution of electron charges. Increased power dissipation is one of the major problems faced by CMOS technology. Reversible computing offers a potential solution to the current challenge, with reversible logic circuits playing an important role in quantum computing. This approach not only promises to overcome obstacles but also provides fault diagnostic features. Quantum-dot cellular automata (QCA) nanotechnology, distinguished by its exceptional attributes such as remarkably high operating frequency, minimal power dissipation, and nanoscale feature dimensions, is increasingly recognized as a compelling alternative to replace CMOS technology. This work presents a cost and energy efficient SRAM array with reversible logic gate. It also presents a comparative analysis of different wire-crossing techniques. The proposed design will be implemented in QCA designer tool and energy dissipation will be estimated using QCA Pro tools.

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