ME333 – Homework 2 – Yael Ben Shalom

Exercise 3:

The four functions that pin 12 can have are:

1. Analog input.
2. Comparator input.
3. Change notification input (which can generate an interrupt when an input changes state).
4. Digital input or output.

Pin 12 is not 5V tolerant.

Exercise 4:

The name of the SFR we have to modify if you want to change pins on PORTC from output to input is TRISC.

Exercise 5:

The reset value of CM1CON in hexadecimal is 00C3.

Exercise 6:

SYSCLK – Clocks the CPU (at maximum frequency of 80 MHz).

PBCLK - Clocks many peripherals and its frequency is set to SYSCLK's frequency divided by 1, 2, 4, or 8.

PORTA to PORTG - Digital I/O ports. allow you to read or output a digital voltage.

Timer1 to Timer5 - 16-bit counters/timers. Count the number of pulses of a signal.

10-bit ADC - Analog-to-digital converter, allows up to 16 analog voltage values to be monitored.

PWM OC1-5 - Output compare pins. Used to generate a single pulse of specified duration, or a continuous pulse train of specified duty cycle and frequency.

Data RAM - Memory storage for temporary data (128KB RAM on the PIC32MX795F512H).

Program Flash Memory - Memory storage for the program (512KB flash on the PIC32MX795F512H).

Prefetch Cache Module - stores recently executed program instructions, which are likely to be executed again soon (as in a program loop). It can minimize or eliminate the need for the CPU to wait for program instructions to load from flash.

Exercise 7:

The peripherals that are not clocked by PBCLK are the peripherals that are on the peripheral bus clocked by SYSCLK. The peripherals that are not clocked by PBCLK are PORTA to PORTG

Exercise 8:

The largest voltage difference that it may not be able to detect is ~3.1mV.

Exercise 9:

The maximum size of a program loop that can be completely stored in the cache is 256 bytes.

Exercise 10:

The path between flash memory and the prefetch cache module is 128 bits wide instead of 32, 64, or 256 bits, because the CPU' is 32 bits, with four times the frequency.

Exercise 11:

A digital output could be configured to swing between 0V and 4V, even though the PIC32 is powered by 3.3V, because an output pin can also be configured as open drain. In this configuration, the pin is connected by an external pull-up resistor to a voltage of up to 5.5V.

Exercise 12:

The maximum amount of RAM and flash memory a PIC32 can have before the current choice of base addresses in the physical memory map would have to be changed is 0x1D000000 for RAM and 0x2800000 for flash.

Exercise 13:

a) In order to set PBCLK frequency to be half the frequency of SYSCLK, we will have to modify bits 12-13 to 1 in the DEVCFG1 register (Device Configuration Register).

b) In order to set the watchdog timer to be enabled we set bit 23 to 1 in the DEVCFG1 (Device Configuration) register.

In order to set the watchdog timer postscale we modify bits 20-16 in the DEVCFG1.

In order to set the time interval to be maximum we set the bits to 10100.

c) In order to select the HS Oscillator mode, we would have to set bit 8-9 in DEVCFG1 register to 10.

In order to enable the primary oscillator and turn on the PLL module we would have to set bit 2-0 to 011 in the DEVCFG1 register.

Exercise 14:

If the load is modeled as a resistor, the smallest resistance that would be safe is 16.6 Ohm (should not plan to draw more than 200-300mA or so from the NU32).

R = V/I = 5V/300mA = 16.6 Ohm

Exercise 15:

A reasonable range of voltages that could be used is 5-9V, because the NU32 input is 5V, but it can regulate up to 9V without overheating.

Exercise 16:

The buttons and two LEDs connected to:

1. Button 1 – pin 55/RD7
2. Button 2 – pin 7/MCLR
3. LED 1 – pin 58/RF0
4. LED 2 – pin 59/FR1