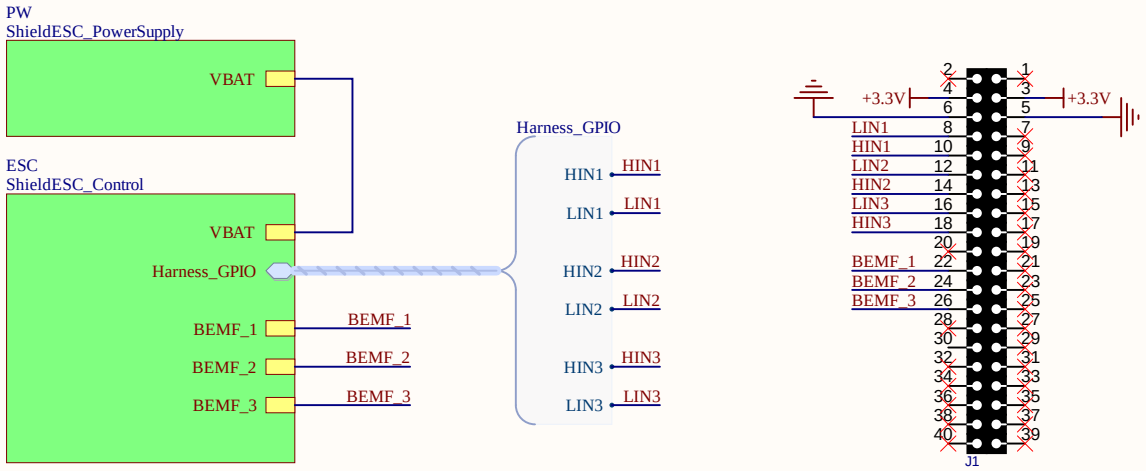
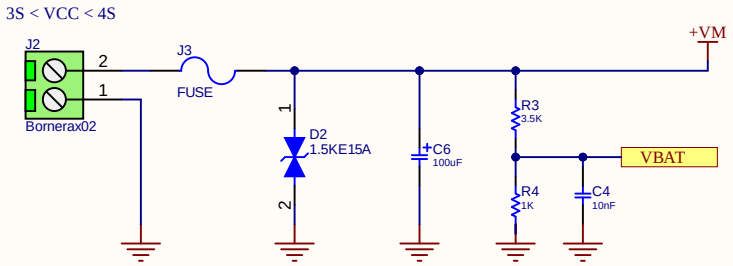


Title	ShieldESC-Cuadripolos.SchDo
Date	20/07/2025
Draw by	Yafhers Mendoza C.
	A4



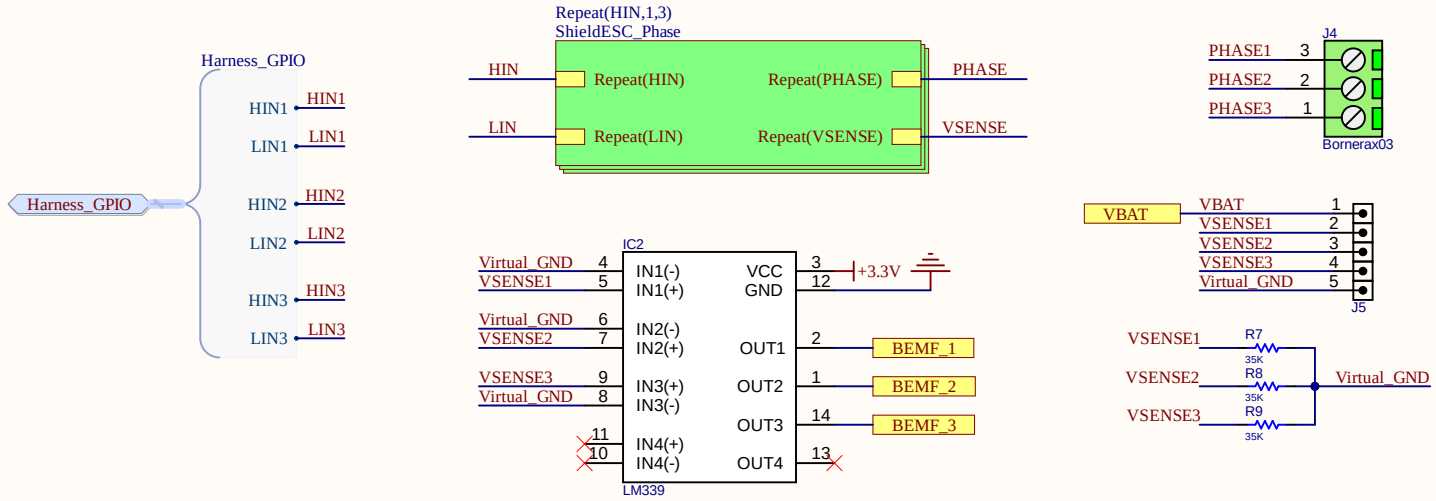
@VPH=4*3.7=14.8V
VSENSE = 3.3V

R3 = (Vin / 3.3) - 1

4S (16.8v) -> R3 > 4.00K para Vin = 14.8v -> Vout = 2.96v
3S (12.6v) -> R3 > 2.81K para Vin = 11.1v -> Vout = 2.91v
2S (08.4v) -> R3 > 1.54K para Vin = 07.4v -> Vout = 2.91v

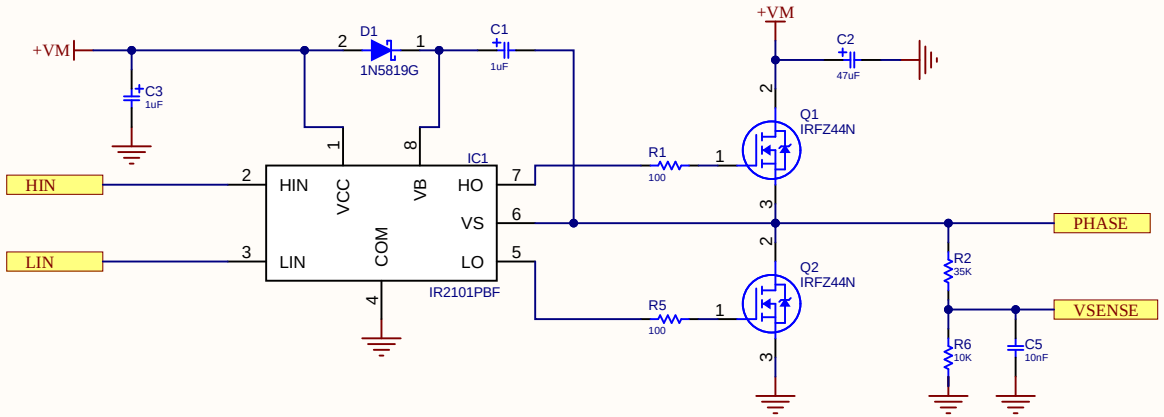
Title	ShieldESC_PowerSupply.SchDoc
Date	18/06/2025
Draw by:	Yafhers Mendoza C.

A4



Title	ShieldESC_Control.SchDoc
Date	26/05/2025
Draw by	Yafhers Mendoza C.

A4



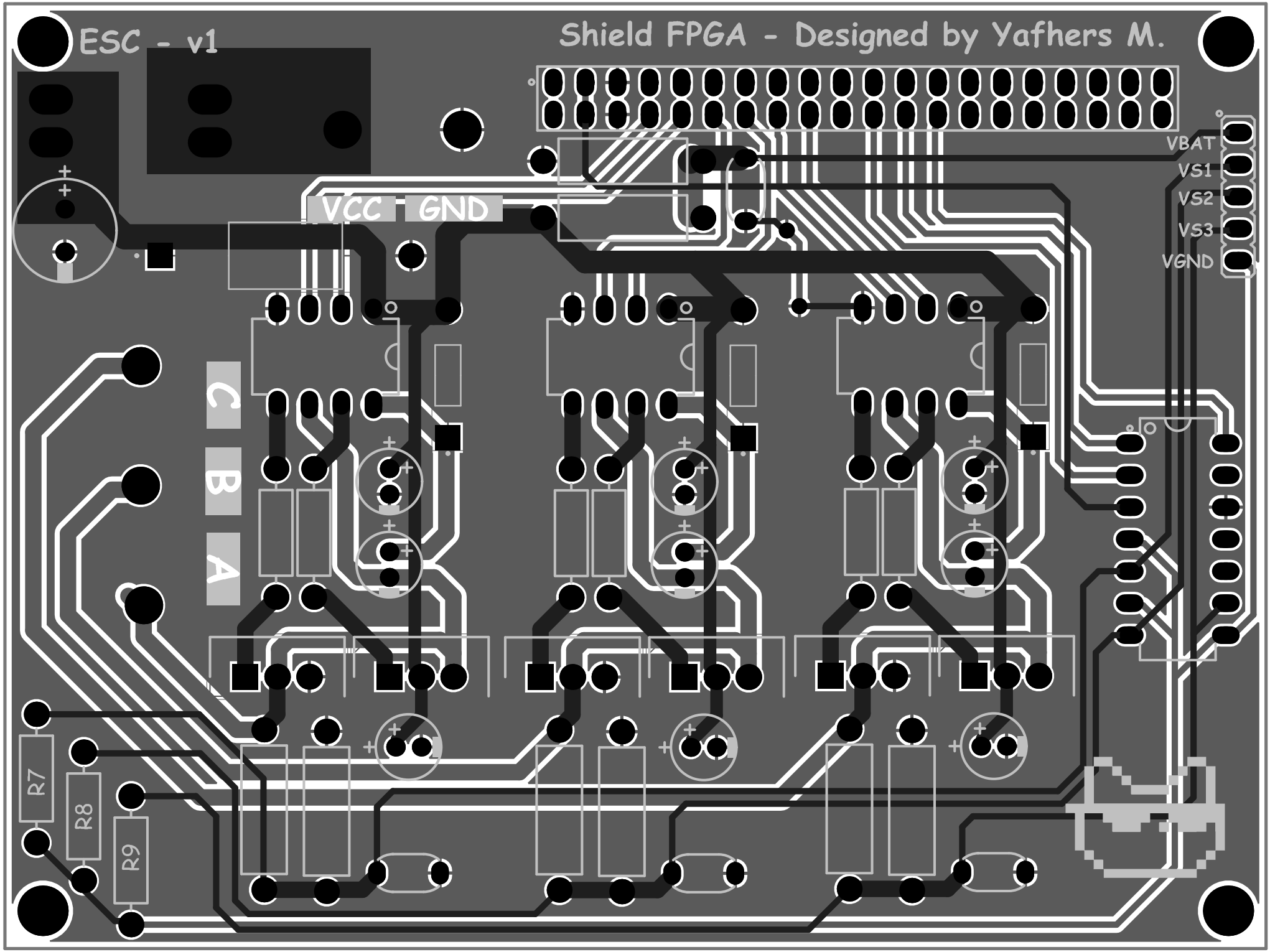
@VPH=4*3.7=14.8V
VSENSE = 3.3V

R2 = (Vin / 3.3) - 1

4S (16.8v) -> R2 > 40.00K para Vin = 14.8v -> Vout = 2.96v
3S (12.6v) -> R2 > 28.10K para Vin = 11.1v -> Vout = 2.91v
2S (08.4v) -> R3 > 15.40K para Vin = 07.4v -> Vout = 2.91v

Title	ShieldESC_Phase.SchDoc
Date	18/06/2025
Draw by:	Yafhers Mendoza C.

A4


ESC - v1
Shield FPGA - Designed by Yafhers M.
VCC
GND
VBAT
VS1
VS2
VS3
VGND
C
B
A
R7
R8
R9