

1

2

3

4

A

A

B

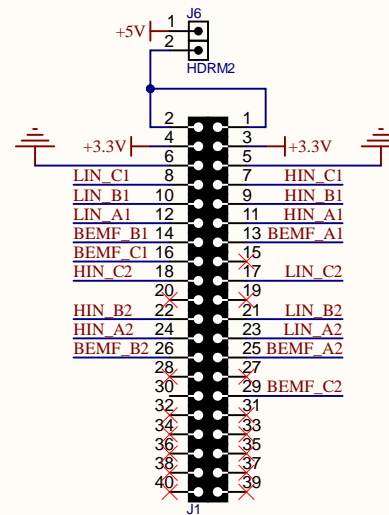
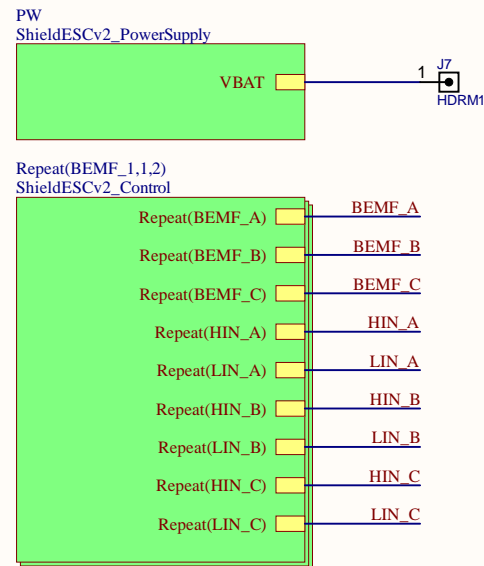
B

C

C

D

D

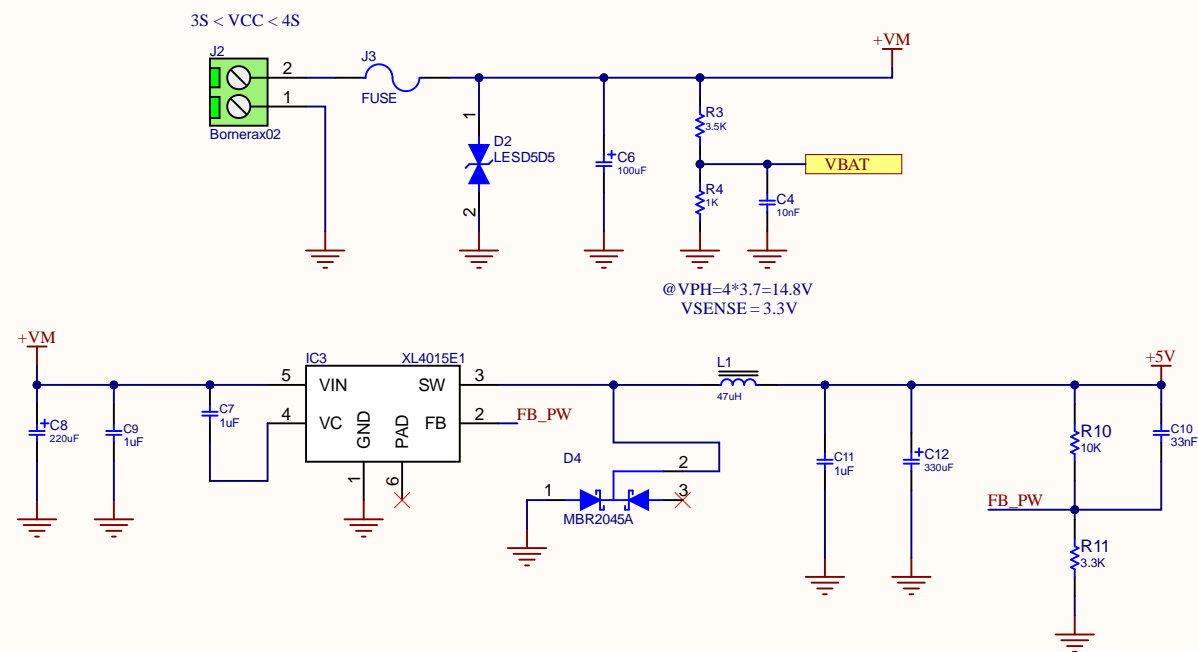


1

2

3

4



1

2

3

4

A

A

B

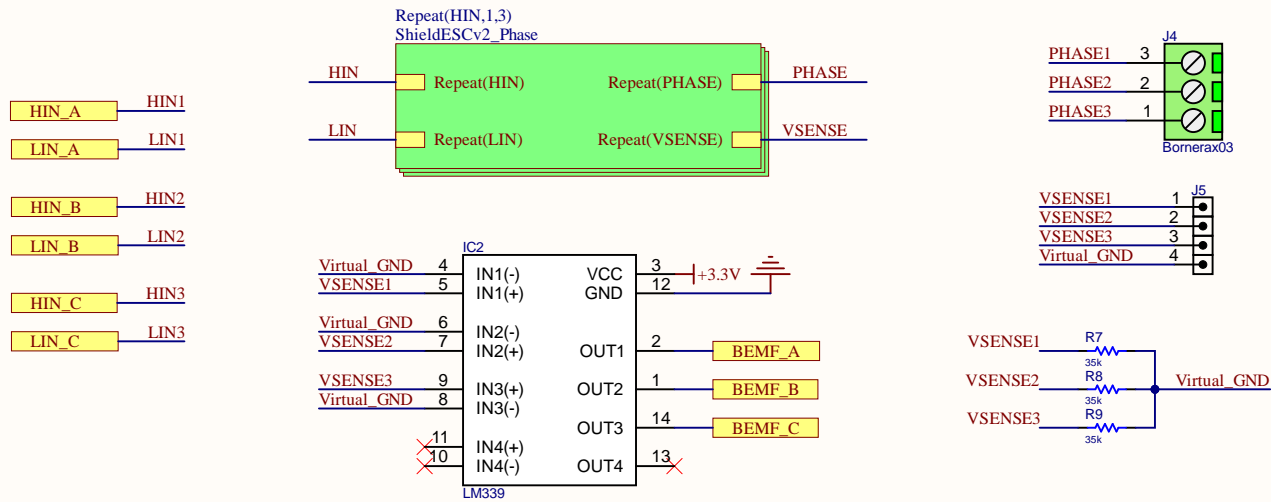
B

C

C

D

D

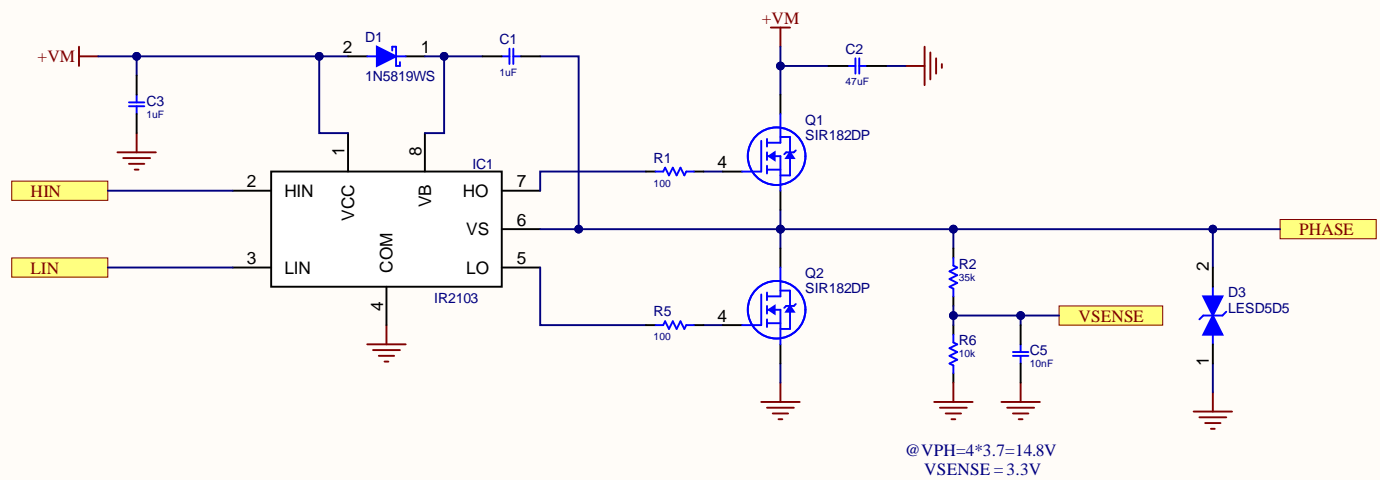


1

2

3

4



Shield FPGA - Designed by Yafhers M.

J7

BAT

VSC_2

VSB_2

VSA_2

VGND_2

VSC_1

VSB_1

VSA_1

VGND_1

VCC GND

ESC - v2

BLDC 1

C

B

A

BLDC 2

C

B

A

