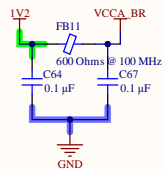
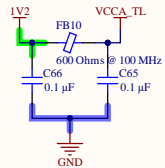
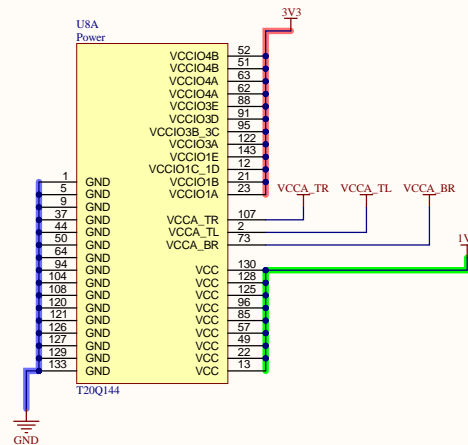


Power up sequence
VCC, VCCA ---> VCCIO



The diagrams show the following connections:

- TP5:** Connected to 5V.
- TP6:** Connected to 3V3.
- TP7:** Connected to GND.
- TP8:** Connected to 1V2.

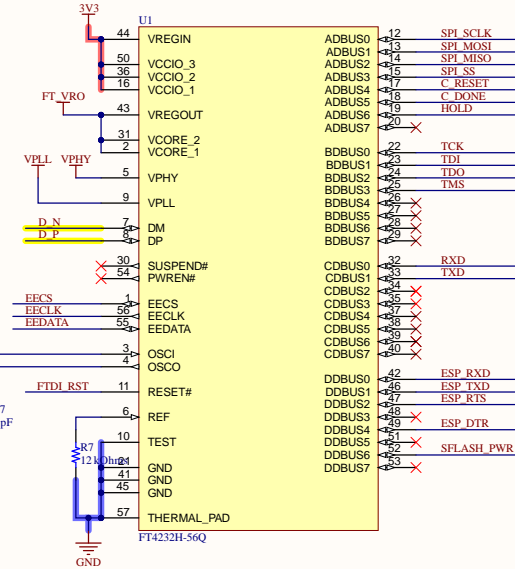
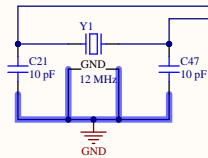
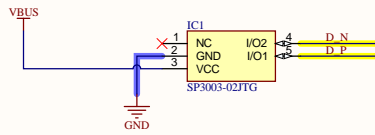
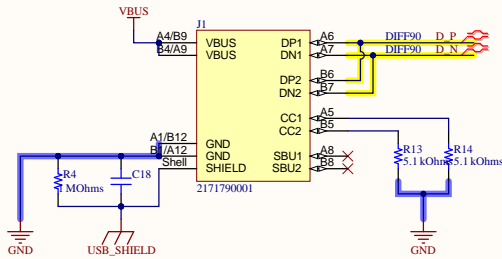
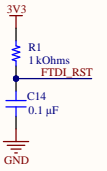
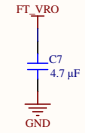
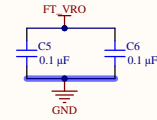
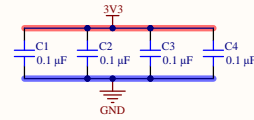
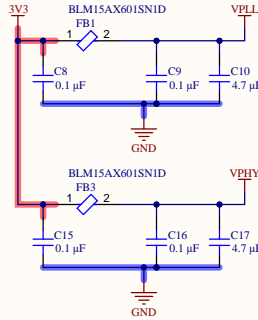
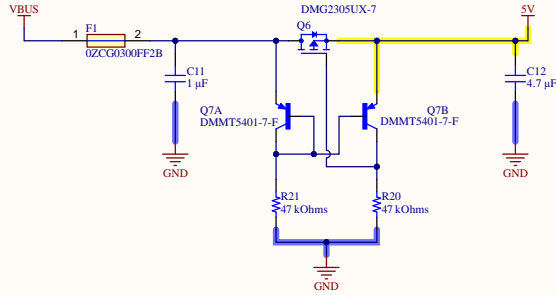


POWER

File: POWER.SchDoc



POWER IN



32	CDBUS0	TXD
33	CDBUS1	RXD
34	CDBUS2	RTS#
35	CDBUS3	CTS#
37	CDBUS4	DTR#
38	CDBUS5	DSR#
39	CDBUS6	DCD#
40	CDBUS7	RI#/TXDEN*

42	DDBUS0	TXD
46	DDBUS1	RXD
47	DDBUS2	RTS#
48	DDBUS3	CTS#
49	DDBUS4	DTR#
51	DDBUS5	DSR#
52	DDBUS6	DCD#
53	DDBUS7	RI#/TXDEN*
54	PWREN#	PWREN#
30	SUSPEND#	SUSPEND#

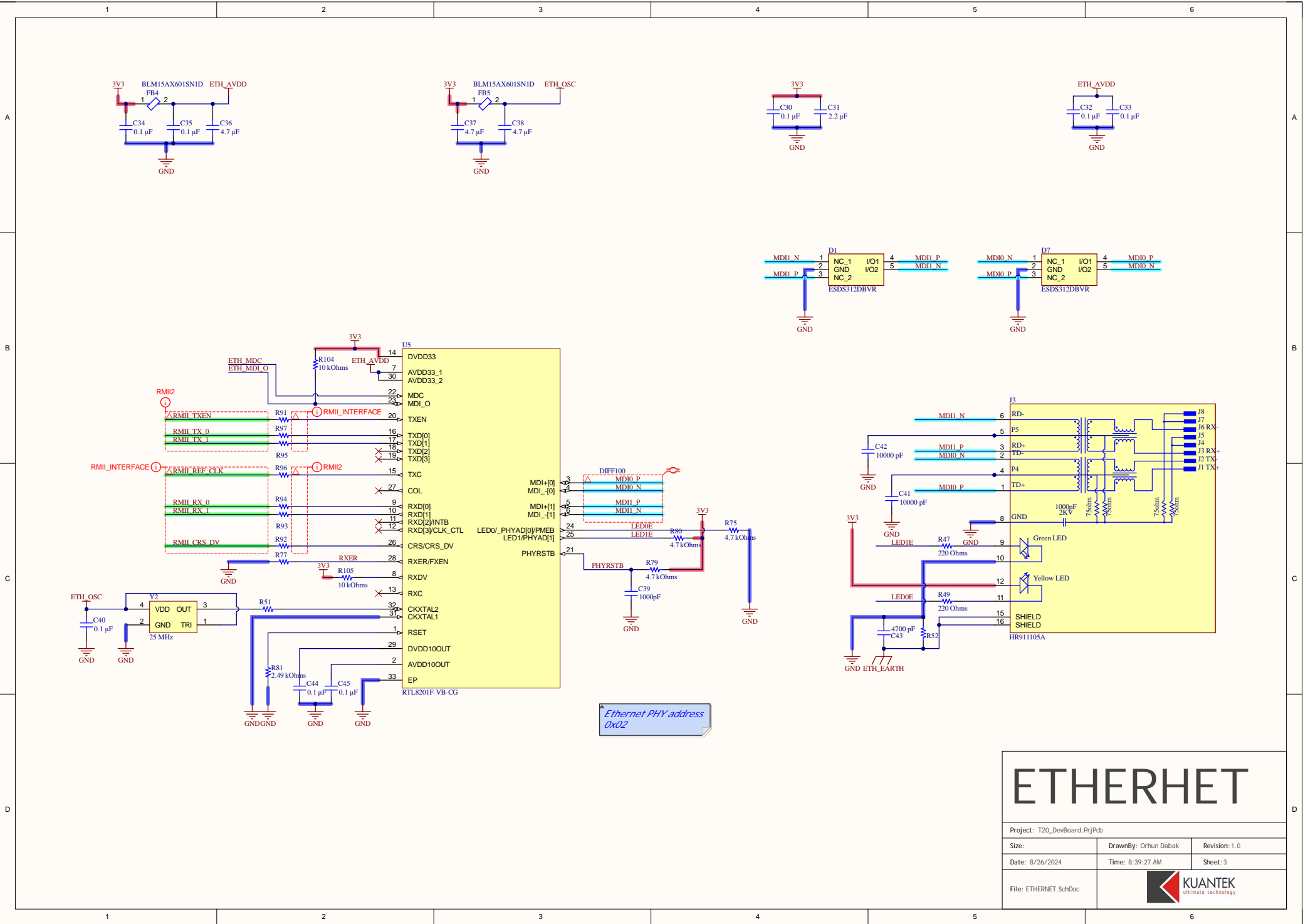
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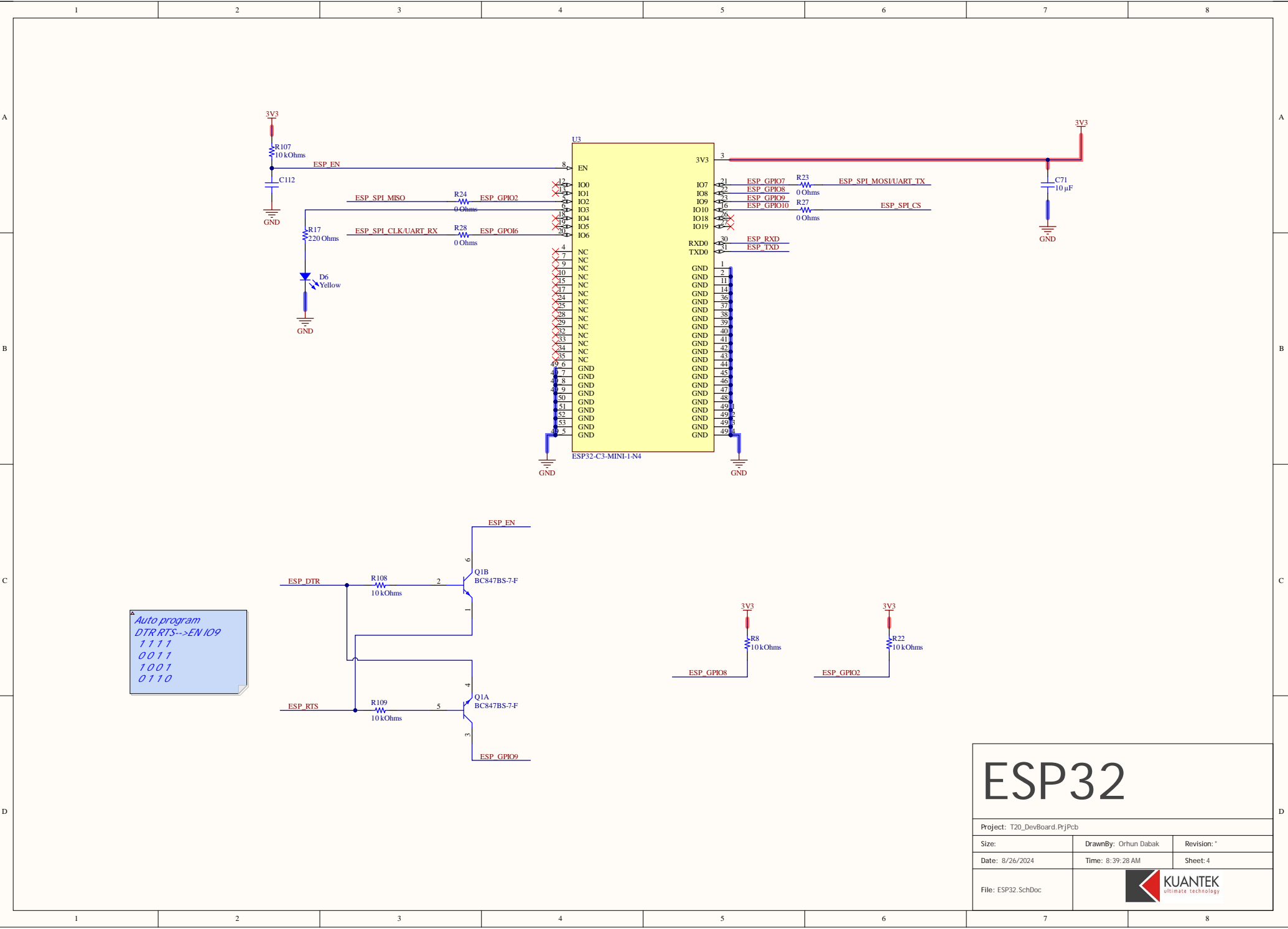
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Size: DrawnBy: Orhun Diabak Revision: 1.0
Date: 8/26/2024 Time: 8:39:26 AM Sheet: 2

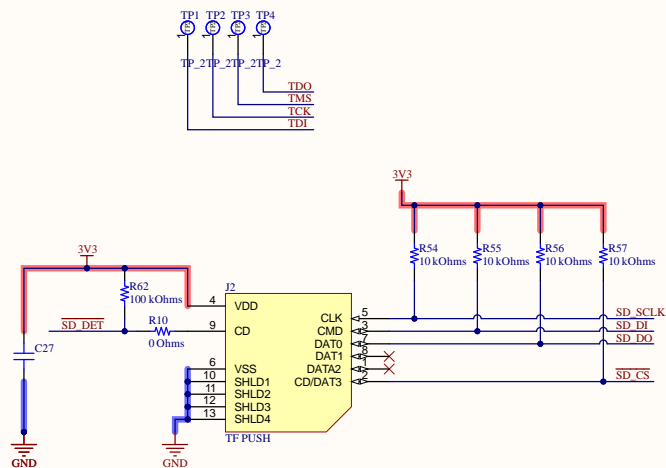
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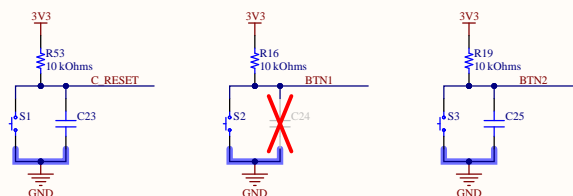




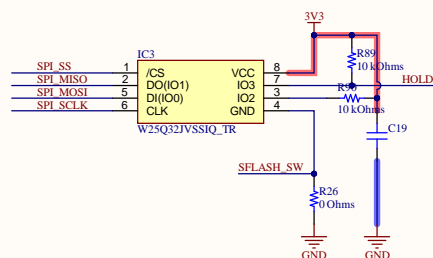
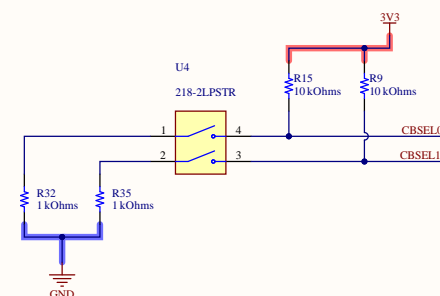
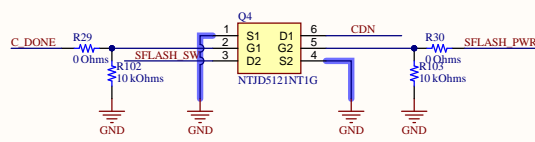
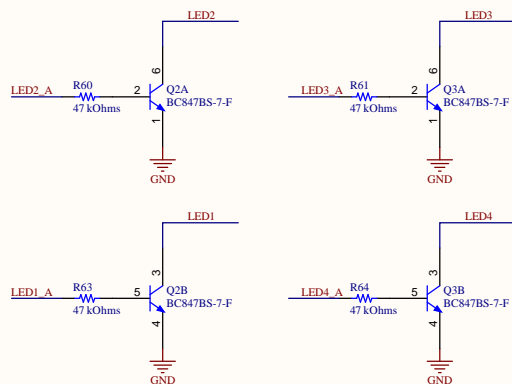
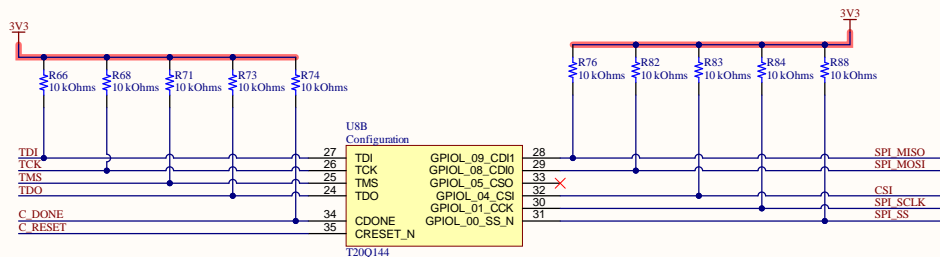
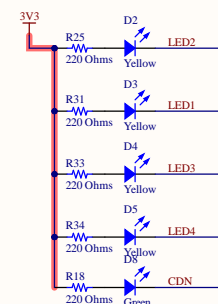
JTAG TESTPOINTS



USER AND C RESET BUTTONS

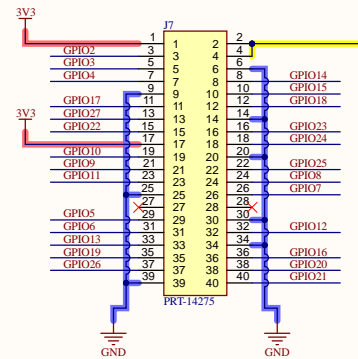
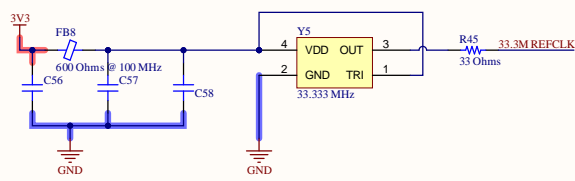
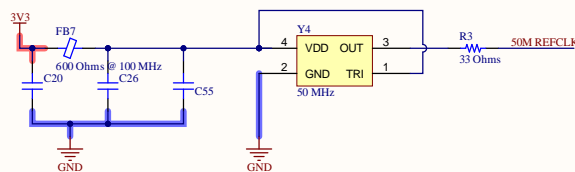
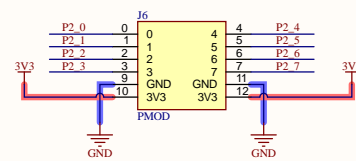
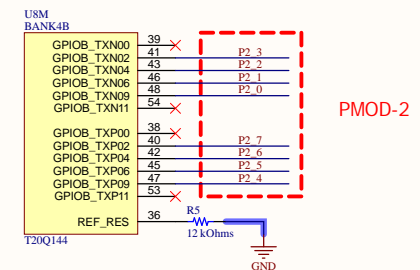
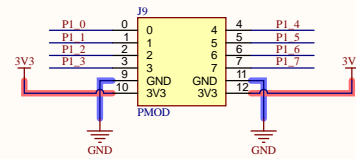
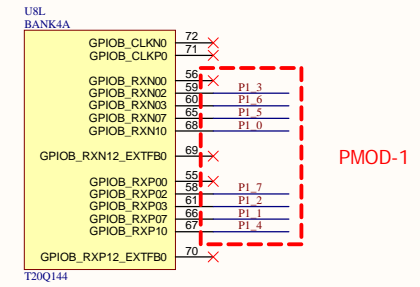
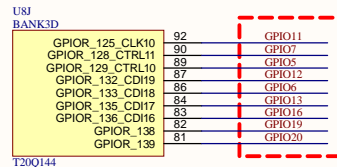
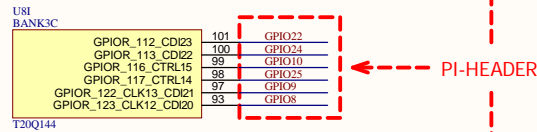
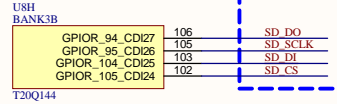
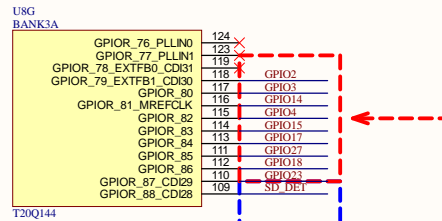
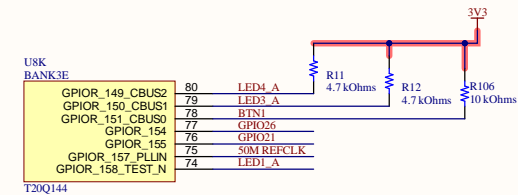
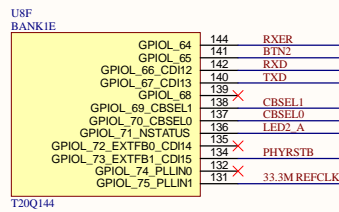
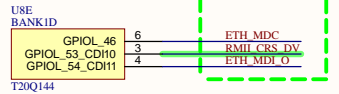
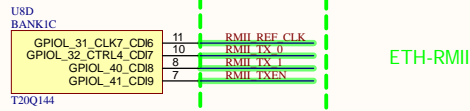
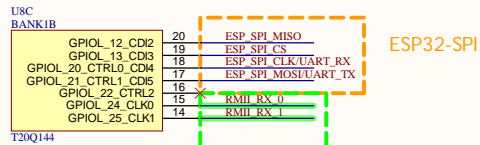


USER LEDs



CONF_USER

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Date: 8/26/2024	Time: 8:39:29 AM	Sheet: 5
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FPGA_GPIO

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Size:	DrawnBy: Orhun Diabak	Revision: 1.0
Date: 8/26/2024	Time: 8:39:30 AM	Sheet: 6
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