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Washing Machine

Finite State Machine

Annadata, Yagna Srinivasa Harsha

yxa210024

Duvvuri, Sai Pravallika

psd220003

Thota, Sai Abhishek

sxt210056

Verilog Code and Test bench

```
`timescale 1ns / 1ps
// Module Name: washingmachine
module washingmachine(clk, reset, closedoor, startmachine, filledmachine,
detergentadded, machinecycle timeout,
waterdrained, spin timeout check, doorlock check, motoron check,
fillvalue check,
                           drainvalue check,
                                                       done,
detergent wash, checkwater wash); input clk, reset; input [255:0]
closedoor;
            input
                   [127:0]
                             startmachine;
                                             input
filledmachine;
              input
                     [127:0] detergentadded;
                                              input
                                                     [127:0]
machinecycle timeout; input [127:0] waterdrained; input [127:0]
spin timeout check; output reg [127:0] doorlock check; output reg
[127:0] motoron check; output reg [127:0] fillvalue check; output
reg [127:0] drainvalue check; output reg [127:0] done; output reg
[127:0] detergent wash; output reg [127:0] checkwater wash;
 //defining the states parameter checkdoor
 = 3'b000; parameter fillwater = 3'b001;
 parameter detergentadder = 3'b010;
 parameter cycling = 3'b011; parameter
 waterdraining = 3'b100; parameter spinning
 = 3'b101; reg[2:0] currentstatecheck,
 nextstatecheck;
 always@(currentstatecheck or startmachine or closedoor or filledmachine
or detergentadded or waterdrained or machinecycle timeout
 or spin timeout check) begin case(currentstatecheck)
 //checking the door if it is locked and closed.
 //machine is started at this stage.
 checkdoor: if(startmachine==1'b1 &&
 closedoor==1'b1) begin nextstatecheck =
 fillwater; motoron check = 1'b0;
 fillvalue check = 1'b0; drainvalue check
 = 1'b0; doorlock check = 1'b1;
 detergent wash = 1'b0; checkwater wash =
 1'b0; done = 1'b0; end else begin
```

```
nextstatecheck = currentstatecheck;
motoron check = 1'b0; fillvalue check =
1'b0; drainvalue check = 1'b0;
doorlock_check = 1'b0; detergent_wash =
1'b0; checkwater wash = 1'b0; done =
1'b0; end
//Water is filled for soaking the clothes.
fillwater: if (filledmachine==1'b1) begin
if(detergent_wash == 1'b0) begin
nextstatecheck = detergentadder;
motoron check = 1'b0; fillvalue check =
drainvalue check = 1'b0;
doorlock check = 1'b1;
detergent wash = 1'b1;
checkwater wash = 1'b0; done =
1'b0; end else begin nextstatecheck
= cycling; motoron check = 1'b0;
fillvalue check = 1'b0;
drainvalue check = 1'b0;
doorlock check = 1'b1;
detergent wash = 1'b1;
checkwater wash = 1'b1; done =
1'b0; end end else begin
nextstatecheck = currentstatecheck;
motoron_check = 1'b0;
fillvalue check = 1'b1;
drainvalue check = 1'b0;
doorlock check = 1'b1;
detergent_wash = 1'b0;
checkwater wash = 1'b0; done =
1'b0; end
//detergent/soap will be added. detergentadder:
if (detergentadded==1'b1)
begin nextstatecheck =
cycling; motoron check =
```

```
1'b0; fillvalue check =
1'b0; drainvalue check =
1'b0; doorlock check =
1'b1; detergent wash =
1'b1; checkwater wash =
1'b0; done = 1'b0; end
else begin nextstatecheck
= currentstatecheck;
motoron check = 1'b0;
fillvalue check = 1'b0;
drainvalue_check = 1'b0;
doorlock check = 1'b1;
detergent wash = 1'b1;
checkwater wash = 1'b0;
done = 1'b0; end
//Washing cycle for the cleaning the clothes
cycling: if(machinecycle timeout == 1'b1)
begin nextstatecheck = waterdraining;
motoron_check = 1'b0; fillvalue_check = 1'b0;
drainvalue_check = 1'b0; doorlock_check =
1'b1; detergent wash = 1'b1; checkwater wash
= 1'b1; done = 1'b0; end else begin
nextstatecheck = currentstatecheck;
motoron_check = 1'b1; fillvalue_check = 1'b0;
drainvalue check = 1'b0;
doorlock check = 1'b1;
detergent wash = 1'b1;
checkwater_wash = 1'b1;
done = 1'b0; end
//draining the water from wet clothes waterdraining:
if(waterdrained==1'b1) begin
if(checkwater_wash==1'b0) begin
nextstatecheck = fillwater;
motoron_check = 1'b0;
fillvalue check = 1'b0;
drainvalue_check = 1'b0;
```

```
doorlock_check = 1'b1;
detergent wash = 1'b1;
checkwater wash = 1'b1; done =
1'b0; end else begin nextstatecheck
= spinning; motoron check = 1'b0;
fillvalue check = 1'b0;
drainvalue check = 1'b0;
doorlock_check = 1'b1;
detergent wash = 1'b1;
checkwater wash = 1'b1; done =
1'b0; end end else begin
nextstatecheck = currentstatecheck;
motoron check = 1'b0;
fillvalue check = 1'b0;
drainvalue check = 1'b1;
doorlock check = 1'b1;
detergent_wash = 1'b1;
checkwater wash = 1'b1; done =
1'b0;
end
//drying the clothes which are drained.
spinning: if(spin timeout check==1'b1)
begin nextstatecheck = checkdoor;
motoron_check = 1'b0; fillvalue_check =
1'b0; drainvalue check = 1'b0;
doorlock check = 1'b1; detergent wash =
1'b1; checkwater wash = 1'b1; done =
1'b1; end else begin nextstatecheck =
currentstatecheck; motoron check =
1'b0; fillvalue check = 1'b0;
drainvalue check = 1'b1; doorlock check
= 1'b1; detergent wash = 1'b1;
checkwater wash = 1'b1; done = 1'b0;
end default: begin nextstatecheck =
checkdoor; motoron check = 1'b0;
```

```
fillvalue check = 1'b0;
drainvalue check = 1'b0;
doorlock check = 1'b1; detergent wash
= 1'b1; checkwater wash = 1'b1; done
= 1'b1; end endcase end
always@(posedge clk or posedge reset)
begin if(reset) begin
currentstatecheck <= 3'b000; end else
begin
currentstatecheck <= nextstatecheck;
end end endmodule
Test bench
`timescale 1ns / 1ps
// Module Name: washing tb
//// module WB_TB(); reg clk, reset; reg [255:0] closedoor; reg
[127:0] startmachine; reg [127:0] filledmachine; reg [127:0]
detergentadded; reg [127:0] machinecycle timeout; reg [127:0]
waterdrained; reg [127:0] spin timeout check; wire [127:0]
doorlock check;
wire [127:0] motoron check;
wire [127:0] fillvalue check;
wire [127:0]
drainvalue check; wire
 [127:0] done; wire [127:0]
 detergent wash; wire [127:0]
 checkwater wash;
washingmachine machinel(clk, reset, closedoor, startmachine,
filledmachine, detergentadded, machinecycle timeout,
waterdrained, spin timeout check, doorlock check,
motoron check, fillvalue check, drainvalue check,
done, detergent wash, checkwater wash); initial begin clk =
8'b0; reset = 8'b1; startmachine = 8'b0; closedoor = 8'b0;
filledmachine = 8'b0; waterdrained = 8'b0; detergentadded =
8'b0; machinecycle timeout = 8'b0; spin timeout check = 8'b0;
```

```
#10 reset=8'b0;
#10 startmachine=8'b1;closedoor=8'b1;
#20 filledmachine=8'b1;
#20 detergentadded=8'b1;
#20 machinecycle_timeout=8'b1;
#20 waterdrained=8'b1; #20
spin_timeout_check=8'b1; end
always begin #10 clk = ~clk;
end endmodule
```

Behavioral and Synthesized waveform

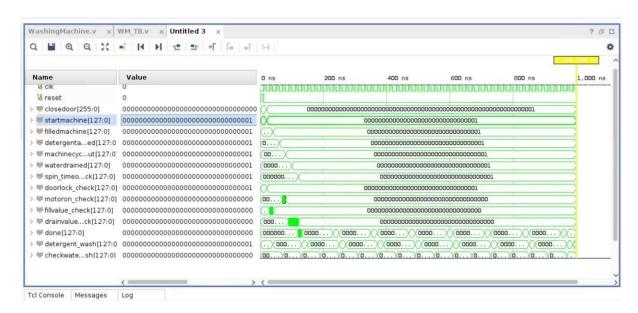
As Finite State Machines are used to create many real-life appliances, as a part of it we have implemented the design of the washing machine which used 6 finite states. The 6 finite states

are as follows

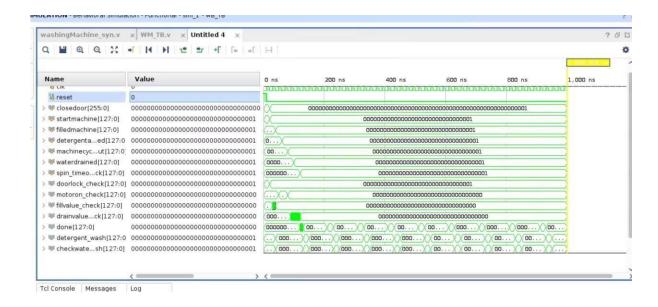
- Closing the door:
- o Washing machine starts when the door is closed and locked.
- Filling the water:
- o Washing machine is filled with water which is used for soaking the clothes.
- Adding detergent/soap:
- o Washing machine uses detergent/soap to clean and wash the clothes.
- Cycle for wash:
- o Cycle for wash is used by the washing machine to wash the clothes for certain time.
- Draining:
- o Wet clothes will be drained after washing and cleaning them.
- Spinning:
- o Spinning is used for drying the wet clothes.

There are 9 inputs and 7 outputs in this finite state design. It also contains about 6 stage parameters. To toggle between the states, we have used switch case scenarios. There are additional 2 registers namely current and next states which are used in the code.

Behavioral waveform

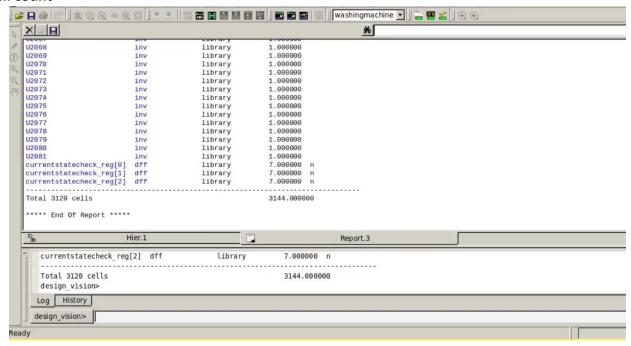


Synthesized waveform

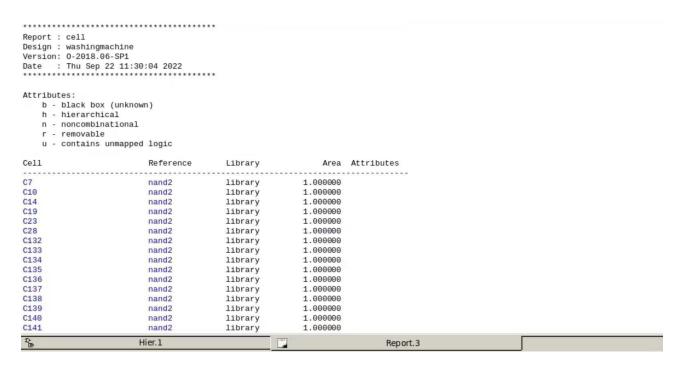


As observed, we were able to successfully generate the same waveforms. All the 6 stages are clearly generated in both the behavioral and synthesized waveforms.

Cell count



The above screenshot shows total of 3120 cells



The above screenshot shows the start process

40	4	146	4 000000		
110	inv	library	1.000000		
11	nand3	library	1.000000		
12	nand2	library	1.000000		
13	nand2	library	1.000000		
14	nand3	library	1.000000		
15	nor2	library	1.000000		
16	nor3	library	1.000000		
17	inv	library	1.000000		
18	nand4	library	1.000000		
19	aoi22	library	2.000000		
20	nand2	library	1.000000		
21	nand4	library	1.000000		
122	aoi12	library	2.000000		
23	inv	library	1.000000		
124	inv	library	1.000000		
25	nor2	library	1.000000		
26	nor2	library	1.000000		
27	inv	library	1.000000		
128	oai22	library	2.000000		
129	nand3	library	1.000000		
130	inv	library	1.000000		
131	nor3	library	1.000000		
132	nor2	library	1.000000		
133	inv	library	1.000000		
134	aoi22	library	2.000000		
135	nand3	library	1.000000		
136	inv	library	1.000000		
J37	nand2	library	1.000000		
J38	nand2	library	1.000000		
139	inv	library	1.000000		
J40	nand4	library	1.000000		
J41	inv	library	1.000000		
	1112	111	4 00000		
E	Hier.1		1001	Report.3	
ge mouse cursor t	to tool used to highlight object	s.			
	atashash mas[0]	dff		library	7.000000
***************************************	atecheck reg[0]	all		IIDIAIY	7.000000
currentst	atecheck reg[1]	dff		library	7.000000
		dff		library	7.000000
currentst	atecheck reg[2]	ull		TINICITY	
currentst	atecheck_reg[2]				
currentst	atecheck reg[2] 				

The above screenshot shows the DFF units and other gates

Conclusion:

As observed, we were able to successfully generate the same waveforms. All the 6 stages are clearly generated in both the behavioral and synthesized waveforms.