

EEDG/CE 6303: Testing and Testable Design (Spring'2023)

Department of Electrical & Computer Engineering

The University of Texas at Dallas

Instructor: Mehrdad Nourani (nourani@utdallas.edu)

Cover Page for All Submissions

(Assignment, Project, Codes/Simulations/CAD, Examinations, etc.)

Last Name (as shown in the official UT Dallas Student ID Card): Annadata

First Name: Yagna Srinivasa Harsha

Submission Materials for (e.g. Homework #, Project #): Homework - 5

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I certify that:

- i. the attached report (for assignment, project, codes/simulations/CAD, examinations, etc.) is my own work, based on my personal study and/or research,
- ii. I have acknowledged all material and sources used in its preparation, whether they be books, articles, reports, lecture notes, and any other kind of document, electronic or personal communication,
- iii. this report has not previously been submitted for assessment in EEDG/CE 6303 or any other course at UT Dallas or elsewhere,
- iv. I have not copied in part or whole or otherwise plagiarized the work of other students and/or persons, and
- v. I have read and understood the Department and University policies on scholastic dishonesty as outlined in: <http://www.utdallas.edu/deanofstudents/dishonesty/>.

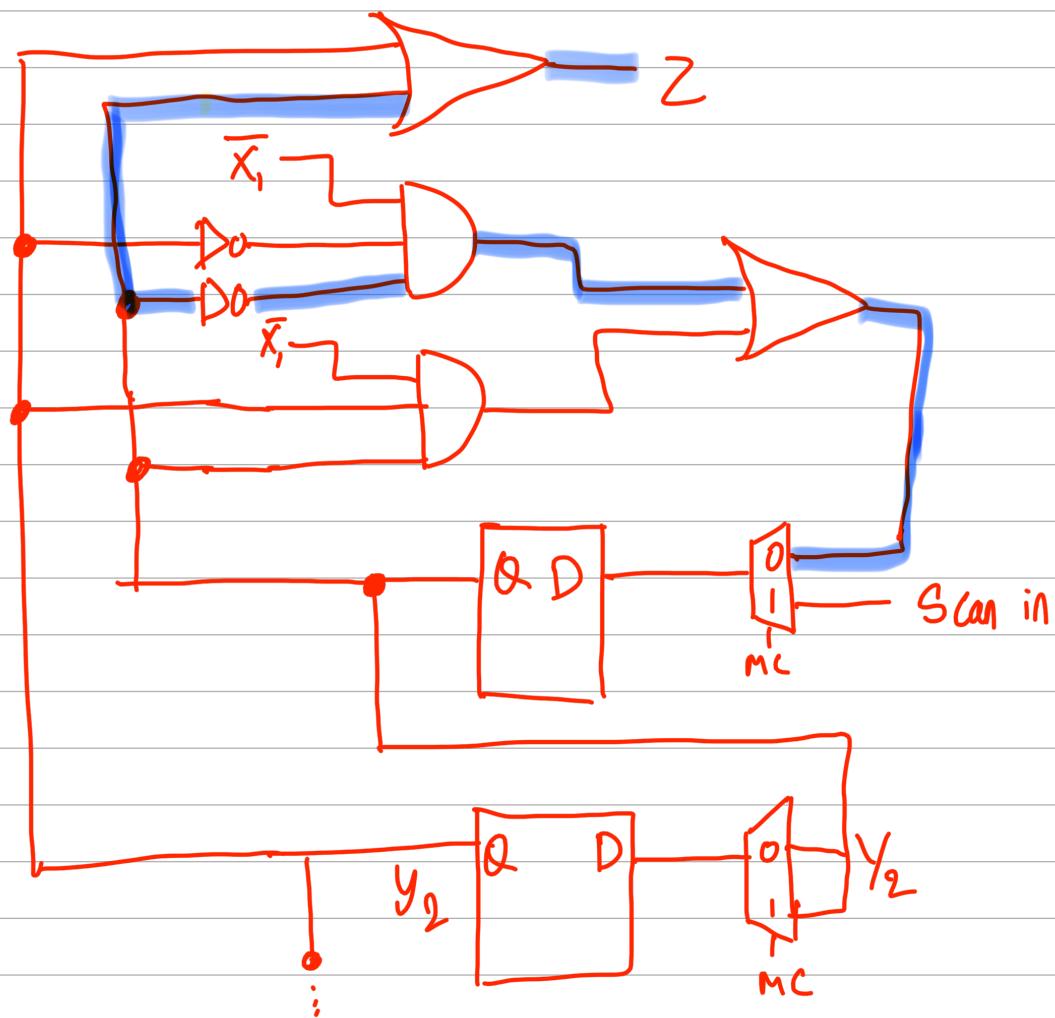
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Signature: _____

Q. 11.5

(a)



assuming gate with k -inputs have k -delays

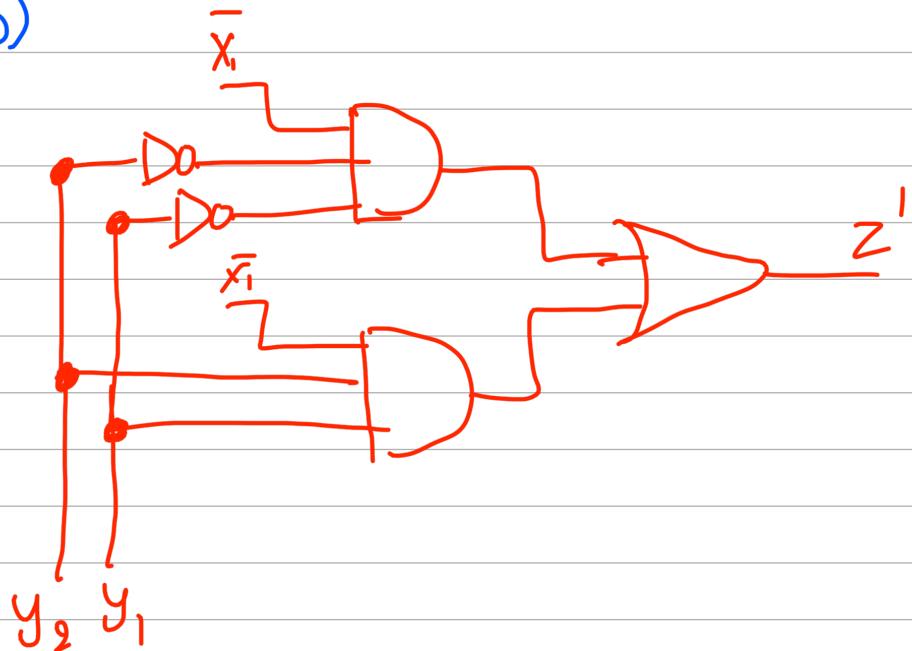
$$\text{Critical Path} = \text{INV} + \text{AND3} + \text{OR2} + \text{MUX2:1}$$

$$= 1k + 3k + 2k + 3k = 9k.$$

\therefore minimum clock period = $9k$.

In non-scan version, MUX is not present
hence there is a penalty = $3k$.

(b)

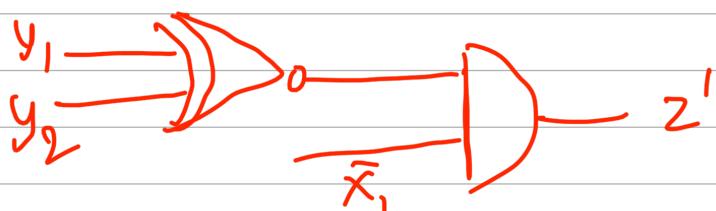


above diagram is the redesigned combinational logic.

Truth table:

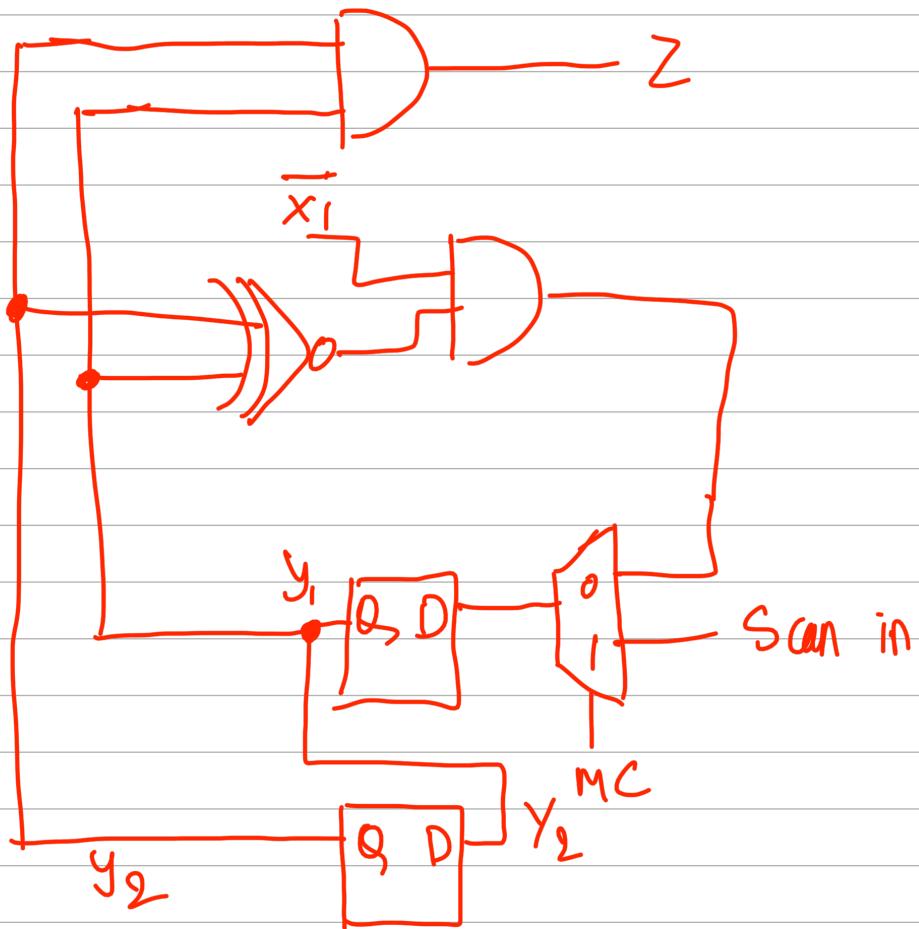
y_1	y_2	\bar{x}_1	z'
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

From truth table we can redesign



We can remove the extra mux at y_2

Redesigned circuit :



Critical path : $XNOR_2 + AND_2 + MUX_{2:1}$

$$\Rightarrow 2K + 2K + 3K = 7K$$

minimum clock period = 7 ns .

Still the penalty is $3K$ due to $MUX_{2:1}$

(C) area of original = 8 combination
+ 2 sequential
= 10 gates.

area of redesigned = 4 combi + 2 seq/
= 6 gates.

Area over head is

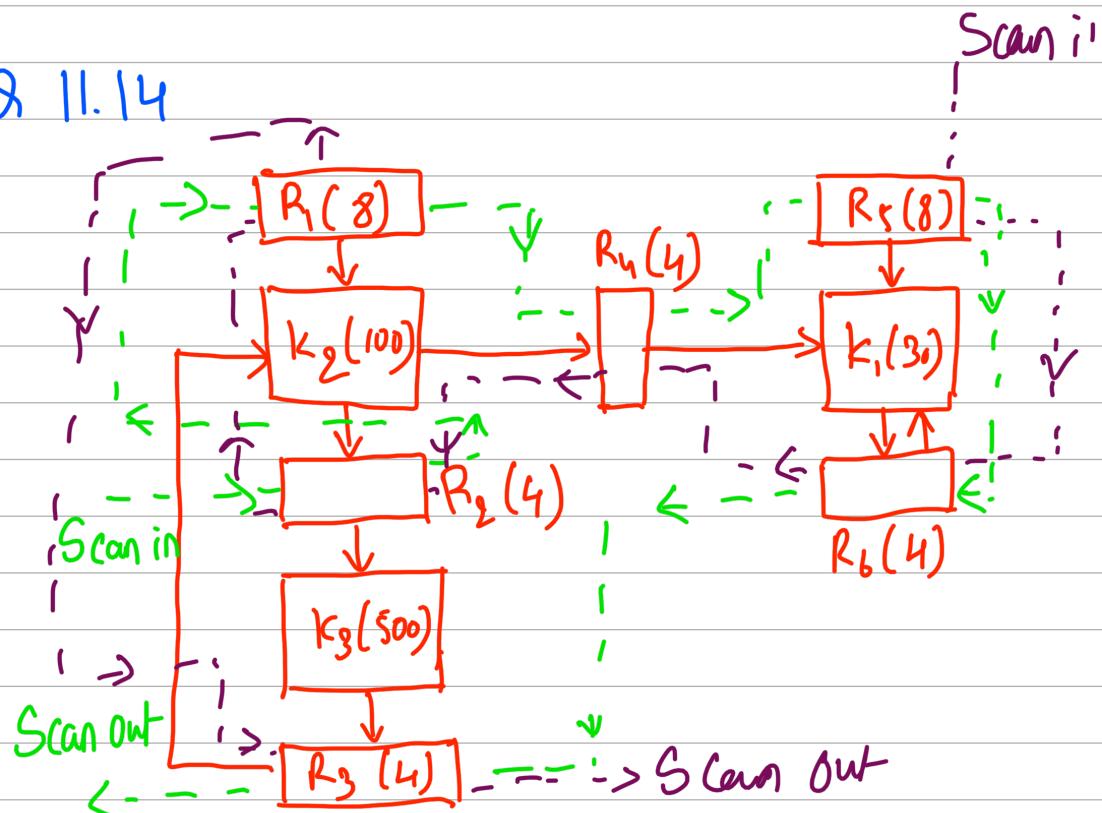
4 gates less for redesigned circuit

Performance of original = 9K.

Performance or redesigned = 7K.

penalty reduces by $2k$

for redesigned circuit



Register	bit width	Type	DRW	R/W
R1	8	Driver	100	0
R2	4	Driver / Receiver	500	100
R3	4	Driver / receiver	100	500
R4	4	Driver / receiver	30	100
R5	8	Driver	30	0
R6	4	Driver / receiver	30	30

Since R2 has highest driving weight, the scan chain can start at R2 and end at R3

$$R_2 \rightarrow R_1 \rightarrow R_4 \rightarrow R_5 \rightarrow R_6 \rightarrow R_3$$

3 - test sessions

#1 → 30 vectors applicable to k_1, k_2, k_3

#2 → 70 vectors applicable to k_2 and k_3

#3 → 400 vectors applicable to k_3

number of cycles: $n_{\text{comb}}(n_{\text{SFF}} + 1) + (n_{\text{YFF}} - 1)$ for single test session.

$$\Rightarrow 30 \frac{(32+1)}{(32-1)} + 70 (32+1) + 400 (4+1) + \\ = 5331 \text{ cycles.}$$

Q 11.15

Register	bit width	Type	DRW	RCW
R1	8	Driver	100	0
R2	4	Driver / Receiver	500	100
R3	4	Driver / Receiver	100	500
R4	4	Driver / Receiver	1000	100
R5	8	Driver	1000	0
R6	4	Driver / Receiver	1000	1000

Since R5 has highest we start from R5 and with R6 at end but since R4, R6

are drivers they cannot be at the end.
R₃ can be taken as end.

$$R_5 \rightarrow R_6 \rightarrow R_4 \rightarrow R_2 \rightarrow R_1 \rightarrow R_3$$

Session 1:

$$k_2 < k_3 < k_1 \Rightarrow 100 \text{ test vectors}$$

$$\begin{aligned} \text{Driving registers} &= R_5, R_6, R_4, R_2, R_1, R_3 \\ &= 8 + 4 + 4 + 4 + 8 + 4 \\ &= 32 \end{aligned}$$

$$\begin{aligned} \text{Receiving register} &= R_2, R_4, R_6, R_3 \\ &= 4 + 4 + 4 + 4 + 8 \\ &= 24 \end{aligned}$$

$$SC_{\text{sess 1}} = 32$$

Session 2:

$$k_3 < k_1 \Rightarrow 400 \text{ Test vectors}$$

$$\begin{aligned} \text{Driving registers} &= R_5, R_6, R_4, R_2 \\ &= 8 + 4 + 4 + 4 \\ &= 20 \end{aligned}$$

$$\begin{aligned} \text{Receiving register} &= R_2, R_4, R_6, R_3 \\ &= 4 + 8 + 4 + 4 = 20 \end{aligned}$$

$$SC_{\text{sess 2}} = 20$$

Section 3:

K1 \Rightarrow 500 test vectors

Driving registers = R5, R6, R4

$$= 8 + 4 + 4 = 16$$

Receiving registers = R2, R4, R1, R3

$$= 4 + 8 + 4 + 4 = 20$$

SL miss 3 = 20

$$\text{Time} = 100(32+1) + 400(20+1) + 500(20+1) \\ + 32 - 1$$

$$= 3300 + 8400 + 10500 + 31$$

$$= 22231$$

Q11.16

Scan chain : R2 \rightarrow R1 \rightarrow R5 \rightarrow R6 \rightarrow R4 \rightarrow R3

T_{seq 1} = 30 Vectors

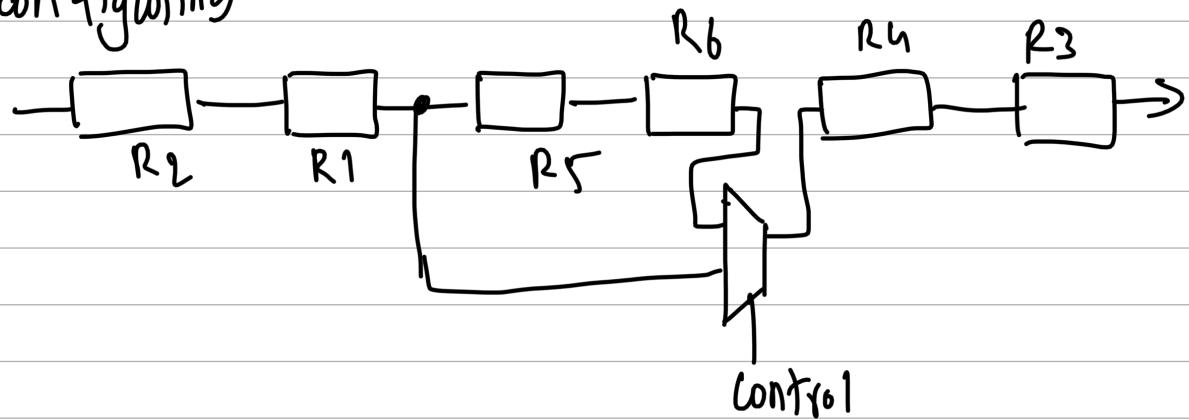
T_{seq 2} = 70 Vectors

T_{seq 3} = 400 Vectors

Chain :



Reconfiguring.



if $\text{control} = 0$, Truss 1 is performed &

if $\text{control} = 1$, Truss 2 is performed.

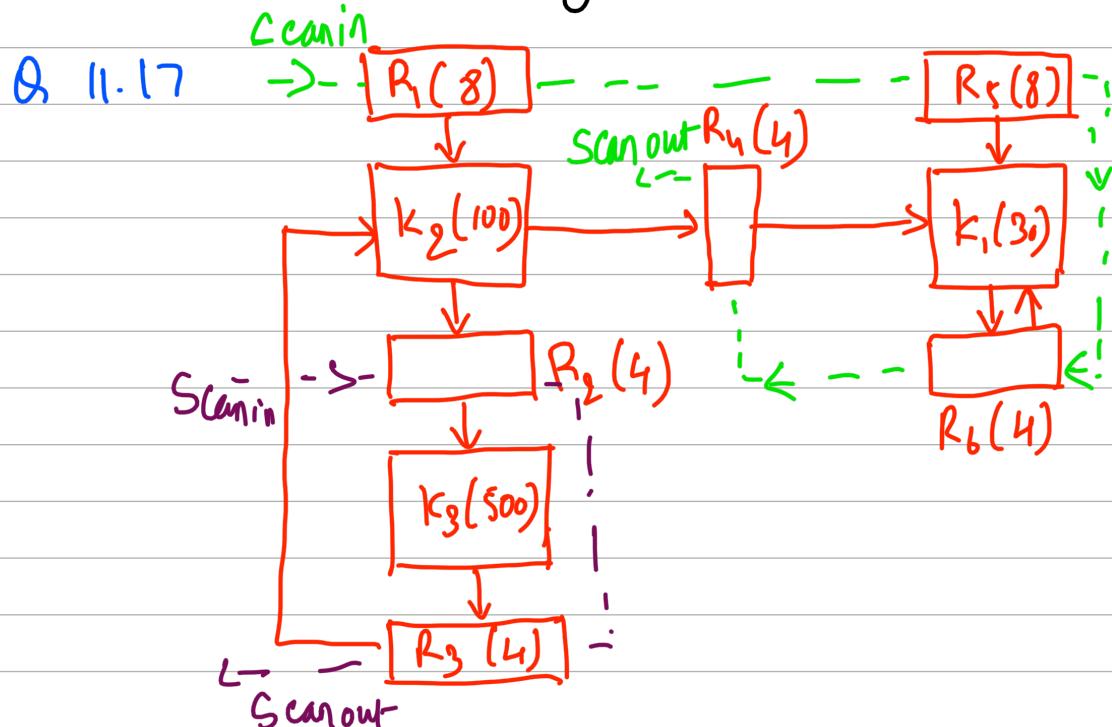
$$\text{Scan in (Truss 2)} = 4 + 8 + 4 + 4 = 20$$

$$\text{Scan out (Truss 2)} = 4 + 8 + 4 + 4 = 20$$

$$SC \text{ Truss 2} = 20$$

$$\text{Time} = 30(32+1) + 70(20+1) + 400(4+1) \\ + (32-1)$$

$$= 4491 \text{ cycles.}$$



Chain 1: R₁ → R₅ → R₆ → R₄

Chain 2: R₂ → R₃

Chain 1:

$$T_{M1S} 1 = 4 + 8 + 8 + 4 = 24$$

$$T_{M2S} 2 = 4 + 8 + 8 + 4 = 24$$

$$T_{M3S} 3 = 0$$

Chain 2:

$$T_{M1S} 1 = 4 + 4 = 8$$

$$T_{M2S} 2 = 4 + 4 = 8$$

$$T_{M3S} 3 = 4 + 4 = 8$$

Final

$$T_{M1S} 1 = 24$$

$$T_{M2S} 2 = 24$$

$$T_{M3S} 3 = 8$$

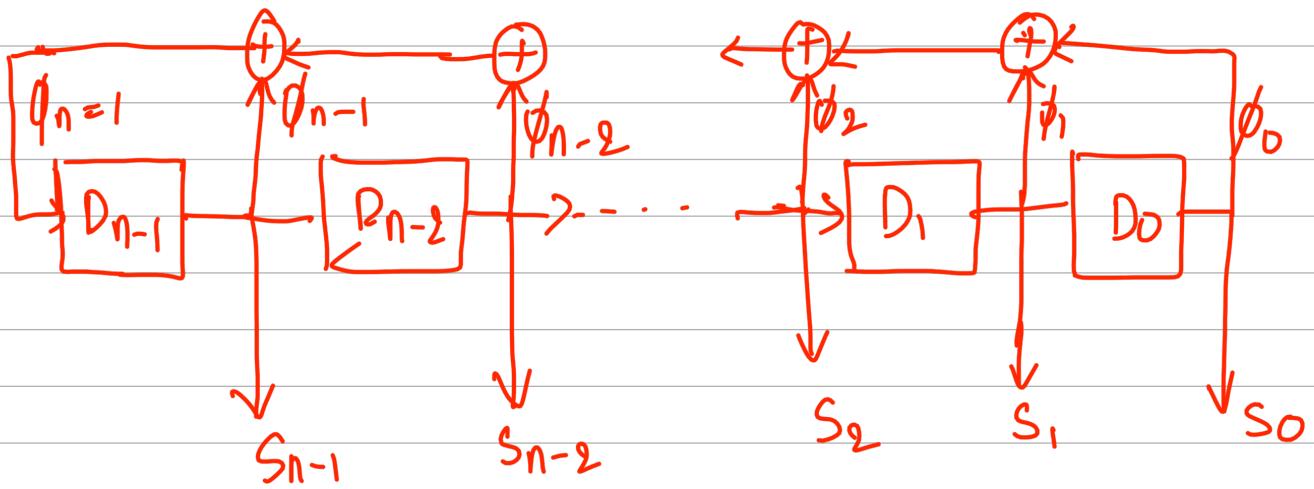
$$\text{Time} = 30(24+1) + 70(24+1) + 400(8+1) + 24 - 1$$

$$= 750 + 1750 + 3600 + 23$$

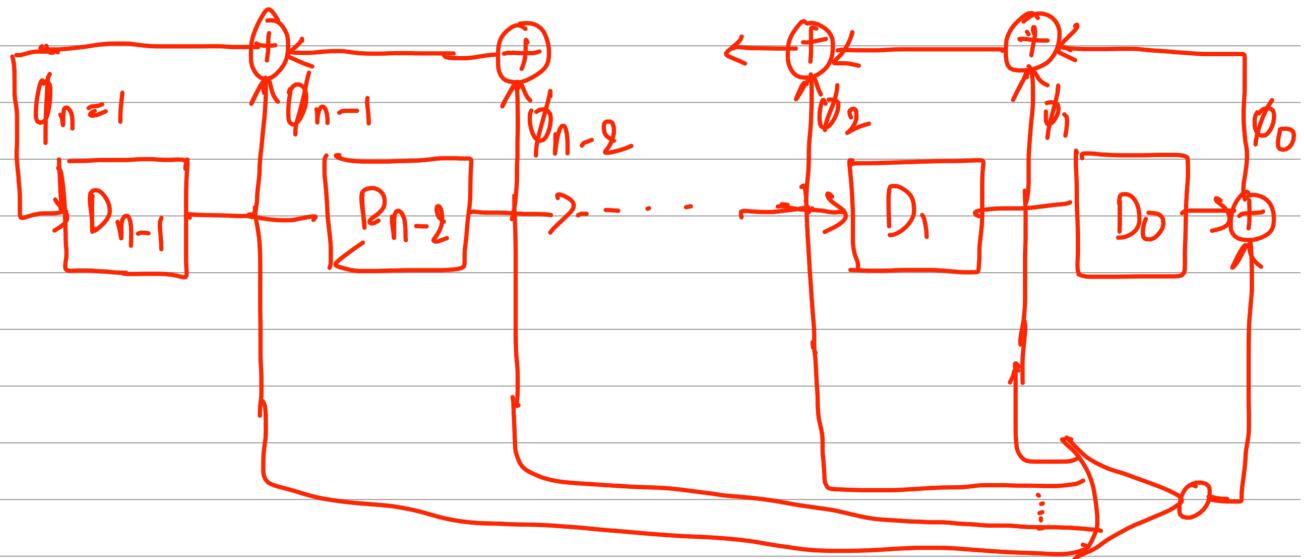
$$= 6123$$

Q 12.8

n - stage external LFSR.



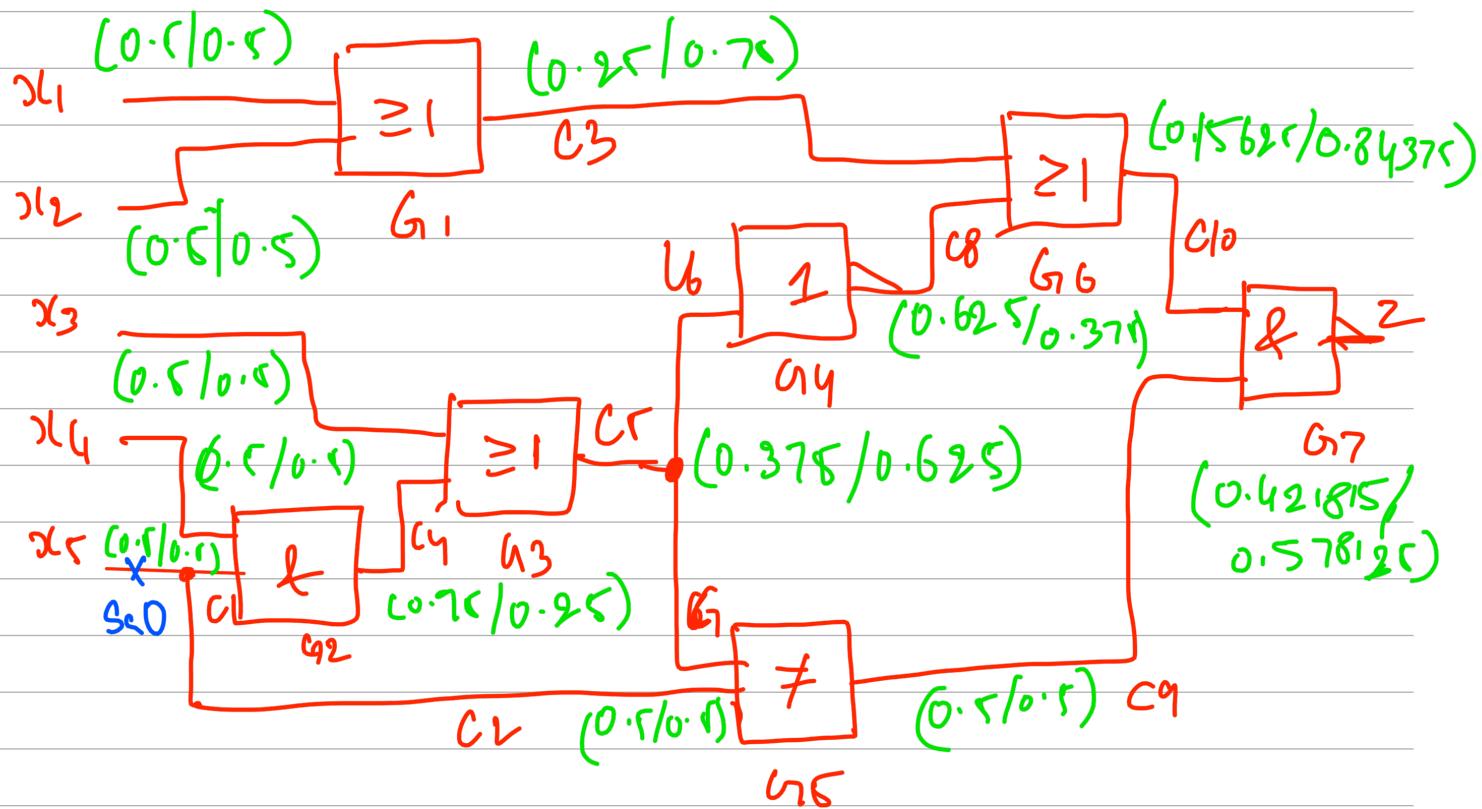
for generating a complete set of n -bit PVTs,
we can convert the above LFSR by adding $(n-1)$ bit
NOR and 2 bit XOR.



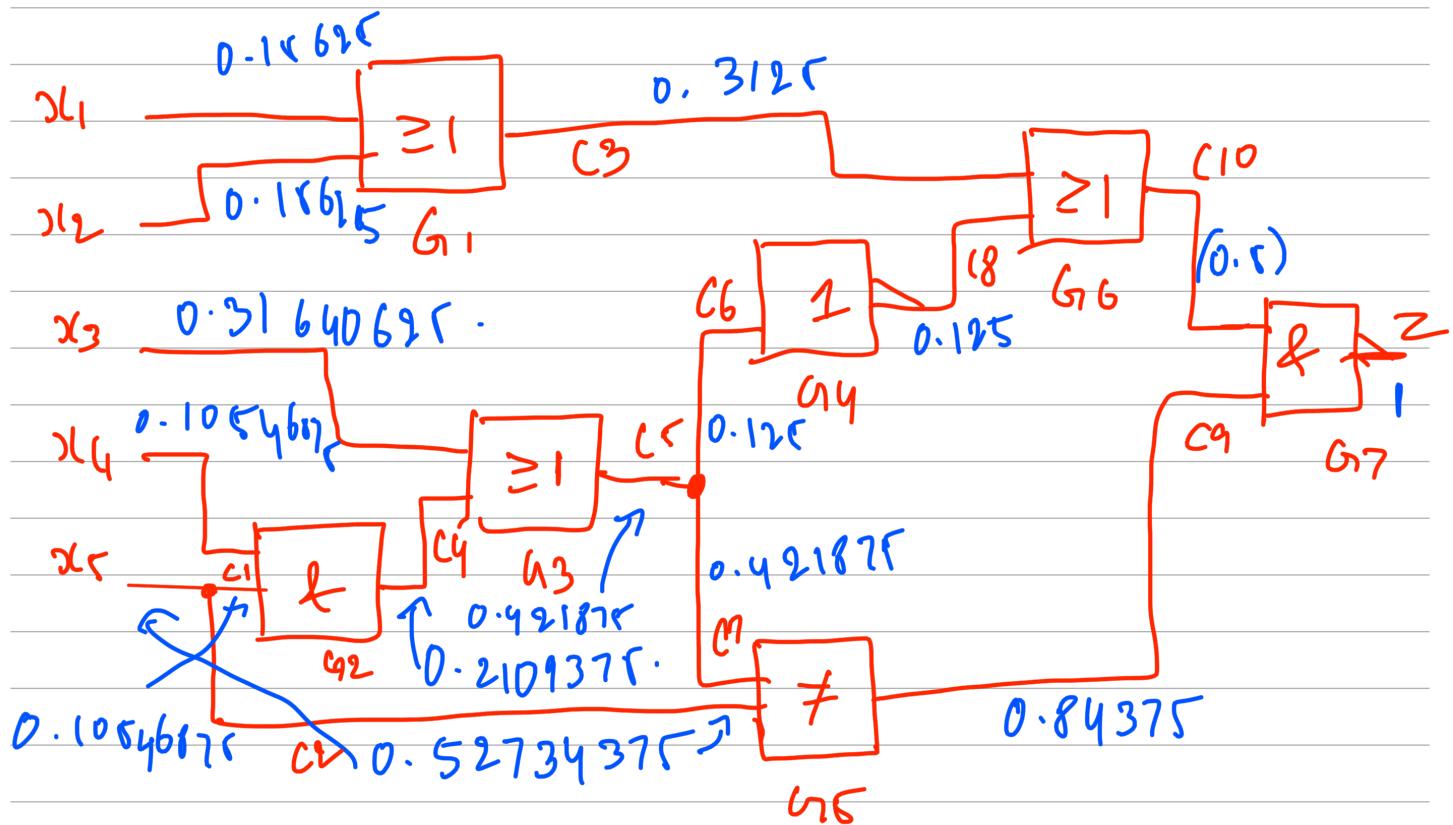
when LFSR has $00\dots01$, the output of NOR is 1 and last XOR injects 0. So, the next state will be $00\dots00$.

Q12-13

Controllability



Observability



Detectability:

$$\text{for } S_{10} : D_p(f) = (C_p^1(c_i) \cap P(c_i))$$

$$\text{for } S_{11} : D_p(f) = (C_p^0(c_i) \cap P(c_i))$$

	S_{10}	S_{11}
x_1	0.078125	0.08125
x_2	0.078125	0.078125
x_3	0.1582	0.1582
x_4	0.05273	0.05273
x_5	0.26367	0.26367
c_1	0.052734	0.052734
c_2	0.26367	0.26367
c_3	0.234375	0.078125
c_4	0.05273	0.15820
c_5	0.26367	0.15820
c_6	0.078125	0.046875
c_7	0.26367	0.15820
c_8	0.046875	0.078125
c_9	0.421875	0.421875
c_{10}	0.421875	0.078125
Z	0.578125	0.421875

Detectability Profile

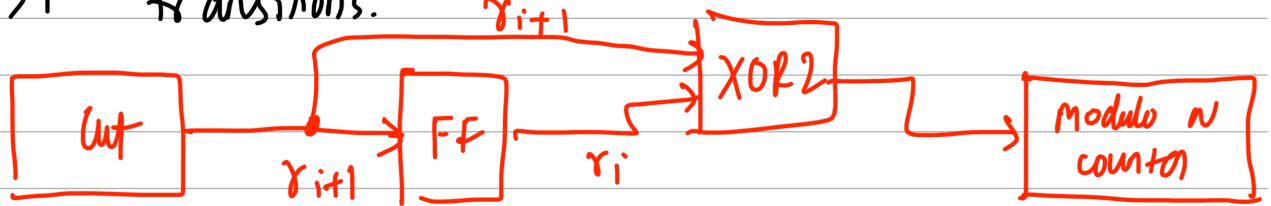
dividing the interval for 0-1 into ranges

of appropriate widths.

Range	# of faults
0 - 0.25	21
0.25 - 0.5	10
0.5 - 0.75	1
0.75 - 1	0

Q12.22

modified transition Count compressor to count
 $0 \rightarrow 1$ transitions.



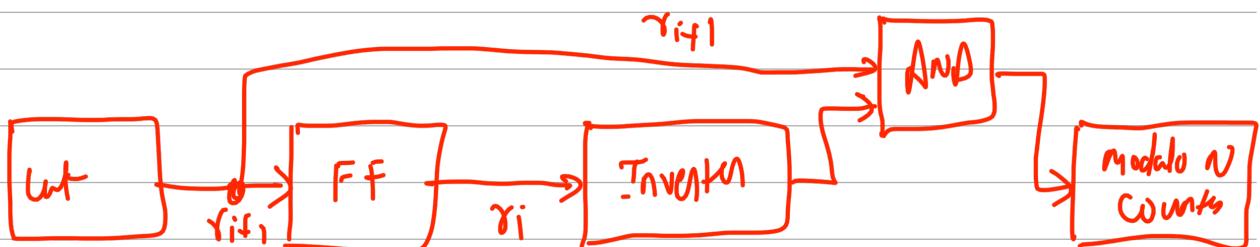
$$r_i \quad r_{i+1} \quad r_i \oplus r_{i+1}$$

0	0	0
0	1	1
1	0	1
1	1	0

for $0 \rightarrow 1$ transitions

$$r_i \quad r_{i+1} \quad (0 \text{ or } 1).$$

0	0	0
0	1	1
1	0	0
1	1	0

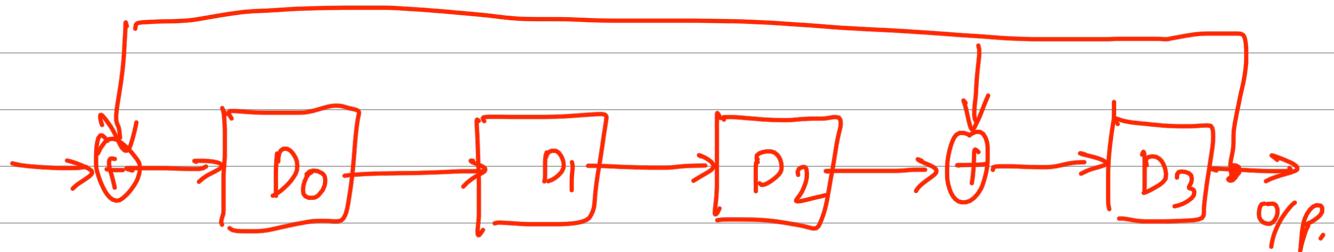


Q. 12-24

$$D(x) = x^6 + x^3 + 1$$

$$r_{LSR} \text{ (Ans)} = x^6 + x^4 + x^2 + x + 1$$

Ans = 1110101



Time	I/P	LFSR State	O/P.
-	-	0000	-
0	1	1000	0
1	0	0100	0
2	1	1010	0
3	0	0101	0
4	1	0011	1
5	1	0000	1
6	1	1000	0

$$\begin{array}{r}
 x^4 + x^3 + 1 \\
) \overline{x^2 + x} \\
 \overline{x^6 + 0 + x^4 + 0 + x^2 + x + 1} \\
 \overline{x^6 + x^5 +} \\
 \overline{ + x^2} \\
 \overline{x^5 + x^4 + 0 + 0 + x + 1} \\
 \overline{x^5 + x^4} \\
 \overline{ + x} \\
 |
 \end{array}$$

$$(1) \text{ Reg}(g_1) = x^5 + x^4 + x + 1$$

$$\begin{array}{r} x \\ \overline{x^4 + x^3 + 1} \\ \overline{x^5 + x^4 + x^3 + 1} \\ \hline x^5 + x^4 + x \\ \hline \end{array}$$

$$(2) \text{ Reg}(g_1) = x^6 + x^5 + x^2 + 1$$

$$\begin{array}{r} x^2 \\ \overline{x^4 + x^3 + 1} \\ \overline{x^6 + x^5 + x^3 + 1} \\ \hline x^6 + x^5 + x^2 \\ \hline \end{array}$$

Q12 25

$V \rightarrow$ vector sequence

m stage MISR Compressor

The equivalent MISR sequence obtained by

column wise XOR.

m_0	$a_{V,0}$	$a_{V-1,0}$	\dots	$a_{1,0}$
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m_1	$a_{V,1}$	\dots	$a_{2,1}, a_{1,1}$
\vdots	\vdots	\vdots	\vdots

m_V	$a_{V,V}$	\dots	$a_{1,W}$
-------	-----------	---------	-----------

\therefore the total length of sequence = $V + M - 1$

→ let $a_{n,n}$ be bits in sequence.

→ the # of error combinations is equivalent to LFSR sequence.

→ the equivalent LFSR error sequence is

$$(a_1, M), (a_1, M-1 \oplus a_2, M) \dots (a_{V-1} \oplus a_V, 2 \oplus \dots \oplus a_{V-1})$$

→ These responses will result in zero equivalent LFSR error sequence.

→ multipoint error sequences will result in aliasing independent of feedback polynomial.

→ Aliasing probability = $\frac{\text{ratio of aliasing volume}}{\text{possible circuit response.}}$

$$\therefore P_{MISR}(m) = \left[\frac{2^{(NL-M)}}{2^M - 1} \right] / \left[\frac{2^N}{2^M - 1} \right]$$

\therefore Probability of aliasing occurring is $2^M \times V$
 $\Rightarrow (V/2^M)$