

Micro-Processor and Embedded Systems

Lab-Session 1 Report for D-FlipFlop

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AIM: This week we were asked familiar with Xilinx vivado tool hence implemented D-flipflop in Xilinx.

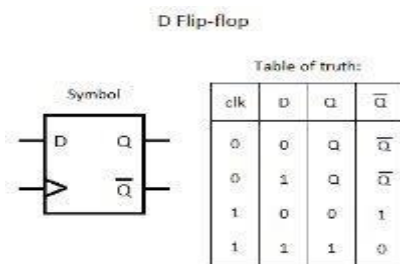
Summary:

1. Using Nomachine access the VIVADO By sourcing **/proj/cad/startup/profile.xilinx_vivado_18.3**.
2. Command to open the tool is **vivado&**
3. Create a new project on the software for ALU and registers.
4. ALU and register file Verilog codes along with the test benches have been complied successfully.
5. Ran the behavioral simulation for the test bench codes.

D-Flipflop:

Truth table

Data Input (D)	Clock (clk)	Output (q)	Inverted Output (q')
0	0	Q	Q'
1	0	Q	Q'
0	1	0	1
1	1	1	0



Characteristic equation: $Q_{n+1} = D$

Characteristic table

D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

Excitation table

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

for negative clock cycle the output in the d flipflop retains its previous value and for positive cycle the output of the d flipflop is the input 'd'.

in short, we can say that in d-flipflop for a positive cycle whatever input is sent in to the flipflop will be the output and for negative cycle output retains its previous value.

Code:

*****the code is written below*****

```
`timescale 1ns / 1ps
/////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 17:41:55 08/26/2022
// Design Name:
// Module Name: test2
// Project Name:
// Target Devices:
// Tool versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
/////////////////////////////////////////////////////////////////
module d_ff( d,clk,q,q_bar);
input d,clk;
```

```

output q,q_bar;
wire d,clk;
reg q,q_bar;
always @ (posedge clk)
begin
    q <= d;
    q_bar <= !d;
end
endmodule

```

Test Bench:

*****Test module*****

```

`timescale 1ns / 1ps
/////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 17:48:36 08/26/2022
// Design Name: d_ff
// Module Name: C:/Users/AXN220008/jc2_ver/d_ff_test.v
// Project Name: jc2_ver
// Target Device:
// Tool versions:
// Description:
//
// Verilog Test Fixture created by ISE for module: d_ff
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
/////////////////////////////////////////////////////////////////
module d_ff_test;
// Inputs
reg d;
reg clk;
// Outputs
wire q;
wire q_bar;
// Instantiate the Unit Under Test (UUT)
d_ff uut (
    .d(d),
    .clk(clk),
    .q(q),
    .q_bar(q_bar)
);

```

```
initial begin
// Initialize Inputs
d =0;
clk = 0;
end
// -----
always #50 clk = ~clk;
// -----
always #100 d = ~d;
initial begin
// Wait 1000 ns for global reset to finish
#1000 $stop;
End
End module
```

Conclusion:

We were able to successfully create the D-flipflop. I would like to learn more about vivado and create an MCU.

Attachments:

We have uploaded the screenshot of the simulation.