Micro-Processor and Embedded Systems Lab-Session 8 Report for Data Hazard and Branch Detection

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AIM: This week we have to introduce the MCU I/O module to the MCU using a top module.

Summary:

1. Using Nomachine access the VIVADO By sourcing **/proj/cad/startup/profile.xilinx_vivado_18.3.**
2. Command to open the tool is **vivado&**
3. Create a new project on the software for ALU and registers.
4. ALU and register file Verilog codes along with the test benches have been complied successfully.
5. Ran the behavioral simulation for the test bench codes.

Conclusion:

We have successfully implemented the MCU with the Verilog code in the Xilinx machine and generated a bitstream which was later loaded in to the Nexys3 Spartan-6.