TetraMAX(R)

Version O-2018.06-SP1 for linux64 - Jul 19, 2018


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  Tcl mode is on by default. Use -notcl to run in native mode.
  Executing startup file
"/proj/cad/synopsys/synopsys_2018/tmax_vO-2018.06-SP1/admin/setup/tmaxtcl.rc".
BUILD-T> read_netlist /home/011/y/yx/yxa210024/spring23/testing/src_ver/gtech_lib.v
  Begin reading netlist (
/home/011/y/yx/yxa210024/spring23/testing/src_ver/gtech_lib.v )...
 Warning: Rule N2 (unsupported construct) was violated 10 times.

  End parsing Verilog file
/home/011/y/yx/yxa210024/spring23/testing/src_ver/gtech_lib.v with 0 errors.
  End reading netlist: #modules=106, top=GTECH_ZERO, #lines=1976, CPU_time=0.00
sec, Memory=0MB
BUILD-T> read_netlist /home/011/y/yx/yxa210024/Q1_project6_combinational_1.v
  Begin reading netlist (
/home/011/y/yx/yxa210024/Q1_project6_combinational_1.v )...
  End parsing Verilog file /home/011/y/yx/yxa210024/Q1_project6_combinational_1.v
with 0 errors.
  End reading netlist: #modules=1, top=Q1_project6_combinational_1, #lines=20,
CPU_time=0.00 sec, Memory=0MB
BUILD-T> run_build_model Q1_project6_combinational_1
  ---------------------------------------------------------------------------
  Begin build model for topcut = Q1_project6_combinational_1 ...
  ---------------------------------------------------------------------------
  There were 2 primitives and 0 faultable pins removed during model optimizations
  End build model: #primitives=12, CPU_time=0.00 sec, Memory=0MB
  ---------------------------------------------------------------------------
  Begin learning analyses...
  End learning analyses, total learning CPU time=0.01 sec.
  ---------------------------------------------------------------------------
DRC-T> run_drc
  ---------------------------------------------------------------------------
  Begin scan design rules checking...
  ---------------------------------------------------------------------------
  Begin simulating test protocol procedures...
  Test protocol simulation completed, CPU time=0.00 sec.
  ---------------------------------------------------------------------------
  Begin scan chain operation checking...
  Scan chain operation checking completed, CPU time=0.00 sec.
  ---------------------------------------------------------------------------
  Begin nonscan rules checking...
  Nonscan cell summary: #DFF=0  #DLAT=0  #RAM_outs=0  tla_usage_type=none
  Nonscan rules checking completed, CPU time=0.00 sec.
  ---------------------------------------------------------------------------
  Begin DRC dependent learning...
  Fast-sequential depth results: control=0(0), observe=0(0), detect=0(0), CPU
time=0.00 sec
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  DRC dependent learning completed, CPU time=0.00 sec.
  ------------------------------------------------------------------------------
  DRC Summary Report
  ------------------------------------------------------------------------------
  No violations occurred during DRC process.
  Design rules checking was successful, total CPU time=0.00 sec.
  ------------------------------------------------------------------------------
TEST-T> remove_faults -all
  0 faults were removed from the fault list.
TEST-T> add_faults -all
  40 faults were added to fault list.
TEST-T> run_atpg -ndetects 1
  ATPG performed for stuck fault model using internal pattern source.
  ----------------------------------------------------------
  #patterns     #faults     #ATPG faults  test      process
  stored     detect/active  red/au/abort  coverage  CPU time
  ---------  -------------  ------------  --------  --------
  Begin deterministic ATPG: #uncollapsed_faults=40, abort_limit=10...
  5              40      0         0/0/0   100.00%      0.00

      Uncollapsed Stuck Fault Summary Report
  -----------------------------------------------
  fault class                     code   #faults
  ------------------------------  ----  ---------
  Detected                         DT         40
  Possibly detected                PT          0
  Undetectable                     UD          0
  ATPG untestable                  AU          0
  Not detected                     ND          0
  -----------------------------------------------
  total faults                                40
  test coverage                           100.00%
  -----------------------------------------------
            Pattern Summary Report
  -----------------------------------------------
  #internal patterns                           5
      #basic_scan patterns                     5
  -----------------------------------------------
TEST-T> report_faults -all
  sa0   DS   Y1
  sa0   --   U6/Z
  sa0   --   U6/A
  sa0   --   U6/B
  sa0   --   x1
  sa0   --   U7/Z
  sa1   DS   x1
  sa1   --   U6/A
  sa1   DS   Y1
  sa1   --   U6/Z
  sa1   DS   U7/Z
  sa1   --   U7/C
  sa1   --   U8/Z
  sa0   --   U8/A
  sa1   --   U6/B
  sa0   DS   U7/A
  sa0   --   U7/B
  sa1   DS   U7/A
  sa1   DS   U7/B
  sa0   DS   U8/Z
```

```
  sa1   --   U8/A
  sa0   --   U7/C
  sa0   DS   y1
  sa1   DS   y1
  sa0   DS   y2
  sa1   DS   y2
  sa0   DS   U9/Z
  sa1   DS   U9/Z
  sa1   --   U9/A
  sa0   --   U9/B
  sa0   --   U10/Z
  sa1   --   U10/A
  sa0   DS   U9/A
  sa1   DS   U10/Z
  sa0   --   U10/A
  sa1   --   U9/B
  sa0   DS   z
  sa1   DS   z
  sa0   DS   Y2
  sa1   DS   Y2
TEST-T> report_patterns -all -internal
  Pattern 0 (basic_scan)
  Time 0: force_all_pis =   111
  Time 1: measure_all_pos = 111
  Pattern 1 (basic_scan)
  Time 0: force_all_pis =   100
  Time 1: measure_all_pos = 010
  Pattern 2 (basic_scan)
  Time 0: force_all_pis =   110
  Time 1: measure_all_pos = 101
  Pattern 3 (basic_scan)
  Time 0: force_all_pis =   101
  Time 1: measure_all_pos = 100
  Pattern 4 (basic_scan)
  Time 0: force_all_pis =   000
  Time 1: measure_all_pos = 000
TEST-T>
```