TetraMAX(R)

Version O-2018.06-SP1 for linux64 - Jul 19, 2018


```
  Tcl mode is on by default. Use -notcl to run in native mode.
  Executing startup file
"/proj/cad/synopsys/synopsys_2018/tmax_vO-2018.06-SP1/admin/setup/tmaxtcl.rc".
BUILD-T> read_netlist /home/011/y/yx/yxa210024/spring23/testing/src_ver/gtech_lib.v
  Begin reading netlist (
/home/011/y/yx/yxa210024/spring23/testing/src_ver/gtech_lib.v )...
 Warning: Rule N2 (unsupported construct) was violated 10 times.

  End parsing Verilog file
/home/011/y/yx/yxa210024/spring23/testing/src_ver/gtech_lib.v with 0 errors.
  End reading netlist: #modules=106, top=GTECH_ZERO, #lines=1976, CPU_time=0.00
sec, Memory=0MB
BUILD-T> read_netlist /home/011/y/yx/yxa210024/Q1_project5_fig54_scan.v
  Begin reading netlist ( /home/011/y/yx/yxa210024/Q1_project5_fig54_scan.v )...
  End parsing Verilog file /home/011/y/yx/yxa210024/Q1_project5_fig54_scan.v with 0
errors.
  End reading netlist: #modules=5, top=Q1_project5_fig54_1, #lines=22,
CPU_time=0.00 sec, Memory=0MB
BUILD-T> run_build_model Q1_project5_fig54_1
  ------------------------------------------------------------------------------
  Begin build model for topcut = Q1_project5_fig54_1 ...
  ------------------------------------------------------------------------------
 Error: Module ( Q1_project5_fig54_1 ) referenced undefined module ( OR2I ). (B5-1)

 Warning: Current simulation model is now deleted. (M39)

BUILD-T> read_netlist /home/011/y/yx/yxa210024/spring23/testing/LIB/class.v
  Begin reading netlist (
/home/011/y/yx/yxa210024/spring23/testing/LIB/class.v )...
  End parsing Verilog file /home/011/y/yx/yxa210024/spring23/testing/LIB/class.v
with 0 errors.
  End reading netlist: #modules=125, top=BIDI, #lines=1039, CPU_time=0.00 sec,
Memory=0MB
BUILD-T> read_netlist /home/011/y/yx/yxa210024/Q1_project5_fig54_scan.v
  Begin reading netlist ( /home/011/y/yx/yxa210024/Q1_project5_fig54_scan.v )...
 Warning: Rule N5 (redefined module) was violated 1 times.

  End parsing Verilog file /home/011/y/yx/yxa210024/Q1_project5_fig54_scan.v with 0
errors.
  End reading netlist: #modules=0, top=BIDI, #lines=22, CPU_time=0.00 sec,
Memory=0MB
BUILD-T> run_build_model Q1_project5_fig54_1
  ------------------------------------------------------------------------------
  Begin build model for topcut = Q1_project5_fig54_1 ...
  ------------------------------------------------------------------------------
  There were 4 primitives and 0 faultable pins removed during model optimizations
```

```
 Warning: Rule N20 (underspecified UDP) was violated 1 times.

  End build model: #primitives=13, CPU_time=0.00 sec, Memory=0MB
  ---------------------------------------------------------------------------
  Begin learning analyses...
  End learning analyses, total learning CPU time=0.00 sec.
  ---------------------------------------------------------------------------
DRC-T> run_drc
  ---------------------------------------------------------------------------
  Begin scan design rules checking...
  ---------------------------------------------------------------------------
  Begin simulating test protocol procedures...
  Test protocol simulation completed, CPU time=0.00 sec.
  ---------------------------------------------------------------------------
  Begin scan chain operation checking...
  Scan chain operation checking completed, CPU time=0.00 sec.
  ---------------------------------------------------------------------------
  Begin clock rules checking...
 Warning: Rule C2 (unstable nonscan DFF when clocks off) was violated 2 times.

  Clock rules checking completed, CPU time=0.00 sec.
  ---------------------------------------------------------------------------
  Begin nonscan rules checking...
  Nonscan cell summary: #DFF=2  #DLAT=0  #RAM_outs=0  tla_usage_type=none
  Nonscan behavior:  #CU=2
  Nonscan rules checking completed, CPU time=0.00 sec.
  ---------------------------------------------------------------------------
  Begin DRC dependent learning...
  Fast-sequential depth results: control=0(0), observe=0(0), detect=0(0), CPU
time=0.00 sec
  DRC dependent learning completed, CPU time=0.00 sec.
  ---------------------------------------------------------------------------
  DRC Summary Report
  ---------------------------------------------------------------------------
 Warning: Rule C2 (unstable nonscan DFF when clocks off) was violated 2 times.

  There were 2 violations that occurred during DRC process.
  Design rules checking was successful, total CPU time=0.00 sec.
  ---------------------------------------------------------------------------
TEST-T> remove_faults -all
  0 faults were removed from the fault list.
TEST-T> add_faults -all
  56 faults were added to fault list.
TEST-T> run_atpg full_sequential_only
  ***********************************************************
  *  NOTICE:  The following DRC violations were previously  *
  *  encountered. The presence of these violations is an    *
  *  indicator that it is possible that the ATPG patterns   *
  *  created during this process may fail in simulation.    *
  *                                                         *
  *  Rules:  N20                                            *
  ***********************************************************
  ATPG performed for stuck fault model using internal pattern source.

  ------------------------------------------------------------
  Begin Full-Sequential ATPG for 56 uncollapsed faults ...
   --- abort limit : 10 seconds, NO BACKTRACK LIMIT
  ------------------------------------------------------------
  #patterns  #faults        #ATPG faults  test       process
```

```
  stored     detect/active  red/au/abort  coverage   CPU time
  ---------  -------------  ------------  --------  ----------
  1                 31     25          0/0/1     63.39%         20.02
  2                  7     18          0/0/1     75.89%         20.02
  3                  4     12          0/2/1     83.04%         20.02
  3                  0      2          0/8/2     83.04%         42.73
  4 faults were identified as detected by implication, test coverage is now 86.61%.

      Uncollapsed Stuck Fault Summary Report
  -----------------------------------------------
  fault class                     code   #faults
  ------------------------------  ----  ---------
  Detected                         DT         46
  Possibly detected                PT          5
  Undetectable                     UD          0
  ATPG untestable                  AU          5
  Not detected                     ND          0
  -----------------------------------------------
  total faults                                56
  test coverage                            86.61%
  -----------------------------------------------
             Pattern Summary Report
  -----------------------------------------------
  #internal patterns                           3
      #full_sequential patterns                3
  -----------------------------------------------
TEST-T> report_faults -all
  sa1   NP   x1
  sa1   NP   __tmp103/B
  sa1   DS   __tmp106/p_dreg0/d
  sa1   DI   __tmp106/p_dreg0/cp
  sa0   DI   __tmp106/p_dreg0/cp
  sa0   DS   __tmp106/p_dreg0/q
  sa0   DS   __tmp106/p_dreg0/d
  sa1   DS   __tmp106/p_dreg0/q
  sa1   DS   __tmp105/Q
  sa1   --   __tmp105/p_dreg0/q
  sa0   DS   __tmp105/Q
  sa0   --   __tmp105/p_dreg0/q
  sa1   DS   __tmp104/Z
  sa1   --   __tmp104/A
  sa1   --   __tmp104/B
  sa1   --   __tmp102/Z
  sa1   --   __tmp103/Z
  sa1   --   __tmp105/p_dreg0/d
  sa0   AN   __tmp103/Z
  sa0   --   __tmp103/B
  sa0   --   __tmp103/A
  sa0   --   __tmp103/C
  sa0   --   __tmp104/B
  sa1   AP   __tmp102/B
  sa1   DS   __tmp103/C
  sa1   DS   __tmp100/Z
  sa0   --   __tmp100/A
  sa1   --   __tmp102/A
  sa0   DI   __tmp105/p_dreg0/cp
  sa1   DI   __tmp105/p_dreg0/cp
  sa1   DS   __tmp103/A
  sa1   DS   __tmp101/Z
```

```
  sa0   --   __tmp101/A
  sa1   --   __tmp102/C
  sa0   DS   __tmp104/Z
  sa0   --   __tmp105/p_dreg0/d
  sa0   DS   __tmp102/Z
  sa0   --   __tmp102/B
  sa0   --   __tmp102/A
  sa0   --   __tmp102/C
  sa0   --   __tmp100/Z
  sa1   --   __tmp100/A
  sa0   --   __tmp101/Z
  sa1   --   __tmp101/A
  sa0   --   __tmp104/A
  sa1   DS   z
  sa1   --   __tmp107/Z
  sa1   --   __tmp107/A
  sa1   --   __tmp107/B
  sa0   DS   __tmp107/B
  sa0   DS   z
  sa0   --   __tmp107/Z
  sa0   DS   __tmp107/A
  sa0   DS   x1
  sa1   AP   clk
  sa0   AP   clk
TEST-T> report_patterns -all -internal
  Pattern 0 (full_sequential)
  Time 0: period = 100
  Time 0: force_all_pis =   00
  Time 140: measure_all_pos =X
  Time 200: force_all_pis = 11
  Time 340: measure_all_pos =X
  Time 400: force_all_pis = 00
  Time 540: measure_all_pos =X
  Time 600: force_all_pis = 11
  Time 740: measure_all_pos =0
  Time 800: force_all_pis = 10
  Time 940: measure_all_pos =0
  Time 1000: force_all_pis =01
  Time 1140: measure_all_pos =1
  Time 1200: force_all_pis =00
  Time 1340: measure_all_pos =1
  Pattern 1 (full_sequential)
  Time 0: period = 100
  Time 0: force_all_pis =   00
  Time 140: measure_all_pos =1
  Time 200: force_all_pis = 11
  Time 340: measure_all_pos =1
  Time 400: force_all_pis = 00
  Time 540: measure_all_pos =1
  Time 600: force_all_pis = 11
  Time 740: measure_all_pos =0
  Time 800: force_all_pis = 10
  Time 940: measure_all_pos =0
  Time 1000: force_all_pis =01
  Time 1140: measure_all_pos =1
  Time 1200: force_all_pis =00
  Time 1340: measure_all_pos =1
  Time 1400: force_all_pis =01
  Time 1540: measure_all_pos =1
```

```
  Time 1600: force_all_pis =10
  Time 1740: measure_all_pos =1
  Time 1800: force_all_pis =01
  Time 1940: measure_all_pos =0
  Pattern 2 (full_sequential)
  Time 0: period = 100
  Time 0: force_all_pis =   00
  Time 140: measure_all_pos =0
  Time 200: force_all_pis = 01
  Time 340: measure_all_pos =0
  Time 400: force_all_pis = 00
  Time 540: measure_all_pos =0
  Time 600: force_all_pis = 11
  Time 740: measure_all_pos =0
  Time 800: force_all_pis = 10
  Time 940: measure_all_pos =0
  Time 1000: force_all_pis =01
  Time 1140: measure_all_pos =1
  Time 1200: force_all_pis =10
  Time 1340: measure_all_pos =1
  Time 1400: force_all_pis =11
  Time 1540: measure_all_pos =1
  Time 1600: force_all_pis =00
  Time 1740: measure_all_pos =1
  Time 1800: force_all_pis =00
  Time 1940: measure_all_pos =1
  Time 2000: force_all_pis =11
  Time 2140: measure_all_pos =0
TEST-T> drc -force
 Warning: Internal pattern set is now deleted. (M133)

TEST-T> read_netlist /home/011/y/yx/yxa210024/Q1_project5_fig54_1.v
 Warning: Current simulation model is now deleted. (M39)

  Begin reading netlist ( /home/011/y/yx/yxa210024/Q1_project5_fig54_1.v )...
 Warning: Rule N5 (redefined module) was violated 1 times.

  End parsing Verilog file /home/011/y/yx/yxa210024/Q1_project5_fig54_1.v with 0
errors.
  End reading netlist: #modules=0, top=BIDI, #lines=22, CPU_time=0.00 sec,
Memory=0MB
BUILD-T> run_build_model Q1_project5_fig54_1
  ----------------------------------------------------------------------------
  Begin build model for topcut = Q1_project5_fig54_1 ...
  ----------------------------------------------------------------------------
  There were 3 primitives and 0 faultable pins removed during model optimizations
  End build model: #primitives=13, CPU_time=0.00 sec, Memory=0MB
  ----------------------------------------------------------------------------
  Begin learning analyses...
  End learning analyses, total learning CPU time=0.00 sec.
  ----------------------------------------------------------------------------
DRC-T> run_drc
  ----------------------------------------------------------------------------
  Begin scan design rules checking...
  ----------------------------------------------------------------------------
  Begin simulating test protocol procedures...
  Test protocol simulation completed, CPU time=0.00 sec.
  ----------------------------------------------------------------------------
  Begin scan chain operation checking...
```

```
  Scan chain operation checking completed, CPU time=0.00 sec.
  ---------------------------------------------------------------------------
  Begin clock rules checking...
 Warning: Rule C2 (unstable nonscan DFF when clocks off) was violated 2 times.

  Clock rules checking completed, CPU time=0.00 sec.
  ---------------------------------------------------------------------------
  Begin nonscan rules checking...
  Nonscan cell summary: #DFF=2  #DLAT=0  #RAM_outs=0  tla_usage_type=none
  Nonscan behavior:  #CU=2
  Nonscan rules checking completed, CPU time=0.00 sec.
  ---------------------------------------------------------------------------
  Begin DRC dependent learning...
  Fast-sequential depth results: control=0(0), observe=0(0), detect=0(0), CPU
time=0.00 sec
  DRC dependent learning completed, CPU time=0.00 sec.
  ---------------------------------------------------------------------------
  DRC Summary Report
  ---------------------------------------------------------------------------
 Warning: Rule C2 (unstable nonscan DFF when clocks off) was violated 2 times.

  There were 2 violations that occurred during DRC process.
  Design rules checking was successful, total CPU time=0.00 sec.
  ---------------------------------------------------------------------------
TEST-T> remove_faults -all
  0 faults were removed from the fault list.
TEST-T> add_faults -all
  54 faults were added to fault list.
TEST-T> run_atpg full_sequential_only
  ATPG performed for stuck fault model using internal pattern source.

  ----------------------------------------------------------
  Begin Full-Sequential ATPG for 54 uncollapsed faults ...
   --- abort limit : 10 seconds, NO BACKTRACK LIMIT
  ----------------------------------------------------------
  #patterns  #faults        #ATPG faults  test       process
  stored     detect/active  red/au/abort  coverage   CPU time
  ---------  -------------  ------------  --------  ----------
  1                13     39         0/2/0     32.41%         0.00
  2                19     20         0/2/0     67.59%         0.00
  3                 4     15         0/3/1     75.00%        20.02
  4                 4      8         0/6/2     82.41%        40.67
  4                 0      2         0/8/2     82.41%        42.72
  4 faults were identified as detected by implication, test coverage is now 86.11%.

      Uncollapsed Stuck Fault Summary Report
  -----------------------------------------------
  fault class                     code   #faults
  ------------------------------  ----  ---------
  Detected                         DT         44
  Possibly detected                PT          5
  Undetectable                     UD          0
  ATPG untestable                  AU          5
  Not detected                     ND          0
  -----------------------------------------------
  total faults                                54
  test coverage                            86.11%
  -----------------------------------------------
            Pattern Summary Report
```

```
  ------------------------------------------------
  #internal patterns                             4
      #full_sequential patterns                  4
  ------------------------------------------------
TEST-T> report_faults -all
  sa1   NP   x1
  sa1   NP   __tmp103/B
  sa1   DI   __tmp105/GTECH_UDP_FD10/CP
  sa0   AN   __tmp103/Z
  sa0   --   __tmp103/B
  sa0   --   __tmp103/A
  sa0   --   __tmp103/C
  sa0   --   __tmp104/B
  sa1   DS   __tmp103/A
  sa1   DS   __tmp101/Z
  sa0   --   __tmp101/A
  sa1   --   __tmp102/C
  sa0   DI   __tmp105/GTECH_UDP_FD10/CP
  sa1   AP   __tmp102/B
  sa1   DS   __tmp103/C
  sa1   DS   __tmp100/Z
  sa0   --   __tmp100/A
  sa1   --   __tmp102/A
  sa0   DS   __tmp102/Z
  sa0   --   __tmp102/B
  sa0   --   __tmp102/A
  sa0   --   __tmp102/C
  sa0   --   __tmp100/Z
  sa1   --   __tmp100/A
  sa0   --   __tmp101/Z
  sa1   --   __tmp101/A
  sa0   --   __tmp104/A
  sa0   DS   __tmp104/Z
  sa0   --   __tmp105/GTECH_UDP_FD10/D
  sa1   DS   __tmp104/Z
  sa1   --   __tmp104/A
  sa1   --   __tmp104/B
  sa1   --   __tmp102/Z
  sa1   --   __tmp103/Z
  sa1   --   __tmp105/GTECH_UDP_FD10/D
  sa0   AP   clk
  sa1   AP   clk
  sa1   DS   __tmp106/GTECH_UDP_FD10/Q
  sa1   DI   __tmp106/GTECH_UDP_FD10/CP
  sa0   DI   __tmp106/GTECH_UDP_FD10/CP
  sa0   DS   __tmp106/GTECH_UDP_FD10/Q
  sa0   DS   __tmp106/GTECH_UDP_FD10/D
  sa1   DS   __tmp106/GTECH_UDP_FD10/D
  sa1   DS   __tmp105/GTECH_UDP_FD10/Q
  sa0   DS   __tmp105/GTECH_UDP_FD10/Q
  sa1   DS   z
  sa1   --   __tmp107/Z
  sa1   --   __tmp107/A
  sa1   --   __tmp107/B
  sa0   DS   __tmp107/B
  sa0   DS   z
  sa0   --   __tmp107/Z
  sa0   DS   __tmp107/A
  sa0   DS   x1
```

```
TEST-T> report_patterns -all -internal
  Pattern 0 (full_sequential)
  Time 0: period = 100
  Time 0: force_all_pis =   00
  Time 140: measure_all_pos =X
  Time 200: force_all_pis = 11
  Time 340: measure_all_pos =X
  Time 400: force_all_pis = 00
  Time 540: measure_all_pos =X
  Time 600: force_all_pis = 01
  Time 740: measure_all_pos =0
  Time 800: force_all_pis = 00
  Time 940: measure_all_pos =0
  Pattern 1 (full_sequential)
  Time 0: period = 100
  Time 0: force_all_pis =   00
  Time 140: measure_all_pos =0
  Time 200: force_all_pis = 11
  Time 340: measure_all_pos =0
  Time 400: force_all_pis = 00
  Time 540: measure_all_pos =0
  Time 600: force_all_pis = 11
  Time 740: measure_all_pos =0
  Time 800: force_all_pis = 10
  Time 940: measure_all_pos =0
  Time 1000: force_all_pis =01
  Time 1140: measure_all_pos =1
  Time 1200: force_all_pis =00
  Time 1340: measure_all_pos =1
  Time 1400: force_all_pis =01
  Time 1540: measure_all_pos =1
  Time 1600: force_all_pis =00
  Time 1740: measure_all_pos =1
  Pattern 2 (full_sequential)
  Time 0: period = 100
  Time 0: force_all_pis =   00
  Time 140: measure_all_pos =1
  Time 200: force_all_pis = 01
  Time 340: measure_all_pos =0
  Time 400: force_all_pis = 00
  Time 540: measure_all_pos =0
  Time 600: force_all_pis = 11
  Time 740: measure_all_pos =0
  Time 800: force_all_pis = 10
  Time 940: measure_all_pos =0
  Time 1000: force_all_pis =01
  Time 1140: measure_all_pos =1
  Time 1200: force_all_pis =10
  Time 1340: measure_all_pos =1
  Time 1400: force_all_pis =11
  Time 1540: measure_all_pos =1
  Time 1600: force_all_pis =00
  Time 1740: measure_all_pos =1
  Time 1800: force_all_pis =00
  Time 1940: measure_all_pos =1
  Time 2000: force_all_pis =11
  Time 2140: measure_all_pos =0
  Pattern 3 (full_sequential)
  Time 0: period = 100
```

```
  Time 0: force_all_pis =   00
  Time 140: measure_all_pos =0
  Time 200: force_all_pis = 11
  Time 340: measure_all_pos =0
  Time 400: force_all_pis = 00
  Time 540: measure_all_pos =0
  Time 600: force_all_pis = 01
  Time 740: measure_all_pos =0
  Time 800: force_all_pis = 10
  Time 940: measure_all_pos =0
  Time 1000: force_all_pis =11
  Time 1140: measure_all_pos =1
  Time 1200: force_all_pis =00
  Time 1340: measure_all_pos =1
  Time 1400: force_all_pis =01
  Time 1540: measure_all_pos =1
  Time 1600: force_all_pis =10
  Time 1740: measure_all_pos =1
  Time 1800: force_all_pis =01
  Time 1940: measure_all_pos =0
TEST-T>
```