Micro-Processor and Embedded Systems Lab-Session 7 Report for Data Hazard and Branch Detection

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AIM: This week we have to implement Data Hazard and Branch Detection Modules

Summary:

1. Using Nomachine access the VIVADO By sourcing **/proj/cad/startup/profile.xilinx_vivado_18.3.**
2. Command to open the tool is **vivado&**
3. Create a new project on the software for ALU and registers.
4. ALU and register file Verilog codes along with the test benches have been complied successfully.
5. Ran the behavioral simulation for the test bench codes.

Data Hazard:

Data hazards occur if an instruction reads a Register that a previous instruction overwrites in a future cycle.

Branch Detection:

A branch Detection is a circuit that tries to guess which way a branch will go before this is known definitively.

Conclusion:

We were able to successfully to implement Data Hazard and Branch Detection Modules . I would like to implement all the modules created into an MCU