Question 1:

Figure 5.4:

Verilog code for circuit:

```
`timescale 1ns / 1ps

module Q1_project5_fig54(x1,z,clk );

input x1,clk;

output z;

wire c1,c2,c3,c4,c5,y1,y2;

GTECH_NOT (y1,c1);

GTECH_NOT (y2,c2);

GTECH_AND3 (c1,x1,c2,c4);

GTECH_AND3 (y1,x1,y2,c3);

GTECH_OR2 (c4,c3,c5);

GTECH_FD1 (c5,clk,y1);

GTECH_FD1 (y1,clk,y2);

GTECH_OR2 (y1,y2,z);

endmodule
```

Verilog code for the combinational circuit:

```
`timescale 1ns / 1ps

module Q1_project6_combinational(x1,z,y1,y2,Y1,Y2);

input x1,y1,y2;

output z,Y1,Y2;

wire c1,c2,c3,c4,c5;

GTECH_NOT (y1,c1);

GTECH_NOT (y2,c2);

GTECH_AND3 (c1,x1,c2,c4);

GTECH_AND3 (y1,x1,y2,c3);

GTECH_OR2 (c4,c3,c5);

assign Y1 = c5;

assign Y2 = y1;

GTECH_OR2 (y1,y2,z);

endmodule
```

Verilog code for the simulation:

```
`timescale 1ns / 1ps

module Q1_project6_combi();

reg x1,y1,y2;

wire z,Y2,Y1;

simulation_Q1_p6 uut(.x1(x1),.y1(y1),.y2(y2),.z(z), .Y1(Y1),.Y2(Y2));

initial begin

x1 <= 0; y1 <= 0; y2 <= 0;

#50

x1 <= 0; y1 <= 1; y2 <= 0;

#50

x1 <= 0; y1 <= 1; y2 <= 1;

#50
```

x1 <= 1; y1 <= 0; y2 <= 1;

#50

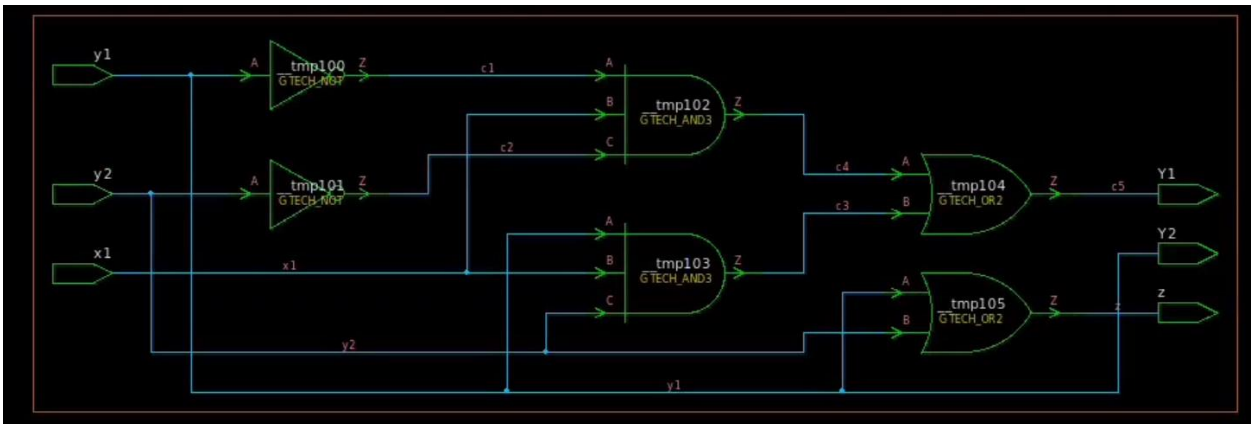
$finish;

end

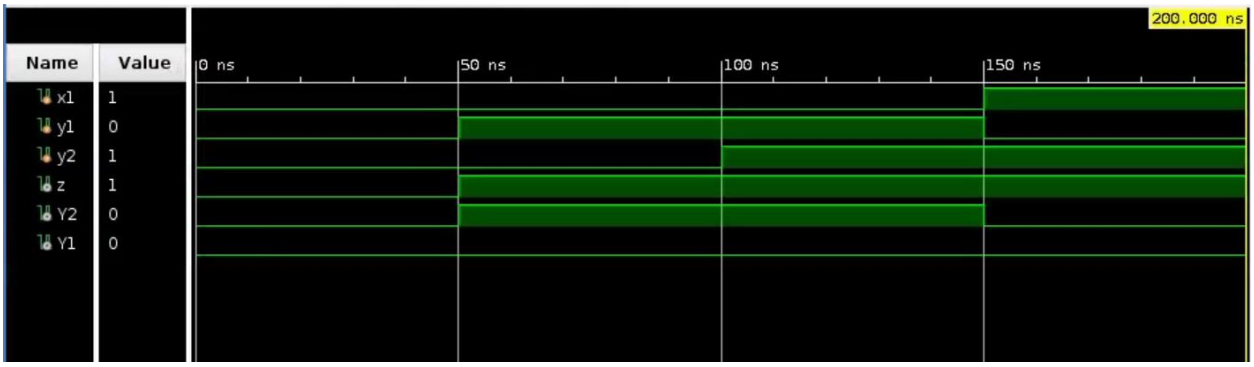
endmodule

Combinational Circuit:

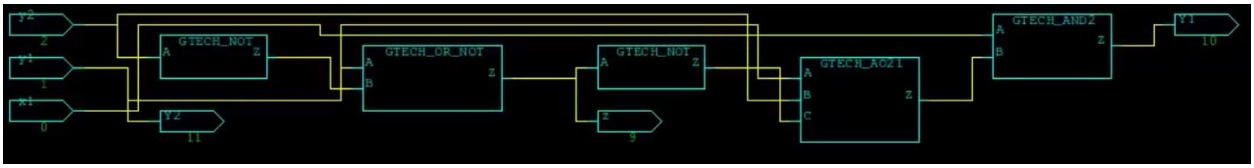
Schematic:



Simulation:



Tetramax Schematic:



Tetramax report:

Reading the gtech_lib.v file:

```
BUILD-T> read_netlist /home/011/y/yx/yxa210024/spring23/testing/src_ver/gtech_lib.v
Begin reading netlist (
/home/011/y/yx/yxa210024/spring23/testing/src_ver/gtech_lib.v )...
Warning: Rule N2 (unsupported construct) was violated 10 times.
End parsing Verilog file
/home/011/y/yx/yxa210024/spring23/testing/src_ver/gtech_lib.v with 0 errors.
End reading netlist: #modules=106, top=GTECH_ZERO, #lines=1976, CPU_time=0.00
sec, Memory=0MB
```

Reading the combination Verilog file:

```
BUILD-T> read_netlist /home/011/y/yx/yxa210024/Q1_project6_combinational_1.v
Begin reading netlist (
/home/011/y/yx/yxa210024/Q1_project6_combinational_1.v )...
End parsing Verilog file /home/011/y/yx/yxa210024/Q1_project6_combinational_1.v
with 0 errors.
End reading netlist: #modules=1, top=Q1_project6_combinational_1, #lines=20,
CPU_time=0.00 sec, Memory=0MB
```

Building the model:

```
BUILD-T> run_build_model Q1_project6_combinational_1
---------------------------------------------------------------------------
Begin build model for topcut = Q1_project6_combinational_1 ...
---------------------------------------------------------------------------
There were 2 primitives and 0 faultable pins removed during model optimizations
End build model: #primitives=12, CPU_time=0.00 sec, Memory=0MB
---------------------------------------------------------------------------
Begin learning analyses...
End learning analyses, total learning CPU time=0.01 sec.
---------------------------------------------------------------------------
```

DRC check:

```
DRC-T> run_drc
---------------------------------------------------------------------------
Begin scan design rules checking...
---------------------------------------------------------------------------
Begin simulating test protocol procedures...
Test protocol simulation completed, CPU time=0.00 sec.
---------------------------------------------------------------------------
Begin scan chain operation checking...
Scan chain operation checking completed, CPU time=0.00 sec.
---------------------------------------------------------------------------
Begin nonscan rules checking...
Nonscan cell summary: #DFF=0 #DLAT=0 #RAM_outs=0 tla_usage_type=none
Nonscan rules checking completed, CPU time=0.00 sec.
---------------------------------------------------------------------------
Begin DRC dependent learning...
Fast-sequential depth results: control=0(0), observe=0(0), detect=0(0), CPU
time=0.00 sec
DRC dependent learning completed, CPU time=0.00 sec.
```

```
---------------------------------------------------------------------------
DRC Summary Report
---------------------------------------------------------------------------
No violations occurred during DRC process.
Design rules checking was successful, total CPU time=0.00 sec.
---------------------------------------------------------------------------
```

ATPG Test:

```
TEST-T> remove_faults -all
0 faults were removed from the fault list.
TEST-T> add_faults -all
40 faults were added to fault list.
TEST-T> run_atpg -ndetects 1
ATPG performed for stuck fault model using internal pattern source.
-----------------------------------------------------------
#patterns #faults #ATPG faults test process
stored detect/active red/au/abort coverage CPU time
--------- ------------ ------------ -------- --------
Begin deterministic ATPG: #uncollapsed_faults=40, abort_limit=10...
5 40 0 0/0/0 100.00% 0.00
Uncollapsed Stuck Fault Summary Report
-----------------------------------------------
fault class code #faults
------------------------------ ---- ---------
Detected DT 40
Possibly detected PT 0
Undetectable UD 0
ATPG untestable AU 0
Not detected ND 0
-----------------------------------------------
total faults 40
test coverage 100.00%
-----------------------------------------------
Pattern Summary Report
-----------------------------------------------
#internal patterns 5
#basic_scan patterns 5
-----------------------------------------------
```

Reported Fault:

```
TEST-T> report_faults -all
sa0 DS Y1
sa0 -- U6/Z
sa0 -- U6/A
sa0 -- U6/B
sa0 -- x1
sa0 -- U7/Z
sa1 DS x1
sa1 -- U6/A
```

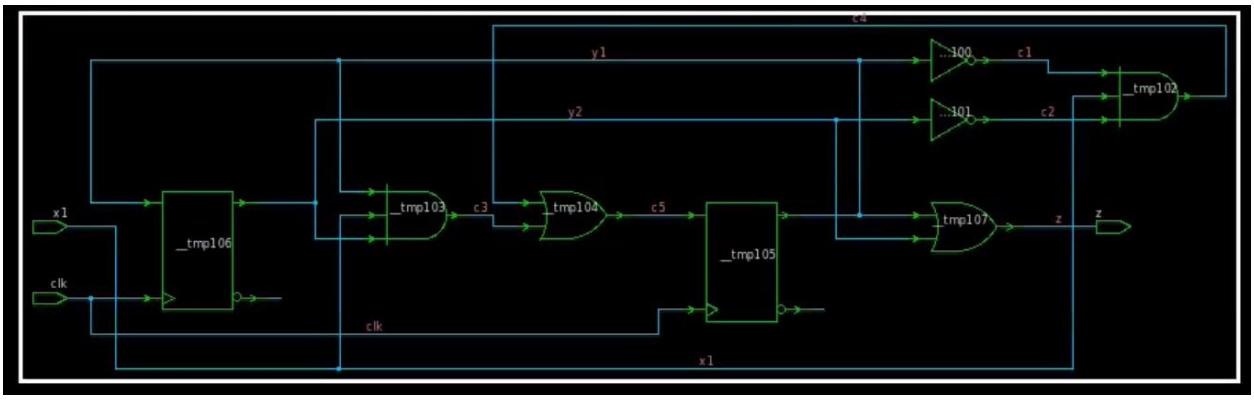
sa1 DS Y1
sa1 -- U6/Z
sa1 DS U7/Z
sa1 -- U7/C
sa1 -- U8/Z
sa0 -- U8/A
sa1 -- U6/B
sa0 DS U7/A
sa0 -- U7/B
sa1 DS U7/A
sa1 DS U7/B
sa0 DS U8/Z
sa1 -- U8/A
sa0 -- U7/C
sa0 DS y1
sa1 DS y1
sa0 DS y2
sa1 DS y2
sa0 DS U9/Z
sa1 DS U9/Z
sa1 -- U9/A
sa0 -- U9/B
sa0 -- U10/Z
sa1 -- U10/A
sa0 DS U9/A
sa1 DS U10/Z
sa0 -- U10/A
sa1 -- U9/B
sa0 DS z
sa1 DS z
sa0 DS Y2
sa1 DS Y2

Patterns Reported:

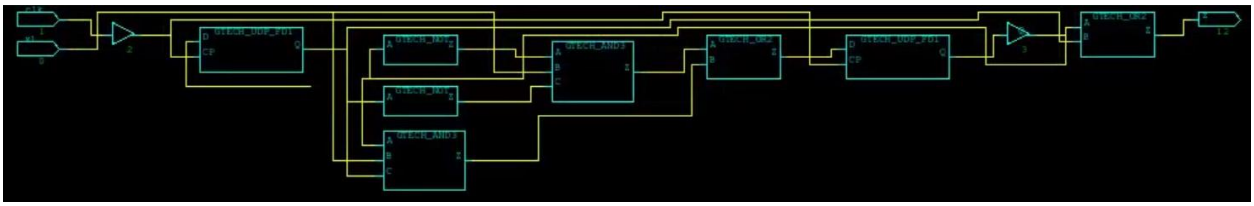
TEST-T> report_patterns -all -internal
Pattern 0 (basic_scan)
Time 0: force_all_pis = 111
Time 1: measure_all_pos = 111
Pattern 1 (basic_scan)
Time 0: force_all_pis = 100
Time 1: measure_all_pos = 010
Pattern 2 (basic_scan)
Time 0: force_all_pis = 110
Time 1: measure_all_pos = 101
Pattern 3 (basic_scan)
Time 0: force_all_pis = 101
Time 1: measure_all_pos = 100
Pattern 4 (basic_scan)
Time 0: force_all_pis = 000
Time 1: measure_all_pos = 000

Original Circuit:

Schematic:



Tetramax Schematic:



Tetramax Report:

Without the scanned flipflops:

Reading the Gtech_lib.v:

BUILD-T> read_netlist /home/011/y/yx/yxa210024/spring23/testing/src_ver/gtech_lib.v
Begin reading netlist (
/home/011/y/yx/yxa210024/spring23/testing/src_ver/gtech_lib.v)...
Warning: Rule N2 (unsupported construct) was violated 10 times.
End parsing Verilog file
/home/011/y/yx/yxa210024/spring23/testing/src_ver/gtech_lib.v with 0 errors.
End reading netlist: #modules=106, top=GTECH_ZERO, #lines=1976, CPU_time=0.00
sec, Memory=0MB

Reading the Verilog file:

TEST-T> read_netlist /home/011/y/yx/yxa210024/Q1_project5_fig54_1.v
Warning: Current simulation model is now deleted. (M39)
Begin reading netlist (/home/011/y/yx/yxa210024/Q1_project5_fig54_1.v)...
Warning: Rule N5 (redefined module) was violated 1 times.
End parsing Verilog file /home/011/y/yx/yxa210024/Q1_project5_fig54_1.v with 0
errors.
End reading netlist: #modules=0, top=BIDI, #lines=22, CPU_time=0.00 sec,
Memory=0MB

```
BUILD-T> run_build_model Q1_project5_fig54_1
---------------------------------------------------------------------------
Begin build model for topcut = Q1_project5_fig54_1 ...
---------------------------------------------------------------------------
There were 3 primitives and 0 faultable pins removed during model optimizations
End build model: #primitives=13, CPU_time=0.00 sec, Memory=0MB
---------------------------------------------------------------------------
Begin learning analyses...
End learning analyses, total learning CPU time=0.00 sec.
---------------------------------------------------------------------------
```

DRC Test:

```
DRC-T> run_drc
---------------------------------------------------------------------------
Begin scan design rules checking...
---------------------------------------------------------------------------
Begin simulating test protocol procedures...
Test protocol simulation completed, CPU time=0.00 sec.
---------------------------------------------------------------------------
Begin scan chain operation checking...
Scan chain operation checking completed, CPU time=0.00 sec.
---------------------------------------------------------------------------
Begin clock rules checking...
Warning: Rule C2 (unstable nonscan DFF when clocks off) was violated 2 times.
Clock rules checking completed, CPU time=0.00 sec.
---------------------------------------------------------------------------
Begin nonscan rules checking...
Nonscan cell summary: #DFF=2 #DLAT=0 #RAM_outs=0 tla_usage_type=none
Nonscan behavior: #CU=2
Nonscan rules checking completed, CPU time=0.00 sec.
---------------------------------------------------------------------------
Begin DRC dependent learning...
Fast-sequential depth results: control=0(0), observe=0(0), detect=0(0), CPU
time=0.00 sec
DRC dependent learning completed, CPU time=0.00 sec.
---------------------------------------------------------------------------
DRC Summary Report
---------------------------------------------------------------------------
Warning: Rule C2 (unstable nonscan DFF when clocks off) was violated 2 times.
There were 2 violations that occurred during DRC process.
Design rules checking was successful, total CPU time=0.00 sec.
---------------------------------------------------------------------------
```

ATPG Test:

```
TEST-T> remove_faults -all
0 faults were removed from the fault list.
TEST-T> add_faults -all
54 faults were added to fault list.
TEST-T> run_atpg full_sequential_only
ATPG performed for stuck fault model using internal pattern source.
---------------------------------------------------------
Begin Full-Sequential ATPG for 54 uncollapsed faults ...
```

--- abort limit : 10 seconds, NO BACKTRACK LIMIT

#patterns #faults #ATPG faults test process
stored detect/active red/au/abort coverage CPU time
--- --- --- --- ---
1 13 39 0/2/0 32.41% 0.00
2 19 20 0/2/0 67.59% 0.00
3 4 15 0/3/1 75.00% 20.02
4 4 8 0/6/2 82.41% 40.67
4 0 2 0/8/2 82.41% 42.72
4 faults were identified as detected by implication, test coverage is now 86.11%.
Uncollapsed Stuck Fault Summary Report
---
fault class code #faults
--- --- ---
Detected DT 44
Possibly detected PT 5
Undetectable UD 0
ATPG untestable AU 5
Not detected ND 0
---
total faults 54
test coverage 86.11%

Pattern Summary Report

#internal patterns 4
#full_sequential patterns 4

Faults Reported:

TEST-T> report_faults -all
sa1 NP x1
sa1 NP __tmp103/B
sa1 DI __tmp105/GTECH_UDP_FD10/CP
sa0 AN __tmp103/Z
sa0 -- __tmp103/B
sa0 -- __tmp103/A
sa0 -- __tmp103/C
sa0 -- __tmp104/B
sa1 DS __tmp103/A
sa1 DS __tmp101/Z
sa0 -- __tmp101/A
sa1 -- __tmp102/C
sa0 DI __tmp105/GTECH_UDP_FD10/CP
sa1 AP __tmp102/B
sa1 DS __tmp103/C
sa1 DS __tmp100/Z
sa0 -- __tmp100/A
sa1 -- __tmp102/A
sa0 DS __tmp102/Z

sa0 -- __tmp102/B
sa0 -- __tmp102/A
sa0 -- __tmp102/C
sa0 -- __tmp100/Z
sa1 -- __tmp100/A
sa0 -- __tmp101/Z
sa1 -- __tmp101/A
sa0 -- __tmp104/A
sa0 DS __tmp104/Z
sa0 -- __tmp105/GTECH_UDP_FD10/D
sa1 DS __tmp104/Z
sa1 -- __tmp104/A
sa1 -- __tmp104/B
sa1 -- __tmp102/Z
sa1 -- __tmp103/Z
sa1 -- __tmp105/GTECH_UDP_FD10/D
sa0 AP clk
sa1 AP clk
sa1 DS __tmp106/GTECH_UDP_FD10/Q
sa1 DI __tmp106/GTECH_UDP_FD10/CP
sa0 DI __tmp106/GTECH_UDP_FD10/CP
sa0 DS __tmp106/GTECH_UDP_FD10/Q
sa0 DS __tmp106/GTECH_UDP_FD10/D
sa1 DS __tmp106/GTECH_UDP_FD10/D
sa1 DS __tmp105/GTECH_UDP_FD10/Q
sa0 DS __tmp105/GTECH_UDP_FD10/Q
sa1 DS z
sa1 -- __tmp107/Z
sa1 -- __tmp107/A
sa1 -- __tmp107/B
sa0 DS __tmp107/B
sa0 DS z
sa0 -- __tmp107/Z
sa0 DS __tmp107/A
sa0 DS x1

Patterns Reported:

TEST-T> report_patterns -all -internal
Pattern 0 (full_sequential)
Time 0: period = 100
Time 0: force_all_pis = 00
Time 140: measure_all_pos =X
Time 200: force_all_pis = 11
Time 340: measure_all_pos =X
Time 400: force_all_pis = 00
Time 540: measure_all_pos =X
Time 600: force_all_pis = 01
Time 740: measure_all_pos =0
Time 800: force_all_pis = 00
Time 940: measure_all_pos =0
Pattern 1 (full_sequential)
Time 0: period = 100
Time 0: force_all_pis = 00

Time 140: measure_all_pos =0
Time 200: force_all_pis = 11
Time 340: measure_all_pos =0
Time 400: force_all_pis = 00
Time 540: measure_all_pos =0
Time 600: force_all_pis = 11
Time 740: measure_all_pos =0
Time 800: force_all_pis = 10
Time 940: measure_all_pos =0
Time 1000: force_all_pis =01
Time 1140: measure_all_pos =1
Time 1200: force_all_pis =00
Time 1340: measure_all_pos =1
Time 1400: force_all_pis =01
Time 1540: measure_all_pos =1
Time 1600: force_all_pis =00
Time 1740: measure_all_pos =1
Pattern 2 (full_sequential)
Time 0: period = 100
Time 0: force_all_pis = 00
Time 140: measure_all_pos =1
Time 200: force_all_pis = 01
Time 340: measure_all_pos =0
Time 400: force_all_pis = 00
Time 540: measure_all_pos =0
Time 600: force_all_pis = 11
Time 740: measure_all_pos =0
Time 800: force_all_pis = 10
Time 940: measure_all_pos =0
Time 1000: force_all_pis =01
Time 1140: measure_all_pos =1
Time 1200: force_all_pis =10
Time 1340: measure_all_pos =1
Time 1400: force_all_pis =11
Time 1540: measure_all_pos =1
Time 1600: force_all_pis =00
Time 1740: measure_all_pos =1
Time 1800: force_all_pis =00
Time 1940: measure_all_pos =1
Time 2000: force_all_pis =11
Time 2140: measure_all_pos =0
Pattern 3 (full_sequential)
Time 0: period = 100
Time 0: force_all_pis = 00
Time 140: measure_all_pos =0
Time 200: force_all_pis = 11
Time 340: measure_all_pos =0
Time 400: force_all_pis = 00
Time 540: measure_all_pos =0
Time 600: force_all_pis = 01
Time 740: measure_all_pos =0
Time 800: force_all_pis = 10
Time 940: measure_all_pos =0

```
Time 1000: force_all_pis =11
Time 1140: measure_all_pos =1
Time 1200: force_all_pis =00
Time 1340: measure_all_pos =1
Time 1400: force_all_pis =01
Time 1540: measure_all_pos =1
Time 1600: force_all_pis =10
Time 1740: measure_all_pos =1
Time 1800: force_all_pis =01
Time 1940: measure_all_pos =0
TEST-T>
```

Without the scanned flipflops:

Reading the gtech_lib.v:

```
BUILD-T> read_netlist /home/011/y/yx/yxa210024/spring23/testing/src_ver/gtech_lib.v
Begin reading netlist (
/home/011/y/yx/yxa210024/spring23/testing/src_ver/gtech_lib.v )...
Warning: Rule N2 (unsupported construct) was violated 10 times.
End parsing Verilog file
/home/011/y/yx/yxa210024/spring23/testing/src_ver/gtech_lib.v with 0 errors.
End reading netlist: #modules=106, top=GTECH_ZERO, #lines=1976, CPU_time=0.00
```

Reading the class.v:

```
BUILD-T> read_netlist /home/011/y/yx/yxa210024/spring23/testing/LIB/class.v
Begin reading netlist (
/home/011/y/yx/yxa210024/spring23/testing/LIB/class.v )...
End parsing Verilog file /home/011/y/yx/yxa210024/spring23/testing/LIB/class.v
with 0 errors.
End reading netlist: #modules=125, top=BIDI, #lines=1039, CPU_time=0.00 sec,
Memory=0MB
```

Reading the Verilog file:

```
BUILD-T> read_netlist /home/011/y/yx/yxa210024/Q1_project5_fig54_scan.v
Begin reading netlist ( /home/011/y/yx/yxa210024/Q1_project5_fig54_scan.v )...
Warning: Rule N5 (redefined module) was violated 1 times.
End parsing Verilog file /home/011/y/yx/yxa210024/Q1_project5_fig54_scan.v with 0
errors.
End reading netlist: #modules=0, top=BIDI, #lines=22, CPU_time=0.00 sec,
Memory=0MB
```

Building the model:

```
BUILD-T> run_build_model Q1_project5_fig54_1
---------------------------------------------------------------------------
Begin build model for topcut = Q1_project5_fig54_1 ...
---------------------------------------------------------------------------
There were 4 primitives and 0 faultable pins removed during model optimizations
Warning: Rule N20 (underspecified UDP) was violated 1 times.
End build model: #primitives=13, CPU_time=0.00 sec, Memory=0MB
---------------------------------------------------------------------------
Begin learning analyses...
End learning analyses, total learning CPU time=0.00 sec.
```

DRC Test:

```
DRC-T> run_drc
---------------------------------------------------------------------------
Begin scan design rules checking...
---------------------------------------------------------------------------
Begin simulating test protocol procedures...
Test protocol simulation completed, CPU time=0.00 sec.
---------------------------------------------------------------------------
Begin scan chain operation checking...
Scan chain operation checking completed, CPU time=0.00 sec.
---------------------------------------------------------------------------
Begin clock rules checking...
Warning: Rule C2 (unstable nonscan DFF when clocks off) was violated 2 times.
Clock rules checking completed, CPU time=0.00 sec.
---------------------------------------------------------------------------
Begin nonscan rules checking...
Nonscan cell summary: #DFF=2 #DLAT=0 #RAM_outs=0 tla_usage_type=none
Nonscan behavior: #CU=2
Nonscan rules checking completed, CPU time=0.00 sec.
---------------------------------------------------------------------------
Begin DRC dependent learning...
Fast-sequential depth results: control=0(0), observe=0(0), detect=0(0), CPU
time=0.00 sec
DRC dependent learning completed, CPU time=0.00 sec.
---------------------------------------------------------------------------
DRC Summary Report
---------------------------------------------------------------------------
Warning: Rule C2 (unstable nonscan DFF when clocks off) was violated 2 times.
There were 2 violations that occurred during DRC process.
Design rules checking was successful, total CPU time=0.00 sec.
---------------------------------------------------------------------------
```

ATPG Test:

```
TEST-T> remove_faults -all
0 faults were removed from the fault list.
TEST-T> add_faults -all
56 faults were added to fault list.
TEST-T> run_atpg full_sequential_only
************************************************************
* NOTICE: The following DRC violations were previously *
* encountered. The presence of these violations is an *
* indicator that it is possible that the ATPG patterns *
* created during this process may fail in simulation. *
* *
* Rules: N20 *
************************************************************
ATPG performed for stuck fault model using internal pattern source.
-------------------------------------------------------------
Begin Full-Sequential ATPG for 56 uncollapsed faults ...
--- abort limit : 10 seconds, NO BACKTRACK LIMIT
```

#patterns #faults #ATPG faults test process
stored detect/active red/au/abort coverage CPU time
--------- ------------ ------------ -------- ----------
1 31 25 0/0/1 63.39% 20.02
2 7 18 0/0/1 75.89% 20.02
3 4 12 0/2/1 83.04% 20.02
3 0 2 0/8/2 83.04% 42.73
4 faults were identified as detected by implication, test coverage is now 86.61%.
Uncollapsed Stuck Fault Summary Report
---
fault class code #faults

Detected DT 46
Possibly detected PT 5
Undetectable UD 0
ATPG untestable AU 5
Not detected ND 0
---
total faults 56
test coverage 86.61%

Pattern Summary Report

#internal patterns 3
#full_sequential patterns 3

Faults Reported:

TEST-T> report_faults -all
sa1 NP x1
sa1 NP __tmp103/B
sa1 DS __tmp106/p_dreg0/d
sa1 DI __tmp106/p_dreg0/cp
sa0 DI __tmp106/p_dreg0/cp
sa0 DS __tmp106/p_dreg0/q
sa0 DS __tmp106/p_dreg0/d
sa1 DS __tmp106/p_dreg0/q
sa1 DS __tmp105/Q
sa1 -- __tmp105/p_dreg0/q
sa0 DS __tmp105/Q
sa0 -- __tmp105/p_dreg0/q
sa1 DS __tmp104/Z
sa1 -- __tmp104/A
sa1 -- __tmp104/B
sa1 -- __tmp102/Z
sa1 -- __tmp103/Z
sa1 -- __tmp105/p_dreg0/d
sa0 AN __tmp103/Z
sa0 -- __tmp103/B
sa0 -- __tmp103/A
sa0 -- __tmp103/C

sa0 -- __tmp104/B
sa1 AP __tmp102/B
sa1 DS __tmp103/C
sa1 DS __tmp100/Z
sa0 -- __tmp100/A
sa1 -- __tmp102/A
sa0 DI __tmp105/p_dreg0/cp
sa1 DI __tmp105/p_dreg0/cp
sa1 DS __tmp103/A
sa1 DS __tmp101/Z
sa0 -- __tmp101/A
sa1 -- __tmp102/C
sa0 DS __tmp104/Z
sa0 -- __tmp105/p_dreg0/d
sa0 DS __tmp102/Z
sa0 -- __tmp102/B
sa0 -- __tmp102/A
sa0 -- __tmp102/C
sa0 -- __tmp100/Z
sa1 -- __tmp100/A
sa0 -- __tmp101/Z
sa1 -- __tmp101/A
sa0 -- __tmp104/A
sa1 DS z
sa1 -- __tmp107/Z
sa1 -- __tmp107/A
sa1 -- __tmp107/B
sa0 DS __tmp107/B
sa0 DS z
sa0 -- __tmp107/Z
sa0 DS __tmp107/A
sa0 DS x1
sa1 AP clk
sa0 AP clk

Patterns Reported:

TEST-T> report_patterns -all -internal
Pattern 0 (full_sequential)
Time 0: period = 100
Time 0: force_all_pis = 00
Time 140: measure_all_pos =X
Time 200: force_all_pis = 11
Time 340: measure_all_pos =X
Time 400: force_all_pis = 00
Time 540: measure_all_pos =X
Time 600: force_all_pis = 11
Time 740: measure_all_pos =0
Time 800: force_all_pis = 10
Time 940: measure_all_pos =0
Time 1000: force_all_pis =01
Time 1140: measure_all_pos =1
Time 1200: force_all_pis =00

Time 1340: measure_all_pos =1
Pattern 1 (full_sequential)
Time 0: period = 100
Time 0: force_all_pis = 00
Time 140: measure_all_pos =1
Time 200: force_all_pis = 11
Time 340: measure_all_pos =1
Time 400: force_all_pis = 00
Time 540: measure_all_pos =1
Time 600: force_all_pis = 11
Time 740: measure_all_pos =0
Time 800: force_all_pis = 10
Time 940: measure_all_pos =0
Time 1000: force_all_pis =01
Time 1140: measure_all_pos =1
Time 1200: force_all_pis =00
Time 1340: measure_all_pos =1
Time 1400: force_all_pis =01
Time 1540: measure_all_pos =1
Time 1600: force_all_pis =10
Time 1740: measure_all_pos =1
Time 1800: force_all_pis =01
Time 1940: measure_all_pos =0
Pattern 2 (full_sequential)
Time 0: period = 100
Time 0: force_all_pis = 00
Time 140: measure_all_pos =0
Time 200: force_all_pis = 01
Time 340: measure_all_pos =0
Time 400: force_all_pis = 00
Time 540: measure_all_pos =0
Time 600: force_all_pis = 11
Time 740: measure_all_pos =0
Time 800: force_all_pis = 10
Time 940: measure_all_pos =0
Time 1000: force_all_pis =01
Time 1140: measure_all_pos =1
Time 1200: force_all_pis =10
Time 1340: measure_all_pos =1
Time 1400: force_all_pis =11
Time 1540: measure_all_pos =1
Time 1600: force_all_pis =00
Time 1740: measure_all_pos =1
Time 1800: force_all_pis =00
Time 1940: measure_all_pos =1
Time 2000: force_all_pis =11
Time 2140: measure_all_pos =0
TEST-T>