The University of Texas at Dallas
Dept. of Electrical and Computer Engineering

EEDG/CE 6303: Testing and Testable Design
HW # 6 (OPTIONAL BONUS): *Due on Friday 5/5/2023 - 11:59 pm (US CST)*

When you submit your homeworks, to help us grade and identify your work, you need to comply with the following guidelines carefully:

- *Have* **a cover page** *for each document (e.g. homework, project, report, etc.) that you submit. A sample of cover page is provided in the course webpage. This page must include: (1) your name as it appears in your* **student ID card***, (2) course name/number, (3) homework/project number, and (4) the* **Statement of Academic Honesty** *that you sign.*

NOTE: This is an OPTIONAL BOUNUS homework. If submitted, it will add additional points (equivalent to credit of one homework $\approx$ 5%) to your overall grade.

1. This problem is for working on a design-for-testability method using **SCAN**.

   (i) Design the circuit shown in Figure 5.4 using two D Flip-Flops without set/reset.

   (ii) Isolate only the combinational part(s) of the circuit and use Synopsys tool to generate a set of test vectors that detect all single SAFs in the combinational part(s). Note that the isolated combinational part will have 3 inputs (input x_1 and two feedback lines y_1, y_2 broken). Show Synopsys reports including synthesis, schematic and the patterns found by ATPG.

   (iii) Use Synopsys Design Compiler to design the complete circuit (combinational plus flips-flops). Then, automatically replace flip-flops with the scan flip-flops to build one scan chain. Report schematic, simulation results and design characteristics (e.g., area and delay) before and after scan insertion.

   (iv) Use Synopsys Tetramax to perform ATPG on both variants of the circuit, i.e. one with regular flip-flops and the other with scan flip-flops. Comment on the differences in results. Show Synopsys reports.

2. This problem is for working on a design-for-testability method using **BIST**.

   (i) Show the circuits of the following six 8-bit designs using the primitive polynomial $x^8+x^4+x^3+x^2+1$: [1] Internal-XOR LFSR, [2] External-XOR LFSR, and [3] MISR. In a table summarize their characteristics in terms of estimate of cost, delay, etc.

   (ii) Simulate circuit [2] above and show the first 16 pseudo-random patterns generated assuming the initial value of LFSR is all-1. You can use Synopsys or matrix/vector MOD 2 calculations (hand-driven or a short script/program). Explain your approach and include the details.

   (iii) Consider the circuit under test (CUT) is a 4-bit unsigned multiplier unit that receives $X = x_3x_2x_1x_0$ and $Y = y_3y_2y_1y_0$ as inputs and produces $Z = z_7z_6z_5z_4z_3z_2z_1z_0$ as outputs such that $Z = X * Y$. For uniformity, assume that $x_3x_2x_1x_0y_3y_2y_1y_0$ are connected in order to $e_7e_6e_5e_4e_3e_2e_1e_0$ the outputs of 8-bit LFSR, respectively. Similarly, assume that eight outputs $z_7z_6z_5z_4z_3z_2z_1z_0$ are connected in order to $d_7d_6d_5d_4d_3d_2d_1d_0$ of the 8-bit MISR (circuit [3] above), respectively.

   Suppose the first 16 pseudo-random patterns that you found in previous part are used to test the CUT. Find the fault-free 8-bit signature assuming the initial value of MISR is all-0.

   Note: You need to first apply 16 8-bit patterns to the CUT and find 16 8-bit outputs. Then, find the result of compacting the outputs using the MISR. The final signature will be 8-bit content of MISR at the end. You can find this using either an implementation in Synopsys or matrix/vector MOD 2 calculations (hand-driven or a short script/program). Explain your approach and include the details.