Micro-Processor and Embedded Systems Lab-Session 4 Report for Instruction Decoder

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AIM: This week we created 17-bit Instruction Decoder.

Summary:

1. Using Nomachine access the VIVADO By sourcing **/proj/cad/startup/profile.xilinx_vivado_18.3.**
2. Command to open the tool is **vivado&**
3. Create a new project on the software for ALU and registers.
4. ALU and register file Verilog codes along with the test benches have been complied successfully.
5. Ran the behavioral simulation for the test bench codes.

Instruction Decoder:

The instruction decoder of a processor is a combinatorial circuit sometimes in the form of a read-only memory, sometimes in the form of an ordinary combinatorial circuit. Its purpose is to translate an instruction code into the address in the micro memory where the micro code for the instruction starts.

Conclusion:

We were able to successfully create the 17-bit Instruction Decoder. I would like to implement all the modules created into an MCU

Attachments:

We have uploaded the codes and testbenches for the Instruction Decoder in the attachments along with a simulation explanation file, screenshot of the simulation and a video explaning the simulation.