

Micro-Processor and Embedded Systems

Lab-Session 3 Report for ALU & Register File

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AIM: This week we created 8-bit ALU and Register File.

Summary:

1. Using Nomachine access the VIVADO By sourcing **/proj/cad/startup/profile.xilinx_vivado_18.3**.
2. Command to open the tool is **vivado&**
3. Create a new project on the software for ALU and registers.
4. ALU and register file Verilog codes along with the test benches have been complied successfully.
5. Ran the behavioral simulation for the test bench codes.

ALU:

An Arithmetic Logic Unit (ALU) is a combinational digital circuit that performs arithmetic and bitwise operations on integer binary numbers.

Register File:

A register file is an array of processor registers in a central processing unit (CPU).

Conclusion:

We were able to successfully create the 8-bit ALU and Register File. I would like to increase the complexity of the 8-bit ALU to 16-bit later to understand the functionality.

Attachments:

We have uploaded the codes and testbenches for the ALU and Register file in the attachments along with a simulation explanation file, screenshot of the simulation and a video showing the simulation.