YAGNA SRINIVASA HARSHA ANNADATA

+1 9452087629 yxa210024@utdallas.edu Yagna Annadata yagna-srinivasa-harsha-annadata

Education

University of Texas at Dallas, Texas **Aug 2022 – May 2024**

MSc, Computer Engineering **GPA: 3.72/4**

- Embedded systems, Machine Learning, Computer Architecture, VLSI, VLSI Testing, Applied Data structures.

Jawaharlal Nehru Technological University, India **Aug 2016 – Aug 2020**

B.Tech, Electronics and Communication Engineering **GPA: 3.5/4**

Technical Skills

Platforms/Tools: Synopsys Design Vision, Cadence Tetramax, Arduino IDE, MATLAB, Primetime, HSpice, PrimeLib, Selenium, Jenkins, Eclipse, JIRA, Confluence, Agile Methodologies, Energia IDE

Languages: Verilog, TCL Script, Java, C, Embedded C, Shell Script

Work Experience

University of Texas at Dallas, Texas, USA

Graduate Teaching Assistant **Aug 2023 – Present**

- Developed projects for embedded systems lab which includes energy efficiency models, UART, SPI and I2C protocols. Guided 50+ students, taught embedded systems concepts, supervised projects with individualized support, fostered collaborative learning.

University of Texas at Dallas, Texas, USA

Webmaster **Jan 2023 – Present**

- Led HTML, CSS, and WordPress development for the IEEE Dallas CAS website, resulting in a visually appealing and user-friendly platform. Increased user engagement by 25% through enhanced design and streamlined navigation.

OpenText, Karnataka, India

Associate Software Engineer **May 2022 – Jul 2022**

- Addressed OpenText Documentum D2's search issues, employing critical thinking to create unit test cases that enhanced product quality by 5%.

Associate Quality Assurance Engineer **Aug 2020 – May 2022**

- Demonstrated adaptability through QA validation for OpenText Documentum D2, utilizing Selenium and CI/CD-Jenkins, while achieving a 95% coverage and 92% positive performance report.

Engineering Intern **Oct 2019 – Apr 2020**

- Employed Appium and Android Studio to create an automation test suite for OpenText Documentum D2 on mobile devices. Covered 70% of product functionality.

Research Experience

Processing-In-Memory

Research in energy-efficient MCU operation, employing PIM and CIM for ML tasks in MCU. Enhancing edge device efficiency and real-time ML execution.

Utilization of Drone in Agriculture via TinyML

Pioneering drone technology for precision agriculture. Capturing vital data, integrating TinyML via Edge Impulse to detect diseases, and providing actionable insights for enhanced crop yield.

Academic Projects

Tiny ML classification model *Embedded C, TinyMl, edgeimpulse,energia, MatLab*

Using Energia and EdgeImpulse, developed a Tiny ML model on the TI Launchpad CC1352P and BOOSTXL-Sensors. Enabled motion and audio detection through data recording and spectral analysis.

GF65 Cell Library *Verilog, Synopsus Design Vision, Hspice, primeLib, modelsim*

Led gate design in Cadence Virtuoso with a 70nm channel length poly process. Developed a customized library for precise static timing analysis using Primilib with PrimeTime, achieving 95% accuracy via HSPICE simulations.

Automatic Scan Chain Insertion *TCL script, Verilog ,TetraMax, Xilinx vivado*

Devised a TCL script in Synopsys Design Compiler for automated scan chain insertion using multiplexer-based D flip-flops in Verilog-based sequential circuits.

CPU performance evaluation *Python, GEM5*

Engaged in teamwork to evaluate cache designs and branch predictors for x86 architecture microprocessor performance, utilizing the GEM5 simulator and Linux environment.

Certifications and Awards

JIRA certification - OpenText, Machine Learning crash course - Google, OpenText Voyager awards for outstanding performance in 2021 and 2022.