YAGNA SRINIVASA HARSHA ANNADATA

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ACADEMIC PROFILE

Master of Science, Computer Engineering **GPA:3.72/4**

University of Texas at Dallas, Texas **August 2022 – May 2024**

Coursework: VLSI, Embedded systems, Advanced Digital Logics, Computer Architecture, Statistics for Data Science, Testing and Testable design, Design Analysis of Reconfigurable systems, Web Programming Languages, Applied Data structures and algorithms.

Bachelor of Technology, Electronics and Communication Engineering **GPA:8.3/10**

Jawaharlal Nehru Technological University, India **August 2016 – August 2020**

SKILLS

- **Platforms/Tools:** Tetramax, Arduino IDE, MATLAB, Primetime, Synopsys Design Vision, Cadence, HSpice, PrimeLib, Selenium, Jenkins, Eclipse, JIRA, Confluence, Agile Methodologies, Energia IDE.
- **Languages:** Verilog, TCL Script, Java, C, Embedded C, Shell Script.

WORK EXPERIENCE

University of Texas at Dallas, Texas, USA

Webmaster **January 2023 – present**

- Development of the website of IEEE Dallas CAS under prof. Tooraj Nikoubin using HTML, CSS and WordPress.

OpenText, Karnataka, India

Associate Software Engineer **May 2022 – July 2022**

- Fixed issues surrounding the search functionality of the OpenText Documentum D2.
- Developed unit test case to access the product robustness and facilitate the improvement of the product quality by 5%.

Associate Quality Assurance Engineer **August 2020 – May 2022**

- Worked on QA validation for OpenText Documentum D2 product on Linux, MAC and Windows.
- The product's functionality was tested and validated through automation using Selenium and CI/CD Jenkins.
- Developed regression test suite to achieve 95% overall coverage, resulting in a 92% positive performance report.

Engineering Intern **October 2019 – April 2020**

- Developed an automation test suite for the OpenText Documentum D2 on mobile platform using Appium and Android studio which covered 70% of the product functionality.

ACADEMIC PROJECTS

- **Tiny ML classification model**
  - Using Energia and EdgeImpulse, developed a Tiny ML model on the TI Launchpad CC1352P and BOOSTXL-Sensors. By recording data, applying spectral analysis, and programming the generated file onto the hardware, the deployed model enables motion and audio detection.
- **GF65 Cell Library**
  - Designed gates (NOR, XOR, NAND, INV, 2:1 MUX, D Flipflop) using Cadence Virtuoso and a 70nm channel length poly process. Developed a customized library with Primilib for accurate static timing analysis using PrimeTime. Achieved 95% accuracy through HSPICE simulations, validating design effectiveness.
- **Automatic Scan Chain Insertion**
  - Designed a TCL script in Synopsys Design Compiler to automate the insertion of scan chains using multiplexer-based D flip-flops in Verilog-based sequential circuits.
- **CPU performance evaluation**
  - Using the GEM5 simulator and Linux, conducted an analysis to determine the impact of different cache designs and branch predictors on the overall performance of the x86 architecture microprocessor.

CERTIFICATION

- System Verilog Accelerated Verification using UVM certification by Cadence.
  - To create verification environments using system Verilog UVM.
- Certification in Physical Verification System by Cadence.
  - Identifying the features and advance debug solutions in PVS with set up and run.

VOLUNTEER

- 16TH IEEE Dallas circuits and systems conference.
  - Organized Tiny ML workshop which helped students to understand and develop projects on edge impulse.
- President for Technolites, technical committee for Electronics and Communication department.
  - Organized and Conducted tech talks, seminars, workshops, technical fests and annual college fests.

ACHIEVEMENTS AND AWARDS

- I was awarded the OpenText Voyager award for clearing the maximum number of bugs present in Documentum D2 v16.7 in 2021. Also, received awards for excellent performance in Documentum D2 for the years 2021 & 2022.