YAGNA SRINIVASA HARSHA ANNADATA
Phn:+19728139584 Email :harshaedu.ays@gmail.com LinkedIn :yagna-srinivasa-harsha-annadata

Education

University of Texas at Dallas, Texas **Aug 2022 – Dec 2024**
MS-Thesis, Computer Engineering, Hardware Automation using AI/ML and VLSI **GPA: 3.71/4**

Jawaharlal Nehru Technological University, India **Aug 2016 – Aug 2020**
B.Tech, Electronics and Communication Engineering **GPA: 3.5/4**

Technical Skills

Platforms/Tools: GEM5, xilinx vivado, Synopsys Design Compiler, Synopsys TetraMAX, Arduino IDE, Innovus, HSpice, Selenium, Jenkins, Eclipse, JIRA, Confluence, Energia IDE, Google Colab, Oscilloscopes, Logic and Protocol Analyzers, Cadence PCB editors, Allegro, Platform Validation, Debugging Tools, JTAG, WinDbg. **Languages**: Python, Verilog, C, Shell Script.

Professional Experience

Intel Corporation, Oregon, USA
CPU E-Core Physical Design Engineer **Mar 2024 – Current**

- Executed timing runs for multiple **clocks** using an **internal pipelining tool** and structured **YAML configurations**, orchestrating **setup analysis**, followed by **max/min timing checks** and functional validations across various STA modes.
- Performed **timing debug and regression analysis** by restoring **PrimeTime sessions**, analyzing **path-level delta slack**, and automating detection of recurring **timing degradations** using custom scripts.
- Currently designing an **AI-driven application** to accelerate **STA flow analysis** and **automation debugging**, aiming to enhance detection of **timing regressions**, **constraint mismatches**, and improve analysis efficiency by **50%**.

Intel Corporation, Oregon, USA
Silicon Integration and Validation Engineer Intern **Feb 2024 – Dec 2024**

- Performed **pre- and post-silicon validation using simulation/emulation tools (Simics, HFPGA)**, developed and automated functional, performance, and stress test cases for new features, and resolved 80+ issues during silicon bring-up of **HSIO interfaces (USB, PCIe, Thunderbolt)** using advanced debugging tools **(JTAG, analyzers, oscilloscopes)**.

University of Texas at Dallas, Texas, USA
Graduate Teaching Assistant **Aug 2023 – Jan 2024**

- Supervised 50+ students in CE6302 embedded systems lab, on TI development boards in areas like **TinyML, energy efficiency, and UART, SPI, and I2C**. Provided mentorship on embedded systems concepts, achieving a 100% completion rate.

OpenText Corporation, Karnataka, India
Associate Software Engineer **Aug 2020 – Jul 2022**

- Fixed OpenText Documentum D2 search issues, emphasizing query-based operations and **client machine content** transfer. Performed comprehensive QA validation of Documentum D2 across **Linux, macOS, and Windows platforms, leveraging Selenium and CI/CD pipelines**. Achieved results with 95% regression test coverage and a positive performance report of 92%.

Publications

Enhancing Drone-Based Precision Agriculture **Published: Springer Nature- Computer Science 2025**

- Illustrating and optimizing the impact of training parameters on multi-disease plant detection using Edge Impulse, while maintaining an accuracy of 80% SN COMPUT. SCI. 6, 132 (2025).

TinyML Powered Drone in Agriculture Application **Published: IEEE DCAS 2024**

- demonstrating plant disease detection via Edge Impulse with up to 80% accuracy. DOI: 10.1109/DCAS61159.2024.10539880.

Projects

CPU performance evaluation **Tech: Python, GEM5, Linux**

- Engaged in teamwork to derive a cost function with varied cache sizes and branch predictors for **x86 architecture** CPU performance, utilizing the **GEM5, Makefile, Python, and Linux**. Identified an optimum configuration with 10% reduction in cost.

3000 Cell State Machine **Tech: Verilog, xilinx vivado, Design Vision, Hspice, Innovus**

- Designed and Characterized standard cells for a 3000-cell state machine using **Xilinx Vivado for GF65nm** technology. Performed simulations **(DRC, LVS, PEX, HSPICE)** with 95% accuracy. Synthesized, and generated **timing diagrams** of the design, and produced cell reports using Design Vision. Developed **schematics, layouts, library generation, and abstract views** for all cells with **automatic placement and routing in Innovus** involved in the state machine.

Volunteering and Recognition

Outstanding Graduate Student of the Year 2024 Award: recognized by Dept of ECE at UTD.

Leadership: Led intern cohort sessions at Intel and served as President of technology clubs. Mentored students at the IEEE DCAS 2024 workshop, on integrating TinyML into embedded systems.

Intel Recognition: Commended for contributions during power-on, resolving config issues, and delivering a key demo to leadership.