YAGNA SRINIVASA HARSHA ANNADATA

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Education

University of Texas at Dallas, Texas **Aug 2022 – Dec 2024**

MS-Thesis, Computer Engineering **GPA: 3.71/4**

- Research: Tiny Machine Learning for Embedded systems, Computer Architecture, VLSI Design & Testing, Data structures.

Jawaharlal Nehru Technological University, India **Aug 2016 – Aug 2020**

B.Tech, Electronics and Communication Engineering **GPA: 3.5/4**

Technical Skills

Platforms/Tools: GEM5, Cadence Virtuoso, Synopsys Design Compiler, Synopsys TetraMAX, Arduino IDE, MATLAB, Primetime, HSpice, PrimeLib, Selenium, Jenkins, Eclipse, JIRA, Confluence, Energia IDE, Google Colab, Oscilloscopes, Logic and Protocol Analyzers, Cadence PCB editors, Allegro, Platform Validation, Debugging Tools, JTAG, WinDgb.

Languages: Verilog, Python, C, Shell Script, Embedded C.

Professional Experience

Intel Corporation, Oregon, USA

Silicon Integration and Validation Engineer Intern **Feb 2024 – Current**

- Executed comprehensive validation for silicon and system integration, focusing on **functional testing (packet and error handling), performance assessments (throughput, latency, packet loss), and interoperability** to ensure 100% platform readiness.
- Applied **debugging techniques** for **post-silicon validation**, resolved 80+ feature issues and supported **silicon bring-up for HSIO interfaces like USB, PCIe, and Thunderbolt**. Used tools like **logic and protocol analyzers, Allegro, and JTAG** for in-depth failure analysis. Integrated **firmware, BIOS, and drivers within Intel's BKC** to ensure system stability and 100% quality.
- Performed functionality and compatibility tests to achieve 100% test coverage, including extended load assessments, utilizing **Simulation and Emulation tools such as HFPGA for pre-silicon validation** of hardware and RTL designs.
- Built automated device compatibility frameworks covering 100% of functionalities with **Python, and Intel tools** to enhance **functional, stress, and performance testing, supporting log analysis, report generation, and optimization** to meet standards.

University of Texas at Dallas, Texas, USA

Graduate Teaching Assistant **Aug 2023 – Jan 2024**

- Supervised 50+ students in CE6302 embedded systems lab, on TI development boards in areas like **TinyML, energy efficiency, and UART, SPI, and I2C**. Provided mentorship on embedded systems concepts, achieving a 100% completion rate.

OpenText Corporation, Karnataka, India

Associate Software Engineer **May 2022 – Jul 2022**

- Fixed OpenText Documentum D2 search issues, emphasizing query-based operations and **client machine content** transfer. Implemented a robust unit test suite, resulting in a 5% boost in overall product quality.

OpenText Corporation, Karnataka, India

Associate Quality Assurance Engineer **Aug 2020 – May 2022**

- Performed comprehensive QA validation of Documentum D2 across **Linux, macOS, and Windows platforms, leveraging Selenium and CI/CD pipelines**. Achieved results with 95% regression test coverage and a positive performance report of 92%.

Projects

Drone Applications in Precision Agriculture **Tech: Micro-Controller, Tiny Machine Learning, Edge Impulse**

- Researched and published at the **2024 IEEE Dallas Circuits and Systems Conference**, it pioneers drone technology in precision agriculture with TinyML via Edge Impulse to detect diseases with **80% accuracy**. DOI: 10.1109/DCAS61159.2024.10539880.

CPU performance evaluation **Tech: Python, GEM5, Linux**

- Engaged in teamwork to derive a cost function with varied cache sizes and branch predictors for **x86 architecture** CPU performance, utilizing the **GEM5, Makefile, Python, and Linux**. Identified an optimum configuration with 10% reduction in cost.

Standard Cell Library **Tech: Verilog, Cadence Virtuoso, Synopsys Design Vision, Hspice, Prime Lib, Modelsim**

- Designed and optimized standard cells in **Virtuoso** for **GF65nm** technology, including an Asynchronous Set and Reset D-FF with minimal diffusion breaks, performed simulations **(DRC/LVS/PEX/HSPICE)** with 95% accuracy, and characterized cell library.

Automatic Scan Chain Insertion **Tech: TCL script, Verilog ,TetraMax, Xilinx Vivado**

- Achieved 100% test coverage through **Automatic Test Pattern Generation(ATPG) in TetraMAX** Utilizing Synopsys Design Vision for **DRC and SFF insertion** using **TCL script**, and developing Verilog-based fault models.

Awards, Volunteering and Recognition

Leadership: Led intern cohort sessions at Intel and served as President of a technology club in both undergrad and high school.

TinyML Workshop IEEE DCAS 2024: Volunteered at a workshop empowering students to integrate ML into embedded systems, enhancing skills in motion, audio, and image recognition.

Intel Recognition: Commended for contributions during power-on, resolving config issues, and delivering a key demo to leadership.