YAGNA SRINIVASA HARSHA ANNADATA
Phn:+19452087629 Email :yxa210024@utdallas.edu Website :Yagna Annadata LinkedIn :yagna-srinivasa-harsha-annadata

Education

University of Texas at Dallas, Texas **Aug 2022 – May 2024**
MSc, Computer Engineering **GPA: 3.72/4**
- Embedded systems, Machine Learning, Computer Architecture, ASIC, VLSI Design, VLSI Testing, Applied Data structures.

Jawaharlal Nehru Technological University, India **Aug 2016 – Aug 2020**
B.Tech, Electronics and Communication Engineering **GPA: 3.5/4**

Technical Skills

Platforms/Tools: GEM5, Cadence Virtuoso, Synopsys Design Compiler, Synopsys TetraMAX, Arduino IDE, MATLAB, Primetime, HSpice, PrimeLib, Selenium, Jenkins, Eclipse, JIRA, Confluence, Energia IDE, Google colab, Code composer studio

Languages: Verilog, TCL Script, Java, C, Embedded C, Shell Script, Python

Research

Processing-In-Memory
Investigating energy-efficient research pathways entails utilizing In-Memory Computing with TinyML on MCU to enhance the efficiency of edge devices while simultaneously reducing the real-time execution demands of ML tasks, thereby optimizing performance.

Utilization of Drone in Agriculture via TinyML
Pioneering drone technology for precision agriculture. Capturing vital data, integrating TinyML via Edge Impulse to detect diseases, and providing actionable insights for enhanced crop yield.

Academic Projects

Standard Cell Library Tech: Verilog, Cadence virtuoso, Synopsys Design Vision, Hspice, Prime Lib, Modelsim
Designed and optimized standard cells in **Cadence Virtuoso** for **GF65nm** technology, including an Asynchronous Set and Reset D-FF with minimal diffusion breaks, performed simulations **(DRC/LVS/PEX/HSPICE)** with 95% accuracy, and characterized cell library.

Automatic Scan Chain Insertion Tech: TCL script, Verilog ,TetraMax, Xilinx Vivado
Utilized Synopsys Design Vision for **DRC and SFF insertion** using a **TCL script**, while devising Verilog-based fault models to achieve 100% test coverage through **ATPG in TetraMAX**.

CPU performance evaluation Tech: Python, GEM5
Engaged in teamwork to evaluate cache designs and branch predictors for **x86 architecture** microprocessor performance, utilizing the **GEM5 simulator and Linux** environment.

RISC Microcontroller Design Tech: Xilinx ISE, Verilog
Implemented, simulated, and synthesized, a custom **4-stage pipelined RISC architecture microcontroller**, optimized with introsuction of stalls for **Data Hazards and Branch detection** on Xilinx ISE.

Artificial Neural Network Tech: Python, Google colab
Built a classification Artificial Neural Network using **one hidden layer and ReLU activation**. Optimized parameters through **hyperparameter tuning**, achieving 45% training and 80% testing accuracy.

Professional Experience

University of Texas at Dallas, Texas, USA
Graduate Teaching Assistant **Aug 2023 – Present**
- Developed projects for embedded systems lab which includes **energy efficiency models, UART, SPI and I2C protocols**. Guided 50+ students, taught embedded systems concepts, supervised projects with support, fostered collaborative learning.

University of Texas at Dallas, Texas, USA
Webmaster **Jan 2023 – Present**
- Led **HTML, CSS, and WordPress** development for the IEEE Dallas CAS website, resulting in a user-friendly and visually appealing platform. Increased user engagement by 25% through enhanced design and streamlined navigation.

OpenText, Karnataka, India
Associate Software Engineer **May 2022 – Jul 2022**
- Addressed OpenText Documentum D2's search issues, employing critical thinking to create unit test cases that enhanced product quality by 5%.

OpenText, Karnataka, India
Associate Quality Assurance Engineer **Aug 2020 – May 2022**
- Demonstrated adaptability through QA validation for OpenText Documentum D2, utilizing Selenium and CI/CD-Jenkins, while achieving a 95% coverage and 92% positive performance report.

OpenText, Karnataka, India
Engineering Intern **Oct 2019 – Apr 2020**
- Employed Appium and Android Studio to create an automation test suite for OpenText Documentum D2 on mobile devices. Covered 70% of product functionality.