YAGNA SRINIVASA HARSHA ANNADATA
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Education

University of Texas at Dallas, Texas **Aug 2022 – Dec 2024**
MS-Thesis, Computer Engineering **GPA: 3.71/4**
- Research: Tiny Machine Learning for Embedded systems, Computer Architecture, VLSI Design & Testing, Data structures.

Jawaharlal Nehru Technological University, India **Aug 2016 – Aug 2020**
B.Tech, Electronics and Communication Engineering **GPA: 3.5/4**

Technical Skills

Platforms/Tools: GEM5, Cadence Virtuoso, Synopsys Design Compiler, Synopsys TetraMAX, Arduino IDE, MATLAB, Primetime, HSpice, PrimeLib, Selenium, Jenkins, Eclipse, JIRA, Confluence, Energia IDE, Google Colab, Code composer studio, Oscilloscopes, Logic and Protocol Analyzers, Cadence PCB editors, Allegro, Platform Validation, Debugging Tools, JTAG, WinDgb.

Languages: Verilog, TCL Script, Java, C, Embedded C, Shell Script, Python.

Professional Experience

Intel Corporation, Oregon, USA
Silicon Integration and Validation Engineer Intern **Feb 2024 – Current**
- Brought-up and configured Hardware boards for Implementing Type C USB and Thunderbolt protocols, resolving issues across **80+ features** and maintaining a 97% product quality rating. Utilized tools like **logic and protocol analyzers, Cadence PCB editors, Allegro, WinDgb, and JTAG for failure analysis and corrective measures.** Managed feature enablement and test case development for each execution cycle. Led automation tasks for Type C subsystems and PCIe/Storage domains using **Python, Intel's frameworks, hardware setups, and VM configurations**. Presented progress to senior leadership, collaborated with multinational teams, and contributed to **pre-silicon and post-silicon enablement, integration, validation, and BKC releases.**

University of Texas at Dallas, Texas, USA
Graduate Teaching Assistant **Aug 2023 – Jan 2024**
- Supervised embedded systems lab for Course, CE6302, leveraging TI development boards to drive advancements in areas such as **TinyML, energy efficiency models, and UART, SPI, and I2C protocols**. Mentored over 50 students, providing invaluable guidance on embedded systems concepts and project support, resulting in a 100% successful project completion rate.

OpenText Corporation, Karnataka, India
Associate Software Engineer **May 2022 – Jul 2022**
- Fixed OpenText Documentum D2 search issues, emphasizing query-based operations and **client machine content** transfer. Implemented a robust unit test suite, resulting in a 5% boost in overall product quality.

OpenText Corporation, Karnataka, India
Associate Quality Assurance Engineer **Aug 2020 – May 2022**
- Performed comprehensive QA validation of Documentum D2 across **Linux, macOS, and Windows platforms, leveraging Selenium and CI/CD pipelines**. Achieved results with 95% regression test coverage and a positive performance report of 92%

Research Projects

Drone Applications in Agriculture with TinyML, UTD, **Jun 2023 – Dec 2023**
- Published at the **2024 IEEE Dallas Circuits and Systems Conference**, research pioneers drone technology in precision agriculture with TinyML via Edge Impulse to detect diseases with **80% accuracy**. DOI: 10.1109/DCAS61159.2024.10539880

Academic Projects

CPU performance evaluation **Tech: Python, GEM5**
- Engaged in teamwork to derive a cost function with varied cache sizes and branch predictors for **x86 architecture** CPU performance, utilizing the **GEM5, Makefile, Python, and Linux**. Identified an optimum configuration with 10% reduction in cost.

Standard Cell Library **Tech: Verilog, Cadence Virtuoso, Synopsys Design Vision, Hspice, Prime Lib, Modelsim**
- Designed and optimized standard cells in **Virtuoso** for **GF65nm** technology, including an Asynchronous Set and Reset D-FF with minimal diffusion breaks, performed simulations **(DRC/LVS/PEX/HSPICE)** with 95% accuracy, and characterized cell library.

Automatic Scan Chain Insertion **Tech: TCL script, Verilog ,TetraMax, Xilinx Vivado**
- Utilized Synopsys Design Vision for **DRC and SFF insertion** using a **TCL script**, while devising Verilog-based fault models to achieve 100% test coverage through **Automatic Test Pattern Generation(ATPG) in TetraMAX**.

Volunteering

TinyML Workshop Supervisor in IEEE DCAS 2024: Empowering students through hands-on workshops to excel in tiny ML and integrate ML into embedded systems, while fostering advanced understanding of motion, audio, and image recognition.

Awards and Recognition

Leadership: Led intern cohort sessions at Intel and served as President of a technology club in both undergrad and high school.

Intel Recognition: Commended for contributions during power-on, resolving config issues, and delivering a key demo to leadership.