

# YAGNA SRINIVASA HARSHA ANNADATA

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## Education

### University of Texas at Dallas, Texas

Aug 2022 – Dec 2024

MS-Thesis, Computer Engineering

GPA: 3.71/4

- Research: Tiny Machine Learning for Embedded systems, Computer Architecture, VLSI Design & Testing, Data structures.

### Jawaharlal Nehru Technological University, India

Aug 2016 – Aug 2020

B.Tech, Electronics and Communication Engineering

GPA: 3.5/4

## Technical Skills

**Platforms/Tools:** GEM5, xilinx vivado, Synopsys Design Compiler, Synopsys TetraMAX, Arduino IDE, Innovus, HSpice, Selenium, Jenkins, Eclipse, JIRA, Confluence, Energia IDE, Google Colab, Oscilloscopes, Logic and Protocol Analyzers, Cadence PCB editors, Allegro, Platform Validation, Debugging Tools, JTAG, WinDbg. **Languages:** Python, Verilog, C, Shell Script.

## Professional Experience

### Intel Corporation, Oregon, USA

CPU E-Core Physical Design Engineer

Mar 2024 – Current

- Performed full-chip **Static Timing Analysis (STA)** using **Synopsys PrimeTime** across multiple **PVT corners**, identifying and resolving **90%+ of critical timing violations** through targeted **physical design enhancements** and **slack optimizations**.
- Contributed to **Clock Tree Synthesis (CTS)** and **physical implementation** efforts, optimizing **clock network topology** to minimize **skew** and **insertion delay**, and ensuring reliable **timing closure** across multiple **voltage and clock domains**.
- Currently designing an **AI-driven application** to accelerate **STA flow analysis** and **automation debugging**, aiming to enhance detection of **timing regressions**, **constraint mismatches**, and improve analysis efficiency by **50%**.

### Intel Corporation, Oregon, USA

Silicon Integration and Validation Engineer Intern

Feb 2024 – Dec 2024

- Performed **pre- and post-silicon validation using simulation/emulation tools (Simics, HFPGA)**, developed and automated functional, performance, and stress test cases for new features, and resolved 80+ issues during silicon bring-up of **HSIO interfaces (USB, PCIe, Thunderbolt)** using advanced debugging tools (**JTAG, analyzers, oscilloscopes**).

### University of Texas at Dallas, Texas, USA

Graduate Teaching Assistant

Aug 2023 – Jan 2024

- Supervised 50+ students in CE6302 embedded systems lab, on TI development boards in areas like **TinyML, energy efficiency, and UART, SPI, and I2C**. Provided mentorship on embedded systems concepts, achieving a 100% completion rate.

### OpenText Corporation, Karnataka, India

Associate Software Engineer

Aug 2020 – Jul 2022

- Fixed OpenText Documentum D2 search issues, emphasizing query-based operations and **client machine content** transfer. Performed comprehensive QA validation of Documentum D2 across **Linux, macOS, and Windows platforms, leveraging Selenium and CI/CD pipelines**. Achieved results with 95% regression test coverage and a positive performance report of 92%.

## Projects

### Developing Autonomous Embedded Systems using TinyML

Tech: Micro-Controllers, TinyML, Edge Impulse

- Researched and published at the **2024 IEEE DCAS Conference**, showcasing the development of a drone using TinyML via Edge Impulse for plant disease detection with up to **80% accuracy**. DOI: 10.1109/DCAS61159.2024.10539880.

### CPU performance evaluation

Tech: Python, GEM5, Linux

- Engaged in teamwork to derive a cost function with varied cache sizes and branch predictors for **x86 architecture** CPU performance, utilizing the **GEM5, Makefile, Python, and Linux**. Identified an optimum configuration with 10% reduction in cost.

### 3000 Cell State Machine

Tech: Verilog, xilinx vivado, Design Vision, Hspice, Innovus

- Designed and Characterized standard cells for a 3000-cell state machine using **Xilinx Vivado for GF65nm** technology. Performed simulations (**DRC, LVS, PEX, HSPICE**) with 95% accuracy. Synthesized, and generated **timing diagrams** of the design, and produced cell reports using Design Vision. Developed **schematics, layouts, library generation, and abstract views** for all cells with **automatic placement and routing in Innovus** involved in the state machine.

## Volunteering and Recognition

**Leadership:** Led intern cohort sessions at Intel and served as President of technology clubs. Mentored students at the IEEE DCAS 2024 workshop, on integrating TinyML into embedded systems.

**Intel Recognition:** Commended for contributions during power-on, resolving config issues, and delivering a key demo to leadership.