2EC601CC24 – VLSI Design

Topic: AND GATE BASED ON RESISTIVE LOAD AND NMOS BASED DRIVER

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Submitted By:

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I. PROBLEM STATEMENT

Two input AND Gate with resitive Load and NMOS as a driver with propagation delay of 2 ns.

INTRODUCTION: -

An AND gate is a fundamental building block in digital circuit design, used to perform logical conjunctions. This report focuses on an AND gate implemented with resistive load technology and NMOS transistors serving as drivers. The resistive load provides a simple means to achieve output high and low levels, while the NMOS driver transistors manage the switching functionality. This configuration, although straightforward, faces challenges related to speed and power efficiency, especially in modern, high-speed applications. Analyzing this design helps understand its performance characteristics, limitations, and potential optimizations in VLSI implementat

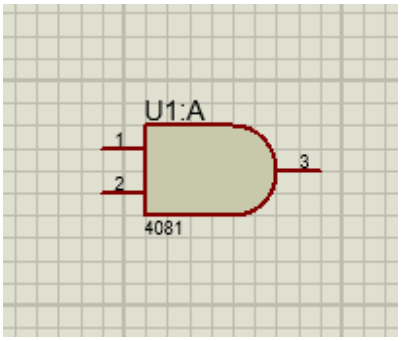
II. DESIGN PROBLEM

1. Optimized Truth Table and Boolean equation:

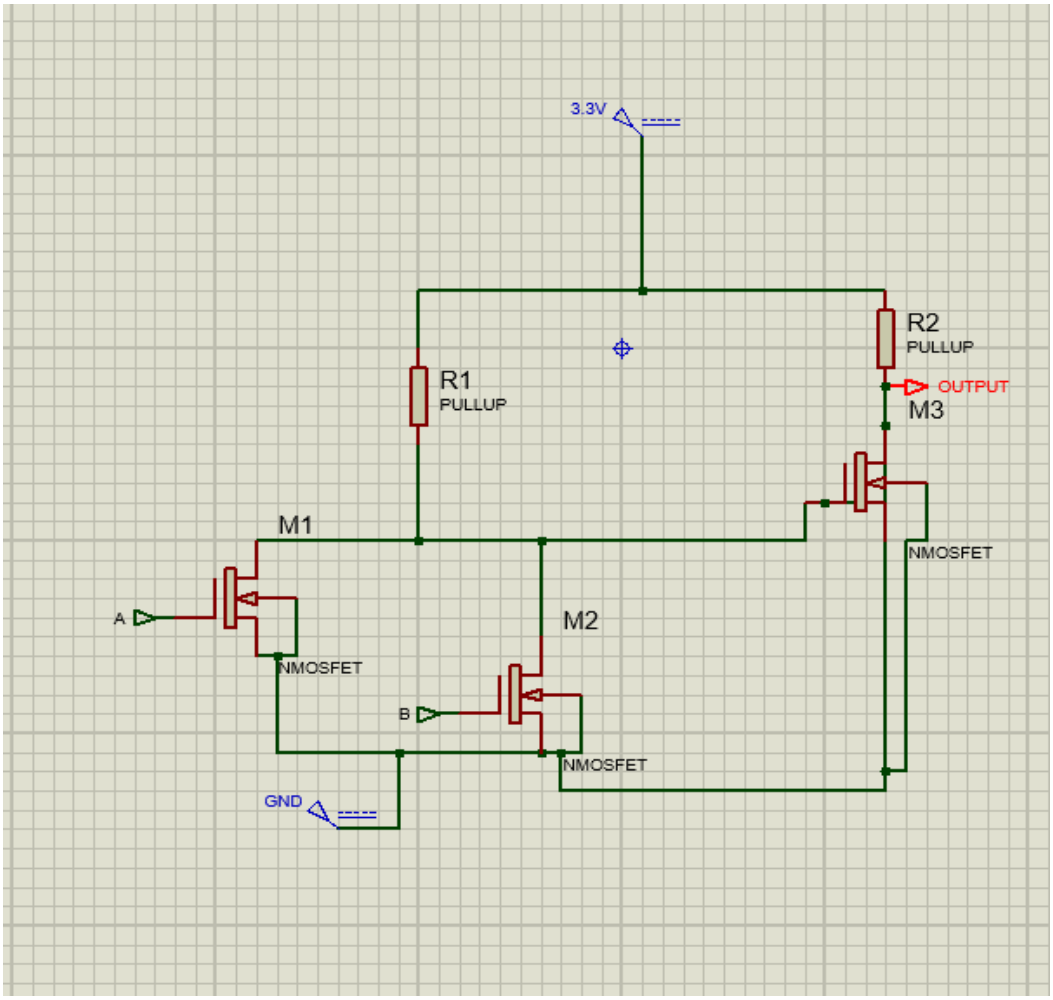
Input		Output
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Output=A.B

2. Optimized Gate level Diagram:



3. Transistor Level Schematic for MOS Implementation:



4. Draw stick diagram for above implementation level using proper colour code.

ANS. I can't drawn stick diagram because in this case this is not cmos based implementation and this is based on resistive load and NMOS driver based report.

5.State the various level of VOL corresponding to various transistor statuses

Voltage Levels (VOL) for AND Gate with NMOS Driver (Using Inverter for NAND-to-AND Conversion)

In the AND gate circuit, the output is derived by first implementing a NAND gate and then inverting its output using an inverter. The inverter is built using an NMOS transistor with a 20K resistor as the load. The following states describe the voltage levels (VOL) under different conditions:

1. NAND Gate Output (Before Inversion):
    - Both Inputs Low: When both inputs of the NAND gate are low (0), the NAND output will be high (1) because the NMOS in the NAND gate is OFF.
    - Both Inputs High: When both inputs of the NAND gate are high (1), the NAND output will be low (0) due to the NMOS conducting in the NAND gate.
2. Inverter Operation:
    - The inverter inverts the output of the NAND gate. Therefore, the output of the AND gate is the inverse of the NAND gate's output.

Voltage Levels After Inverter:

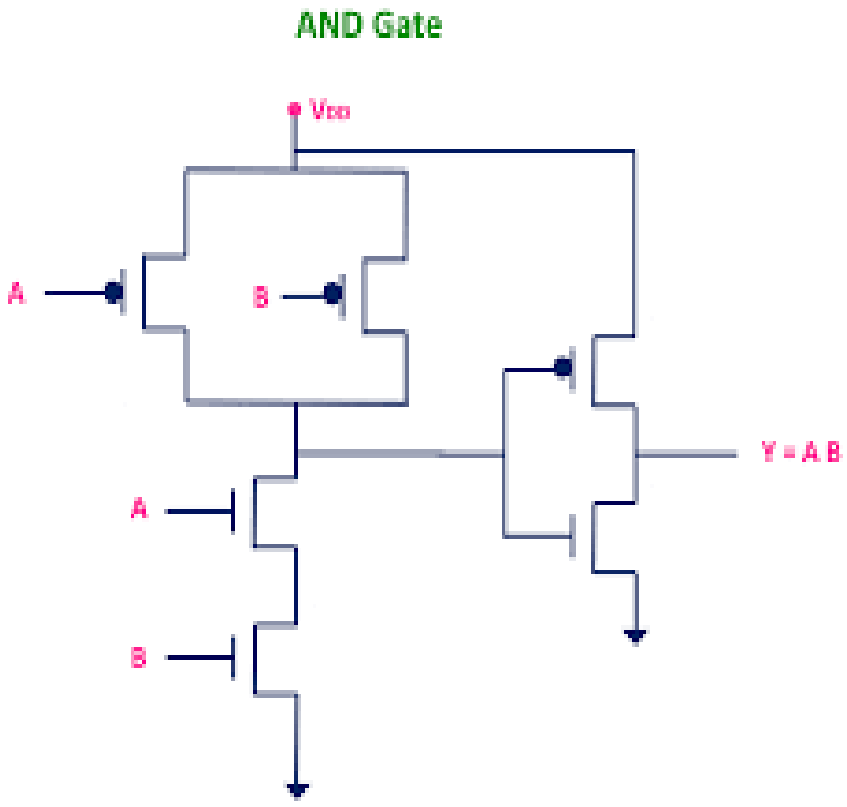
1. NAND Gate Output High (Both Inputs Low)
    - When the inputs to the NAND gate are low, its output is high (1). The inverter will invert this high to low.
    - AND Gate Output (After Inversion) = VOL ≈ 0V (logic 0).

2. NAND Gate Output Low (Both Inputs High)
    - When both inputs to the NAND gate are high, the NAND output is low (0). The inverter will invert this low to high.
    - AND Gate Output (After Inversion) = VOL ≈ Vdd (typically 5V, 3.3V, or any specified voltage).
3. Intermediate State (One Input High, One Input Low in NAND Gate)
    - If one input to the NAND gate is high and the other is low, the NAND gate will output high (1). The inverter will invert this to low (0).
    - AND Gate Output (After Inversion) = VOL ≈ 0V (logic 0).

Total number of VOL levels are 3.

6. Find an equivalent CMOS inverter circuit.

ANS. Equivalent CMOS inverter circuit as per below:



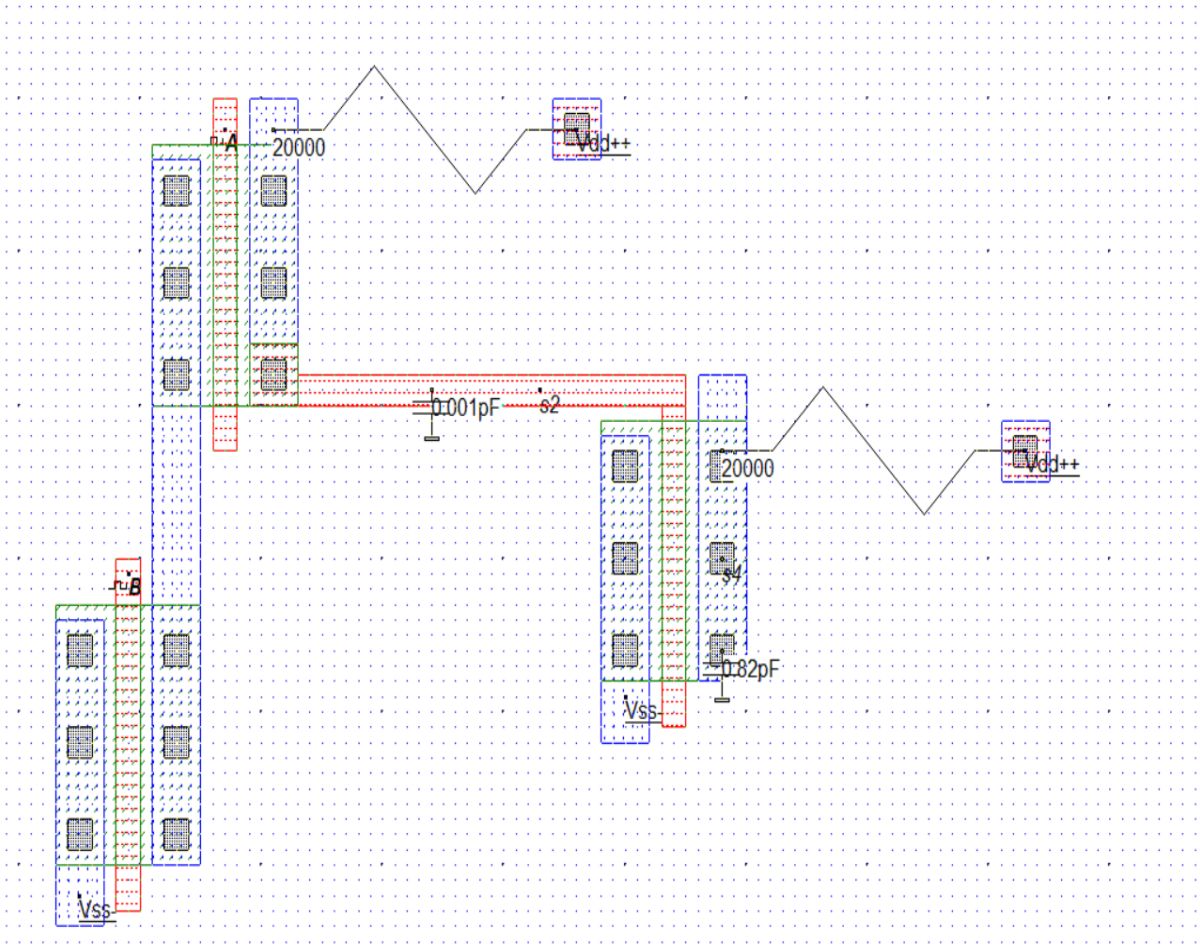
7. For MOS implementation, what input patterns give the lowest output resistance when the output is low? What is the value of that resistance?

ANS. I got low output when A/B=1 or A=0 and B=0 at that time the lowest output resistance is 10K because resistor of NAND gate and inverter become parallel.

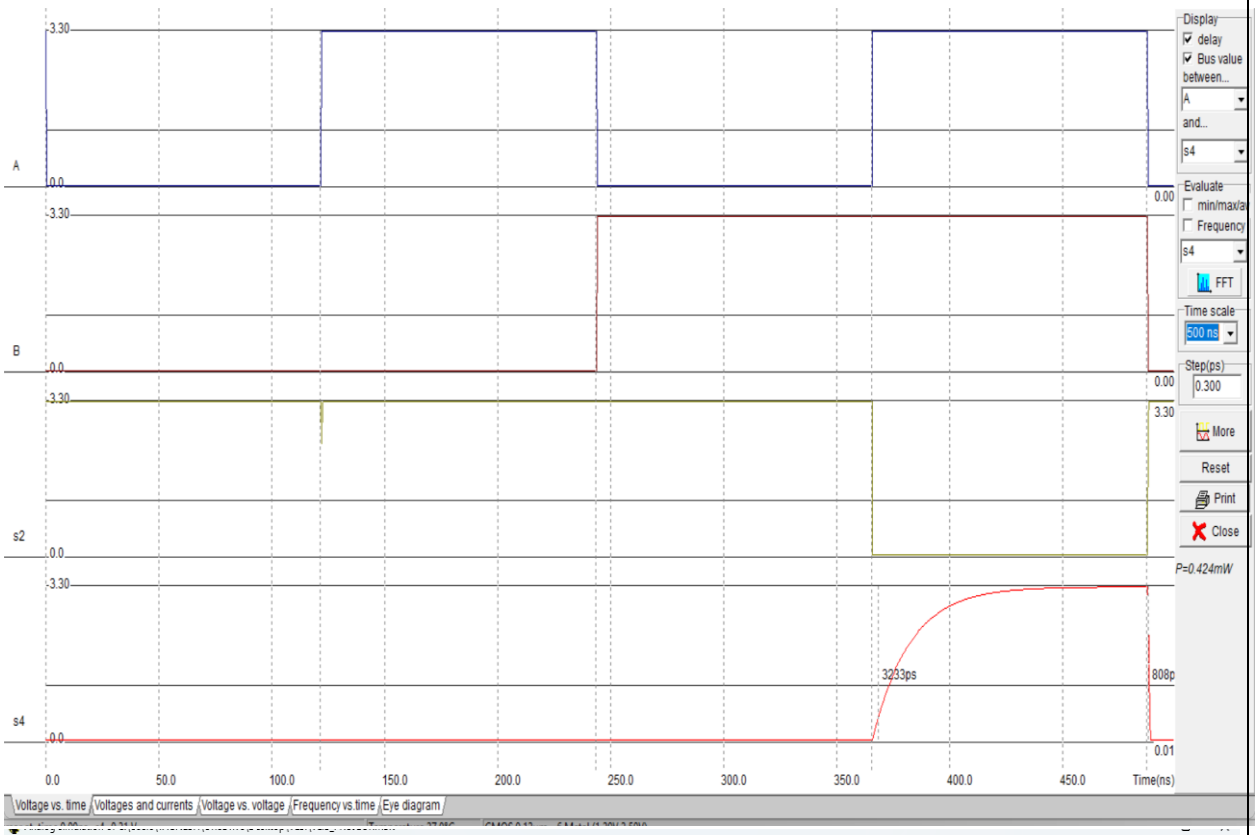
8. For MOS implementation, what input patterns give the lowest output resistance when the output is high? What is the value of that output resistance?

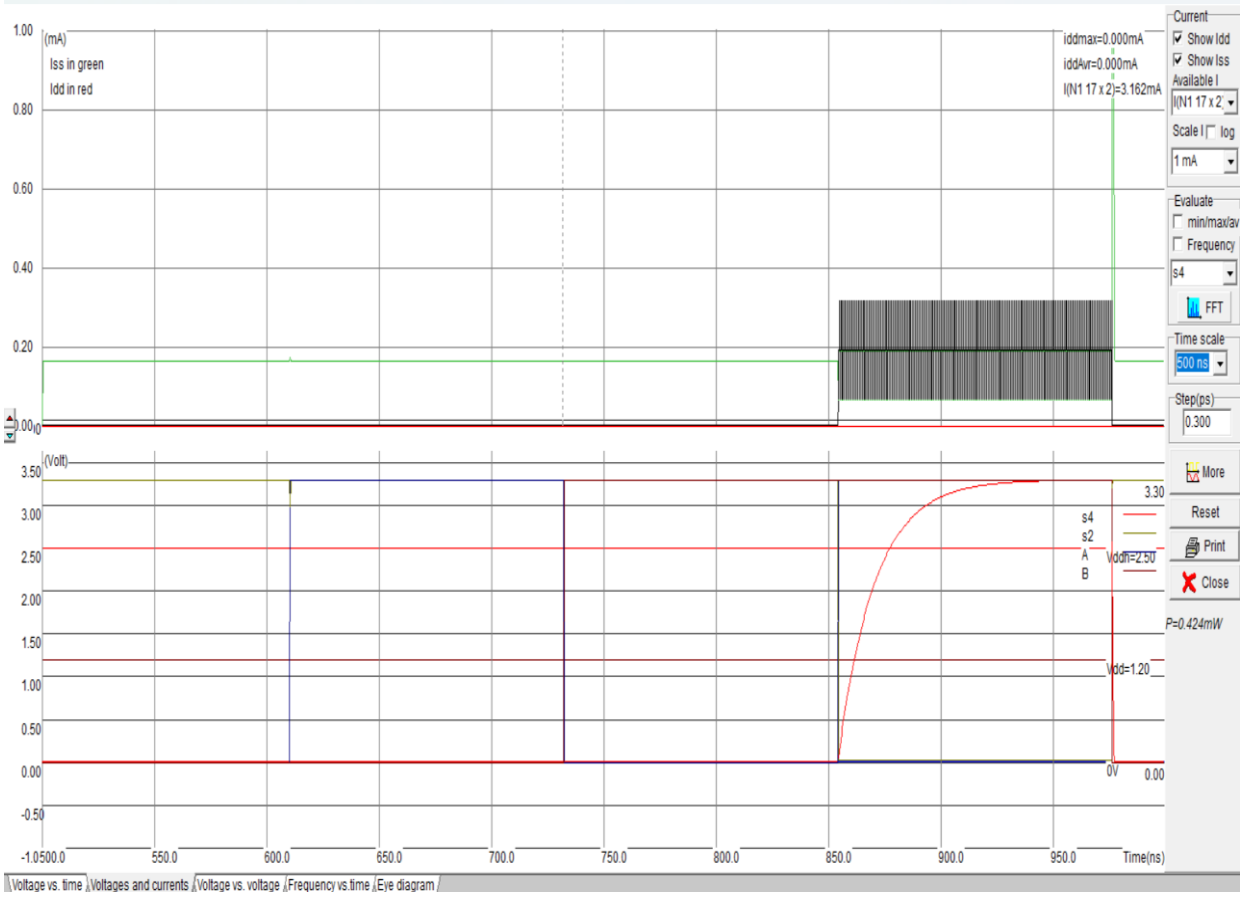
ANS. Output is high when A=1 and B=1 at that time lowest output resistance is 1.043Kohm because input voltage is 3.3V and at the time of output current is 3.162Ma.

9. Prepare the layout using Microwind tool.

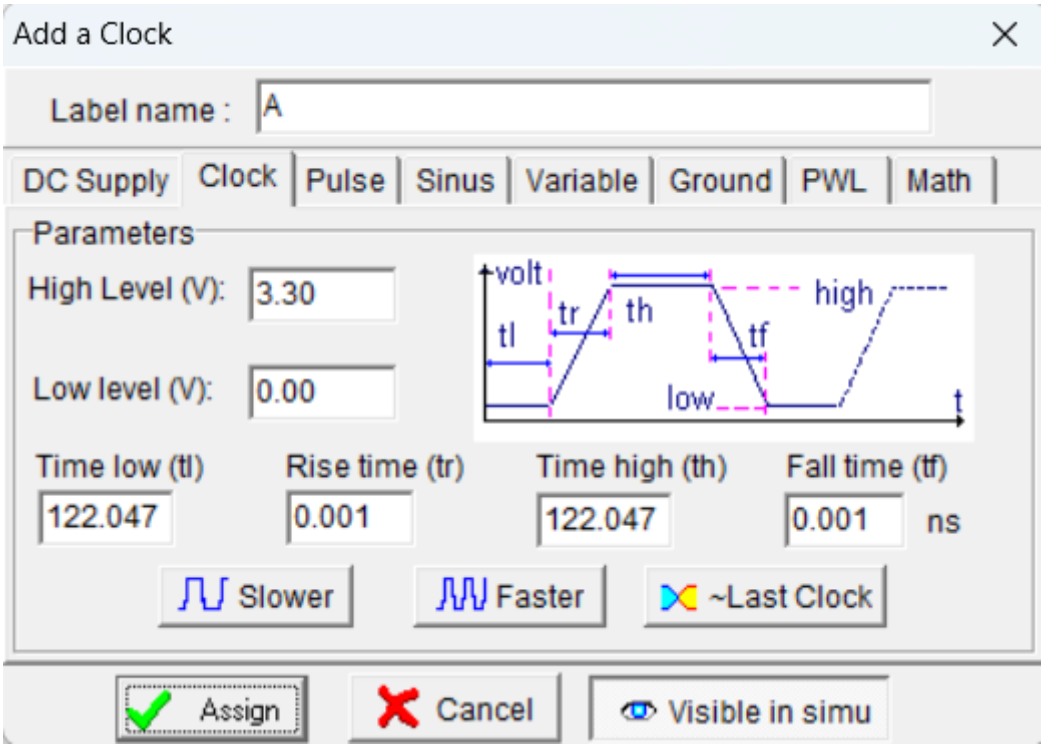


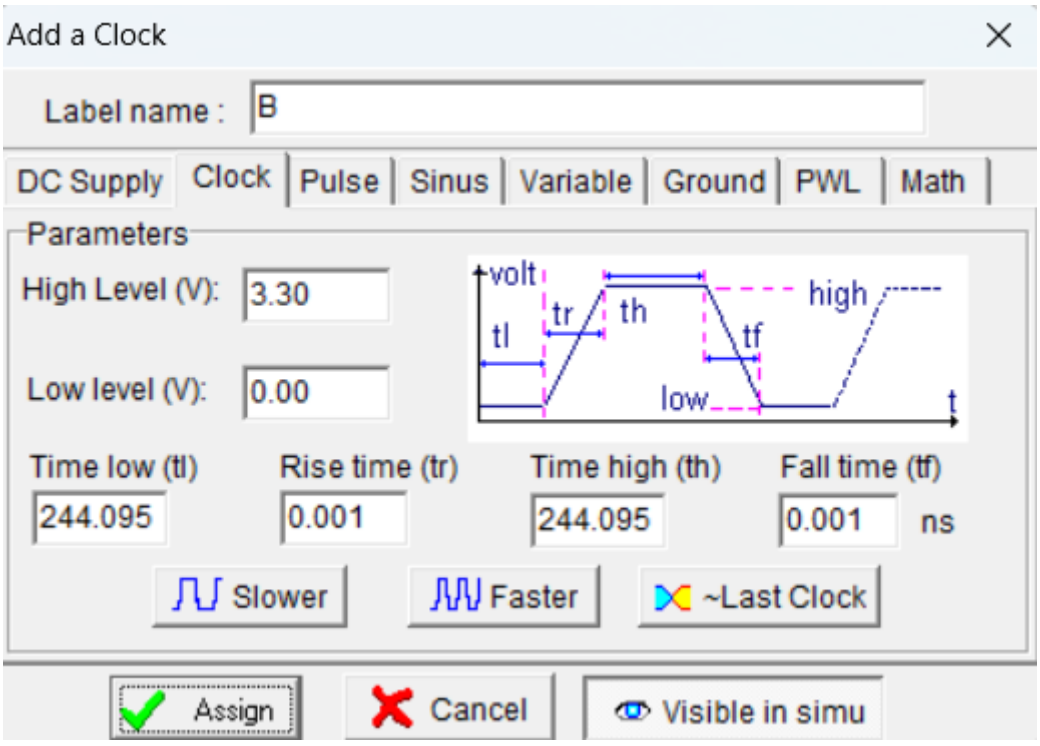
10. Simulate it for various combinations of inputs.





11. Measure the rise time, fall time, propagation delay and other parameters.





Rise time=0.0001ns

Fall time=0.001
TPLH=3233
TPHL=808
TP=(3233+808)ps/2=2020.5ps=2.02ns
Where TP is progation delay which we achived as per mentioned in problem statement.

Conclusion: -

the AND gate was constructed using a 20 kΩ resistor as the load and NMOS transistors as drivers to form a NAND gate, which was then passed through an inverter built with similar components to achieve the final AND gate output. Capacitors (0.0001 pF in the intermediate stage and 0.82 pF at the output) were used to manage delay and response time, achieving a 2ns delay at the output.

The voltage levels at the output (VOL and VOH) were carefully controlled to ensure correct logic operation. VOL (output low voltage) was near 0V, indicating proper NMOS conduction when the gate is low. VOH (output high voltage) was close to Vdd, confirming proper logic high output when the NMOS was off. These voltage levels remained within acceptable ranges, ensuring reliable logic state representation.

The delay was optimized in the 10-50 ps range, balancing speed and accuracy. The 20 kΩ resistor controlled the current, preventing excessive power dissipation and maintaining efficient switching. Overall, this design successfully demonstrated the functionality of an AND gate, with controlled delay and precise voltage levels for accurate logic output.