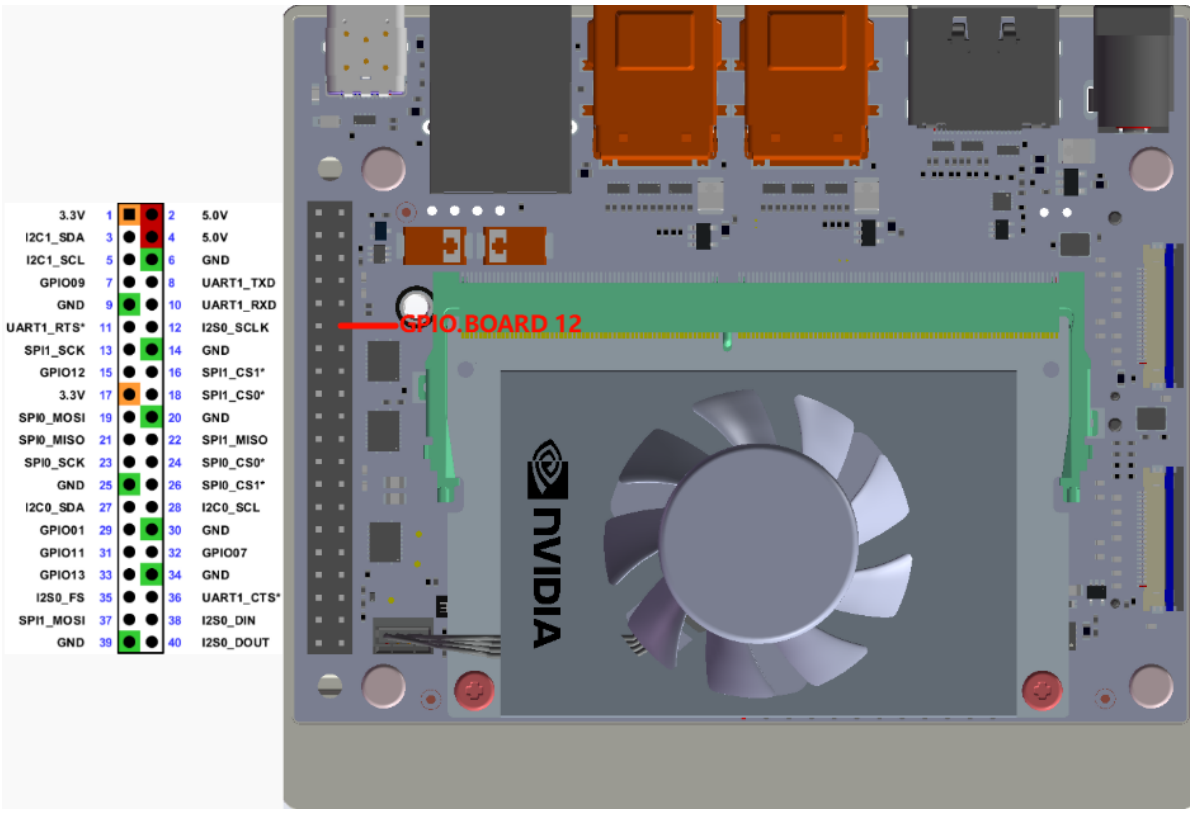
GPIO output function

1. GPIO pin diagram comparison table

GPIO.BOARD 12 pin corresponds to GPIO.BCM 18 pin:



2. Jetson orin super GPIO repair

Note: After upgrading to Jetson orin super, most GPIO ports have changed from the original bidirectional (input + output) to input only. Now two solutions are provided to modify GPIO to a bidirectional interface.

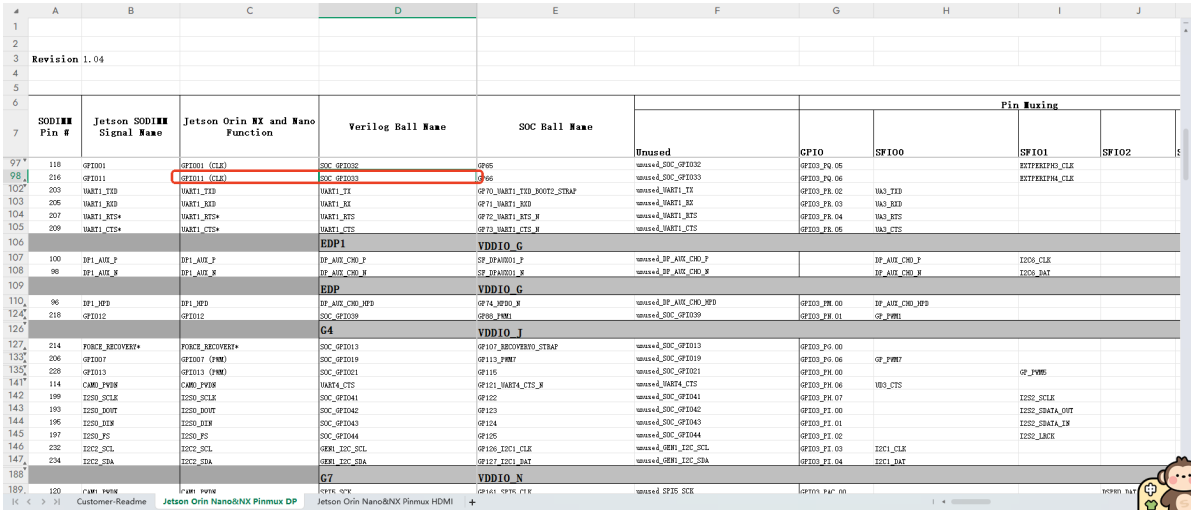
1. Busybox modifies registers (taking physical pin 31 as an example)

This solution is a temporary solution. After modifying the register configuration, it will become invalid every time it is restarted. If you need to keep it in effect, refer to the second solution.

The documents in the picture can be found in the attachment - jetson gpio, which are all found and downloaded from the official website (software data\data documents\jetson-gpio).

After inquiry, it is found that: physical pin 31 ---- corresponds to GPIO11--- corresponds to SOC_GPIO33, the corresponding **PADCTL_G3** address = **PADCTL_A0** is 0x2430000, and the corresponding SOC_GPIO33 is 0x2430070 (refer to the following picture)

Sysfs GPIO	Name	Pin	Pin	Name	Sysfs GPIO
Jetson Xavier NX J12 Header					
	3.3 VDC *Power*	1	2	**5.0 VDC** *Power*	
	I2C1_SDA *I2C Bus 8*	3	4	**5.0 VDC** *Power*	
	I2C1_SCL *I2C Bus 8*	5	6	**GND**	
148 gpio436	**GPIO9** *AUDIO_MCLK*	7	8	**UART1_TX** */dev/ttyTHS0*	
	GND	9	10	**UART1_RX** */dev/ttyTHS0*	
140 gpio428	**UART1_RTS**	11	12	**I2S0_SCLK**	*157* gpio445
192 gpio480	**SPI1_SCK**	13	14	**GND**	
20 gpio268	**GPIO12** *Alt: PWM*	15	16	**SPI1_CS1**	*196* gpio484
	3.3 VDC *Power*	17	18	**SPI1_CS0**	*195* gpio483
205 gpio493	**SPI0_MOSI**	19	20	**GND**	
204 gpio492	**SPI0_MISO**	21	22	**SPI1_MISO**	*193* gpio481
203 gpio491	**SPI0_SCK**	23	24	**SPI0_CS0**	*206* gpio494
	GND	25	26	**SPI0_CS1**	*207* gpio495
	I2C0_SDA *I2C Bus 1*	27	28	**I2C0_SCL** *I2C Bus 1*	
133 gpio421	**GPIO01**	29	30	**GND**	
134 gpio422	**GPIO11**	31	32	**GPIO07** *Alt: PWM*	*136* gpio424
105 gpio393	**GPIO13** *Alt: PWM*	33	34	**GND**	
160 gpio448	**I2S0_FS**	35	36	**UART1_CTS**	*141* gpio429
194 gpio482	**SPI1_MOSI**	37	38	**I2S0_SDIN**	*159* gpio447
	GND	39	40	**I2S0_SDOUT**	*158* gpio446



Revision 1.04

SODIMM Pin #	Jetson SODIMM Signal Name	Jetson Orin NX and Nano Function	Verilog Ball Name	SOC Ball Name	Pin Muxing				
					Unused	GPIO	SFIO0	SFIO1	SFIO2
118	GPIO01	GPIO01 (CLK)	SOC_GPIO32	GP85	unused_SOC_GPIO32	GPIO3_PQ.05		EXTPERIPH3_CLK	
216	GPIO11	GPIO11 (CLK)	SOC_GPIO33	GP86	unused_SOC_GPIO33	GPIO3_PQ.06		EXTPERIPH4_CLK	
203	UART1_TXD	UART1_TXD	UART1_TX	GP70_UART1_TXD_BOOT2_STRAP	unused_UART1_TX	GPIO3_PR.02	UA3_TXD		
205	UART1_RXD	UART1_RXD	UART1_RX	GP71_UART1_RXD	unused_UART1_RX	GPIO3_PR.03	UA3_RXD		
207	UART1_RTS*	UART1_RTS*	UART1_RTS	GP72_UART1_RTS_N	unused_UART1_RTS	GPIO3_PR.04	UA3_RTS		
209	UART1_CTS*	UART1_CTS*	UART1_CTS	GP73_UART1_CTS_N	unused_UART1_CTS	GPIO3_PR.05	UA3_CTS		
			EDP1	VDDIO_G					
100	DP1_AUX_P	DP1_AUX_P	DP_AUX_CHO_P	SF_DPAUX01_P	unused_DP_AUX_CHO_P		DP_AUX_CHO_P	I2C6_CLK	
98	DP1_AUX_N	DP1_AUX_N	DP_AUX_CHO_N	SF_DPAUX01_N	unused_DP_AUX_CHO_N		DP_AUX_CHO_N	I2C6_DAT	
			EDP	VDDIO_G					
96	DP1_HPD	DP1_HPD	DP_AUX_CHO_HPD	GP74_HPD0_N	unused_DP_AUX_CHO_HPD	GPIO3_PM.00	DP_AUX_CHO_HPD		
218	GPIO12	GPIO12	SOC_GPIO39	GP99_PWM1	unused_SOC_GPIO39	GPIO3_PN.01	GP_PWM1		
			G4	VDDIO_J					
214	FORCE_RECOVERY*	FORCE_RECOVERY*	SOC_GPIO13	GP107_RECOVERY0_STRAP	unused_SOC_GPIO13	GPIO3_PG.00			
206	GPIO07	GPIO07 (PWM)	SOC_GPIO19	GP113_PWM7	unused_SOC_GPIO19	GPIO3_PG.06	GP_PWM7		
228	GPIO13	GPIO13 (PWM)	SOC_GPIO21	GP115	unused_SOC_GPIO21	GPIO3_PH.00		GP_PWM5	
114	CAM0_PWDN	CAM0_PWDN	UART4_CTS	GP121_UART4_CTS_N	unused_UART4_CTS	GPIO3_PH.06	UA3_CTS		
199	I2S0_SCLK	I2S0_SCLK	SOC_GPIO41	GP122	unused_SOC_GPIO41	GPIO3_PH.07		I2S2_SCLK	
193	I2S0_DOUT	I2S0_DOUT	SOC_GPIO42	GP123	unused_SOC_GPIO42	GPIO3_PI.00		I2S2_SDATA_OUT	
195	I2S0_DIN	I2S0_DIN	SOC_GPIO43	GP124	unused_SOC_GPIO43	GPIO3_PI.01		I2S2_SDATA_IN	
197	I2S0_FS	I2S0_FS	SOC_GPIO44	GP125	unused_SOC_GPIO44	GPIO3_PI.02		I2S2_LRCK	
232	I2C2_SCL	I2C2_SCL	GEN1_I2C_SCL	GP126_I2C1_CLK	unused_GEN1_I2C_SCL	GPIO3_PI.03	I2C1_CLK		
234	I2C2_SDA	I2C2_SDA	GEN1_I2C_SDA	GP127_I2C1_DAT	unused_GEN1_I2C_SDA	GPIO3_PI.04	I2C1_DAT		
			G7	VDDIO_N					
120	CAM1_PWDN	CAM1_PWDN	SPI5_SCK	GP161_SPI5_CLK	unused_SPI5_SCK	GPIO3_PAC.00		DCMD_DAT	

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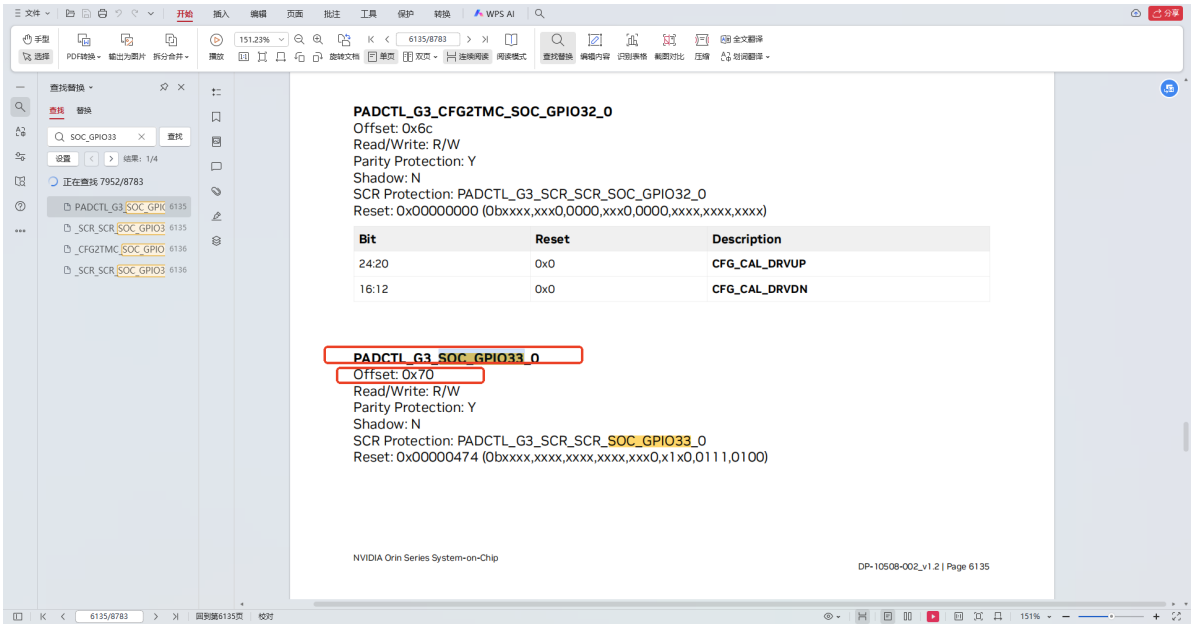


PADCTL_G3_CFG2TMC_SOC_GPIO32_0
Offset: 0x6c
Read/Write: R/W
Parity Protection: Y
Shadow: N
SCR Protection: PADCTL_G3_SCR_SCR_SOC_GPIO32_0
Reset: 0x00000000 (0bxxxx,xxx0,0000,xxx0,0000,xxxx,xxxx,xxxx)

Bit	Reset	Description
24:20	0x0	CFG_CAL_DRVUP
16:12	0x0	CFG_CAL_DRVDN

PADCTL_G3_SOC_GPIO33_0
Offset: 0x70
Read/Write: R/W
Parity Protection: Y
Shadow: N
SCR Protection: PADCTL_G3_SCR_SCR_SOC_GPIO33_0
Reset: 0x00000474 (0bxxxx,xxxx,xxxx,xxxx,xxx0,x1x0,0111,0100)

NVIDIA Orin Series System-on-Chip
DP-10508-002_v1.2 | Page 6135

Pinmux register address:

System Components

- Multi-Purpose I/O Pins and Pin Multiplexing (PinMux) Registers
  - G3 PAD Control Registers; Updated note to use Block Name (PADCTL_A0) to find the Base Address of these registers in the System Address Map
  - UFS PAD Control Registers; Updated note to use Block Name (PADCTL_A17) to find the Base Address of these registers in the System Address Map
- Design for Debugging (DFD); Updates to FSI TSC section: added FSI_CSITE_TSINTP Render Configuration, Connectivity, Calculating Time-Interval Using Timestamps subsections
- Always-On Cluster (AON) and SPE; new chapter

PADCTL_A	0x02430000	0x0244ffff	SYSTEM
PADCTL_A0	0x02430000	0x02430fff	SYSTEM
PADCTL_A2	0x02432000	0x02432fff	SYSTEM
PADCTL_A4	0x02434000	0x02434fff	SYSTEM
PADCTL_A5	0x02435000	0x02435fff	SYSTEM
PADCTL_A6	0x02436000	0x02436fff	SYSTEM
PADCTL_A7	0x02437000	0x02437fff	SYSTEM
PADCTL_A8	0x02438000	0x02438fff	SYSTEM
PADCTL_A11	0x0243b000	0x0243bfff	SYSTEM
PADCTL_A13	0x0243d000	0x0243dfff	SYSTEM
PADCTL_A16	0x02440000	0x02440fff	SYSTEM
PADCTL_A17	0x02441000	0x02441fff	SYSTEM
PADCTL_A20	0x02444000	0x02444fff	SYSTEM
PADCTL_A21	0x02445000	0x02445fff	SYSTEM
PADCTL_A24	0x02448000	0x02448fff	SYSTEM
PADCTL_A25	0x02449000	0x02449fff	SYSTEM

- The Offset is 0x70.
- The Pinmux register address is 0x2430070

1.1 Install busybox

```
sudo apt install busybox
```

1.2 Set the gpio pin to output:

```
sudo busybox devmem 0x02430070 w 0x004
```

1.3 Test output

GPIO and BCM comparison table

BCM Coding	Function Name	Physical Pins		Function Name	BCM Coding
	3V3	1	2	5V	
2	SDA	3	4	5V	
3	SCL	5	6	GND	
4	D4	7	8	D14(TXD)	14
	GND	9	10	D15(RXD)	15
17	D17	11	12	D18	18
27	D27	13	14	GND	
22	D22	15	16	D23	23
	3V3	17	18	D24	24
10	D10	19	20	GND	
9	D9	21	22	D25	25
11	D11	23	24	D8	8
	GND	25	26	D7	7
0	D0(ID_SD)	27	28	D1(ID_SC)	1
5	D5	29	30	GND	
6	D6	31	32	D12	12
13	D13	33	34	GND	
19	D19	35	36	D16	16
26	D26	37	38	D20	20
	GND	39	40	D21	21

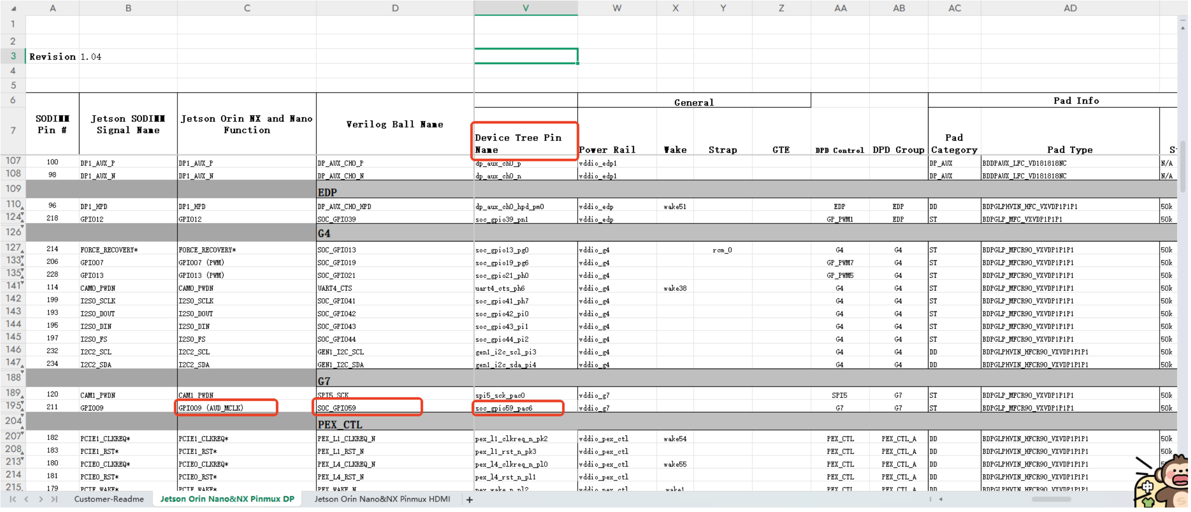
```
cd ~/jetson-gpio/samples

export JETSON_MODEL_NAME=JETSON_ORIN_NANO

python3 simple_out.py
```

After the setting is completed, refer to the BCM code, change the code in the test case to the corresponding value, and then run the following test case to find the physical pin 31 Switching high and low levels back and forth

2. Change the device tree (taking the change of physical pin 7 as an example)

Note: This solution requires a certain understanding of the device tree and is not recommended for novices. After this solution is successful, the set gpio pin will become a bidirectional pin, that is, input + output.

Physical pin 7 corresponds to GPIO 09, corresponds to SOC_GPIO59, and the corresponding device tree name is soc_gpio59_pac6



Revision 1.04

	SODIMM Pin #	Jetson SODIMM Signal Name	Jetson Orin NX and Nano Function	Verilog Ball Name	Device Tree Pin Name	Power Rail	Wake	Strap	GTE	DPD Control	DPD Group	Pad Category	Pad Type	S
107	100	DP1_AUX_P	DP1_AUX_P	DP_AUX_CH0_P	dp_aux_ch0_p	vddio_edp1						DP_AUX	BDDPAUX_LFC_VD181818NC	N/A
108	98	DP1_AUX_N	DP1_AUX_N	DP_AUX_CH0_N	dp_aux_ch0_n	vddio_edp1						DP_AUX	BDDPAUX_LFC_VD181818NC	N/A
109				EDP										
110	96	DP1_HPD	DP1_HPD	DP_AUX_CH0_HPD	dp_aux_ch0_hpd_pm0	vddio_edp	wake51			EDP	EDP	DD	BDPGLPHVIN_HFC_VXVDP1P1P1	50k
124	218	GPIO12	GPIO12	SOC_GPIO39	soc_gpio39_pn1	vddio_edp				GP_PWM1	EDP	ST	BDPGLP_MFC_VXVDP1P1P1	50k
126				G4										
127	214	FORCE_RECOVERY*	FORCE_RECOVERY*	SOC_GPIO13	soc_gpio13_pg0	vddio_g4		rcm_0		G4	G4	ST	BDPGLP_MFCR90_VXVDP1P1P1	50k
133	206	GPIO07	GPIO07 (PWM)	SOC_GPIO19	soc_gpio19_pg6	vddio_g4				GP_PWM7	G4	ST	BDPGLP_MFCR90_VXVDP1P1P1	50k
135	228	GPIO13	GPIO13 (PWM)	SOC_GPIO21	soc_gpio21_ph0	vddio_g4				GP_PWM5	G4	ST	BDPGLP_MFCR90_VXVDP1P1P1	50k
141	114	CAM0_PWDN	CAM0_PWDN	UART4_CTS	uart4_cts_ph6	vddio_g4	wake38			G4	G4	ST	BDPGLP_MFCR90_VXVDP1P1P1	50k
142	199	I2S0_SCLK	I2S0_SCLK	SOC_GPIO41	soc_gpio41_ph7	vddio_g4				G4	G4	ST	BDPGLP_MFCR90_VXVDP1P1P1	50k
143	193	I2S0_DOUT	I2S0_DOUT	SOC_GPIO42	soc_gpio42_pi0	vddio_g4				G4	G4	ST	BDPGLP_MFCR90_VXVDP1P1P1	50k
144	195	I2S0_DIN	I2S0_DIN	SOC_GPIO43	soc_gpio43_pi1	vddio_g4				G4	G4	ST	BDPGLP_MFCR90_VXVDP1P1P1	50k
145	197	I2S0_FS	I2S0_FS	SOC_GPIO44	soc_gpio44_pi2	vddio_g4				G4	G4	ST	BDPGLP_MFCR90_VXVDP1P1P1	50k
146	232	I2C2_SCL	I2C2_SCL	GEN1_I2C_SCL	gen1_i2c_scl_pi3	vddio_g4				G4	G4	DD	BDPGLPHVIN_HFCR90_VXVDP1P1P1	50k
147	234	I2C2_SDA	I2C2_SDA	GEN1_I2C_SDA	gen1_i2c_sda_pi4	vddio_g4				G4	G4	DD	BDPGLPHVIN_HFCR90_VXVDP1P1P1	50k
188				G7										
189	120	CAM1_PWDN	CAM1_PWDN	SPI5_SCK	spi5_sck_pac0	vddio_g7				SPI5	G7	ST	BDPGLP_MFCR90_VXVDP1P1P1	50k
195	211	GPIO09	GPIO09 (AUD_MCLK)	SOC_GPIO59	soc_gpio59_pac6	vddio_g7				G7	G7	ST	BDPGLP_MFCR90_VXVDP1P1P1	50k
204				PEX_CTL										
207	182	PCIE1_CLKREQ*	PCIE1_CLKREQ*	PEX_L1_CLKREQ_N	pex_l1_clkreq_n_pk2	vddio_pex_ctl	wake54			PEX_CTL	PEX_CTL_A	DD	BDPGLPHVIN_HFCR90_VXVDP1P1P1	50k
208	183	PCIE1_RST*	PCIE1_RST*	PEX_L1_RST_N	pex_l1_rst_n_pk3	vddio_pex_ctl				PEX_CTL	PEX_CTL_A	DD	BDPGLPHVIN_HFCR90_VXVDP1P1P1	50k
213	180	PCIE0_CLKREQ*	PCIE0_CLKREQ*	PEX_L4_CLKREQ_N	pex_l4_clkreq_n_pl0	vddio_pex_ctl	wake55			PEX_CTL	PEX_CTL_A	DD	BDPGLPHVIN_HFCR90_VXVDP1P1P1	
214	181	PCIE0_RST*	PCIE0_RST*	PEX_L4_RST_N	pex_l4_rst_n_pl1	vddio_pex_ctl				PEX_CTL	PEX_CTL_A	DD	BDPGLPHVIN_HFCR90_VXVDP1P1P1	
215	179	PCIE_WAKE*	PCIE_WAKE*	PEX_WAKE_N	pex_wake_n_pl2	vddio_pex_ctl	wake1			PEX_CTL	PEX_CTL_A	DD	BDPGLPHVIN_HFCR90_VXVDP1P1P1	

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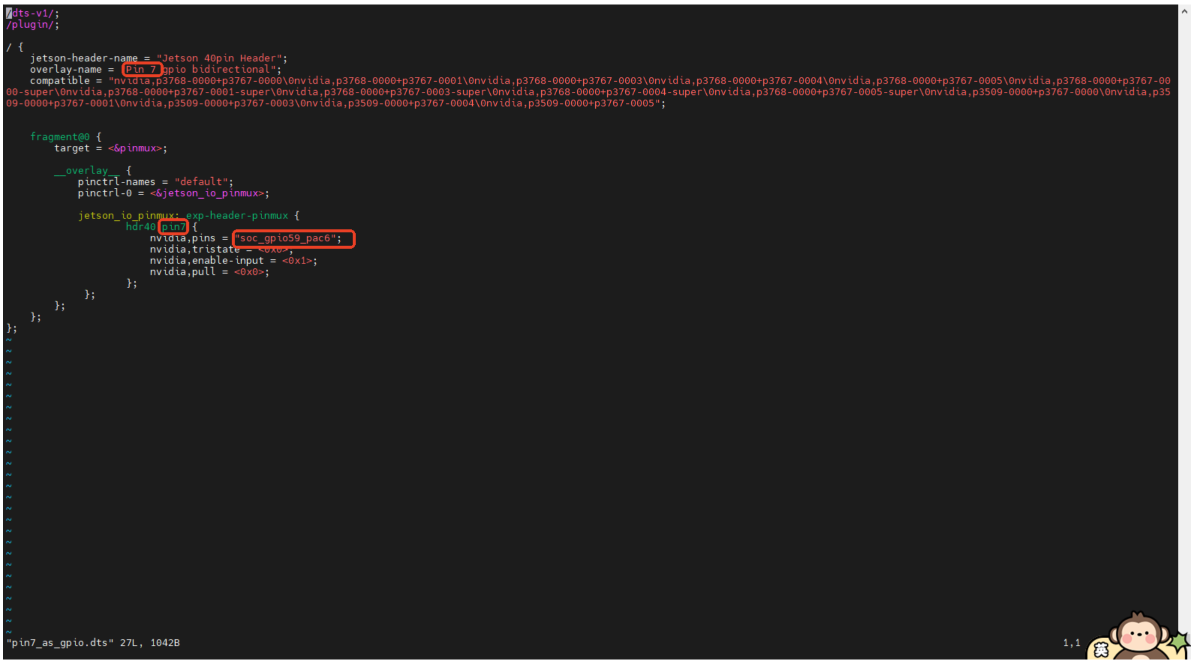
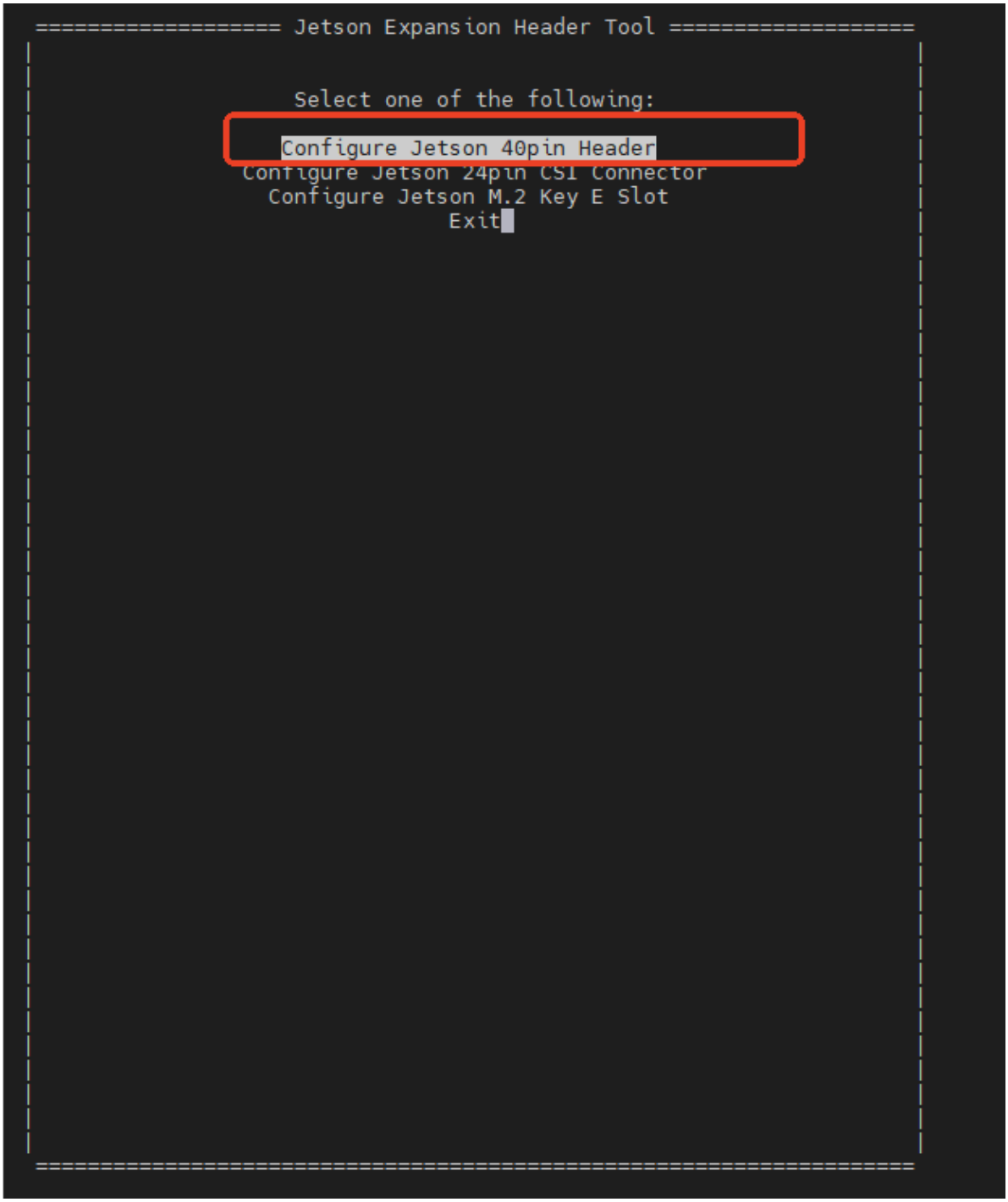
Put the jetson-orin-gpio-patch-main file in software data\data document\jetson-gpio into jetson orin, open the pin7_as_gpio.dts file, and change the circled area to the GPIO pin you need to change

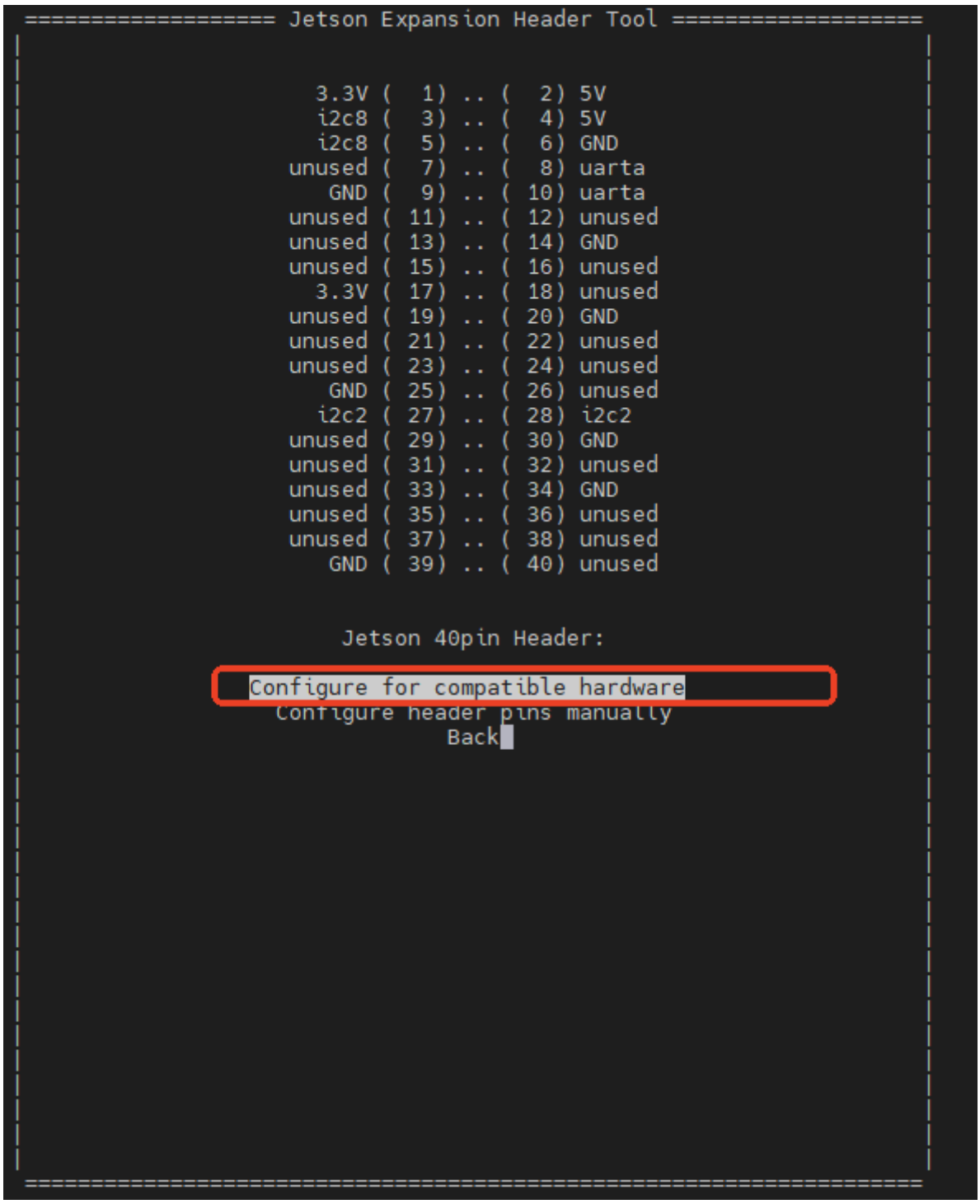


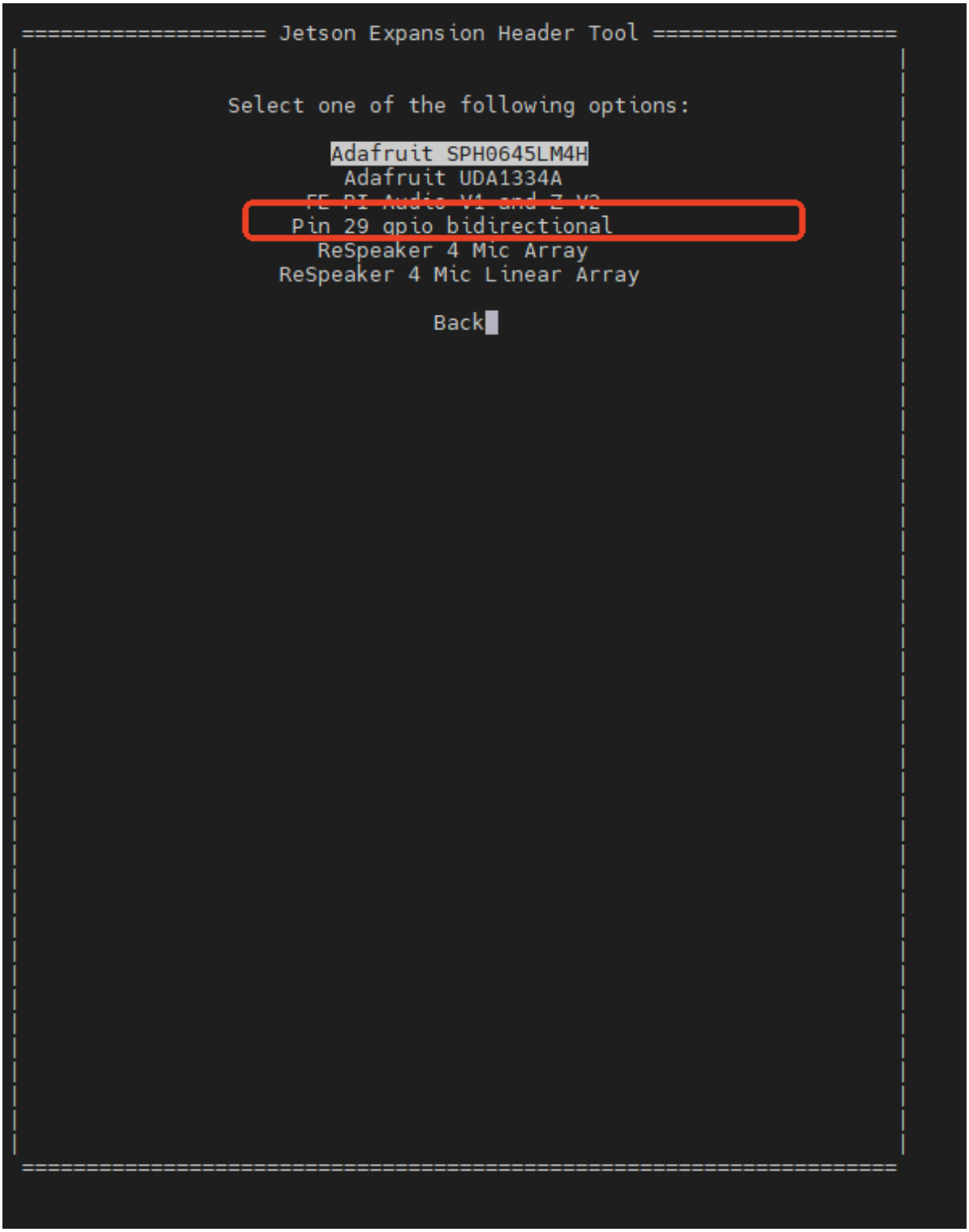
```
/dts-v1/;
/plugin/;

/ {
    jetson-header-name = "Jetson 40pin Header";
    overlay-name = "Pin 7 gpio bidirectional";
    compatible = "nvidia,p3768-0000+p3767-0000\0nvidia,p3768-0000+p3767-0001\0nvidia,p3768-0000+p3767-0003\0nvidia,p3768-0000+p3767-0004\0nvidia,p3768-0000+p3767-0005\0nvidia,p3768-0000+p3767-0000-super\0nvidia,p3768-0000+p3767-0001-super\0nvidia,p3768-0000+p3767-0003-super\0nvidia,p3768-0000+p3767-0004-super\0nvidia,p3768-0000+p3767-0005-super\0nvidia,p3509-0000+p3767-0000\0nvidia,p3509-0000+p3767-0001\0nvidia,p3509-0000+p3767-0003\0nvidia,p3509-0000+p3767-0004\0nvidia,p3509-0000+p3767-0005";


    fragment@0 {
        target = <&pinmux>;

        __overlay__ {
            pinctrl-names = "default";
            pinctrl-0 = <&jetson_io_pinmux>;

            jetson_io_pinmux: exp-header-pinmux {
                hdr40-pin7 {
                    nvidia,pins = "soc_gpio59_pac6";
                    nvidia,tristate = <0x0>;
                    nvidia,enable-input = <0x1>;
                    nvidia,pull = <0x0>;
                };
            };
        };
    };
};

"pin7_as_gpio.dts" 27L, 1042B                                    1,1
```

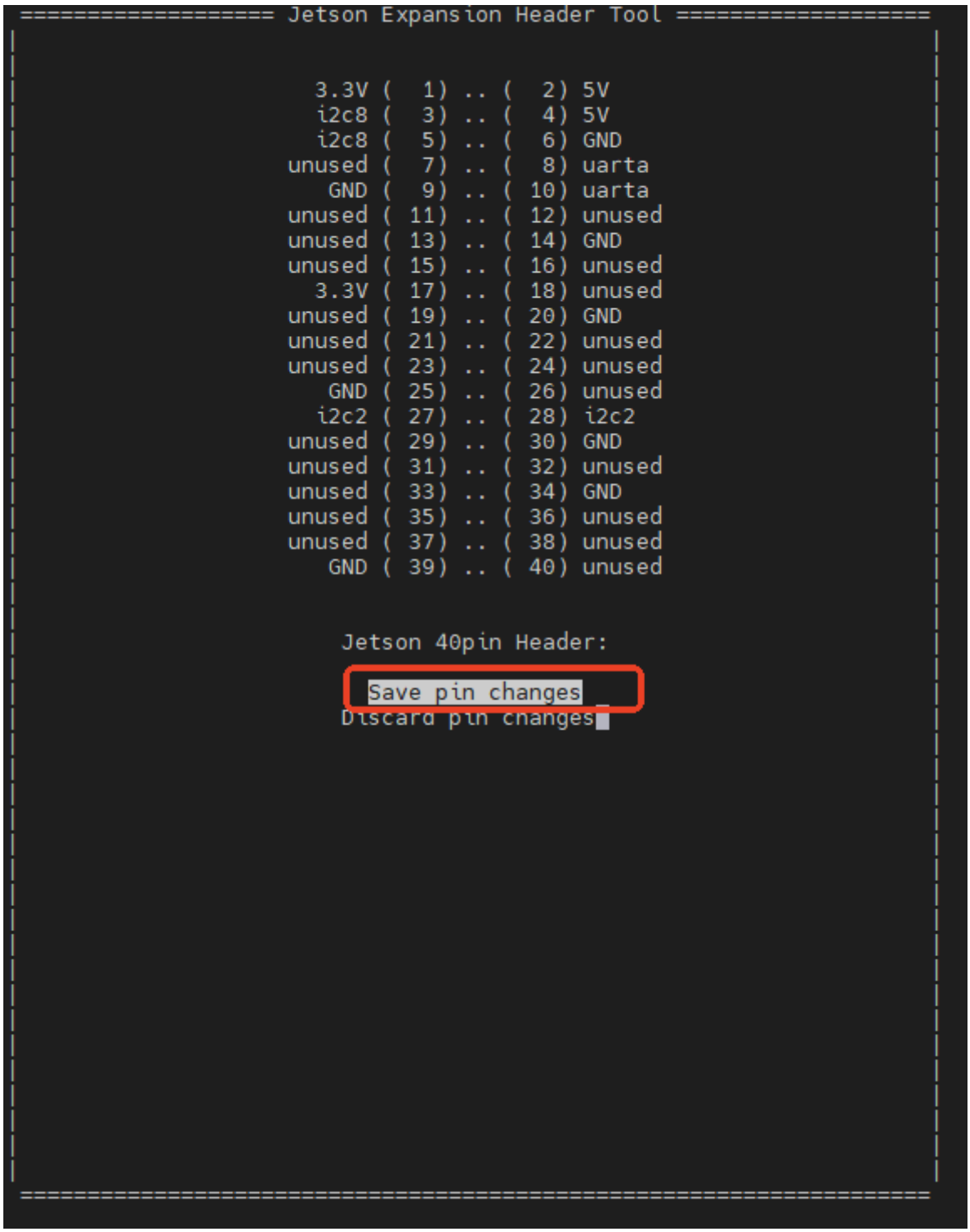
In jetson-orin-gpio-patch Run the following commands respectively

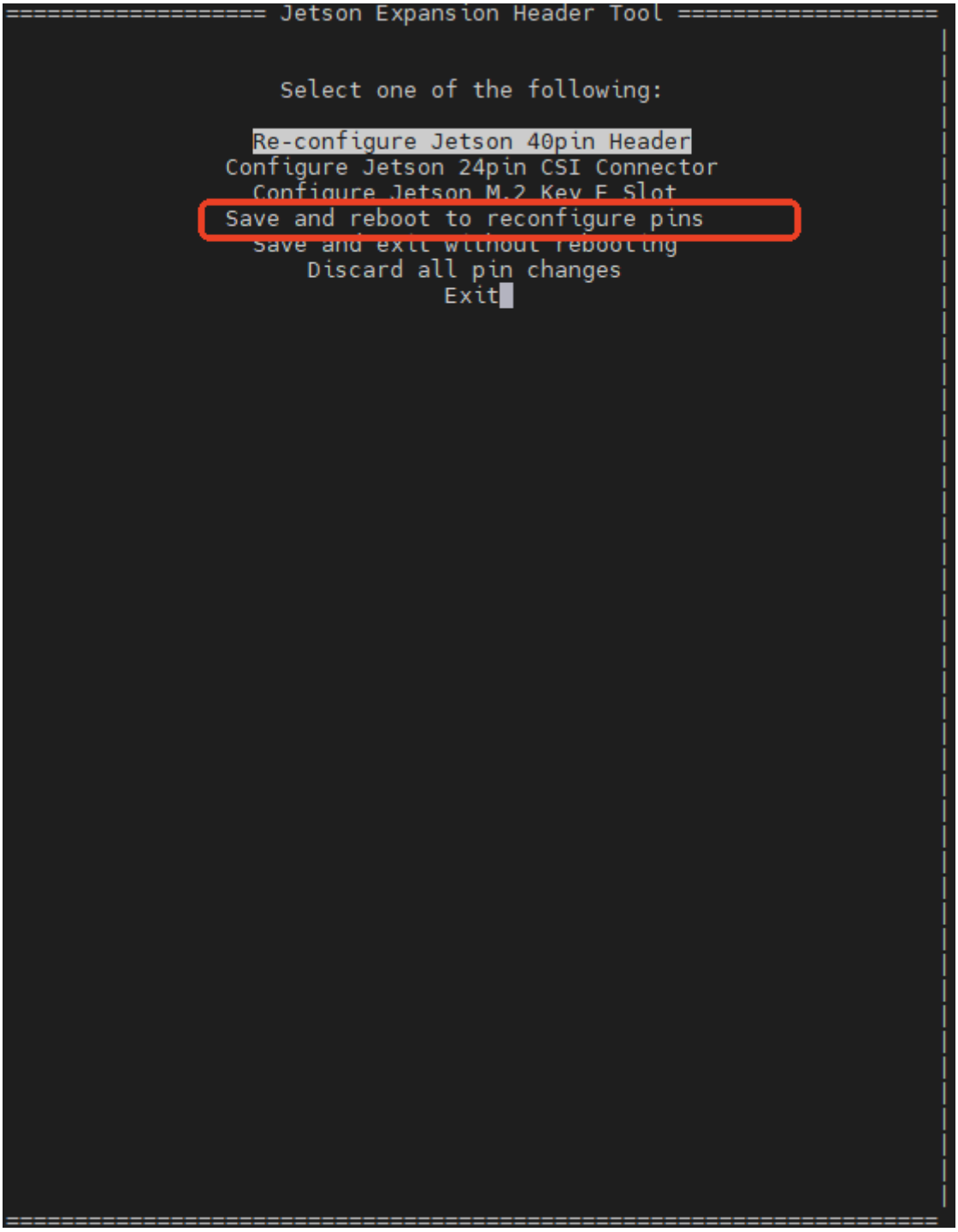
```
dtc -O dtb -o pin7_as_gpio.dtbo pin7_as_gpio.dts #You can change the generated file name according to the different GPIO port names
sudo cp pin7_as_gpio.dtbo /boot
sudo /opt/nvidia/jetson-io/jetson-io.py
```


Jetson Expansion Header Tool
Select one of the following:
Configure Jetson 40pin Header
Configure Jetson 24pin CSI Connector
Configure Jetson M.2 Key E Slot
Exit


Jetson Expansion Header Tool
3.3V (1) .. (2) 5V
i2c8 (3) .. (4) 5V
i2c8 (5) .. (6) GND
unused (7) .. (8) uarta
GND (9) .. (10) uarta
unused (11) .. (12) unused
unused (13) .. (14) GND
unused (15) .. (16) unused
3.3V (17) .. (18) unused
unused (19) .. (20) GND
unused (21) .. (22) unused
unused (23) .. (24) unused
GND (25) .. (26) unused
i2c2 (27) .. (28) i2c2
unused (29) .. (30) GND
unused (31) .. (32) unused
unused (33) .. (34) GND
unused (35) .. (36) unused
unused (37) .. (38) unused
GND (39) .. (40) unused
Jetson 40pin Header:
Configure for compatible hardware
Configure header pins manually
Back


Jetson Expansion Header Tool
Select one of the following options:
Adafruit SPH0645LM4H
Adafruit UDA1334A
Pin 29 gpio bidirectional
ReSpeaker 4 Mic Array
ReSpeaker 4 Mic Linear Array
Back


Jetson Expansion Header Tool
3.3V (1) .. (2) 5V
i2c8 (3) .. (4) 5V
i2c8 (5) .. (6) GND
unused (7) .. (8) uarta
GND (9) .. (10) uarta
unused (11) .. (12) unused
unused (13) .. (14) GND
unused (15) .. (16) unused
3.3V (17) .. (18) unused
unused (19) .. (20) GND
unused (21) .. (22) unused
unused (23) .. (24) unused
GND (25) .. (26) unused
i2c2 (27) .. (28) i2c2
unused (29) .. (30) GND
unused (31) .. (32) unused
unused (33) .. (34) GND
unused (35) .. (36) unused
unused (37) .. (38) unused
GND (39) .. (40) unused
Jetson 40pin Header:
Save pin changes
Discard pin changes



Start the test:

```
cd ~/jetson-gpio/samples
```

```
export JETSON_MODEL_NAME=JETSON_ORIN_NANO
```

```
python3 simple_out.py
```

After the settings are completed, refer to the BCM code, change the code in the test case to the corresponding value, and then run the following test case, you can find that the physical pin 7 switches back and forth between high and low levels

3. Program effect

Use DuPont wire to lead out GPIO.BOARD 6 and GND pins, and use a multimeter to measure the pin voltage change:

Note: Do not connect incorrectly or cause pin short circuits, as mistakes may cause damage to the motherboard hardware!