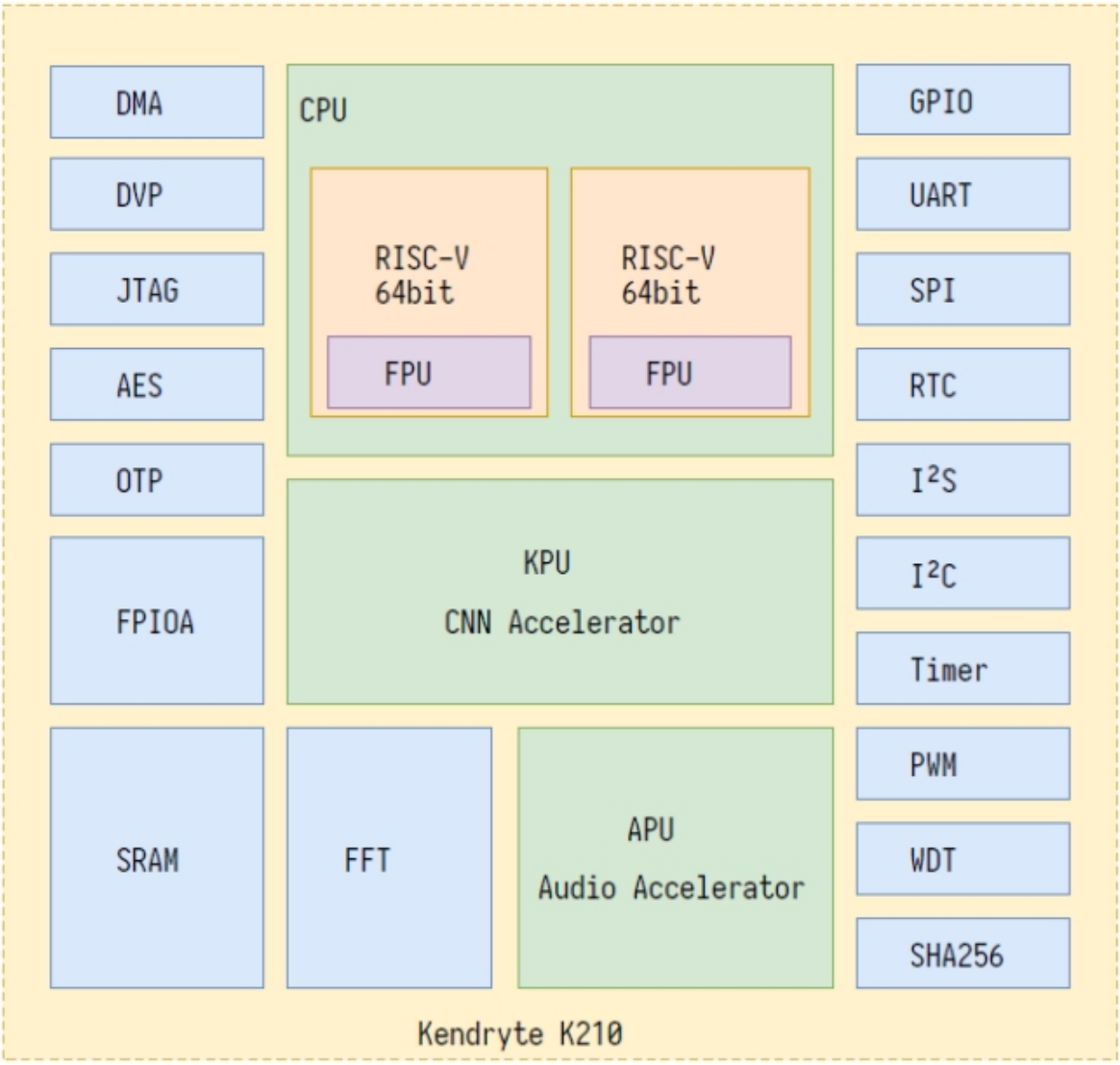
# 1. the main chip introduction



## 1.1 what is K210 chip?

1. K210 is based on the RISC-V RISC of a MCU, in many features, the chip architecture contains a self-study of neural network hardware accelerator KPU belong to the most characteristic, and can be high-performance convolutional neural network operation. In the MCU AI computing context, K210 chip power is very great, according to the Jia Nan official website of description, K210 the KPU hash rate can reach 0. 8TFLOPS, which is equivalent to what level? For example, the latest Raspberry PI 4B power less than 0. 1TFLOPS, and to the neural network processing as a selling point of the Jetson Nano has 128 CUDA unit, the hash rate is only 0. 47TFLOPS。
2. In addition to the KPU's hash rate good addition, K210 chip support FPIOA (field programmable IO array, you can each peripheral freely mapped to any pin, simplifying the developer's pin assignments and GPIO wiring problem.
3. K210 chip with dual-core CPU, the instruction sets for RISC-V 64-bit, each of the core built-in FPU, can be a separate floating-point arithmetic.
4. In order to better in machine vision and hearing on the role of the K210 chip comes with computing the convolutional artificial neural network accelerator KPU, as well as the processing of the microphone array of the APU can be a high-performance machine vision and auditory processing.
5. Not only that, K210 also built-in Fast Fourier transform accelerator, can be complex FFT calculation.
6. In the strong performance of the premise, K210 chip also very focused on security, built-in AES and SHA256 algorithm accelerator for user data security provides effective protection.
7. Then look at the MCU aspect of the property, K210 chip has a rich peripheral units, respectively, DVP, JTAG, OTP, FPIOA, GPIO, UART, SPI, RTC, I2S, I2C, WDT, TIMER, PWM, these peripherals in actual use play a huge role, basically meet most of the MCU peripherals needs.
8. K210 also have a high-performance, low-power SRAM, for a total of 8M, 2M dedicated to AI computing, 6M for the program; dedicated external FLASH interface, increasing its storage space; the data transfer can use the powerful DMA, the data throughput capacity of the aspects of performance is excellent.

9. The following is K210 chip architecture diagram, for reference only, with specific reference to the information available K210 chip technical manual document.




## 1.2 what is the RISC-V instruction set?

RISC-V is based on a reduced instruction set, RISC principle of open-source instruction set architecture ISA is. V represents the fifth generation of reduced instruction set, University of California, Berkeley after the previous four generations of improvements and upgrades come. The project began in 2010 and the University of California at Berkeley, and later through the many contributors of hard work, after 10 years'sword', the RISC-V instruction set has been on the worldwide gradually active, I believe in the near future there will be more and better of the RISC-V chip was launched.

RISC-V has the following characteristics:

1. Fully open source: any business can be free free to use the RISC-V instruction set to the manufacturing and marketing its own chip, without the need to pay high licensing fees, and can according to their own needs extended instruction set, their extended instruction set need not be open, you can achieve a differentiated development.

2. Architecture simple: with the mainstream of the X86 and ARM architecture compared to RISC-V is a new instruction set, need not be compatible with older products, so extraordinarily simple, the entire RISC-V base instruction set only 40 more, plus the other modular extensions instruction in total it was only several tens of bars.
3. Easy to transplant, modern operating systems do a privilege level instruction and a user-level command of the separation, the privileged instructions can only operating system calls, and the user-level instructions to the user-mode call, the security of the operating system stable. RISC-V provides privilege level instruction and a user-level instruction, while providing detail of the RISC-V privileged instruction specification and RISC-V user-level instruction specification details so that developers can very easily ported to linux and the unix system to the RISC-V platform.
4. Modular design: RISC-V architecture may be composed of different modules for different functions, and flexible use of the module combination, can be customized to your own needs of MCU. For example, for a small area of low-power embedded scene, you can select the RV32IC combination of instruction set, only the use of a machine mode, you can greatly reduce the power consumption and the volume itself; and high-performance applications operating system of the scene can be selected RV32IMFDC instruction set, can use the machine mode and user mode, in order to achieve higher performance.
5. A complete tool chain: a tool chain for the CPU, it can be understood as a screwdriver for the screws without a screwdriver role, the screw is simply unable to hold the play to its performance. The tool chain is a software development and CPU interaction of the window, if there is no tool chain, a software developer can't even get the CPU to work together. Fortunately, the RISC-V due to the contributors to years of enthusiastic contribution to the community has been to provide a complete tool chain, and by the RISC-V Foundation for the maintenance of the tool chain.