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Milestone 3 Journal

24 Nov 2025 (Mon)

- Added the factorial test case.
- Moved assembly code into a new folder.
- Added the clock divider to the top module.
- Updated pipeline debug outputs for the FPGA.
- Updated decompression unit testbench.
- Fixed the ADDI negative immediate bug that decoded as SUB.
- Fixed load/store macros.
- Integrated full RV32C compressed extension into the CPU.

22 Nov 2025 (Sat)

- Created the decomp_unit and decomp_unit_tb

19 Nov 2025 (Wed)

- Removed the separate instruction memory module.

18 Nov 2025 (Tue)

- Reordered the CPU module structure (no logic changes).

17 Nov 2025 (Mon)

- Tested all modules and confirmed correctness.
- Updated pipeline to add new control signals and modified module ports for pipeline registers.

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