Design of High-Efficiency Current-Mode Class-D Amplifiers for Wireless Handsets

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***Abstract*—Design considerations are discussed for current-mode class-D (CMCD) microwave power amplifiers. Factors affecting amplifier efficiency are described analytically and via simulation. Amplifiers are reported that incorporate parallel *LC* resonators alongside the switching transistors. To reduce parasitic resistance, bond-wires were utilized to implement a high Q inductor in the *LC* resonator. An experimental CMCD amplifier based on GaAs HBTs is reported, with collector efficiency of 78.5% at an output power of 29.5 dBm (0.89 W) at 700 MHz.**

***Index Terms*—Bond-wire inductor, class-D, high efficiency, power amplifiers.**

I. Introduction

POWER-AMPLIFIER efficiency is a significant factor for the efficiency of most wireless systems. Poor efficiency of the last power-amplifier stage leads to large energy loss, not only deteriorating system efficiency, but also exacerbating thermal issues with devices.

Switching-mode power amplifiers can potentially provide high collector efficiency up to 100% and partially mitigate thermal runaway concerns by operating transistors as switches [1]–[3]. However, due to parasitic reactance, transition time, and turn-on resistance of the transistors, amplifier efficiency degrades with increasing frequency. For instance, the class-D amplifier is very popular for high-efficiency applications at low audio frequencies. However, it is hard to maintain this high efficiency at RF frequencies because the output shunt capacitance of the transistors causes significant loss. Energy 1/2 CV^2 is dissipated per cycle when the output capacitance *C* discharges from an initial voltage [1]–[5]. The class-E amplifier topology solves this problem by achieving zero voltage switching (ZVS) operation [6]–[12]. However, uncertain duty cycle, nonlinear capacitance, and other parasitic reactance can degrade class-E operation.

Manuscript received April 21, 2004; revised August 3, 2004. This work was supported in part by the U.S. Army Research Office under the Multifunctional Adaptive Radio Radar and Sensors–Multiuniversity Research Initiative Program, and by the University of California at San Diego Center for Wireless Communications.

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Digital Object Identifier 10.1109/TMTT.2004.839327

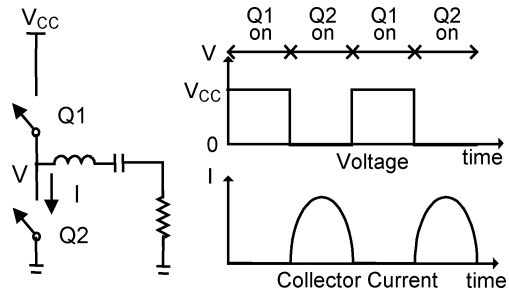

Fig. 1. Simplified schematic and voltage/current waveforms of the voltage-mode class-D amplifier.

Current mode class-D (CMCD) amplifier operation is similar to that of a conventional class-D amplifier (voltage mode class-D) with interchanged voltage and current waveforms. As a result, the output shunt capacitance loss can be eliminated due to ZVS. Recently, a CMCD amplifier was demonstrated to attain high efficiency (75.6%) at RF frequency (900 MHz) with output power 28.6 dBm (0.73 W) using discrete circuit elements [13]. A CMCD power amplifier for the base-station applications was also shown to achieve high efficiency (60%) with high output power (13 W) [14]. An amplifier of the closely related class-E/$F_{2,\mathrm{odd}}$ with 85% drain efficiency at 7 MHz has also been reported [15]–[17]. However, detailed design analysis of the CMCD amplifier has not been well developed. In this paper, the factors degrading the CMCD amplifier efficiency are discussed analytically. We show that by integrating the parallel *LC* resonator on-chip, it is possible to reduce the circuit complexity and eliminate parasitic reactance loss. Two CMCD amplifiers integrated with different *LC* resonator structures are compared and both show reasonable efficiency characteristics. The CMCD amplifier using a bond-wire inductor is shown to achieve collector efficiency of 78.5% at 700 MHz with output power of 29.5 dBm (0.89 W) [18]. The design analysis and measurement results show CMCD amplifiers are a potential solution for wireless systems with constant envelope modulation. In Section II, the basics of CMCD operation are described. Section III covers the analysis of efficiency in nonideal circuits. Prototype CMCD amplifier designs and measurement results are shown in Sections IV and V.

II. Basics of Operation

Fig. 1 shows the simplified schematic and ideal voltage/current waveforms of a voltage mode class-D (referred to as conventional class-D) amplifier. By driving two transistors out-of-phase, the voltage across the transistors is a square

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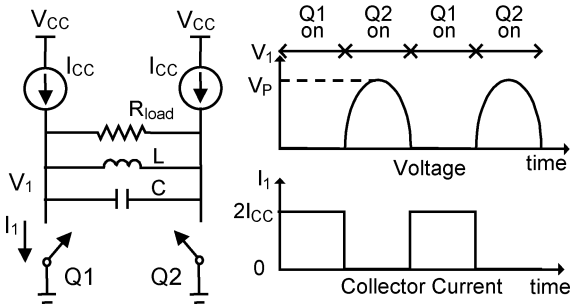

Fig. 2. Simplified schematic and voltage/current waveforms of the CMCD amplifier.

waveform alternating between V_{CC} and zero. Through a series *LC* filter, higher order harmonics are blocked and only the fundamental component passes to the load. The current waveform becomes a half sine wave for each transistor. Ideally, since there is no overlap between voltage and current waveforms, efficiency of 100% can be achieved. However, if the transistors have output shunt capacitance, this capacitance must be charged or discharged to V_{CC} or ground. The resultant energy loss per cycle E_C can be expressed as

$$E_C = \frac{1}{2} C_{\mathrm{CE}} V^2 \tag{1}$$

where C_{CE} is the collector–emitter capacitance and V is the collector–emitter voltage when the transistor is turned on. This output shunt capacitance discharge loss becomes dominant at high frequencies.

The CMCD amplifier, as shown in Fig. 2, is similar to the voltage-mode class-D amplifier with interchanged voltage and current waveforms. The current through the transistors is a square wave, while the voltage across the transistors is a half sine wave. The overlap of high voltage and high current is thus avoided to attain high efficiency and, additionally, when the transistor turns on, the voltage across the transistor is zero, thus, the output capacitance discharge problem is eliminated. A parallel *LC* resonator provides a short circuit for higher order harmonics and only the fundamental component reaches the load.

In addition to the energy dissipated from stored energy in the switch output capacitance, there can be dissipation of energy stored in parasitic inductance in series with the switch. The loss per cycle is given by

$$E_L = \frac{1}{2} L_{\mathrm{series}} I_L^2 \tag{2}$$

where L_{series} is the parasitic inductance, and I_L is the current flowing through the inductance prior to the turn off of the switch. While the CMCD amplifier is capable of avoiding losses due to the parasitic capacitance through ZVS, losses associated with inductive parasitics are still present. In most cases (as further described below), it is beneficial to decrease L_{series} as far as possible. This can be accomplished if the *LC* resonator is integrated on-chip with the switching transistors.

III. Design Considerations for CMCD Amplifiers

In practical operation, several factors distorting the ideal voltage/current waveforms tend to degrade the CMCD amplifier efficiency. For example, the real passive components have finite Q factors and the real transistors have parasitic reactance, nonzero turn-on resistance, nonzero transition time, and nonzero knee voltage. To simplify the discussion and to study the effects of each factor independently, this analysis evaluates each circuit imperfection factor separately. Combining all the factors can approximate the practical amplifier efficiency. The resultant CMCD amplifier efficiency η_{CMCD} can be expressed as

$$\eta_{\mathrm{CMCD}} = \eta_{po} \cdot \eta_{tt} \cdot \eta_{tk} \cdot \eta_{pp} \cdot \eta_{pm} \tag{3}$$

where η_{po} represents the loss factor due to the odd harmonic leakage currents, η_{tt} represents the loss factor due to the finite transition time of the transistors, η_{tk} represents the loss factor due to the nonzero knee voltage of the transistors, η_{pp} represents the loss factor due to the parasitic resistance of the *LC* tank, and η_{pm} represents the loss factor for the output impedance matching network. In ideal operation, all these factors are equal to one. The analysis results are useful to predict the amplifier performance and guide circuit design. Details of each factor are discussed below.

A. Higher Order Odd Harmonic Effects (η_{po})

The shunt capacitor *C* in the *LC* resonator is intended to provide a short circuit for the higher order odd harmonic currents. Practically, there are higher order leakage current flowing though the load when the capacitor provides a nonideal short circuit. If we assume the shunt inductor is an open circuit for the higher order currents, the leakage current (i_n) and the voltage across the load (v_{load}) can be expressed in terms of phase angle $\theta = \omega t$ by

$$i_n = \frac{4}{n\pi} I_{CC} \sin(n\theta) \tag{4}$$

$$v_{\mathrm{load}} = -\frac{4}{\pi} I_{CC} \sin\theta \cdot R_{\mathrm{load}} - \sum_{n=3,5,7\ldots}^{\infty} \frac{4}{n\pi} I_{CC} \frac{\sin n\theta - nQ\cos n\theta}{1+(n\cdot Q)^2} \cdot R_{\mathrm{load}} \tag{5}$$

where n is the harmonic index, I_{CC} is the dc current from the power supply, and R_{load} is the load resistance. The first term in (5) represents the voltage across the load induced by the fundamental current. The second term indicates the voltage induced by the higher order leakage current. The distortion of the voltage waveform across the load due to i_n depends on the Q factor of the resonator given by $Q = \omega \cdot R_{\mathrm{load}} \cdot C$. Fig. 3 shows the voltage waveform (normalized to $(4/\pi^2) I_{CC} R_{\mathrm{load}}$) across the load with different Q values.

The total dc power consumption can be obtained by

$$P_{\mathrm{DC}} = \frac{1}{2\pi} \int_0^{2\pi} v_{\mathrm{load}}(\theta) \cdot \left[\sum_{n=1,3,5\ldots}^{\infty} i_n \right] d\theta = \frac{8}{\pi^2} I_{CC}^2 R_{\mathrm{load}} + \sum_{n=3,5,7}^{\infty} \frac{8}{n^2\pi^2} I_{CC}^2 R_{\mathrm{load}} \frac{1}{1+(n\cdot Q)^2} \cdot \tag{6}$$

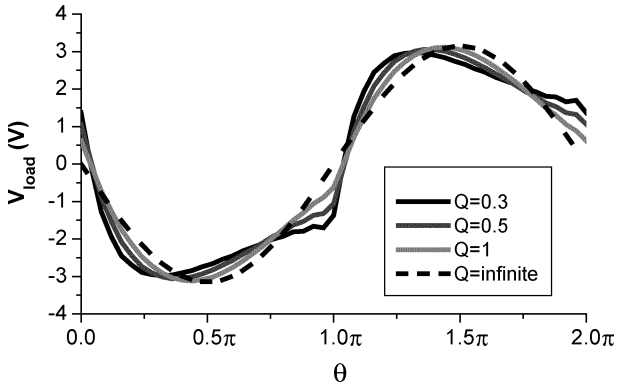

Fig. 3. Normalized voltage waveform across the load, showing distortion by the higher order harmonic leakage current. With lower Q factor, the voltage waveform has more distortion.

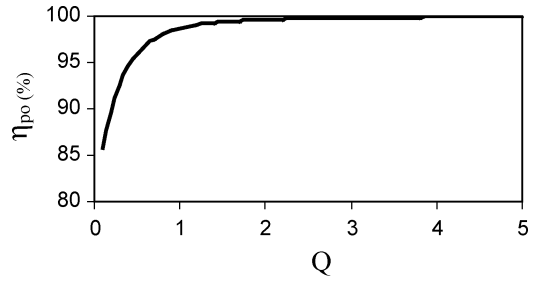

Fig. 4. Efficiency factor η_{po} increases with the increasing Q factor. $Q = \omega \cdot R_{\rm load} \cdot C$.

Since the leakage currents do not affect the fundamental signal, the output power (Pout) remains at $(8/\pi^2)I_{CC}^2 R_{\rm load}$. The efficiency factor η_{po} can be derived as

$$\eta_{po} = \frac{P_{\rm out}}{P_{\rm DC}} = \frac{1}{1 + \sum\limits_{n=3,5,7}^{\infty} \frac{1}{n^2} \cdot \frac{1}{1+(n\cdot Q)^2}}. \tag{7}$$

Fig. 4 shows the efficiency factor η_{po} with different Q factors. When Q is large enough, η_{po} can approximately reach 100%. This result suggests a high Q *RLC* circuit is preferred to reduce the loss from the leakage currents. It also shows that third harmonic is the dominant term.

B. Effect of Nonzero Transition Time (η_{tt})

When bipolar junction transistors operate in the saturation region, the forward-biased base–collector (BC) junction and the base–emitter (BE) junction store minority carriers in the base region, and potentially the collector region. To turn the transistors off, it takes time to remove these minority carriers before the BC junction becomes reverse biased. For simplicity, a fixed-time alignment between the voltage and current waveforms has been assumed. With different circuit embeddings, this alignment can vary (as discussed below). Based on this assumption, the current (i_1) flowing through the transistor $Q1$ is depicted in Fig. 5. τ represents the nonzero transition time expressed in radians.

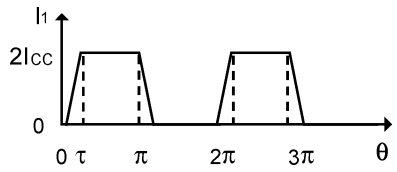

Fig. 5. Waveform of the current i_1, considering a nonzero transition time (τ).

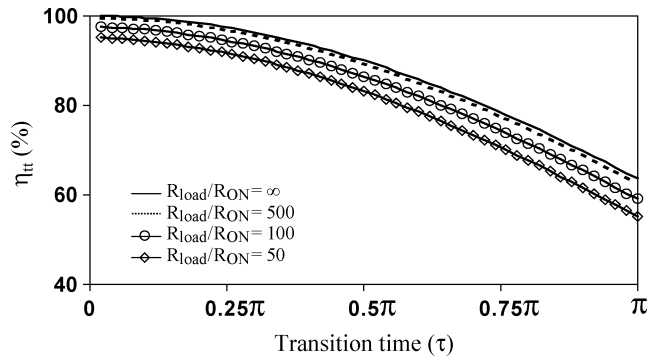

Fig. 6. Efficiency factor η_{tt} drops with increasing transition time (τ).

By Fourier decomposition of the current waveform, the amplitude of the fundamental component of i_1 can be derived as

$$|i_{1\_\rm fund}| = \frac{8}{\pi} I_{CC} \frac{\sin\left(\frac{\tau}{2}\right)}{\tau}. \tag{8}$$

The dc term of the voltage is given by

$$V_{\rm DC} = \frac{1}{2\pi}\int_0^{2\pi} V_G(\theta)d\theta + \frac{|v_{1\_\rm fund}|}{\pi} \tag{9}$$

where

$$V_G(\theta) = \begin{cases} 2I_{CC}R_{\rm ON}, & 0 \le \theta \le \pi + \tau \\ 0, & \pi + \tau \le \theta \le 2\pi \end{cases} \tag{10}$$

and $|v_{1\_\rm fund}| = |i_{1\_\rm fund}| \cdot R_{\rm load}$. $R_{\rm ON}$ is the turn-on resistance of the transistors. The efficiency factor η_{tt} can be derived as

$$\eta_{tt} = \frac{\frac{16}{\pi}\frac{R_{\rm load}}{R_{\rm ON}}\frac{\sin^2\left(\frac{\tau}{2}\right)}{\tau^2}}{\pi + \tau + \frac{8}{\pi}\frac{R_{\rm load}}{R_{\rm ON}}\frac{\sin\left(\frac{\tau}{2}\right)}{\tau}}. \tag{11}$$

When $R_{\rm ON}$ is zero, the efficiency factor η_{tt} can be simplified as

$$\eta_{tt} = \frac{2\sin\left(\frac{\tau}{2}\right)}{\tau}. \tag{12}$$

From (12), when τ is zero, η_{tt} can be 100%. Fig. 6 shows how η_{tt} degrades with increasing transition time.

C. Nonzero Knee Voltage of the Transistors (η_{tk})

The knee voltage of a transistor includes an offset voltage $(V_{\rm offset})$ and the voltage across the transistor on-state resistance $(R_{\rm ON})$. A circuit model considering the transistor parasitic capacitance $C_{\rm CE}$ and the turn-on resistance of the transistors is

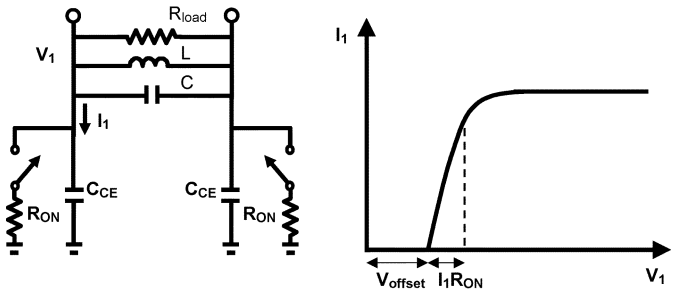

Fig. 7. Simplified model for evaluating the effects of the knee voltage of the transistors.

shown in Fig. 7. The equations of the voltage and current waveform can be written as

$$i_1 = \begin{cases} 2I_{cc} - C_{\rm CE}\omega_0\pi V_{cc}\cos(\theta), & 0 \le \theta \le \pi \\ -C_{\rm CE}\omega_0\pi V_{cc}\cos(\theta), & \pi \le \theta \le 2\pi \end{cases} \tag{13}$$

$$v_1 = \begin{cases} V_{\rm offset} + \big(2I_{cc} - C_{\rm CE}\omega_0\pi V_{cc}\cos(\theta)\big)R_{\rm ON}, \\ \quad 0 \le \theta \le \pi \\ V_{\rm offset} - V_p\sin(\theta) + \big(-C_{\rm CE}\omega_0\pi V_{cc}\cos(\theta)\big)R_{\rm ON}, \\ \quad \pi \le \theta \le 2\pi. \end{cases} \tag{14}$$

Using (13) and (14), we can derive the efficiency factor η_{tk} by

$$\begin{aligned} \eta_{tk} &= 1 - \frac{P_{\rm loss}}{P_{\rm DC}} \\ &= 1 - \frac{2I_{CC}V_{\rm offset} + 4I_{CC}^2R_{\rm ON} + (C_{\rm CE}\omega_0\pi V_{CC})^2R_{\rm ON}}{2I_{CC}V_{CC}} \end{aligned} \tag{15}$$

where loss in the transistors ($P_{\rm loss}$) is given by

$$P_{\rm loss} = \frac{1}{\pi}\int_0^{2\pi} i_1 \cdot v_1 d\theta. \tag{16}$$

In ideal operation, the parasitic capacitance $C_{\rm CE}$ can be absorbed in the *LC* resonator so there is no power consumption due to the capacitance $C_{\rm CE}$. However, if $R_{\rm ON}$ is not equal to zero, the capacitance term starts to degrade the amplifier efficiency. This result indicates that there is a design tradeoff between the transistor sizes.

D. Parasitic Resistance of the LC Resonator (η_{pp})

The finite Q factor of the *LC* resonator not only degrades the efficiency but also increases the stress of the transistors. According to the model shown in Fig. 7, $R_{\rm ON}$ is assumed to be zero. The efficiency factor η_{pp} can be expressed as

$$\eta_{pp} = \frac{G_{\rm load}}{G_{\rm load} + G'} \tag{17}$$

where $G_{\rm load}$ $(= 1/R_{\rm load})$ is the conductance of the load. G' represents the total parasitic conductance from the capacitor and the inductor. G' increases as the Q factor of the inductor and the capacitor decreases. The waveform of the current flowing through the transistor $Q1$ (i_1) can be given by

$$i_1 = \begin{cases} \frac{1}{2}\pi^2 V_{CC}(G_{\rm load} + G') - C_{\rm CE}\omega_0\pi V_{CC}\cos(\theta), \\ \quad 0 \le \theta \le \pi \\ -C_{\rm CE}\omega_0\pi V_{CC}\cos(\theta), \quad \pi \le \theta \le 2\pi. \end{cases} \tag{18}$$

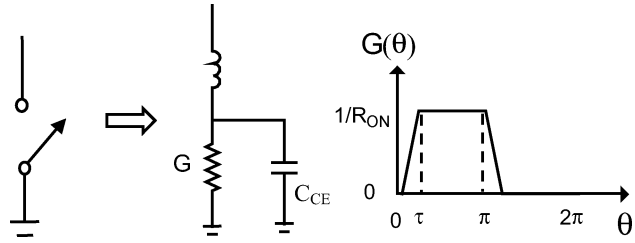

Fig. 8. Switch model with parasitic reactance and finite transition time (τ).

TABLE I
COMPARISON OF THE TOTAL EFFICIENCY

I_{CC} (A)	C_{CE}(F)	G' (1/Ω)	Total efficiency (η_{CMCD})	
			Simulation	Calculation
0.15	0	0	83.3%	87.9%
0.15	4.5pF	0	82%	85.4%
0.15	4.5pF	0.0059	78.2%	80.7%

V_{CC}=3.4V, Q=1.44, τ=0.1π, R_{ON}=0.58Ω, V_{OFFSET}=0.2V were used in simulations and calculations.

The peak of the current i_1 increases with lower Q during the time the transistor is turned ON. This higher current peak increases the stress of the transistors. The efficiency factor η_{pp} is a dominant factor for the experimental prototypes described below.

E. Loss of the Output Matching Network (η_{pm})

Nonideal passive components in the output matching network also degrade the efficiency. For an impedance transformation from $R_{\rm load}$ to R_P, the Q factor of the impedance transformation Q_m is given by

$$Q_m = \sqrt{\frac{R_p}{R_{\rm load}} - 1}. \tag{19}$$

It is assumed that the matching network consists of a series inductor L_m with a Q factor of Q_L. The efficiency factor η_{pm} can then be expressed by

$$\eta_{pm} = \frac{Q_L}{Q_L + Q_m}. \tag{20}$$

η_{pm} decreases with the increasing ratio of Q_m and Q_L. Therefore, a smaller impedance transformation ratio and higher Q factor for the matching network components are helpful to reduce the loss.

F. Comparison of the Simulated and Calculated Efficiency

In order to validate the results of the preceding analysis, circuit simulation was carried out assuming an idealized CMCD amplifier, utilizing a harmonic-balance simulation approach with the Agilent ADS simulator. The switches were modeled as simplified elements, as depicted in Fig. 8. They have a conductance that varies as a function of time between a value of zero (for the switch in an open position) and a value of $G = 1/R_{\rm ON}$ (for the switch in a closed position) according to a simple linear time dependence shown in this figure.

Simulated efficiency for various CMCD designs, compared with the efficiency computed analytically by means of the preceding equations, is shown in Table I. Parameter values were chosen to resemble the experimental circuits.

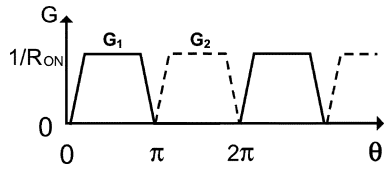

Fig. 9. Switch control waveforms for the highest collector efficiency.

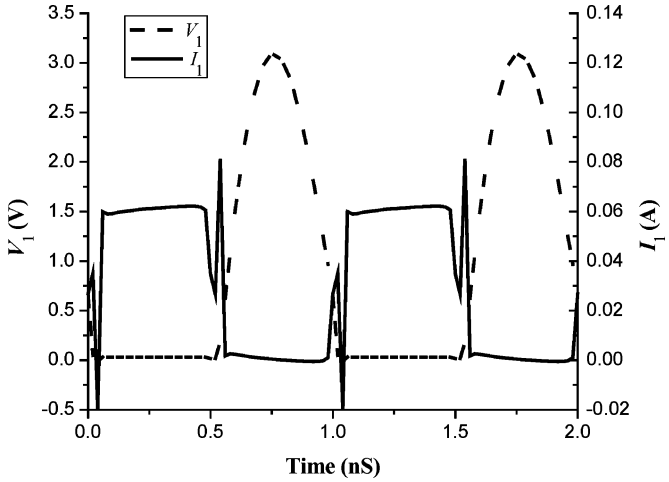

Fig. 10. Simulated current waveform, showing spiking phenomena due to the overlap of voltage waveform and the time-varying conductance.

G. Additional Design Considerations and Limitations of Analysis

1) Duty Cycle of Switching Control Waveform: The efficiency is affected by the extent to which both switches in the CMCD amplifier are simultaneously on or partially on. The highest efficiency is obtained (via simulation) when the degree of overlap is minimized. This typically requires that the duty cycle for switch "on time" is less than 50% in order to account for the finite turn-on and turn-off time of the switches. For example, the highest collector efficiency is obtained for the waveform of Fig. 9.

2) Overlap of the Conductance and Switching Voltage Waveforms: In the analysis of the nonzero transition time effect, for simplicity, the time-varying conductance of the transistors is assumed to have 50% duty cycle and the current flowing through the transistor $Q1$ varies, as shown in Fig. 5. However, the evaluation of the efficiency based on this assumption ignores the overlap of the voltage waveform and the time-varying conductance of the transistors. In practice, when there is substantial overlap between the transient of the switch conductance and the switch voltage, the current transient can be complex, and can display spiking behavior. Fig. 10 shows representative waveforms of the voltage (v_1) and the current (i_1) for substantial overlap. For short transition time, this loss can be neglected. The comparison of simulated and calculated results in Table I corresponds to nonzero transition time of 0.1π.

3) Effect of Series Inductance: As described in Section II, the energy stored in parasitic switch inductance at the time that the switch is opened tends to be dissipated within the switch, and lost to the circuit. As a result, for highest efficiency, in most circumstances, the series inductance should be minimized. In cases where the switching transient is particularly long, however, leading to low values of efficiency factor η_{tt} (associated with transition time), it is found that adding inductance to the switch can improve efficiency. This results from the fact that the series inductance modifies the voltage across the switch, reducing its value during the current on-to-off transient, thereby lowering the switch loss (by more than the energy cost $1/2LI_{\rm ON}^2$).

4) Circuit Symmetry: In the analysis, the even harmonics are ignored because we assume the amplifier circuitry is symmetric. If this assumption fails, even harmonics will pass through the load and induce additional loss.

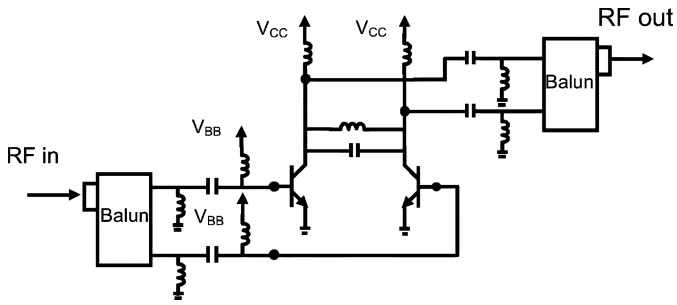

Fig. 11. Schematic of the CMCD amplifier.

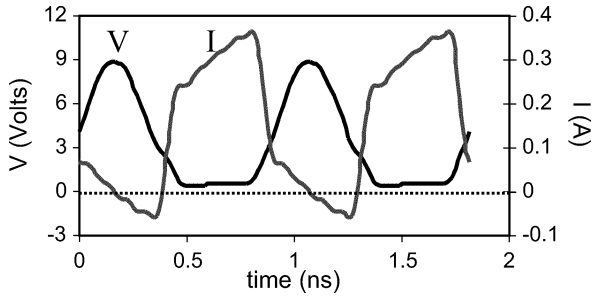

Fig. 12. Simulated collector voltage and current waveform showing desired characteristics of ZVS.

IV. Experimental CMCD Amplifier Design

CMCD amplifiers were implemented with GaInP/GaAs HBTs. Switching devices consisted of 80 emitter fingers of dimension 2 μm $\times$ 20 μm. Resistive ballasting was employed to prevent thermal runaway. Ground connections to the emitters were achieved with through-substrate vias. Harmonic-balance simulation was performed by an ADS circuit simulator. Fig. 11 shows the schematics of a CMCD amplifier for simulation. A 180°-input balun generates differential input signals and an output balun converts the balanced output to single-ended output signal. Input and output matching networks are applied for each transistor to increase tuning flexibility. Fig. 12 shows the simulated voltage and current waveforms. The voltage across the transistors shows the desired characteristic of ZVS. The nonideal current waveforms are due primarily to leakage currents through the parasitic capacitances of the transistors (and do not impact amplifier efficiency). If all passive components are assumed to be lossless, the simulated efficiency can reach 80%.

Two CMCD amplifiers integrated with different *LC* resonator structures were fabricated and measured. Fig. 13 shows the

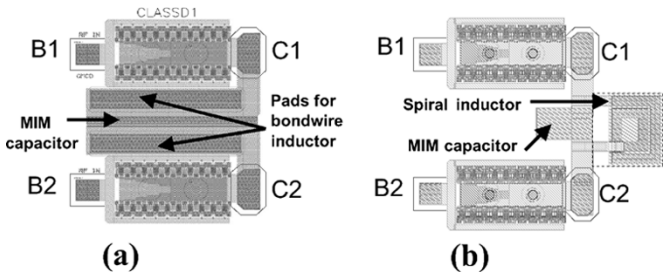

Fig. 13. CMCD amplifier chip geometry. (a) CMCD1: with pads for bond-wire inductor. (b) CMCD2: with on-chip spiral inductor.

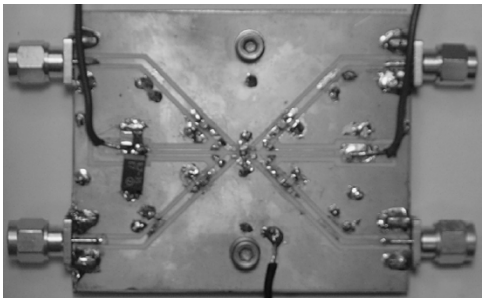

Fig. 14. CMCD amplifier prototype. The overall amplifier employed external matching and baluns.

CMCD amplifier chip layouts. The switching devices used in the two CMCD amplifiers are identical. For the chip marked as CMCD1, shown in Fig. 13(a), the *LC* resonator comprises a bond-wire inductor and a metal–insulator–metal (MIM) capacitor. The capacitor is placed between two HBTs and two parallel bonding pads for making the bond-wire inductor. The inductor consists of six Ω-shaped bond-wire loops in parallel with spacing of 100 μm. The fabrication of the inductor is reproducible with standard production wire-bonding techniques. This on-chip resonator minimizes the parasitic reactance and resistance along the *LC* path and uses the chip area more efficiently. For comparison, another amplifier chip, CMCD2, as shown in Fig. 13(b), uses a spiral inductor and a MIM capacitor to form the on-chip *LC* resonator.

To evaluate the amplifier performance by the results of the preceding analysis, the required circuit parameters $R_{\rm ON}$, $V_{\rm offset}$, $C_{\rm CE}$, and τ were extracted from the transistor model. Q and Y' were obtained from the measurement. The parameters used in the calculation are listed in Table I. If the loss factor η_{pp} (associated with the finite Q of the *LC* resonator) is not included, the efficiency $\eta_{\rm CMCD}$ is calculated to be 85.4%. With the factor of η_{pp} included, the efficiency $\eta_{\rm CMCD}$ of 80.7% can be estimated.

V. Measurement Results

Fig. 14 shows a photograph of the CMCD amplifier prototype. The input and output matching network were tuned for maximum efficiency. An Agilent ESG signal generator was used to generate an input signal sent to a commercial PA (ZHL-2, Mini-circuits, Brooklyn, NY), which amplifies the power to the desired level. MA-COM 180° hybrids were used to convert the signal between single and double ended. The loss, including cable and broad-band balun, is approximately 2 dB between the input and output.

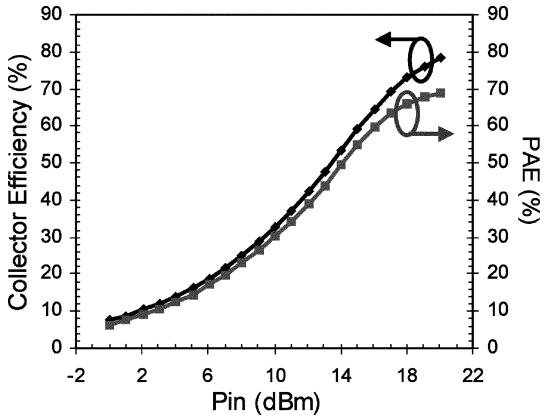

Fig. 15. Measured efficiency versus input power for CMCD1, showing collector efficiency of 78.5% at maximum PAE of 68.5%.

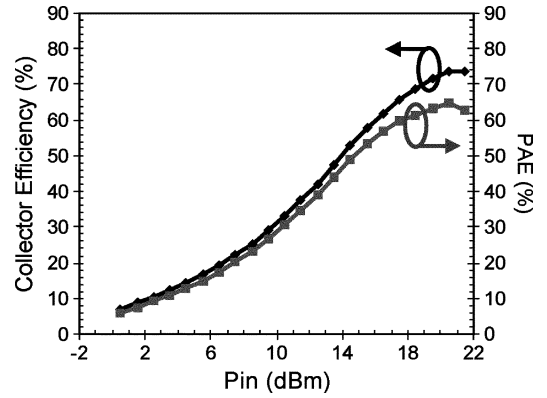

Fig. 16. Measured efficiency versus input power for CMCD2, showing collector efficiency of 73.5% at maximum PAE of 64.6%.

For both CMCD amplifier chips, the bases of the HBTs are biased to a turn-on voltage of 1.2 V for operation as switches. The collector bias is set to 3.4 V. Under these conditions, after calibrating the input and output loss of the cable and balun, amplifier efficiency of the two CMCD amplifiers, i.e., CMCD1 and CMCD2, was measured against the input power, with results shown in Figs. 15 and 16, respectively. The collector efficiency and power-added efficiency (PAE) increase dramatically with increasing the input power. When the input power is increased, the two transistors switch states with shorter transition times and the CMCD amplifier operates in switching mode. For CMCD1, collector efficiency reaches 78.5% at an output power of 29.5 dBm (0.89 W) with maximum PAE of 68.5%, as shown in Fig. 15. For CMCD2, collector efficiency reaches 73.5% at an output power of 29.1 dBm (0.81 W) with maximum PAE of 64.6%, as shown in Fig. 16. Examining Fig. 17, the CMCD1 amplifier shows a wide operating bandwidth. For collector efficiency higher than 70%, it has bandwidth of 300 MHz. The measurement results show reasonable efficiency characteristics of CMCD amplifiers with different inductor implementation.

The GaAs HBTs each have emitter area of 3200 μm^2. The peak current density at maximum power output is 0.11 mA/μm^2. Fig. 18 shows the gain and output power of the CMCD amplifiers, which is nearly identical for the two structures. Due to gain reduction at a high drive level, the PAE starts to drop when output power approaches its maximum

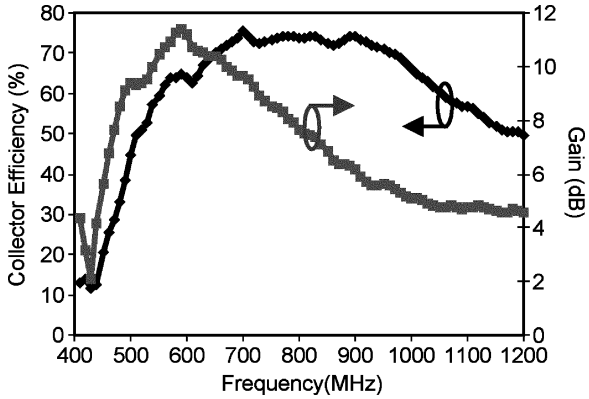

Fig. 17. Measured collector efficiency, gain versus frequency of CMCD1, showing the operation bandwidth of 300 MHz for collector efficiency greater than 70%.

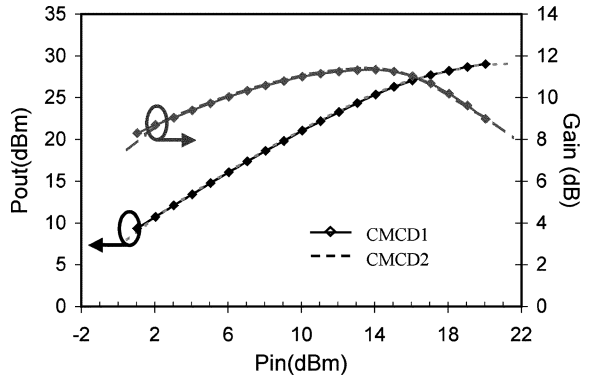

Fig. 18. Measured gain and $P\mathrm{out}$ versus input power.

value. One of the possible reasons for limited gain is saturation charge. The gain can be improved by superior matching, by suppressing saturation charge storage, and by reducing the ballasting resistance, yielding higher PAE.

VI. Conclusion

In this paper, design considerations of the current-mode class-D amplifier have been discussed analytically. Based on the analytical results, the efficiency of the CMCD amplifier can be estimated from the transistor and circuit parameters, providing a useful guide for circuit design. Experimental CMCD amplifiers with different integrated resonator structures have been demonstrated to achieve high efficiency. An amplifier with a bond-wire inductor can reach a collector efficiency of 78.5% at an output power of 29.5 dBm (0.89 W) with a maximum PAE of 68.5%. This CMCD amplifier is suitable for wireless systems with constant envelope modulation. For example, by using larger transistors and adjusting the matching networks to achieve higher output power, the CMCD amplifiers have the potential for use in GSM applications.

Acknowledgment

The authors would like to thank K. Weller, Skyworks Solutions Inc., Newbury Park, CA, for access to industry resource and GaAs HBT fabrication. The authors would also like to thank H. Kobayashi for insightful discussion.

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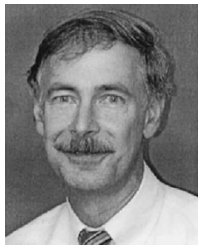

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