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A Study of Different Switched Mode Power Amplifiers for the Burst Mode Operation

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Abstract

Power-amplifier efficiency is a significant issue for the overall efficiency of most wireless system. Therefore, currently there are different kind of Switched mode power amplifiers are developed which are showing very high efficiency also at higher frequencies but all of these amplifiers are subjected to drive with the constant envelope signals. Whereas, for the increasing demand of high data rate transmissions in wireless communication there are some new modulation schemes are introduced and which are generating no more a constant envelope signal but a high peak to average power signal. Therefore, recently a new technique is proposed called the burst mode operation for operating the switched mode power amplifiers efficiently while driven by a high peak to average power signal.

The purpose of this master thesis work was to review the theory of this burst mode operation and some basic investigations of this theory on switched mode power amplifiers were performed in simulation environments. The amplifiers of class D, inverse D, DE and J are studied. The thesis work was mainly carried out by ADS and partly in MATLAB SIMULINK environment. Since this burst mode operation is a completely new technique therefore a new Harmonic balance simulation setups in ADS and Microwave Office are developed to generate the RF burst signals.

A Class J amplifier based on LDMOS technique is measured by a 16 carrier multi-tone signal having peak to average power ratio of 7 dB and achieved the drain efficiency of 50% with -30 dBc linearity at 946 MHz.

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This work is dedicated to my lovely Parents !!

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Introduction:

High efficiency and good linearity becomes a key issue of 3G radio base stations because these base stations consuming a huge amount of power everyday and a remarkable quantity of power is wasted instead of being used. However, the most power consuming parts of the base stations are the power amplifiers. This high power consumption is mainly due to the lower efficiency of power amplifier where a large portion of DC supply is converted into heat. This requires mutually cost and larger spacing for cooling the system. Also, the power consumption causes degradation of device performances for example, battery life time. There is also a trade off between the linearity and the efficiency. Sometimes, good linearity is achievable but of course by the cost of efficiency and vice-versa.

The key reason for less efficient power amplifiers is due to the amplifiers running under 'Back off' condition most of the time. For High increasing demand of high data rate transmission, modern modulation schemes i.e. W-CDMA, OFDM, 16-QPSK etc. are introduced which have very high peak to average power (PAP) signal (typically 10dB or higher) and push the amplifiers to drive in a 'Back off' condition as well. Apparently, the efficiency of an amplifier is better when it is working under saturation or close to saturation but with the 'Back off' condition it is not possible to operate the amplifiers in saturation, as a result efficiency goes down very quickly. For a Rayleigh-envelope (multicarrier) signal with 10 dB PAP ratio, the efficiencies drastically goes down to 5% and 28% for ideal class A and class B amplifiers respectively, as stated in [1].

As it is mentioned, amplifiers can achieve high efficiency when it is operating in the saturation region. This requirement is only be fulfilled by the switched mode amplifiers (SMPAs). The SMPAs offer very high efficiency, at least in theory 100%. However, this high efficiency is only obtainable when the SMPA will driven by a constant envelop signal but a W-CDMA signal is no more a constant envelope signal. Therefore, we have to make sure that the switched mode power amplifiers will operate in a saturation region even under the back off conditions. In order to satisfy the above condition some pre-techniques have to implement before driving the SMPA.

Researches are continuously going on to find out the optimum operation for achieving high efficiency. There are several methods which have already been implemented and some are proposed to enhance the efficiency both for conventional and switched mode power amplifiers [2]. Here, some promising techniques are described very briefly.

The efficiency can be improved by using Doherty technique [3] both for conventional [4] and switched mode power amplifiers [5]. In this technique, commonly there are two amplifiers are used. One is the carrier amplifier and another is the peak amplifier. For low to medium input power, the carrier amplifier is active and for high input power the peak amplifier is turned on and carrier amplifier goes into saturation. By proper combination of these two amplifiers high efficiency and good linearity is achievable. However, the Doherty technique has few disadvantages as well. For instance, complex circuitry, bulky size, gain degradation, bad linearity and narrow bandwidth [4].

There is a way to obtain high efficiency by controlling the drain DC voltage to manage the output power. This technique is known as Envelope elimination and restoration (EER) [2, 6, 7]. In this technique the input signal is split into separate amplitude and phase signals. The Phase information is feed to the SMPA along with RF carrier and the amplitude signal controls the drain DC voltage to maintain the output power thus causes high efficiency. Regrettably, it is hard to implement the DC-DC power supply in efficient manner and also to have time alignment between the supply and RF paths [2].

Another interesting method is recently employed called load modulation technique [1]. In this method time varying control signals are applied to a tunable output network which turns out varying output power by dynamically changing the load impedance seen by the transistor. The phase information is passed through the gate with the RF carrier. High efficiency is achieved by proper selection of the load impedance. The drawback of this method is that a number of matching networks are required because each transistor requires a different matching network depending on the model [8]. Also, another limiting factor is the limitations of the tunable capacitances [9].

As from the theory, switched mode power amplifiers are driven only between an on and off state and during the on state the SMPA is forced hardly to operate into saturation and at the off state the transistor is switched off thus no current is flowing. That is how, high efficiency is achieved. Therefore, if high data rate modulated signal like W-CDMA is processed at the baseband in a way that the SMPA will operate only between an on and an off state for example kind of a PWM signal, then a high efficiency is obtainable (theoretically 100%) with the same simple circuit configuration of the SMPA which is designed for the constant envelope signals. This technique is known as the Burst mode operation [10, 11]. In this technique the high PAP signals are processed

in baseband to build a square waveform of different duty cycles. This baseband processing could be done by a Delta-sigma modulator, PWM modulator, etc. Before this signal is feed to the amplifier the square shape waveform is multiplied by a RF carrier containing phase information.

There are some other techniques proposed for the Digital architecture where the RF input signal directly converted into the pulse trains i.e. Class S [2, 12]. These types of digital architecture demand very high sampling rate or switching frequency (usually four times that of the signal) which are not flexible for implementation.

The proposed Burst mode operation is a completely new technique to transmit signals in a high efficient way. In this thesis paper, all studies and investigations are based on the SMPAs driven by the Burst signals. This work includes mainly, the theory of burst mode operation and the investigation of the behavior of the different SMPAs. Also a key part of this thesis work is to develop the simulation setups in different software which are fit for the burst mode operation. Some measurements are also carried out by the burst signals processed from a multi-tone signal to see the performance of the different SMPAs which are designed for the constant envelope signals.

This study is carried out by performing the simulations in Advance Design System (ADS 2008) and partly Microwave Office as well as MATLAB Simulink.

1.1 Report Outline:

In chapter two, the theory of this new burst mode operation is reviewed. Also, some indications of circuit design for optimum operation in burst mode operation is presented.

In chapter three, the time domain simulation of different switched mode power amplifiers, mainly Class D, inverse class D and Class DE which are excited by the burst signals are presented.

In chapter four, Harmonic balance simulation setups for the burst mode operation are presented both in ADS and Microwave office.

Finally, in chapter five, the measured and simulated results for the class J and inverse class-D amplifier (designed for constant envelope signal) excited by the burst signals are presented.

1.2 Thesis Limitations:

This thesis work focusing mainly on simulation to get a better understanding of the theory of the burst mode operation rather than a complete design. The vital portion of this technique is to process the baseband signal in an optimum way but which was not considered at all in this work. The requirements for circuit design is studied and realized from the simulation and measurement results. However, the optimum circuit suitable for this operation is not designed due to the limitation of time.

1.3 Previous achievements:

The Burst mode operation is a completely new and it is still an ongoing research project. There is no published paper or achieved result which exactly fits to this technique. As it is mentioned there are some promising techniques for enhancing the PA efficiency, therefore table 1.1 is presenting measured result of different techniques as well as the result of this thesis work.

Techniques	Driving Signal	Power back off	Efficiency	Linearity
Doherty with switch PA [5] @ 2.1 GHz.	W-CDMA	10 dB	**45%** (Drain Efficiency)	**-32 dBc**
EER [13]	W-CDMA	7.67 dB	**50.7%** (Power Added Efficiency)	**-51 dBc** (After digital pre-distortion)
The Burst mode operation [in this work] @ 946 MHz. **N.B.** the measured PA is not optimized for the burst mode operation.	16-Carrier Multi-tone	7 dB	**50%** (Drain Efficiency)	**-30 dBc** (without Digital pre distortion)

Table 1.1: Measured efficiency and linearity for different Transmission techniques.

Chapter 2

Theory of Burst mode operation:

The main concept of this Burst mode operation for the RF application is that a square wave is generated and which has a certain frequency called PWM frequency with the varying duty cycles following the amplitude information of the incoming baseband signal. The square wave is then multiplied with a RF carrier which is containing the phase information of the baseband signal. After multiplication, the RF burst signal is fed to the Switched mode PA. During the 'HIGH/ON' period of a square wave, the amplifier is driven exactly with constant envelop signal which gives high efficiency (Ideally 100% for SMPA) because it is operated under the saturation region. During the 'OFF/LOW' period there is no signal at the gate of the transistor to switch them on, therefore the SMPA will be in 'OFF' state. So, there will be no output power and DC power burning during this 'OFF' period. As a result, SMPA is an on state only at high stage and no DC power burning (ideally) over a full period of operation and eventually very high efficient amplification is achievable, theoretically 100%. After this efficient amplification a narrowband band pass filter is placed after the SMPA to demodulate the RF burst signals before it has been transmitted by the antenna. Figure 2.1 shows the transmission chain for this burst mode operation.

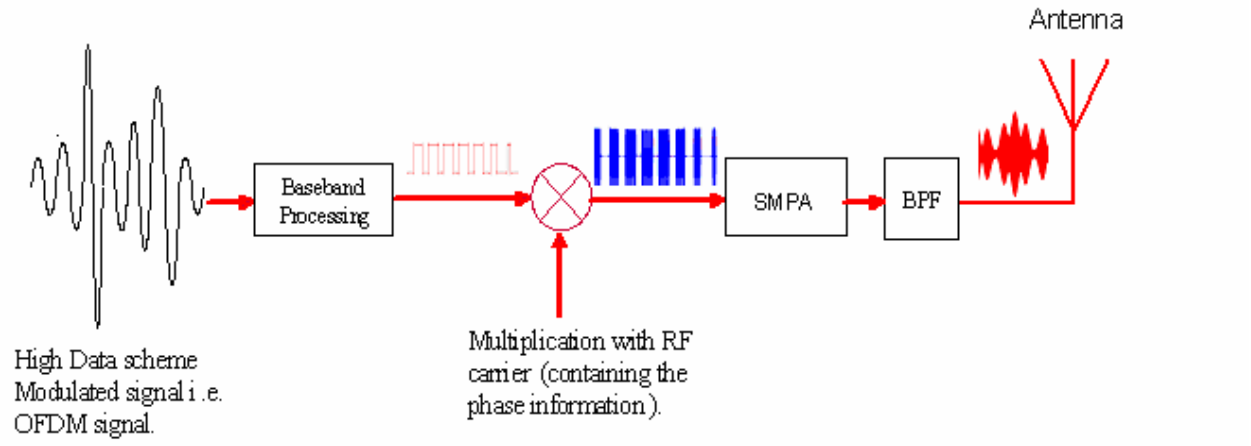


Fig 2.1: Block diagram of a simplified digital transmitter

2.1 Pulse Width Modulation Technique:

There are several ways to code or modulate the baseband signal into square wave or PWM signal. The signal could be from Pulse Width modulator, Pulse density modulator, Band-pass delta sigma modulator, Baseband delta-sigma modulator and so on.

The pulse width modulation technique is very famous in Audio application for transmitting signal in an efficient way. Currently, researches are going on for RF application in a same fashion to transmit signals. In this thesis work, the investigation was to drive the switched mode PA with three levels Pulse width modulated signal (Negative, positive and zero) c.f. fig. 2.2 (b).

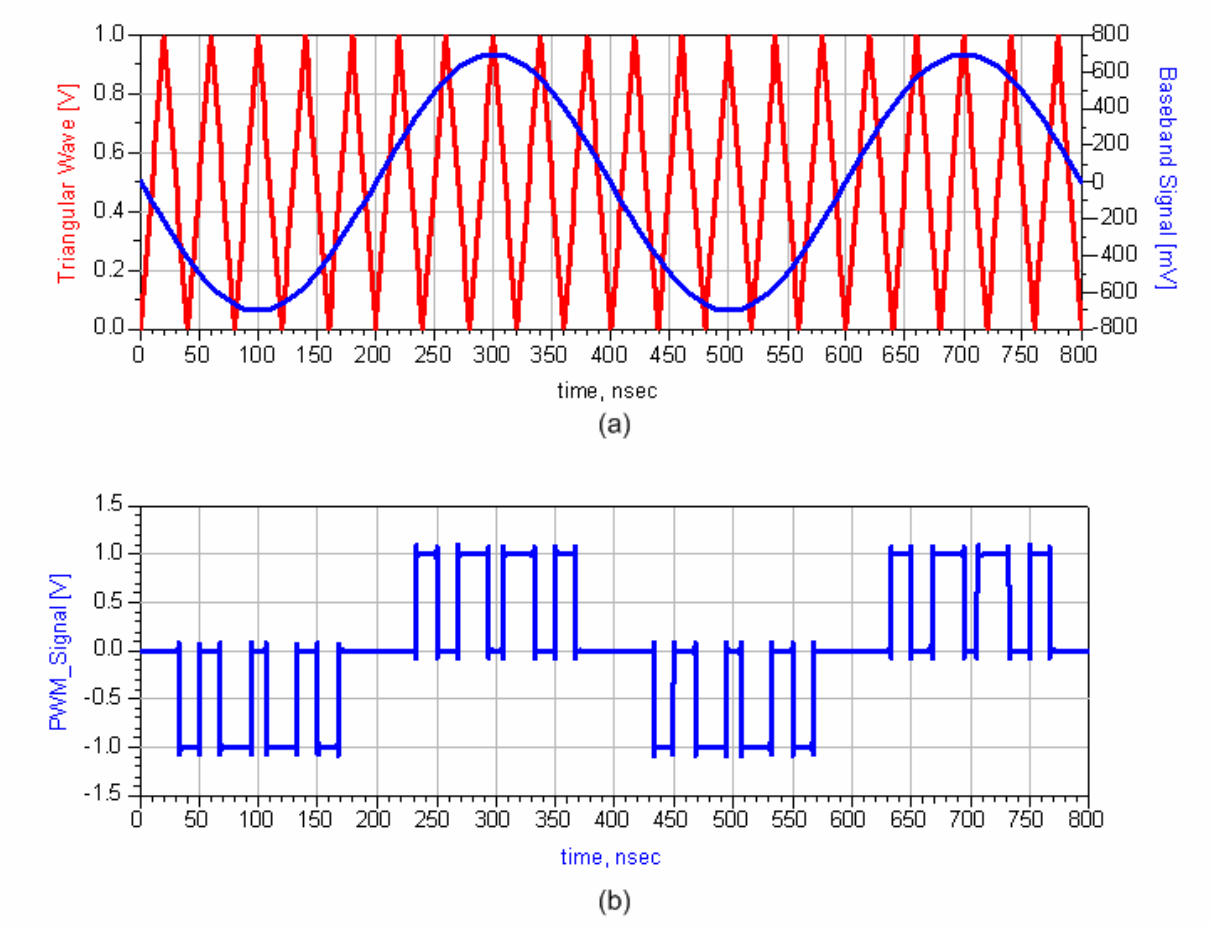


Fig 2.2: (a) A simple way of coding the envelope information of a baseband signal into a PWM signal. (b) Corresponding PWM Signal after the coding.

In order to code a simple sinusoidal signal into a square wave signal or a PWM signal, the sinusoidal signal is compared with a Saw tooth or a triangular wave. When the absolute magnitude of the sinusoidal signal (blue) is larger than the triangular wave (red) and if the magnitude of the sine wave is less than zero then the PWM signal is in the negative state (fig. 2.2 (b)) and also if the magnitude of the sine wave is higher than zero then the PWM signal is in the positive state (fig. 2.2 (b)) otherwise the PWM signal is in the zero state [14]. The frequency of this saw tooth or triangular wave will determine the frequency of the desired PWM signal and the envelope information of the baseband signal will be coded into the different duty cycles of the PWM waveform. Figure 2.2 (a) shows that a sinusoidal wave is compared with a triangular wave to code the envelope information of the baseband signal into a PWM signal and figure 2.2 (b) shows the corresponding PWM signal produced from figure 2.2 (a).

Since the PWM modulator itself is a non-linear system therefore consideration must be taken while coding the baseband signal into a PWM waveform. The frequency of the Saw tooth waveform must be much higher than the frequency of sinusoidal signal. Otherwise, extra non-linear distortion will be introduced at the band of interest (fig. 2.3) which is caused by the modulator itself [14]. Figure 2.3 shows that the extra products which are produced by the modulator (red lines) are interfering into the band of interest (blue lines). These extra products will introduce some distortions in original signals. Since we are interested to transmit only the baseband information therefore a narrowband band pass filter is placed at the output of the PA. In that concern, if the PWM rate is low compare to the required rate then it will be hard to filter out these interfering components from the band of interest, whereas with higher PWM rate it will be easy to filter out these modulation products from original signal components. Low distortion design use higher factors of PWM rate, typically at least 5 to 10 times more than the baseband rate.

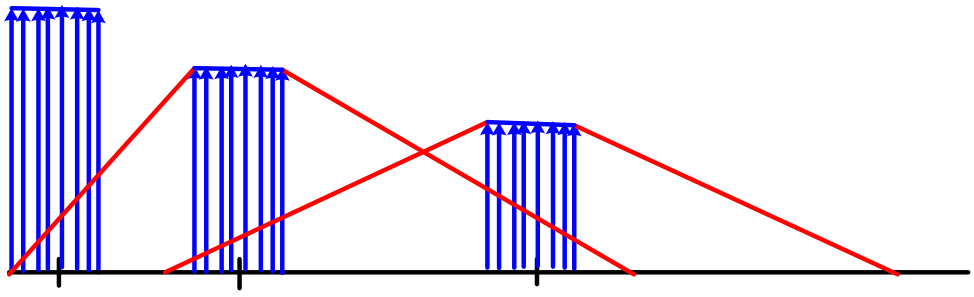


Fig 2.3: Modulation products are interfering into original signal.

On the other hand, there are also some problems with higher PWM rate. Higher PWM frequency demands broader input matching of the SMPA to keep the high efficiency. This phenomenon is discussed in the next section.

2.2 Requirements of Switched mode Power Amplifiers for the Burst mode Operation:

For designing and handle an SMPA optimally for this burst mode operation consideration must be taken on following issues:

- ✓ Input matching network.
- ✓ Filtering and Output matching Network.
- ✓ PWM rate.
- ✓ Threshold voltage or gate voltage.
- ✓ Drain voltage.

2.2.1 Input Matching Network:

In order to transmit signal in an efficient way a perfect RF burst signal (fig. (2.4)) must be delivered at the gate of the PA. Figure 2.4 shows a perfect RF burst signal to drive an SMPA in an efficient way. Now, a question may be raised that how to assign a perfect burst signal at the gate and why it is important?

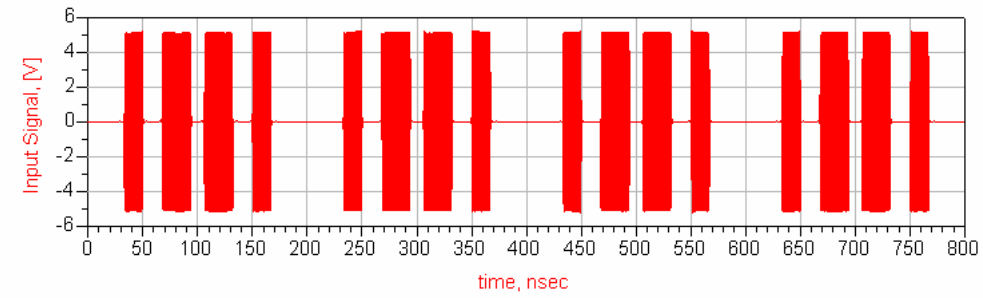


Fig 2.4: Driving signal to the SMPA for burst mode operation (Multiplied with RF carrier)

If we look at the modulated signal (PWM Signal), it's a simple square wave nothing else. Therefore crudely it can be said that a perfect square wave has to allow at the gate. Figure 2.5 (a) shows a square wave with 50% of the duty cycle.

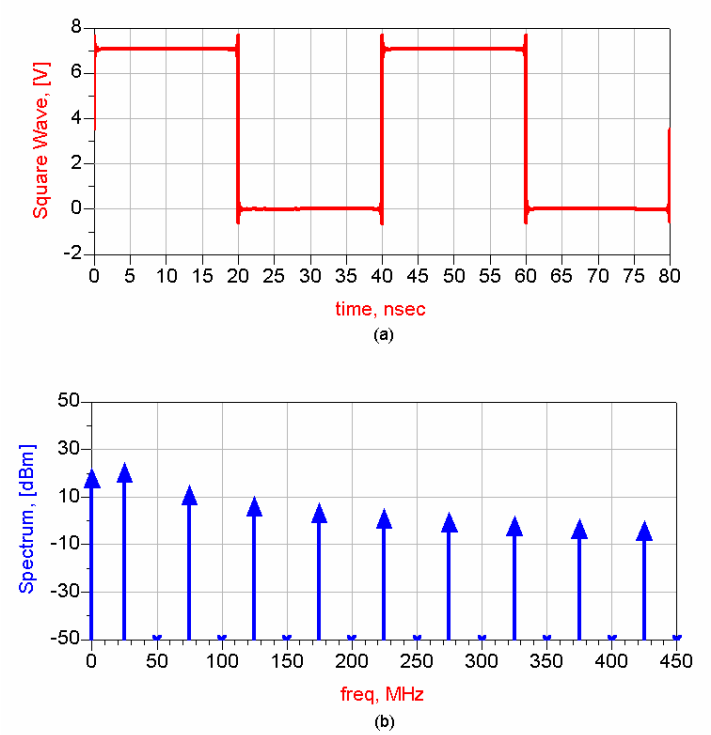


Fig 2.5: (a) Square wave with 50% duty cycle. (b) Corresponding frequency spectrum

It can be observed from figure 2.5 (b) and also from Fourier series expansion [23] of a square wave that in order to get an ideal square wave, infinite number of odd harmonics has to be considered. In practical, it is impossible to consider infinite number of harmonics but some reasonable number of odd harmonics must be considered to obtain a sufficiently accurate square waveform.

In this situation, if we concentrate on circuit design of a Power Amplifier, there must have an input matching and the bandwidth of the input matching will determine how many harmonics can be allowed to the gate of the transistor. Therefore, a wide band input matching network is required at the input of the SMPA to assign an accurate square waveform which will force the transistor to operate in a switched mode operation.

As it is discussed earlier that the PWM signal is multiplied with the RF carrier before it is feed to the PA therefore the spectrum shown in figure 2.5 (b) will be up shifted to the RF carrier frequency (fig. 2.6). Figure 2.6 shows the spectrums a RF burst signal of the constant duty cycle of 50%.

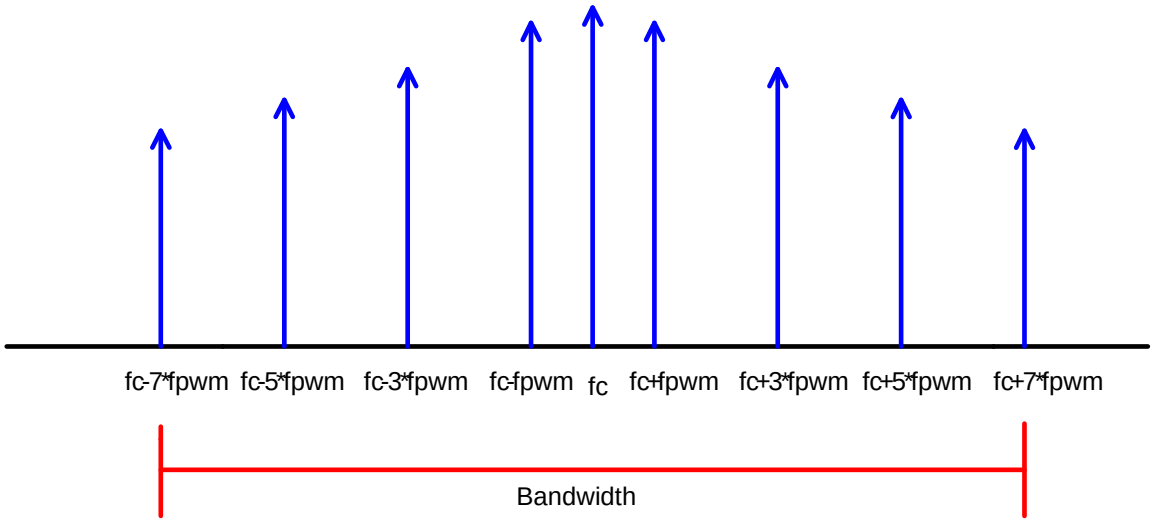


Fig 2.6: Spectrum of Burst signal after multiplying with carrier.

If the PWM frequency is only 25 MHz and considered only eight components from the left and right centered with the carrier frequency (fig. 2.6) then 350 MHz of bandwidth is required at the input of the PA. Therefore, it is clear from the overall discussions and figures that a wider bandwidth is required at the input of the PA for achieving a high efficiency.

Now, it is also worth to discuss that how the efficiency goes down by a narrower input bandwidth of the PA. If the input bandwidth is narrow then only a few harmonics will be allowed at the gate of the PA and eventually the PWM signal will have no more square shape as discussed earlier. As a result, at the gate of the transistor there will be a distorted burst signal. In reality there are lots of other effects which may influence the shape of the driving signal. Below figure 2.7 is illustrating the effect of the input bandwidth in an ideal situation.

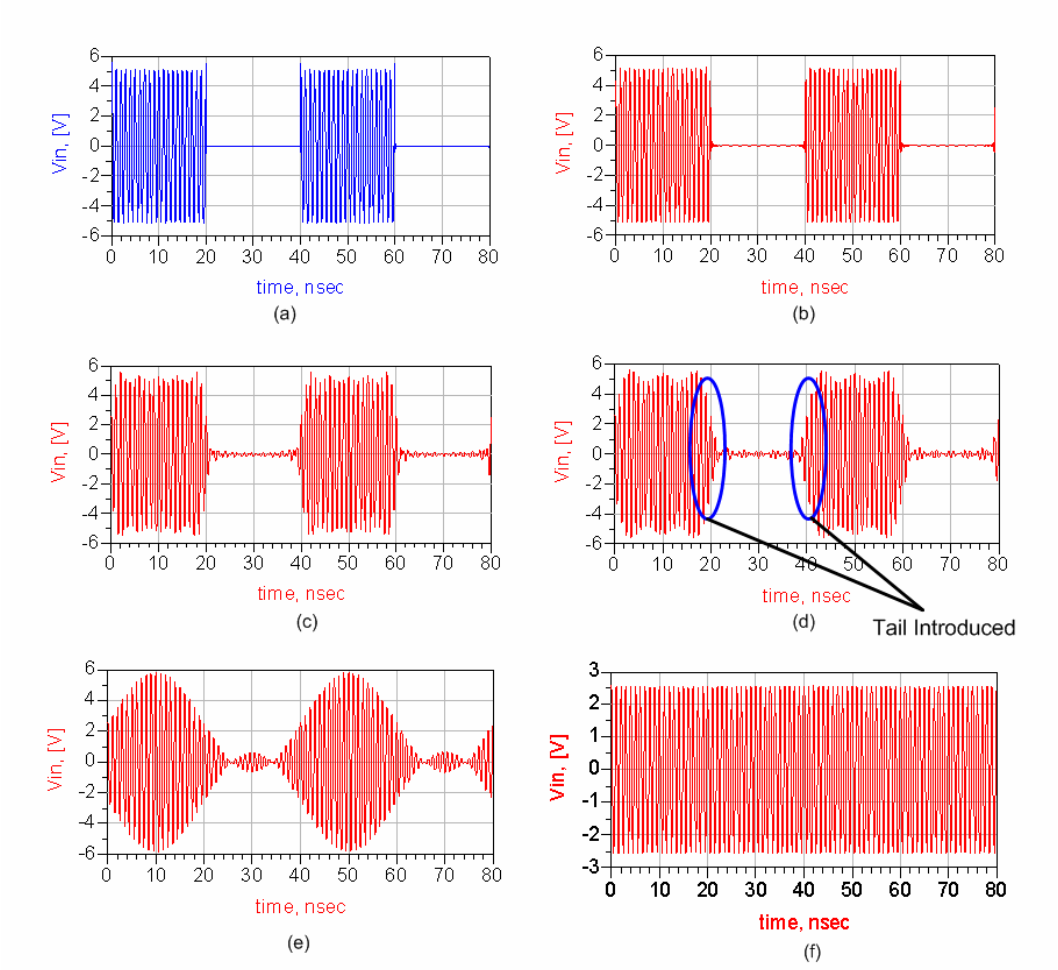


Fig 2.7: Input signal for 25 MHz PWM frequency of 50% constant Duty cycle. (a) Without any input matching/bandwidth. (b) 5 GHz bandwidth. (c) 500 MHz bandwidth. (d) 300 MHz bandwidth. (e) 100 MHz bandwidth. (f) 40 MHz bandwidth.

From figure 2.7 (b) we can observe that with a very broad band input matching network a perfect burst signal is assignable at the gate of the PA. As the bandwidth starts to decrease, the signal tails are introduced at the beginning and the ending of the 'ON' period or at transitions (fig. 2.7 (d), blue marked).

By that kind of driven signal (fig. 2.7 (d)) having tail at transitions there is a possibility to loose the linearity. Furthermore, during the 'OFF' period of a perfect burst signal, ideally there will be no current flowing through the drain of the transistor therefore also no DC power will burn and finally a high efficiency is achievable. However, by a distorted burst signal the transistor will turn on with the tail signal which has low amplitude than expected. Therefore, the SMPA

will operate in a linear region and not in a saturation region on that instance of time. As a result, overall efficiency will goes down.

With a very narrow input bandwidth the driving signal will not be a burst signal anymore. A simple AM signal will introduced at the gate of the PA (fig. 2.7 (e)). If the driving signal is like an AM signal then there is no benefit to consider an SMPA because eventually it will become a low efficient system. Furthermore, with extremely narrow band matching network all spectral components of the burst signal will be trunked and amplifier will be driven by a constant envelope signal (fig. 2.7 (f)) and which has no envelope information at all.

2.2.2 Filtering and Output Matching Network:

Since we are interested to transmit only the baseband signal or in-band signal therefore the modulated RF burst signals must be demodulated before feeding it to the antenna. For that reason, this burst mode operation required a very narrowband band-pass filter at the output of the PA. This filter should have very low insertion loss as well. Now, the problem is to connect the filter in an optimum way because from the investigation and the measurement results conclusion is made that the connection of the filter has a great influence on the efficiency of the SMPA. In this instance, it is worth to discuss why the filter connection is so critical.

It has already been discussed in the earlier section that a wider input bandwidth is required for allowing large number of modulation products for an efficient transmission. Therefore, the entire components which are considered at the input will also appear at the output of the PA as desired. Figure 2.8 shows the input and the output voltage of the SMPA and corresponding frequency spectrum (without filter) of the constant duty cycle of 50% with 25 MHz PWM rate.

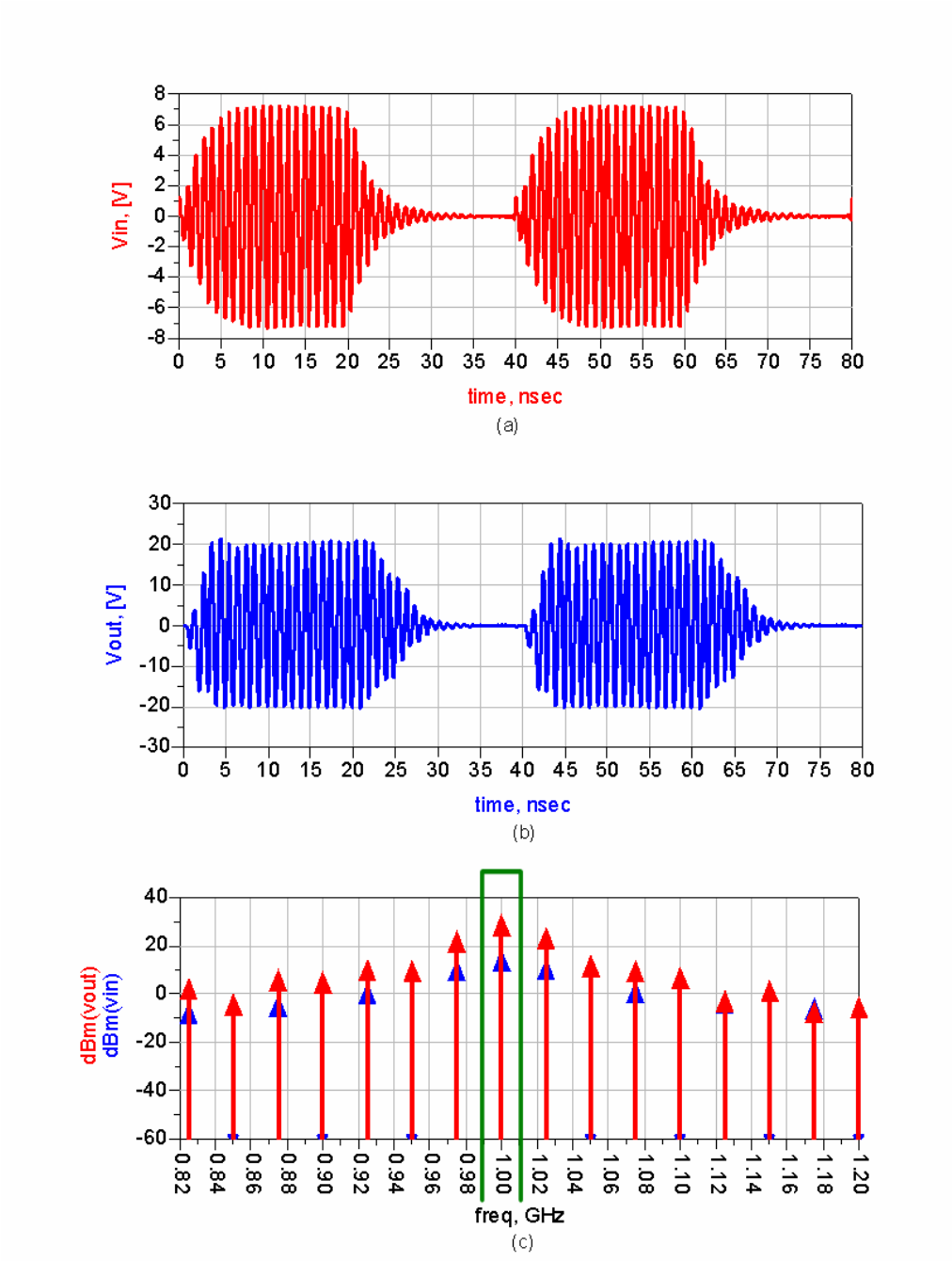


Fig 2.8: (a) Signal at the gate of the transistor. (b) Signal from the drain of the transistor. (c) Corresponding frequency spectrum, Input (blue) and output (red).

It is clear from figure 2.8 (c) that at the output of the SMPA has all the modulation products along with some unwanted products. Therefore a narrowband band pass filter has to place at the output of the SMPA to filter out the modulation products or to demodulate the RF burst signals. The green curve on figure 2.8 (c) marked the interested component which has to transmit from all other modulated components.

Usually, for a GMSK modulated signal or a CW (continuous wave) signal a band pass filter is placed at the output of the PA for the precise transmission along with a circulator to prevent any reflection from the filter and antenna. The connection could be mapped in a way as shown in figure 2.9.

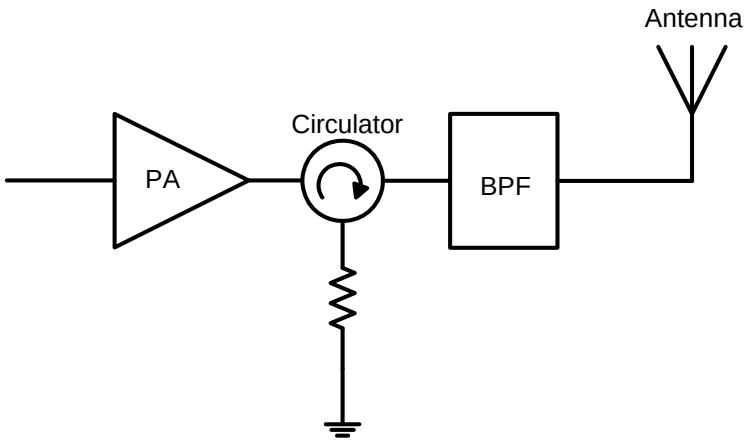


Fig 2.9: General feeding technique to an Antenna.

For these types of modulated signals there is no problem to feed the output signal to the antenna in the way which is depicted in figure 2.8. On the other hand in burst mode operation, this concept is not an optimum way to demodulate or filter out the output signal because all the out of band components will burn in 50 Ω load of the circulator which means loss of efficiency. However, if there is no circulator then the out of band components will reflected back from the filter and destroy the drain voltage and current which will ultimately ended up with the lower efficiency. Therefore it is still an open and hard problem for this burst mode operation to connect the filter in an optimum way. However, some possible approaches regarding this filtering issue are described below.

2.2.2.1 Approach 1:

One of the possible solutions could be to connect the filter in close to the drain of the transistor as much as possible and the output signal from the transistor will feed to a band pass filter which is designed to 50 Ω for the in-band components and very high impedance for the out of band components (fig. 2.10).

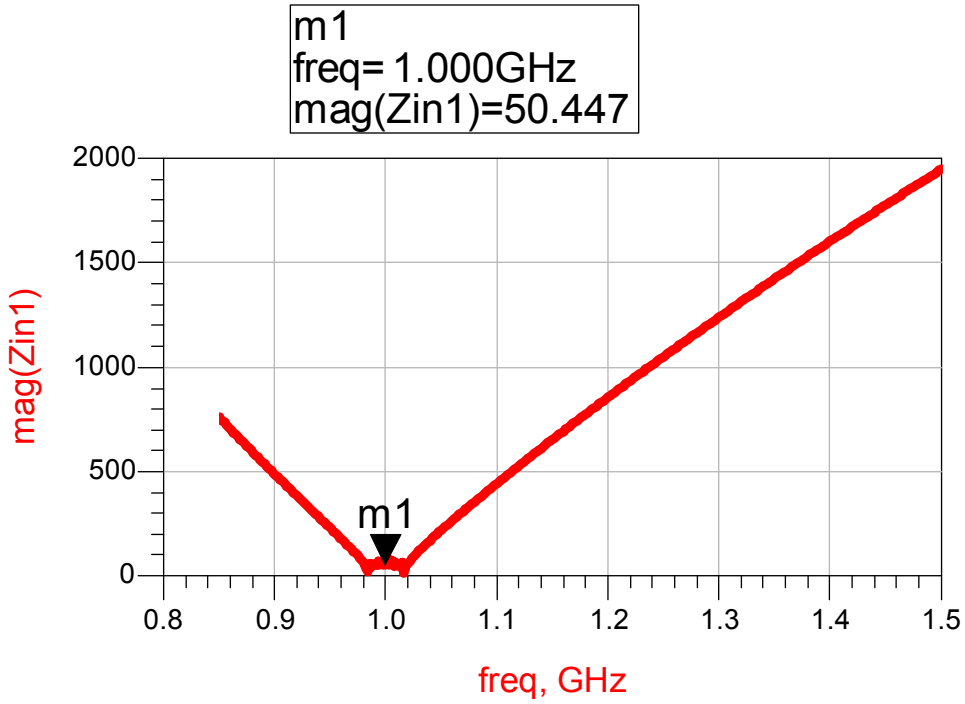


Fig 2.10: Characteristic of the Input impedance of the band pass filter

Figure 2.10 shows the input impedance over different frequencies of the intended band pass filter. In this approach, only the in-band output voltage will be allowed to reach to the load and will produce only the in-band output power but the voltage of the out of band components will see open circuit to the load due to high impedance of the implemented filter which means no power will produce for the out of band components and eventually high efficiency can be achieved.

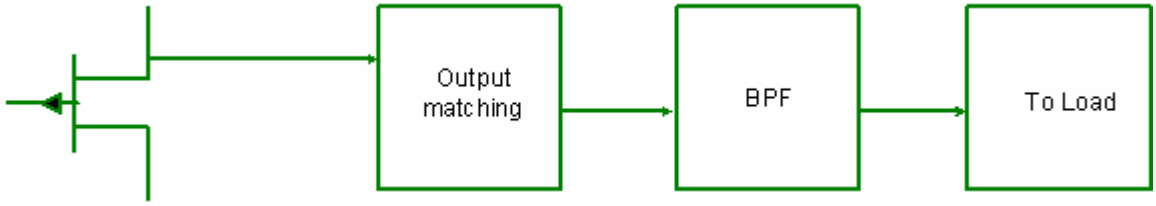


Fig 2.11: One possible way of filtering RF burst signal.

Figure 2.11 showing a way of placing the filter for this burst mode operation. Since there is no extra cable between the output matching and the band pass filter therefore no reflection will occur for this proposed way (fig. 2.11). In this concern, clearly the demand is to optimize the filter while designing the SMPA.

On the other hand, if the filter is connected with the output of the SMPA by a 50 ohm cable of arbitrary lengths as shown figure 2.12, then there are lot of impacts on efficiency and linearity due to the reflections of the out of band components from the filter.

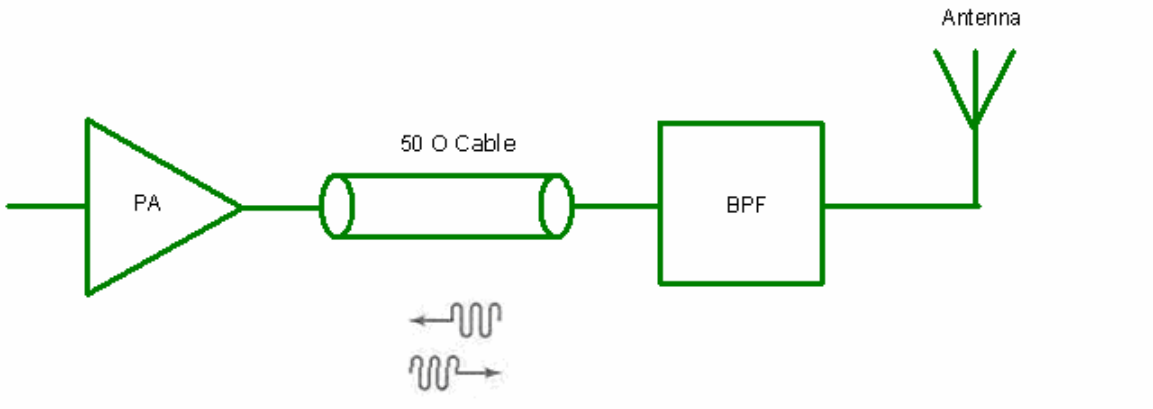


Fig 2.12: Filter is connected in a traditional way.

This reflection is mainly caused by the cable placed between the PA and the band pass filter (fig. 2.12). Therefore, different lengths of this cable will introduced different output efficiency by means of different reflections.

2.2.2.2 Approach 2:

One could try to find out the optimum load impedance seen by the transistor which will allow only the in-band components to the load and will suppress the out of band components. That's means the output matching network will take the filtering task. Another possible way could be implemented which is similar to harmonic tune for different SMPA (inv D, F, etc.) circuit designing. For example in Class F circuit [15] at least some reasonable number of resonators is required to short out the even and to block the odd harmonics. If major out of band components (modulation products) for this burst mode operation are tuned out in a similar fashion as mentioned earlier (Class F configuration) then high efficiency could achievable. Also, this approach will give some relax to the band pass filter. However, then the open point is what will be the optimum impedances of these out of band components which are about to tuned out.

2.2.3 PWM rate:

It is discussed in section 2.1 that higher PWM frequency is required for producing good quality modulated signal. On the other hand, in order to drive the PA efficiently PWM rate should not be much higher because with the higher PWM rate a broader range of input matching network is required (sec. 2.2.1). Apart from this bandwidth issue there is another problem associated with the higher PWM rate.

Usually an SMPA operates in an efficient way when it is capable to achieve zero voltage switching (ZVS) [16] at the switching instances. Even if the designed SMPA is achieved ZVS for the constant wave (CW) operation but it is difficult to achieve ZVS for the PWM transitions. Now, with the PWM signal having higher PWM rate has definitely high number of transitions (fig. 2.12) which will lead to lower efficiency. However, with lower PWM rate there is a problem to filter out the out of band components at the output of the PA (sec. 2.2.1). Therefore, here a trade off between the efficiency and the output filtering effect on the output side of the SMPA. Below figure 2.12 shows the effect of PWM rate on modulated signal (PWM signal).

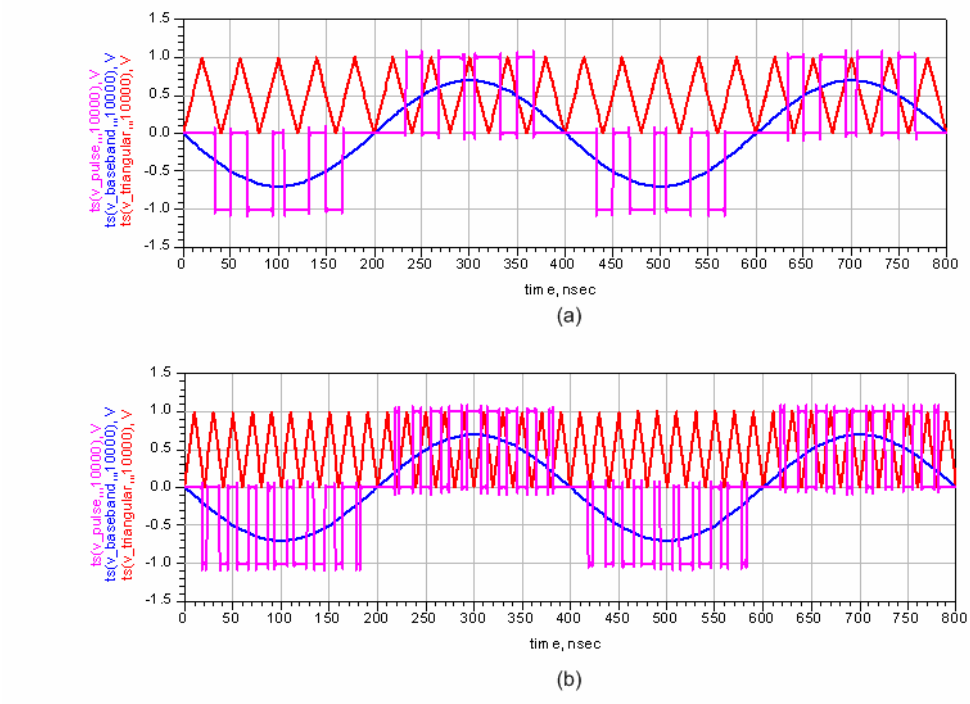


Fig 2.12: (a) Modulation process with 25 MHz PWM rate. (b) Modulation process with 50 MHz PWM rate.

2.2.4 Threshold voltage or gate voltage:

In order to drive the PA in the burst mode operation attention must be paid on the level of gate voltage. Figure 2.13 shows the input signal of the burst mode operation.

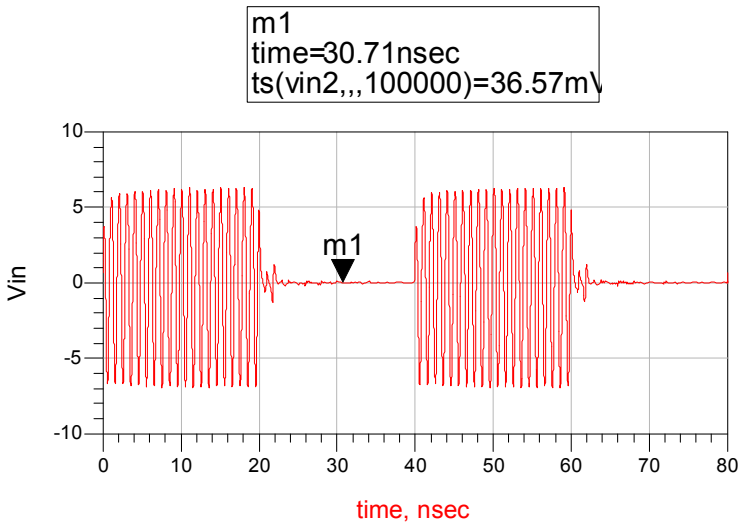


Fig 2.13: Output voltage from the RF burst signal generator

Apparently, when the gate biasing voltage will apply then the input voltage will superimpose on it. Figure 2.14 shows the input voltage at the gate of the PA for the burst mode operation.

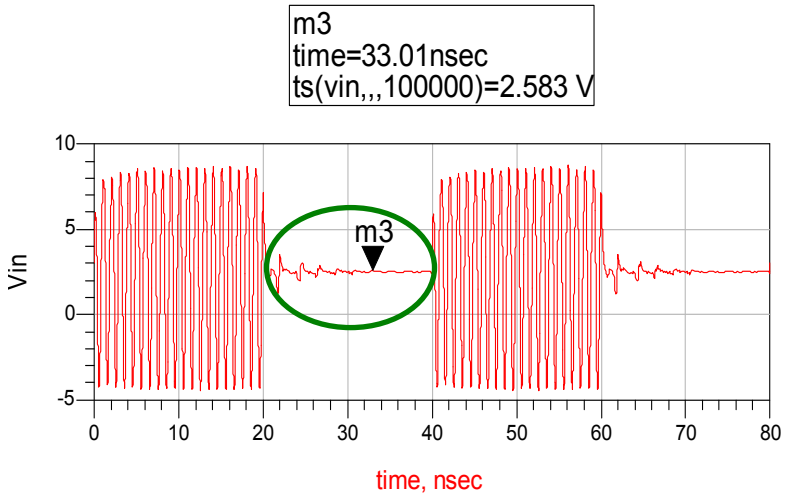


Fig 2.14: Input Voltage waveform at the gate of the PA after employed the gate bias voltage.

From figure 2.14 it is clear that the voltage level at the 'OFF' state (green marked) is also increased up to the gate biasing voltage. Therefore, if the gate biasing voltage is set to the threshold voltage of the transistor as in the constant envelope operation mode then the transistor will turn on during the 'OFF' state in the burst mode operation which is not desired. Thus, the gate biasing voltage should be lower than the threshold voltage of the used transistor in the burst mode operation.

2.2.5 Drain voltage:

In burst mode operation there is a possibility to produce the high peak currents and high peak voltages across the device (fig. 2.15) during the transitions of the RF burst signals. Therefore, to avoid these overshoot at the drain of the transistor it would be good to drive the SMPA with the lower drain voltage in the burst mode operation compare to the CW operation. Figure 2.15 shows the drain voltage and current of the ideal current mode class D amplifier driven by the RF burst signal.

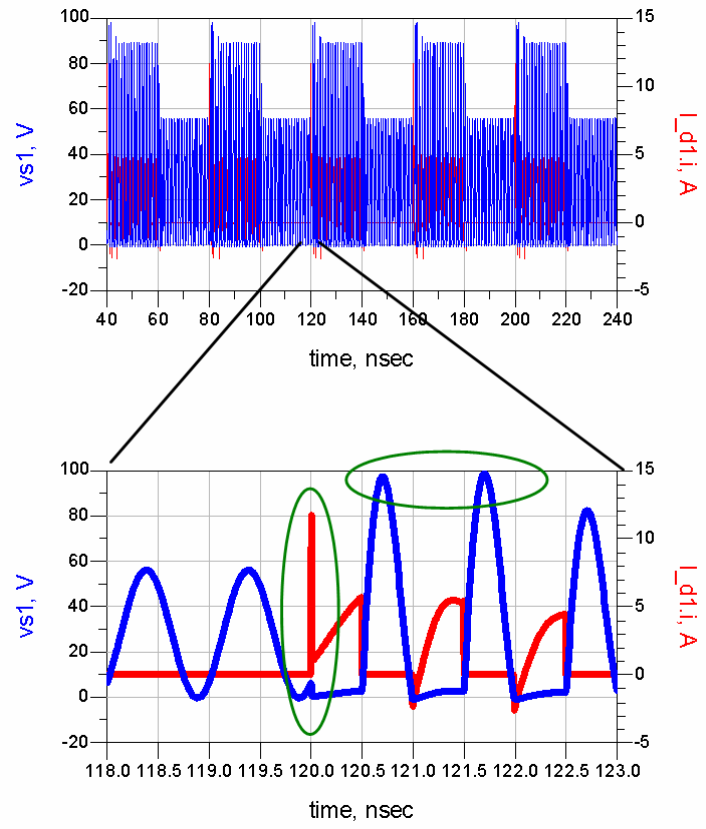


Fig 2.15: Current and voltage waveform over the device in burst mode operation.

2.3 Characterizations of an SMPA with the Burst Signal:

Since all the baseband information are coded into the different duty cycles of the PWM waveform therefore it is important to know the output behavior at the different duty cycles of the PWM waveform in order to characterize the SMPA. As we know that the PWM signal is nothing but a square wave therefore to figure out the dependency of the duty cycle a pulse wave is considered for primary investigation which is shown in figure 2.16.

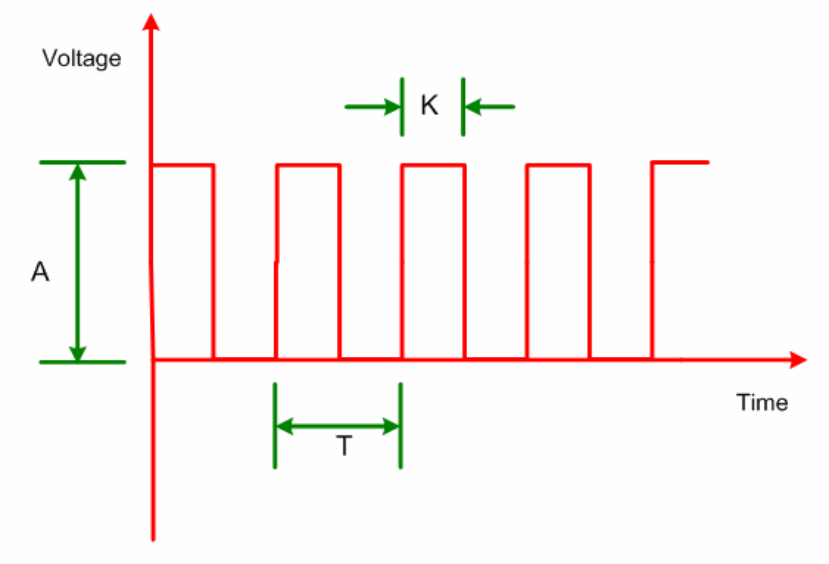


Fig. 2.16: A Simple Pulse wave signal in time domain

Figure 2.16 shows a simple pulse wave signal in time domain where T is the time of one period and K as well as A are representing the width and the amplitude of the pulse respectively. Therefore, the duty cycle can be expressed by

$$DC, \text{ duty cycle} = K/T \tag{2.1}$$

Now, if we make the Fourier series expansion of this pulse wave the coefficients can be expressed by the following equation.

$$\begin{aligned} a_0 &= A(DC) \\ a_n &= \frac{2A}{n\pi}\sin(n\pi DC) \\ b_n &= 0 \end{aligned} \tag{2.2}$$

Where,

a_0 = *Constant term.*

a_n = *Sine coefficient.*

b_n = *Cosine coefficient and n= 1,2,3,……...*

The equation 2.2 shows that the coefficients are dependent on the duty cycles of the pulse wave. From the equation 2.2, the total power over a period of a pulse wave can be derived as follows.

$$Pout\_total = P_{\max} \times DutyCycle \tag{2.3}$$

Since we are only interested to transmit the in-band components (sec. 2.2.2) therefore it is worth to know the in-band power over the different duty cycles. The in-band power which is related to the duty cycles can be derived from the constant term of the equation 2.2. Here the in-band power is considered by assuming perfect filtering condition.

$$Pout\_inband = P_{\max} \times (DutyCycle)^2 \tag{2.4}$$

Now, from the equation 2.3 and 2.4 an important curve can be plotted (fig. 2.17) by which we can characterize the SMPA for the RF burst signal.

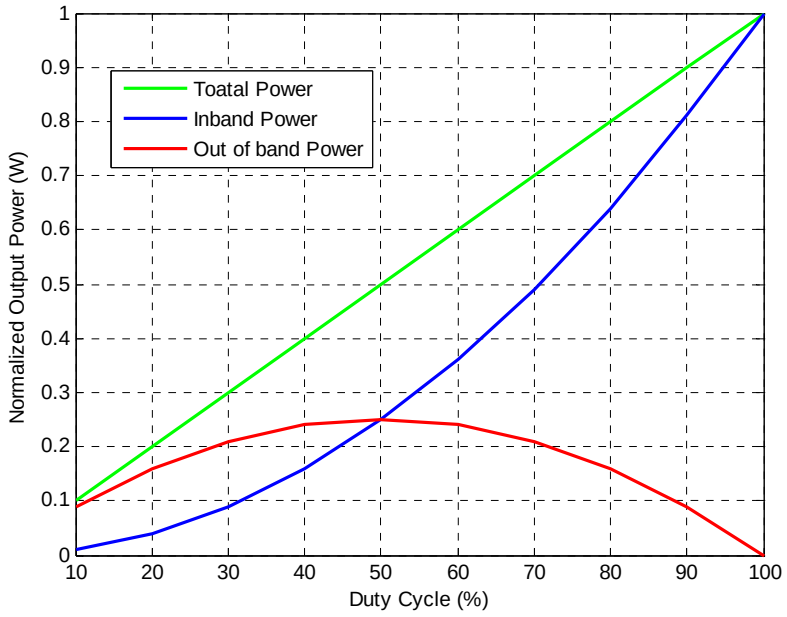


Fig 2.17: Different kind of output power over different duty Cycles in an ideal case.

Figure 2.17 shows that the total output power is directly proportional to the duty cycle whereas the in-band power is proportional to the square of the duty cycle. Due to this behavior, during the duty cycles which are below 50% the out of band power (red curve of fig. 2.17) is higher than the in-band power. This is one of the fundamental problems for this burst mode operation. However, as it is discussed before that the PWM waveform is a square wave with the varying duty cycles therefore, the average duty cycle of the PWM signals which are coded from two-tone or multi-tone signals can be determined. By that particular duty cycle one can easily determine the probable total output power and the in-band power (fig. 2.17) and the efficiencies (fig. 2.18) as well.

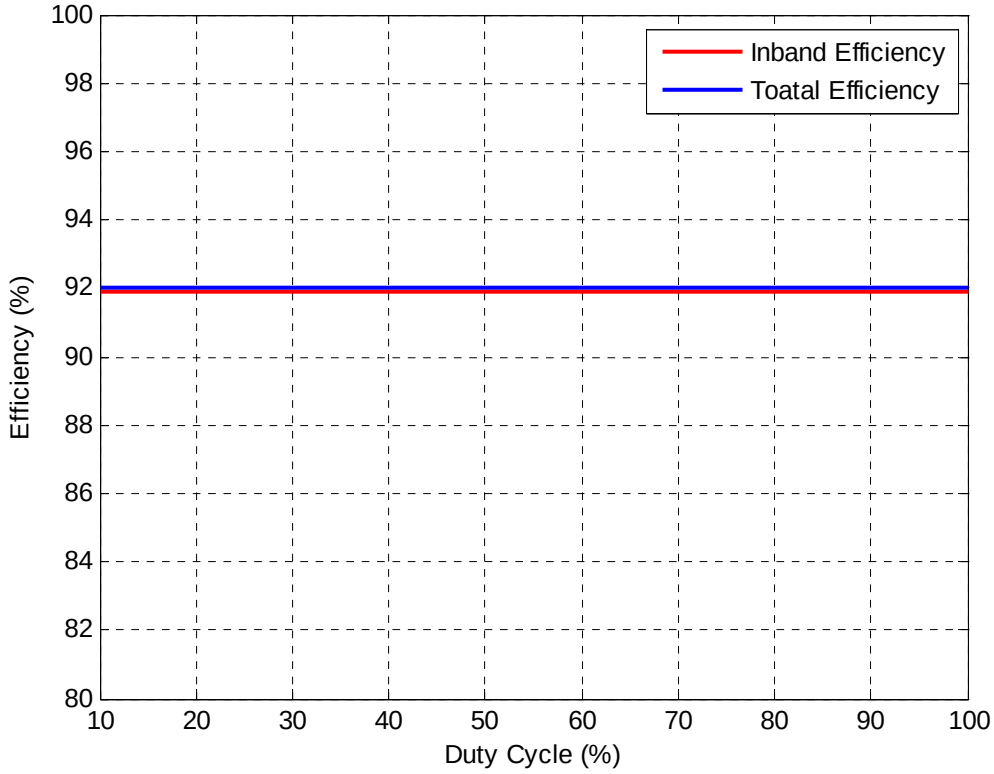


Fig 2.18: Efficiencies over different duty Cycles in ideal case.

Figure 2.18 shows the in-band efficiency (efficiency after filtering) and the total efficiency (efficiency before filtering) over the different duty cycles in an ideal situation. Ideally, the total consumed DC power before filtering and after filtering should follow the equation 2.3 and 2.4 respectively. Since the total output power before filtering and after filtering will also follows the above equations respectively therefore the flat efficiency over entire duty cycles can be achieved

in both cases (fig. 2.18). However, it is impossible to have such an output characteristic in the reality but it is the goal of a designer to accomplish that optimum operation.

By using equation (2.4) another very interesting and useful figure of merit can be obtained. It is shown below in figure 2.19.

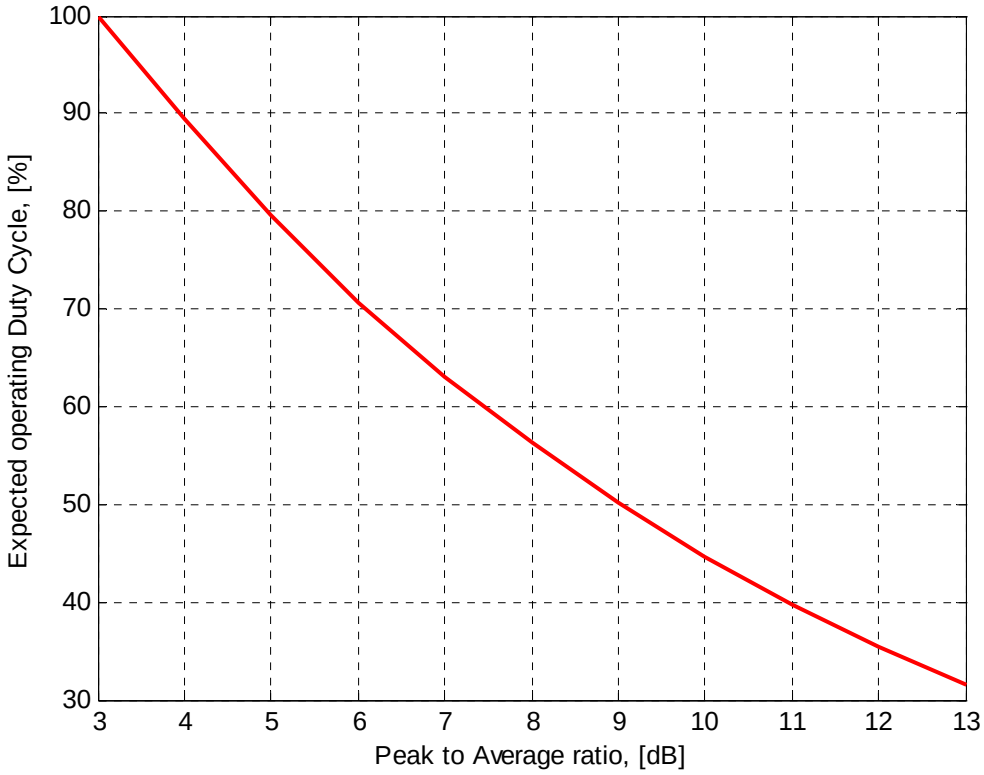


Fig 2.19: Effective Duty cycle over Peak to average Power ratio

Figure 2.19 shows the average operating duty cycle over the peak to average power ratio. If the baseband signal has peak to average power ratio of 6dB then the approximate operating duty cycle will be in the range of 70% and after determining the operating duty cycle we can have a feeling how will be the approximate output power and the efficiency for a particular PAP signal.

Chapter 3

Time Domain Simulations of Different SMPAs

There are mainly two categories of power amplifiers. One of the categories are the conventional amplifiers (Class A, Class B, Class C and Class AB) [11] and another are the Switched mode amplifiers (Class D, inv Class D, Class DE, Class E and Class F) [14,15]. A transistor can be operated in a saturation region (switched mode amplifiers) or in a linear region (conventional amplifiers) by controlling its operating point or the threshold voltage [11,14,15]. It is believed that the switched mode power amplifiers are more efficient than the conventional power amplifiers. For this reason this thesis work is focused only on SMPAs. Normally, the efficiency of these SMPAs is high because the active devices (transistors) are operated as a switch. Ideally, when the switch is on then the voltage is zero and a high current is passed through the switch and when the switch is off then the current becomes zero and a high voltage is found across the switch. Therefore, in an ideal SMPA no overlapping is occurred between the current and the voltage across the transistor and gives 100% efficiency (ideally).

In this section, ideal switches are considered for active devices and transient simulations in ADS are presented to learn how these types of SMPAs behave in a burst mode operation. The reason behind for this time domain simulation is to simulate these SMPAs very easily and also to compare the results with other simulation software like MATLAB SIMULINK. Because this burst mode operation is a new technique and there is no pallet for a burst source in any software therefore it is worth to compare the results between two simulators for having trust on the simulation results.

3.1 Class D (Voltage Mode Class-D) Amplifier:

Voltage mode class D (VMCD) amplifier or simply Class D amplifiers [15] are the first proposed switched mode amplifiers and are widely used in Audio applications since many years. This is a very simple circuit configuration which has push-pull configuration with a series LC resonator tuned for the fundamental component. Figure 3.1 shows the circuit configuration of a VMCD amplifier.

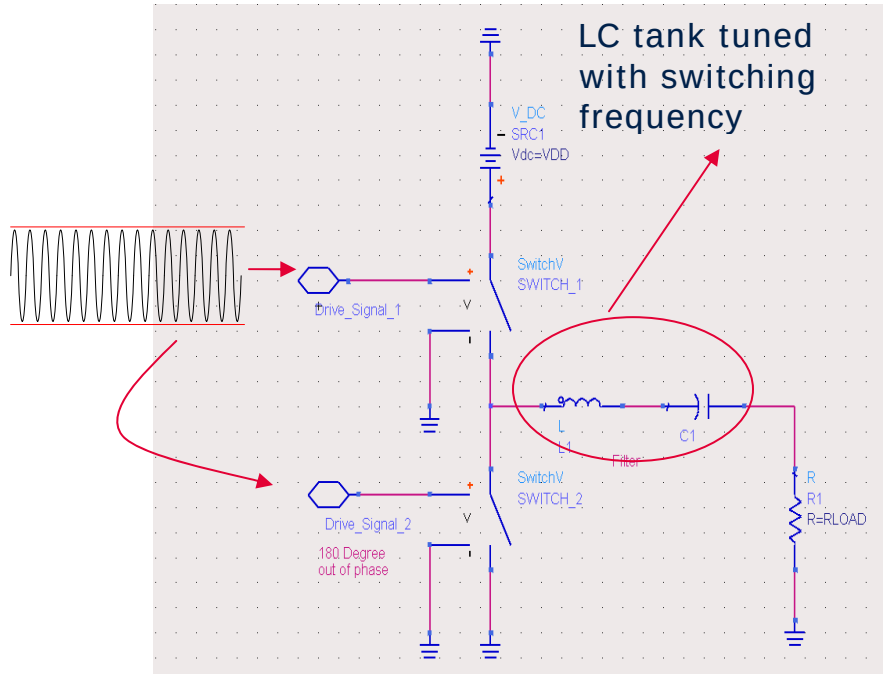


Fig 3.1: Ideal VMCD amplifier circuit.

In figure 3.1 the two ideal switches are alternately switched on and off by the driving signal and leads the device voltage switched between the VDD (supplied drain voltage) and zero (fig. 3.2 (blue curve)). When the switch is turned on then the switch current becomes half sinusoidal due to the resonator (LC tank) and when the switch is turned off then there is no current across it (fig. 3.2 (red curve)). Detail operation for this amplifier is described in Appendix A.

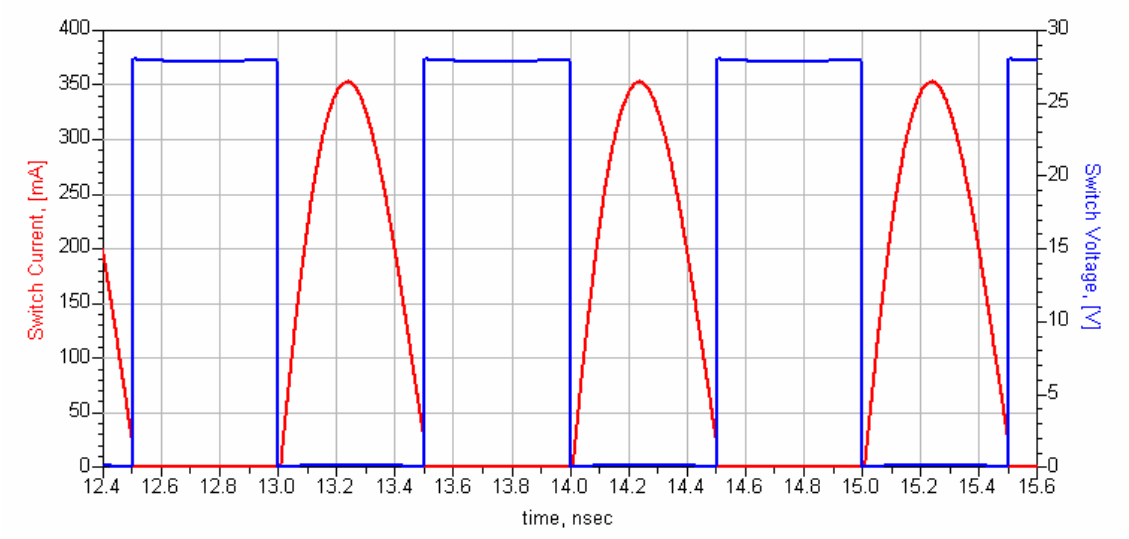


Fig. 3.2: Ideal Current and Voltage through the switch

The simulation results of the circuit shown in figure 3.1 are tabulated in the table 3.1. The results are obtained by using both simulator, ADS and MATLAB SIMULINK.

Parameters, VDD=28V, Rload=50Ω, R_on=0.5Ω, fc=1 GHz

Identity	Unit	Theoretical value	ADS Simulation	MATLAB Simulation
L1	[nH]	25.3	25.3	25.3
C1	[pF]	1	1	1
Isw, peak	[A]	0.353	0.3526	0.352
Idc, avg	[A]	0.112	0.112	0.112
Vsw	[V]	27.82	27.82	27.82
Iout, peak	[A]	0.353	0.3526	0.351
Vout, peak	[A]	17.65	17.64	17.63
Pin, DC	[W]	3.15	3.144	3.15
Pout	[W]	3.115	3.113	3.111
η, drain	[%]	99%	98.95%	98.75%

Table 3.1: Theoretical values and simulation results for the VMCD amplifier shown in fig. 3.1

Table 3.1 shows the good agreement between the theoretical values and the results from the both simulators. However, in real transistor there are some parasitic capacitors between the drain and source (Cds), the gate and source (Cgs) and also between the drain and gate (Cgd) of the transistor (fig. 3.3).

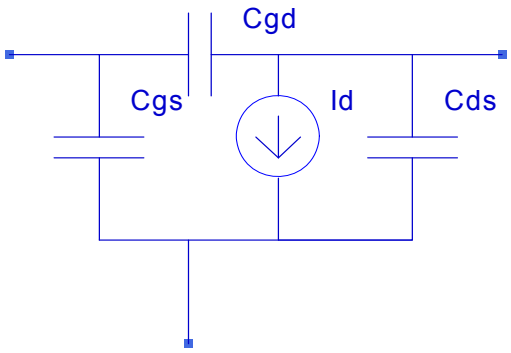


Fig 3.3: Real LDMOS Transistor model

Basically for the common-source configuration, the drain to source capacitor becomes the more dominant parasitic component of the device. This parasitic capacitor makes the VMCD amplifiers less efficient. During the switching operation (fig. 3.4 (a)), when one of the devices become turned off then the capacitor charged very quickly to the DC supply voltage VDD and the stored energy in Cds (fig. 3.3) can be described as [16]:

$$E_{ds} = \frac{C_{ds} V_{DD}^2}{2} \tag{3.1}$$

Furthermore, when the device becomes on, the parasitic capacitor found a path through the internal device resistance (R_{ON}) to discharge the stored energy in it and causes power loss. The discharged power loss, Pd could be described by the equation 3.2 [16].

$$P_d = \frac{C_{ds} V_{DD}^2}{2 f_s} \tag{3.2}$$

Where f_s describes the switching frequency.

Now from the equation 3.2 it is clear that the power loss is depend linearly on the operating frequency, f_s . A significant power loss is happened if the PA is operated with a higher frequency which causes lower efficiency. The current waveform across the switch of a VMCD amplifier (fig. 3.4 (a)) is depicted in figure 3.4 (b) by considering VDD=28V, R_on=0.5 Ω, Rload=50 Ω, Cds=6.4 pF, fc=1 GHz.

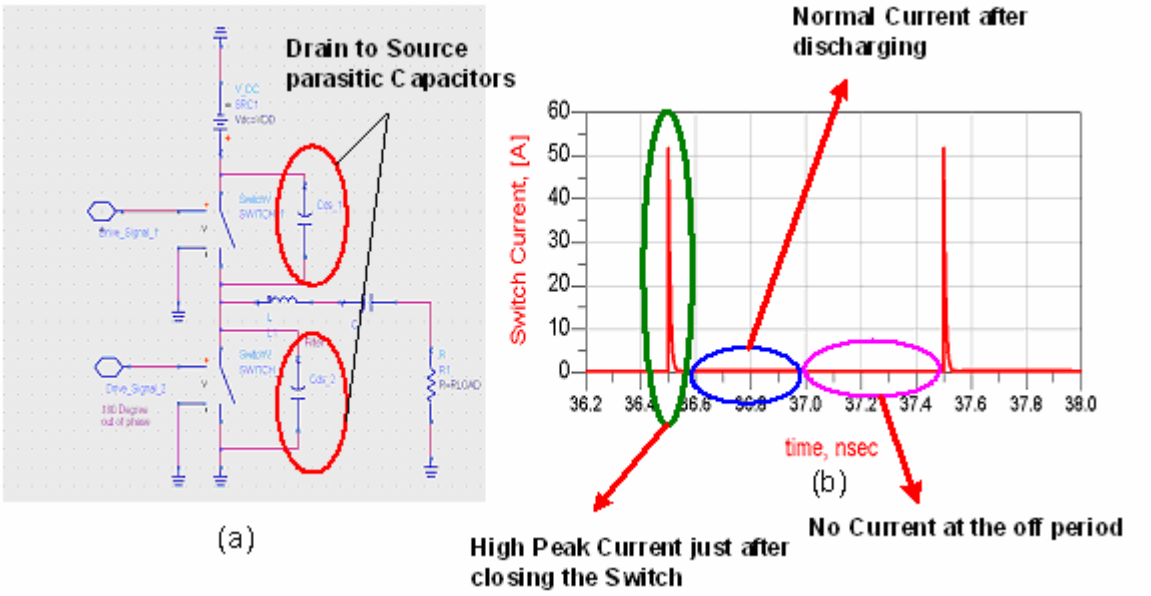


Fig. 3.4: (a) VMCD amplifier circuit with parasitic capacitor. (b) The corresponding current waveform across the switches.

The simulation results of the VMCD amplifier (fig. 3.4 (a)) with the parameters mentioned earlier are tabulated in table 3.2 below.

Identity	Unit	ADS Simulation	MATLAB Simulation
L1	[nH]	25.3	25.3
C1	[pF]	1	1
Isw,peak	[A]	55.517	55.95
Vsw	[V]	27.82	27.82
Iout,peak	[A]	0.352	0.352
Vout,peak	[A]	17.62	17.62
Pin,DC	[W]	13.59	10.38
Pout	[W]	3.113	3.107
η, Drain	[%]	22.89%	29.92%

Table 3.2: Simulation results of the VMCD amplifier (fig. 3.4 (a)).

It is clear from the above tables that efficiency goes down extensively after considering the parasitic capacitor across the device of the VMCD amplifier circuit. This problem is avoidable by providing the ZVS (Zero voltage switching) [16] during the switching operation. The ZVS can be achieved with the current mode class D or inverse class D amplifier circuit configuration [17].

3.2 Current Mode Class D (CMCD) Amplifier:

In this circuit configuration (fig. 3.5), the drain to source parasitic capacitor becomes a part of the resonator. Due to the resonance at the switching frequency, there is no voltage over the transistor at any switching instances and the wanted ZVS is achieved [17]. In this configuration, the switch voltage and current is the half sinusoidal and the square wave respectively (opposite to VMCD). Detailed operation principal of this circuit is described in Appendix B. Figure 3.5 shows the CMCD amplifier circuit and the table 3.3 shows the simulation results of this circuit for the parameters: VDD=28V, R_on=0.5 Ω, Rload=50 Ω, fc=1 GHz, Cds=6.4 pF, L2=L3= 3.96 nH and L1= 7.91 nH.

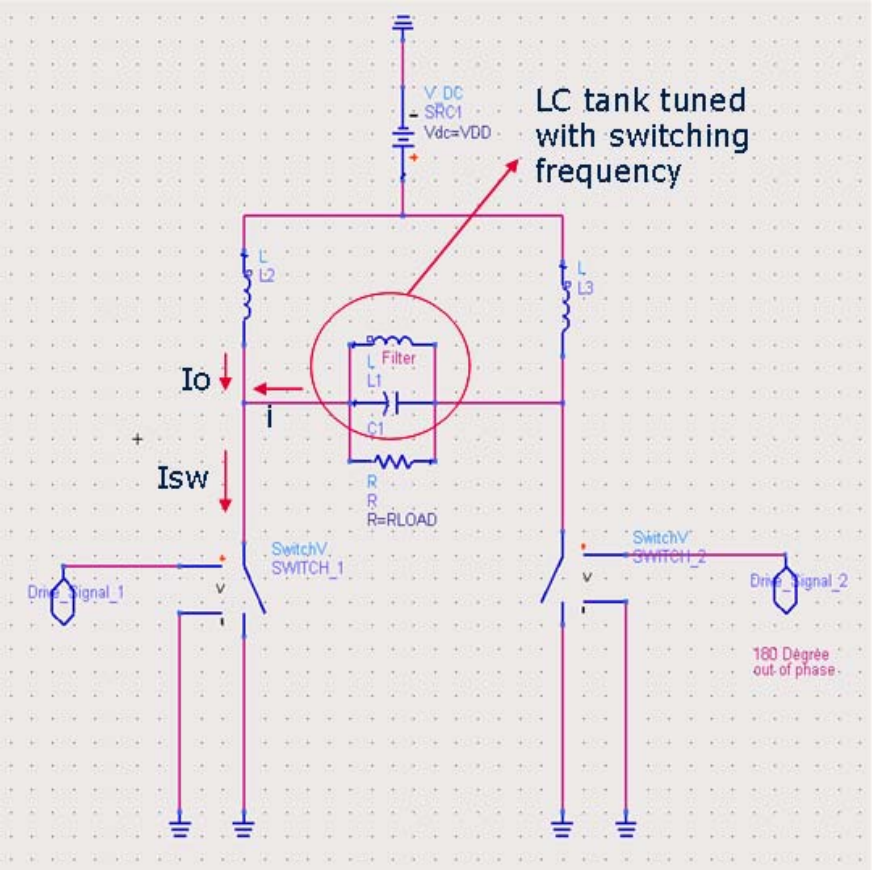


Fig 3.5: Current mode Class D amplifier.

Identity	Unit	Theoretical value	ADS Simulation	MATLAB Simulation
L (at resonance)	[nH]	3.95	3.95	3.95
C	[pF]	6.4	6.4	6.4
Isw, peak	[A]	5.2	4.89	4.89
Idc, avg	[A]	2.76	2.810	2.810
Vsw	[V]	87.92	89.40	89.40
Iout, peak	[A]	1.758	1.760	1.759
Vout, peak	[A]	87.89	87.98	88
Pin, DC	[W]	77.82	78.68	78.68
Pout	[W]	77.25	72.268	72.58
η, Drain	[%]	99%	91.84%	92.24%

Table 3.3: Simulation results for the Current mode Class D amplifier.

From table 3.3 it is clear that the CMCD amplifier has very good efficiency at the high frequency operation even by considering the parasitic capacitors across the switches. Since this amplifier gives the promising results (table 3.3) compare to the VMCD amplifier (table 3.2) in high frequency application therefore only the CMCD amplifier is investigated in the burst mode operation which is our ultimate goal.

3.3 Burst mode operation:

The basic principle of the burst mode operation is already been discussed in chapter 2. In this section some basic investigation is made by the transient analysis for the CMCD amplifier in burst mode operation. As it is mentioned before that the burst mode operation is a new technique and there is no pallet for the RF burst source in any simulation software therefore, in order to simulate a circuit in burst mode operation some simple techniques are applied in the both simulators, ADS (fig. 3.6) and MATLAB SIMULINK (fig. 3.8) for making the RF burst sources.

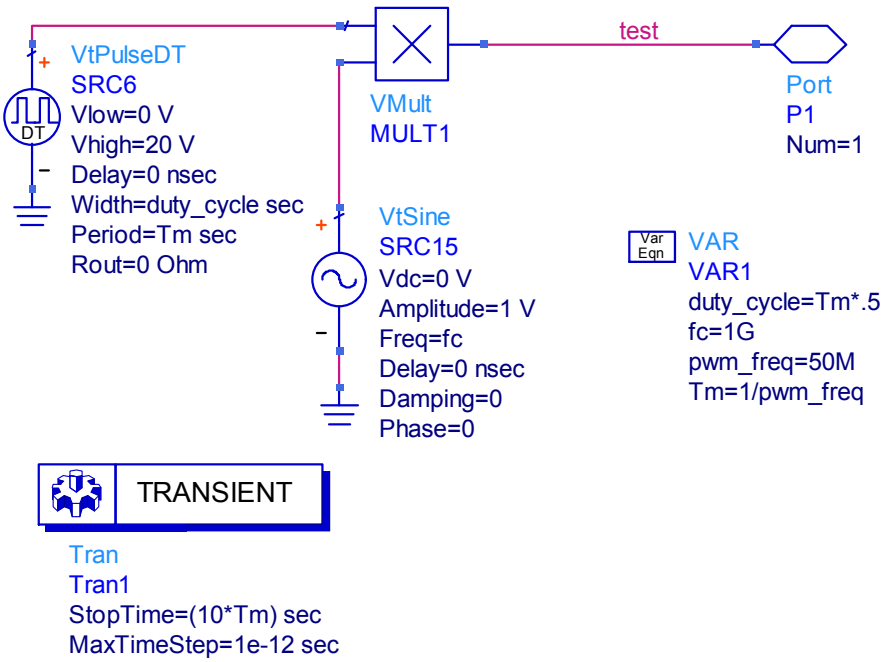


Fig. 3.6: The Procedure of generating a simple RF burst signal (constant duty cycle) for the transient analysis in ADS

Figure 3.6 shows the procedure of generating a simple RF burst signal (constant duty cycle) for the transient analysis in ADS. In that circuit a pulse waveform is multiplied with the high frequency (RF carrier) sinusoidal signal by a voltage multiplier. Figure 3.7 shows the generated RF burst signal by the circuit which is shown in figure 3.6. The intended circuit will be driven by this type of input signal.

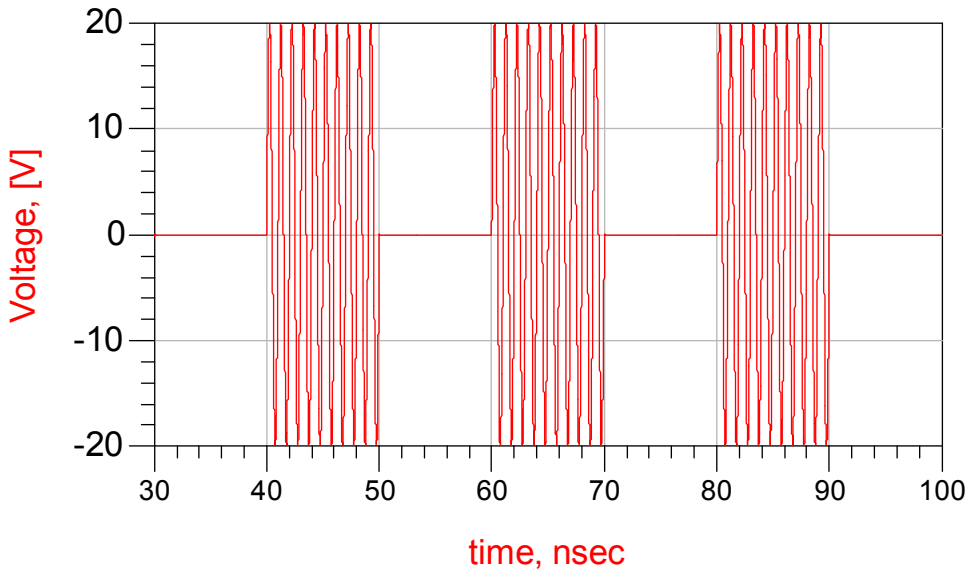


Fig 3.7: A simple RF Burst Signal (constant duty cycle) which is generated by the circuit shown in figure 3.6

To perform simulations in MATLAB SIMULINK the same procedure which is described for the ADS simulation is also applied to generate the RF burst signal. Figure 3.8 shows the circuit for generating the RF burst signal in MATLAB SIMULINK and figure 3.9 shows the output signal (RF burst signal) generated from the circuit shown in figure 3.8.

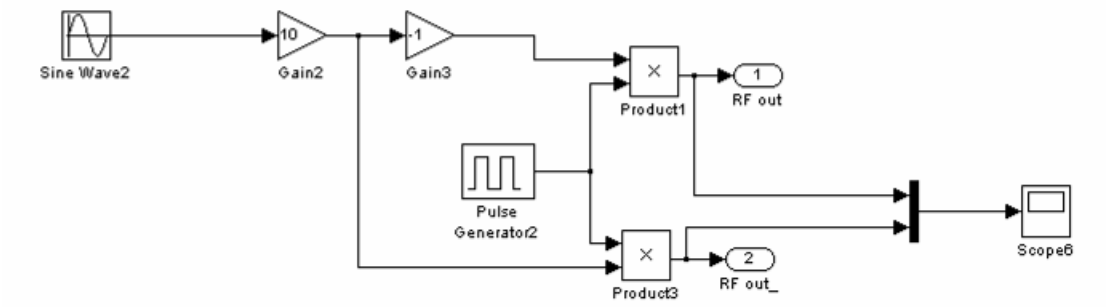


Fig. 3.8: The Procedure of generating a simple RF burst signal (constant duty cycle) for the transient analysis in MATLAB SIMULINK

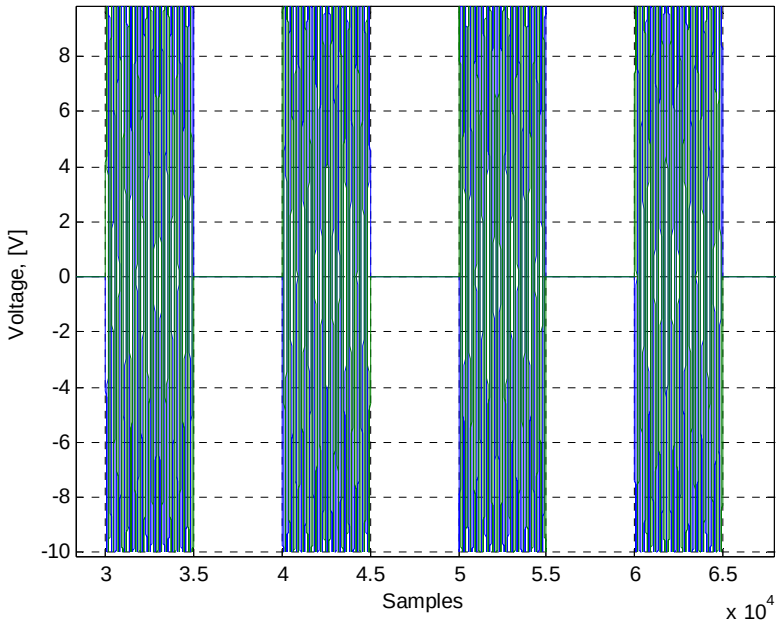


Fig 3.9: A simple RF Burst Signal (constant duty cycle) which is generated by the circuit shown in figure 3.8

Now, the CMCD circuit (fig. 3.5) is simulated in the ADS and the MATLAB SIMULINK environment by the generated RF burst signals (fig. 3.7 and 3.9). It is discussed in section 2.3 that the output of an amplifier i.e. efficiency, output power, etc. over the different duty cycles is the key test in burst mode operation to characterize the considered SMPA. For this reason the duty cycle test is performed to the ideal CMCD circuit (fig. 3.5) in both simulators. Figure 3.10 shows the output power and the efficiency over the different duty cycle.

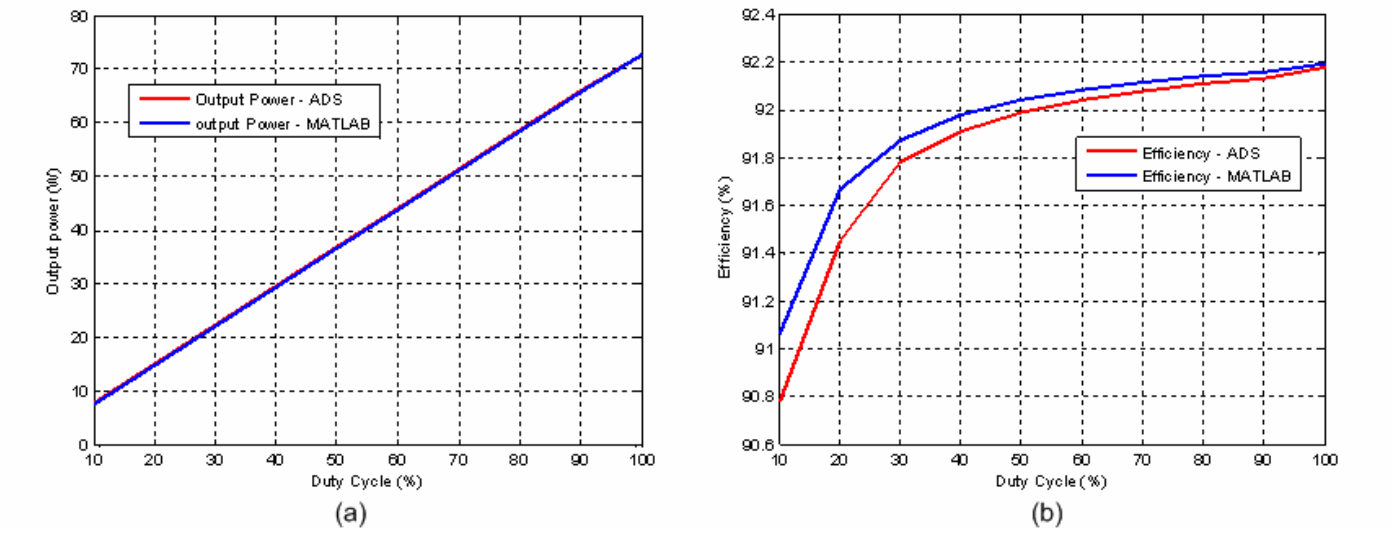


Fig. 3.10: Output from the ideal CMCD amplifier driven by the constant duty cycle RF burst signal (25 MHz PWM rate). (a) Output power vs. duty cycle. (b) Efficiency vs. duty cycle.

In figure 3.10 the ideal CMCD circuit (fig.3.5) is used with the parameters VDD=28V, R_on=0.5 Ω, Rload=50 Ω, fc=1 GHz, fpwm=25 MHz, Cds=6.4 pF, L2=L3= 3.96 nH and L1= 7.91 nH. The output power and the efficiency over the different duty cycles in figure 3.10 are obtained by the CMCD circuit while it is driven with the constant duty cycle RF burst signals. The output power over the different duty cycles in figure 3.10 (a) shows the good agreement with the theory (eqn. 2.3) and the ideal curve of output power as shown in figure 2.17 (green). The efficiencies are also almost flat over the entire duty cycles. However, the figure 3.10 shows the results from the SMPA where the band pass filter is not connected at the output of the SMPA. Since we are only interested to feed the baseband signal to the antenna therefore a band pass filter must be connected at the output of the SMPA to demodulate the RF burst signals. However, for the further investigations, the simulation in MATLAB environment is not considered anymore because so far from all the results it becomes clear that both simulators generate very similar results. Therefore, from now on all simulations presented in this thesis work are mainly done in ADS environment.

Anyway, to observe the output results after connecting the filter the transient simulation in ADS is performed and an ideal 6th order Butterworth band pass filter is considered which has 20 MHz bandwidth around the center frequency.

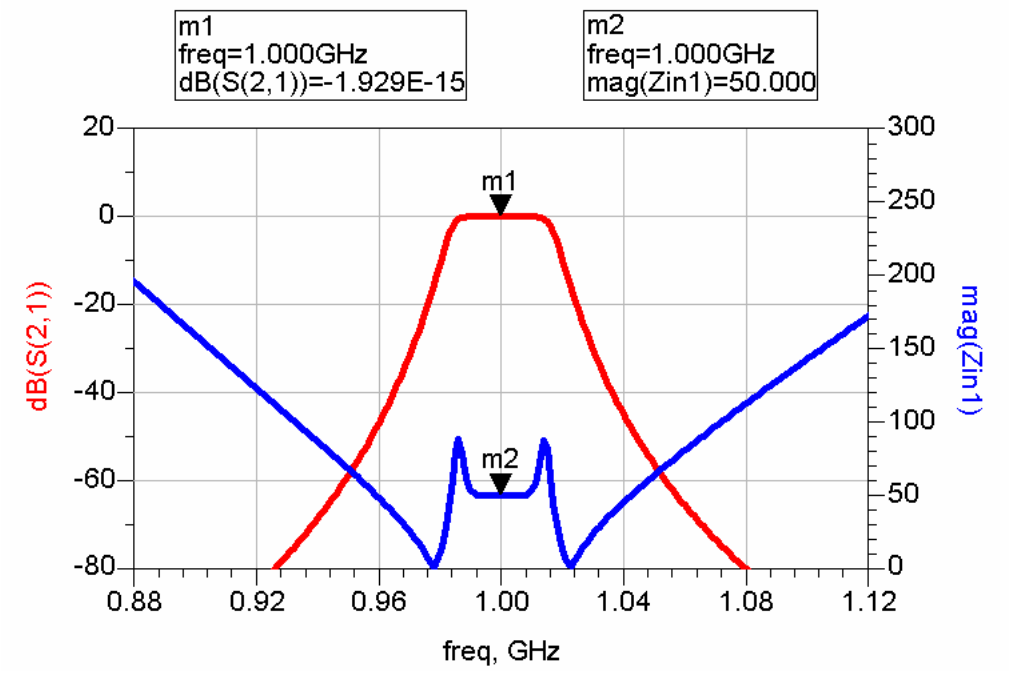


Fig. 3.11: Characteristics of the an ideal 20 MHz band pass 6th order Butterworth filter

Figure 3.11 shows the characteristic of the implemented band pass filter where the red curve shows the transmission characteristic and the blue curve shows the input impedance over the different frequencies.

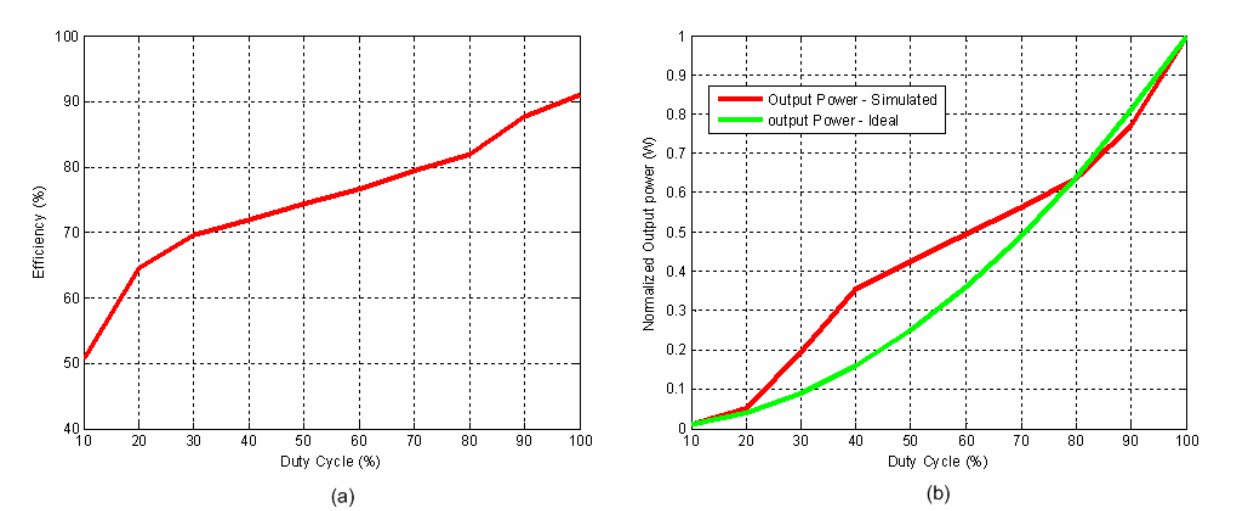


Fig. 3.12: The Output of an ideal CMCD amplifier after connecting the band pass filter at the output of the PA. (a) Efficiency vs. Duty cycle. (b) Output power vs. Duty Cycle.

Now, figure 3.12 shows the output results from the CMCD amplifier (fig. 3.5) with connecting the band pass filter (fig. 3.11) at the output of the PA. The parameters are used for this simulation, VDD=28V, R_on=0.5 Ω, Rload=50 Ω, fc=1 GHz, fpwm=25 MHz, Cds=6.4 pF, L2=L3= 3.96 nH and L1= 7.91 nH. Figure 3.12 (b) shows the output power over the different duty cycles but the results are not perfectly fit to the ideal or expected one (green curve). This dissimilarity may be caused by the transient simulation. The implemented band pass filter is made by the lumped elements and these elements take sometime to charge up in transient analysis and may produce some erroneous results. However, the tendency is quite similar with the ideal one. From figure 3.12 (a) it is also noticeable that the efficiencies over the different duty cycles are degraded extensively (compare with fig. 3.10 (b)) after connecting the filter. The particular reason for this degradation is difficult to describe properly. However, the switch voltage and current from the simulation can give some indication where the power is burning. Figure 3.13 and 3.14 shows the switch voltage and current and also the power before connecting the filter and after connecting the filter respectively.

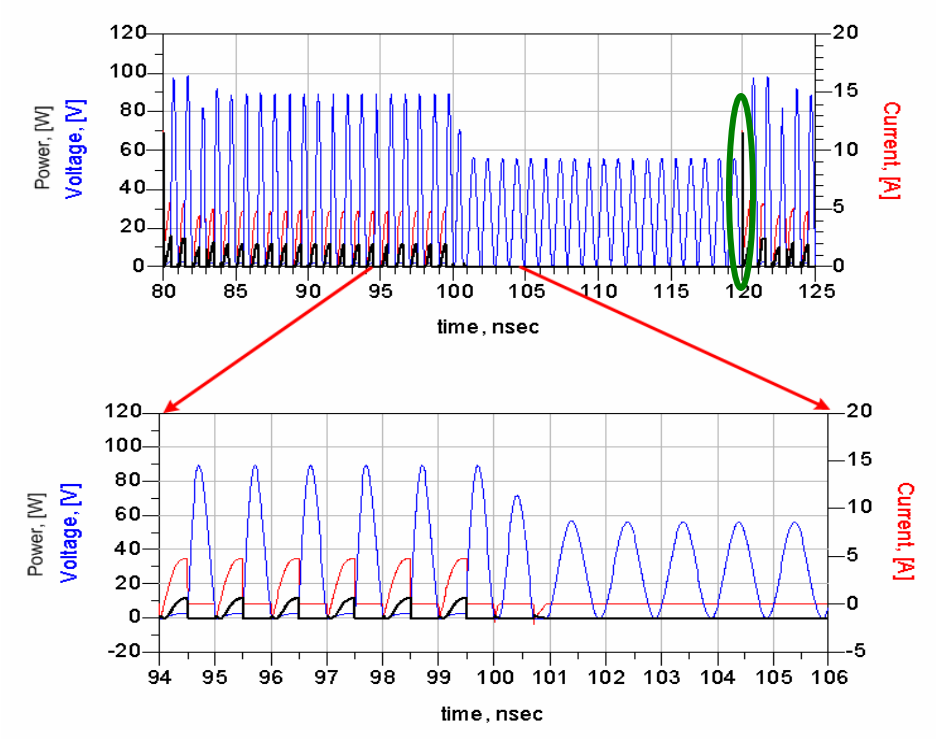


Fig. 3.13: The Voltage, current and the power dissipation across the switch before connecting the filter at the output of the SMPA.

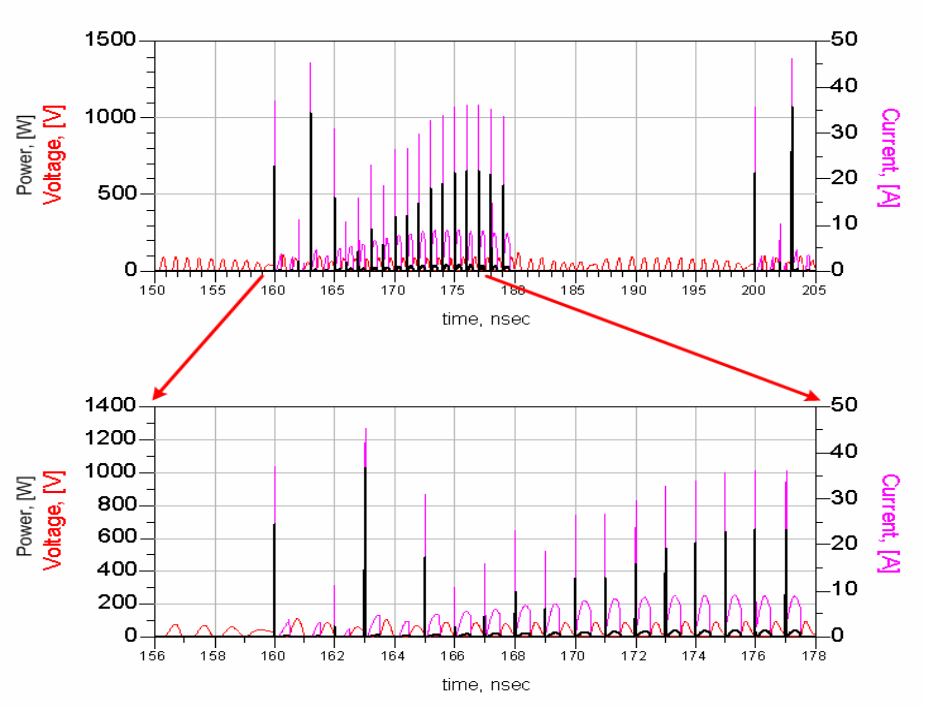


Fig. 3.14: The Voltage, current and the power dissipation across the switch after connecting the filter at the output of the SMPA.

From figure 3.14 it is clear that after connecting the filter the switch voltages and currents are partially overlapped and the high peak currents occur at every switching instances whereas the high peak currents occur only at the PWM transitions (green marked in figure 3.13) before connecting the filter. These high peak currents across the switches cause the loose of efficiency. Before connecting the filter at the output of the PA, all the output frequency components was seeing 50 ohm load but after connecting the filter only the in-band components are seeing 50 ohm and rest of the components are seeing very high load impedance and may be some portion of these components are reflected back to the switch. This could be one of the possible reasons for this corruption of the switch voltage and current and ruin the switching efficiency. Therefore, it is also clear from this simulation that to connect the filter in an optimum way is the big challenge of this burst mode operation to achieve the high efficiency.

However, figure 3.12 shows the 50% efficiency at the 10% duty cycle which is giving a very good indication for the high efficient transmission because in figure 2.19 (chapter 2), it was depicted that for a signal having 10dB 'back off'; the approximate operating point will be at 44% duty cycle and at this operating point the switching efficiency is more than 75% (fig. 3.12) which is more than above from the traditional RF power amplifiers.

Apart from the high efficiency issue there is another key issue for better transmission is the linearity. When the CMCD or the VMCD amplifier is driven with constant envelope signal then the two transistors alternately switched between the on and off state and always have the defined impedance. However, in burst mode operation, the CMCD amplifiers can give high efficiency but during the off period of burst signal (fig. 3.15 (blue marked)) when both switches become turned off then the impedance becomes undefined. As a result the whole circuit turns into a time variant system which will definitely introduce time-variant distortion.

In this concern, by slight modifying of the driving signal the VMCD circuit configuration could help to get rid off from this distortion. If the VMCD amplifier is driven with the RF burst signal and during the off period of the RF bursts (fig. 3.15 (blue marked)) the lower transistor becomes turned on (fig. 3.15 (red marked)) then the system will see same impedance as like constant envelope operation. Since it is a lower transistor and not directly connected to the DC source therefore no extra DC power will burn during that instance of time (the off period) and the efficiency will be same as by the normal RF burst signal. However, In a CMCD configuration both transistors are directly connected to the DC supply (fig. 3.5) therefore the proposed

technique (fig. 3.15) for avoiding the time-variant distortions in burst operations is not feasible for a CMCD amplifier.

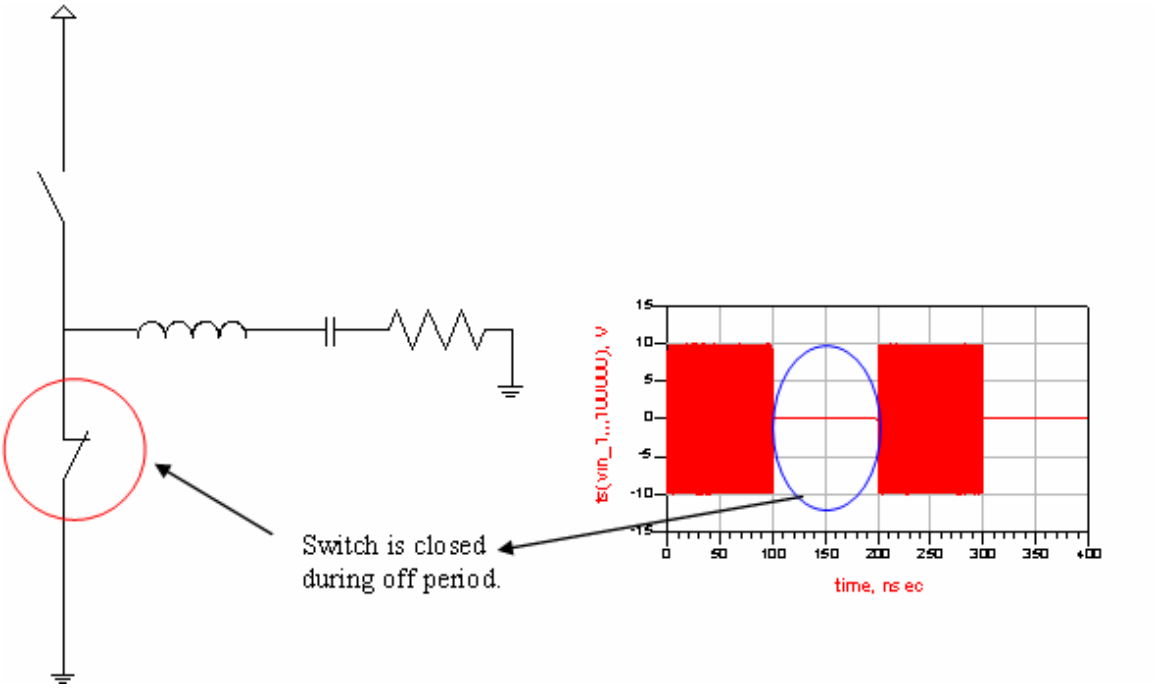


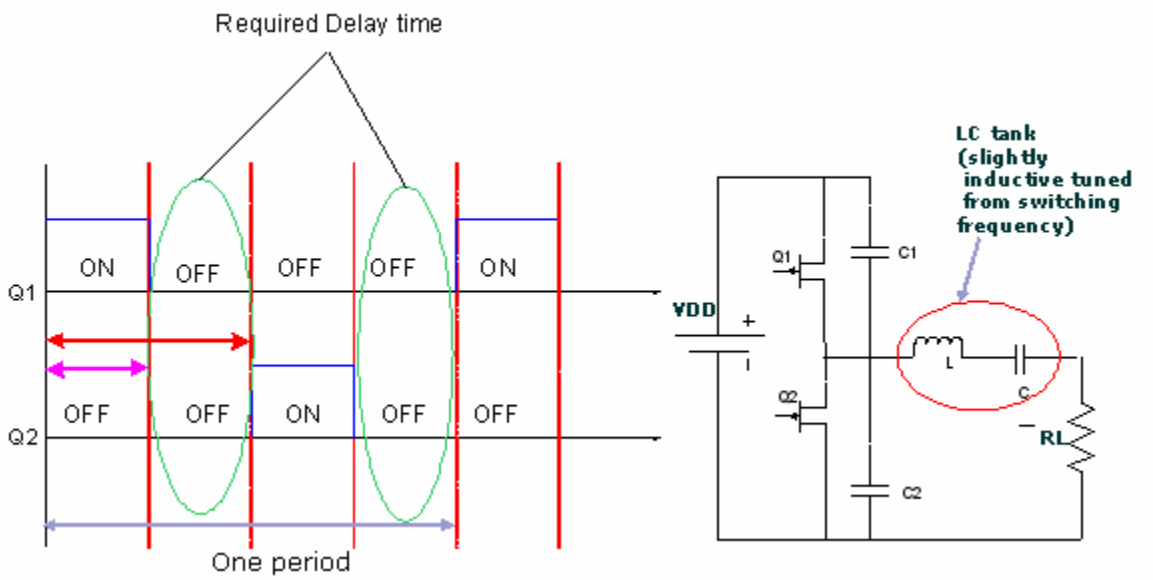
Fig 3.15: The Proposed operation principle for the VMCD circuit to avoid the time-variant distortions.

Now, the problem with the VMCD configuration is that it is a less efficient system for high frequency application (table 3.2). However, the efficiency can be improved for the VMCD circuit along with the Class E [15] switching which is another kind of amplifier known as Class DE [15, 16].

3.4 Class DE Amplifier:

This class of amplifier is the combination of class D and E. The circuit configuration is very similar to the traditional class D amplifier and the switching operation follows the class E operation while turn on. This circuit was first proposed in Russia [18] which was unknown to west for a long time. Later on, this circuit configuration for some applications is found [16, 20].

The main concept of this topology is that to assign certain delay time before closing the switch for achieving ZVS in VMCD configuration. By providing certain delay time the parasitic capacitor of the transistor can be discharged before the transistor becomes turned on.



(a) (b)

Fig 3.16: (a) Gate driving signal of Class DE. (b) Circuit configuration of Class DE.

Figure 3.16 showing the circuit configuration and driving signal of class DE. Usually, when a push-pull configured circuit driven by a continuous wave signal then half of the time of a switching period is conducted by one transistor and the other transistor is conducted in other half of the time whereas in class DE configuration the driving time period is different than the CW operation (fig. 3.16 (a)). Here the transistor is not conducted the half of the period but a percentage of that half of the period is conducted. Figure 3.16 (a) shows the transistors are conducting 50% (magenta arrow) time of that half of the period (red arrow).

Furthermore, in this circuit the LC tank is slightly inductive tuned from switching frequency. In all of the presented paper related to this topology is discussed to assign an extra shunt capacitor across the transistor to have class E switching. Since in high frequency operation, LDMOS has already the parasitic capacitors (fig. 3.3) across the drain therefore no need to adopt extra shunt capacitor. Just fine adjustment of inductance can give the optimum solution.

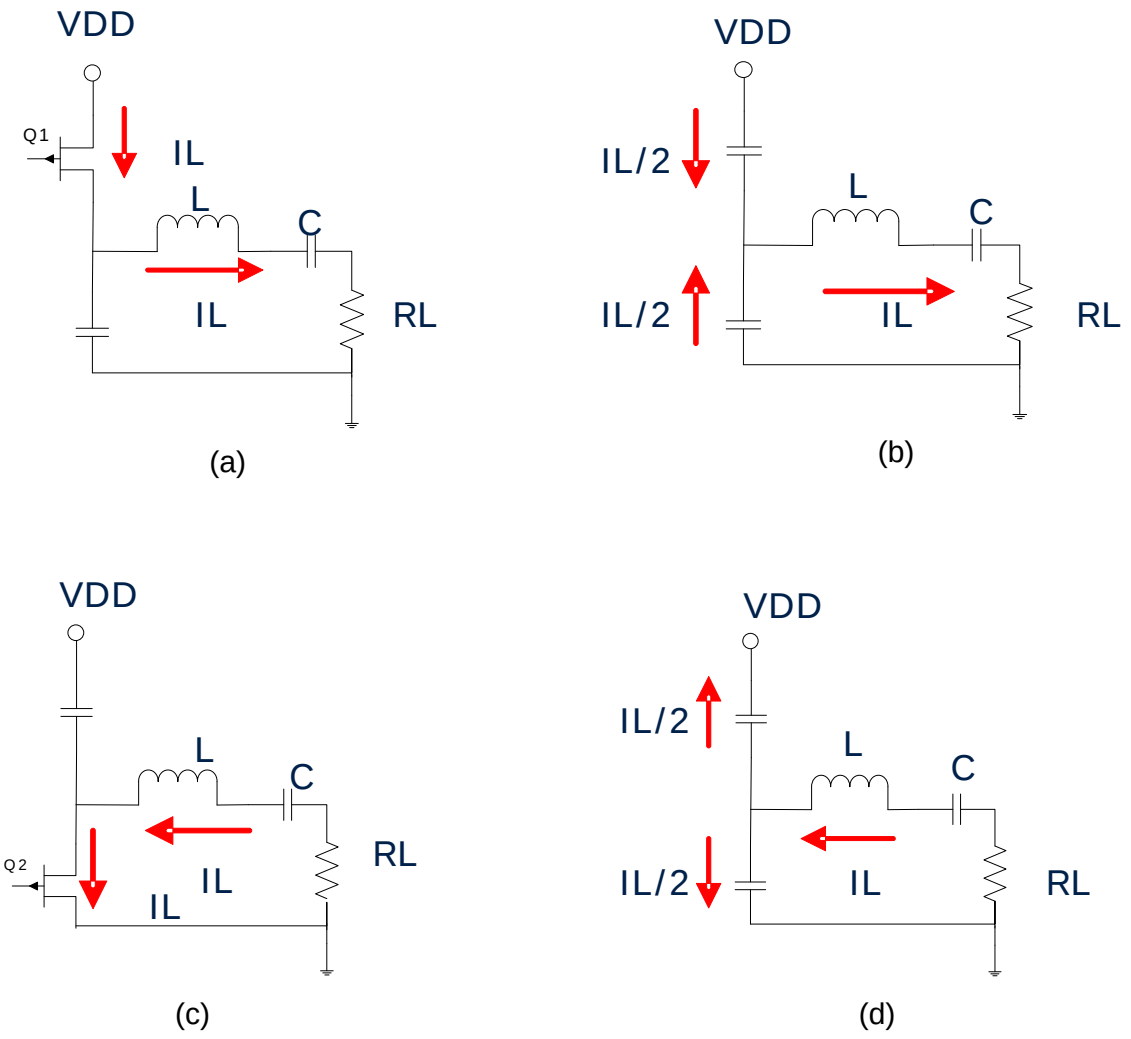


Fig 3.17: Operation of class DE over a full period.

IL= Load current.

Figure 3.17 is describes the operation at different time instances over one period. The circuit is derived by the signal which is depicted in figure 3.16(a). At the starting of switching operation, the upper device is on and conducting load current (figure 3.17(a)). Now, the upper device is turned off while the lower device is still off. Due to the LC tank which is slightly inductive tuned the current will continue to flow through the device capacitances. In this instance of time, the upper capacitor will charged up and the lower capacitor will discharged (figure 3.17(b)). Here, it is assumed that the both capacitances of the devices are equal. Therefore, current is equally divided between them. However, device capacitance can be different to each other which will discuss later. Anyway, now the lower transistor is turned on and upper device is still off. Since

the lower device capacitor fully discharged during the delay time therefore no voltage across the device at the instant of switched on, means ZVS is achieved. During this period of time current following in opposite direction through the load (figure 3.17(c)). At the end of this on period, the lower device turned off while the upper one is still off. The current starts to flow in the capacitors and charged the lower one as well as discharged the upper one (figure 3.17 (d)). This process is continued over whole operation and every time voltage across the device become zero or close to zero which has no significant loss and finally, this circuit configuration achieve high efficiency.

From the above figures and discussions it is apparent that the delay time has the great impact on charging and discharging of device capacitance and in order to achieve ZVS, the capacitor should be fully discharged before closing the switch. Also, it is clear that the load current has great influence on discharging issue which heavily depends upon load network. Figure 3.18 shows different scenario of drain voltage caused by the different delay time and load current.

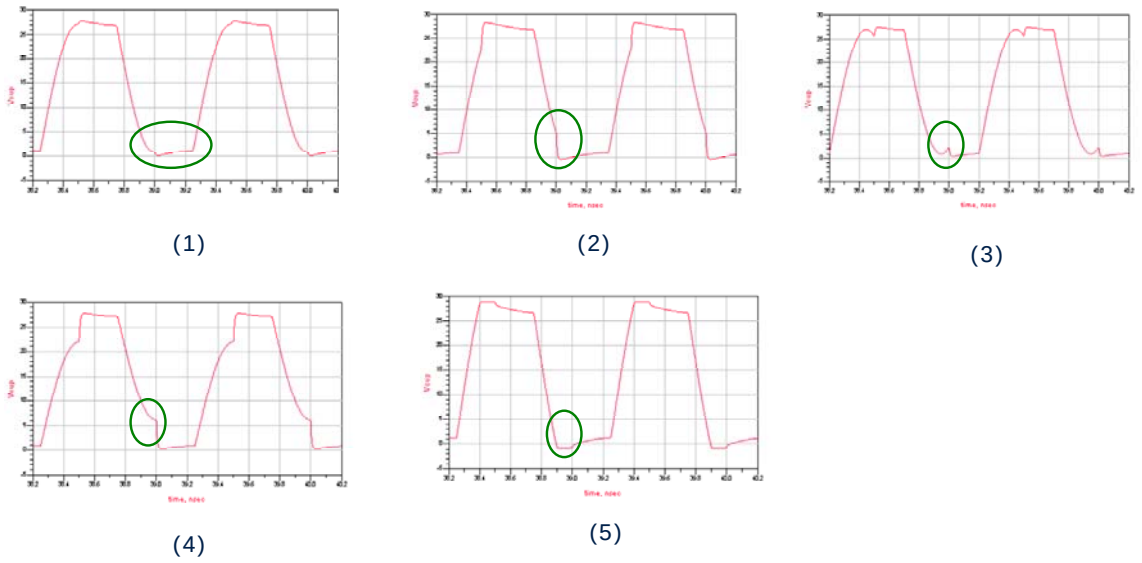


Fig 3.18: Effect of delay time. (1) Optimum operation. (2) Delay time is short. (3) Delay time is long. (4) Current is low to discharge the capacitor fully. (5) Current is high, which causes the voltage across the device to switch polarity.

At optimum condition the voltage reach to zero before closing the switch (fig. 3.18 (1)). If the delay time is too short (fig 3.18 (2)) or too high (fig 3.18 (3)), the voltage will not reach to zero and a certain amount of loss will occur. Likewise, if the current is too low it will fail to discharge the voltage (fig. 3.18 (4)).

Also, if the current is too high, the voltage will cross the zero twice (fig. 3.18 (5)) and reverses polarity across the device. The detail phenomenon for this operation is described very well in [16].

3.4.1 Load network

Apart from assigning a certain delay time the other technique of this configuration is to set the proper load network which is slightly inductive. The Class DE circuit can also be depicted as shown in figure 3.19.

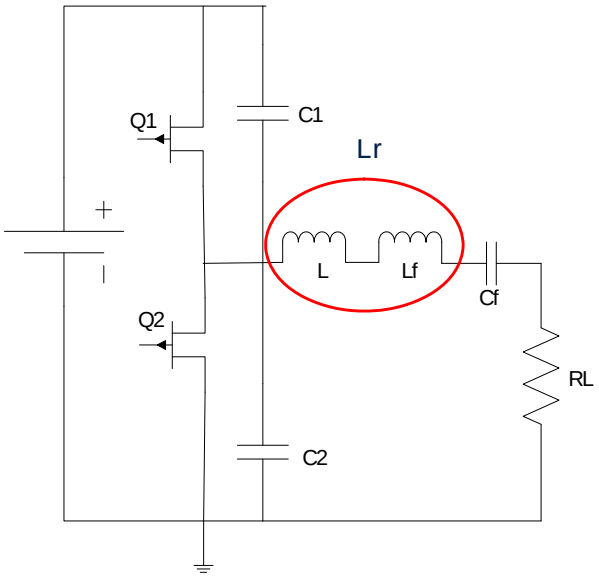


Fig 3.19: Clear configuration of Class DE circuit.

In [19] detail derivation of the equations for this circuit is described. However, the derived important equations are reviewed here. If C1=C2=C, then the approximate value of RL is

$$R_L = \frac{1}{2\pi\omega C} \tag{3.3}$$

The value of L can be determined by

$$L = \frac{\pi R_L}{2\omega} \tag{3.4}$$

Moreover, the value of Lr could be determined by

$$L_r = Q\frac{R_L}{\omega} \tag{3.5}$$

Where, ω is Switching frequency and Q is usually 10 or above.

Once the values of L, Lr and RL are determined then the values of Lf and Cf can easily be calculated by the equation 3.6 and 3.7.

$$L_f = L_r - L \tag{3.6}$$

$$C_f = \frac{1}{L_f \omega^2} \tag{3.7}$$

Also, from Lr the required resonance frequency can be determined. By setting all calculated parameter values and with the drive signal having 50% of delay time (fig. 3.16) the results obtained from the Class DE circuit are presented in table 3.4 and figure 3.20 and 3.21.

Parameters, VDD=28V, C1=C2=6.4pF, fc=1GHz, R_on=0.5 ohm, Q_factor=10.

Delay Time [nS]	**'ON' Time [nS]**	**Lr [nH]**	**Cf [pF]**	**RL [Ω]**	**Output Power [W]**	**η [%]**
0.25	0.25	5.31	4.77	3.97	9.103	94

Table 3.4: The simulated results for Class DE Amplifier.

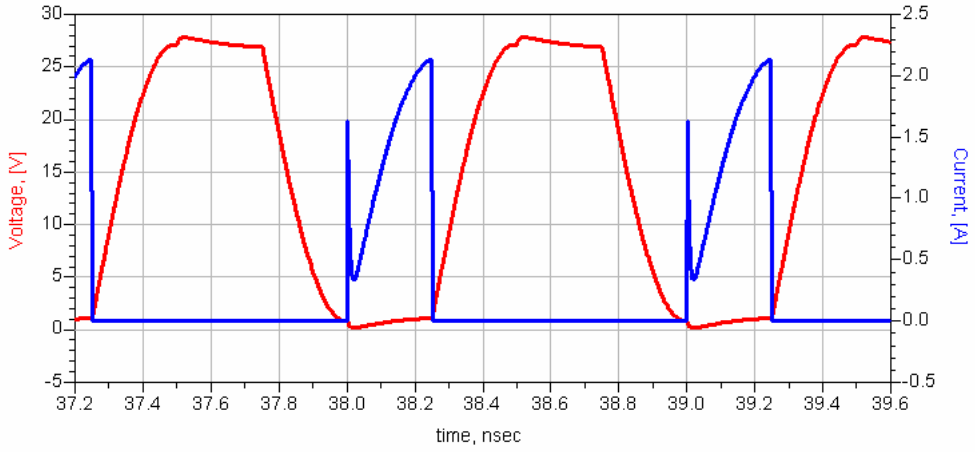


Fig 3.20: The drain voltage and current over one switch for the Class DE amplifier

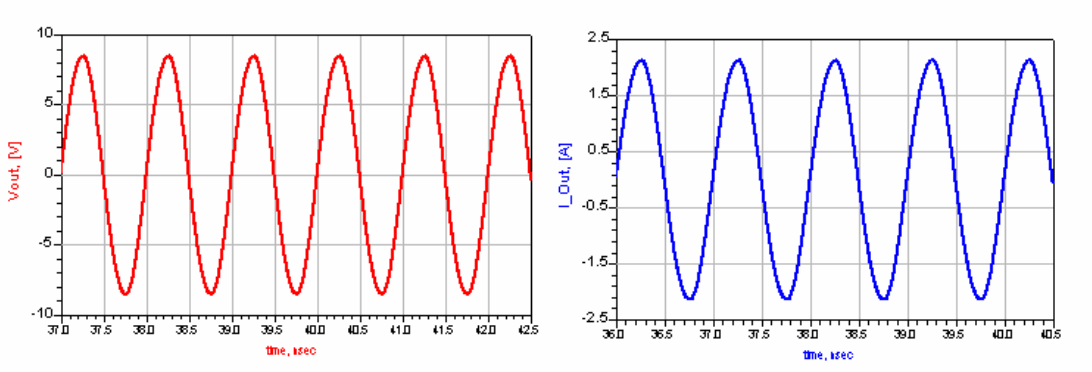


Fig 3.21: Output Voltage and current.

So far, the discussion in this work and the reference papers was only for 50% of delay time. Therefore, the open problem was to find out the possibilities of implementing different delay times in this configuration. In order to make it meaningful, some assumptions are made and an equation is developed from [20].

From equation 3.4 and 3.5 the resonance frequency can be determined easily. Alternatively, resonance frequency can be determined arbitrary which should slightly below than switching frequency. Once the resonant frequency is determined then the LC constant can also be determined. After calculating these values, the following equation [3.6] can be used to find out the optimum load resistance for the different delay time.

$$R_L = Z_0 \times \sqrt{\frac{t_{delay} \times \left\{ 2 \times \left(\frac{f_s}{f_r} - \frac{f_r}{f_s} \right) \right\}}{\pi C_{eq} Z_0} - \left(\frac{f_s}{f_r} - \frac{f_r}{f_s} \right)^2} \qquad (3.6)$$

Where, $Z_0 = \sqrt{\frac{L_r}{C_f}}$, $C_{eq} = C_1 + C_2$, *fs* representing the Switching frequency and *fr* representing the resonance frequency. Table 3.5 shows results for different delay time by using equation 3.6.

Parameters, VDD=28V, C1=16.4 pF, C2=6.6 pF, fs=1 GHz, fr= 920 MHz.

Delay Time [%]	'ON' Time [nS]	Lr [nH]	Cf [pF]	RL [Ω]	Output Power [W]	η/Ron 0.5Ω [%]	η/Ron 0.1Ω [%]
50	0.25	3.67	8.15	2.89	14.53	91	99
40	0.30	2.51	11.94	2.28	22.63	88	95
30	0.35	2.45	12.24	1.98	23.81	85	96.7
20	0.40	1.73	17.3	1.13	32.21	76	94
10	0.45	1.23	24.46	2.3	38.98	73	82

Table 3.5: Time domain simulated result for different delay time.

In above simulation, C1 is chosen much higher than C2 because the source for upper device in Class DE or VMCD configuration is not directly connected to the ground. Therefore, the gate to source capacitor (fig.3.3) becomes more dominant than the drain to source capacitor. However, from table 3.5 it is clear that the high efficiency is also achievable at the different delay time by adjusting the load network.

By keeping resonance frequency constant and varying L and C a number of choices can be made for the load resistance. Also, by fine tuning of load resistance the optimum efficiency can be achieved. From the simulation, decision is taken that the value between $\pm 2\Omega$ of calculated load resistance (eqn. 3.6) can provide a good efficiency. Figure 3.22 shows different values of the load resistance, output power and efficiency by varying the inductance (Lr) for 50% delay time.

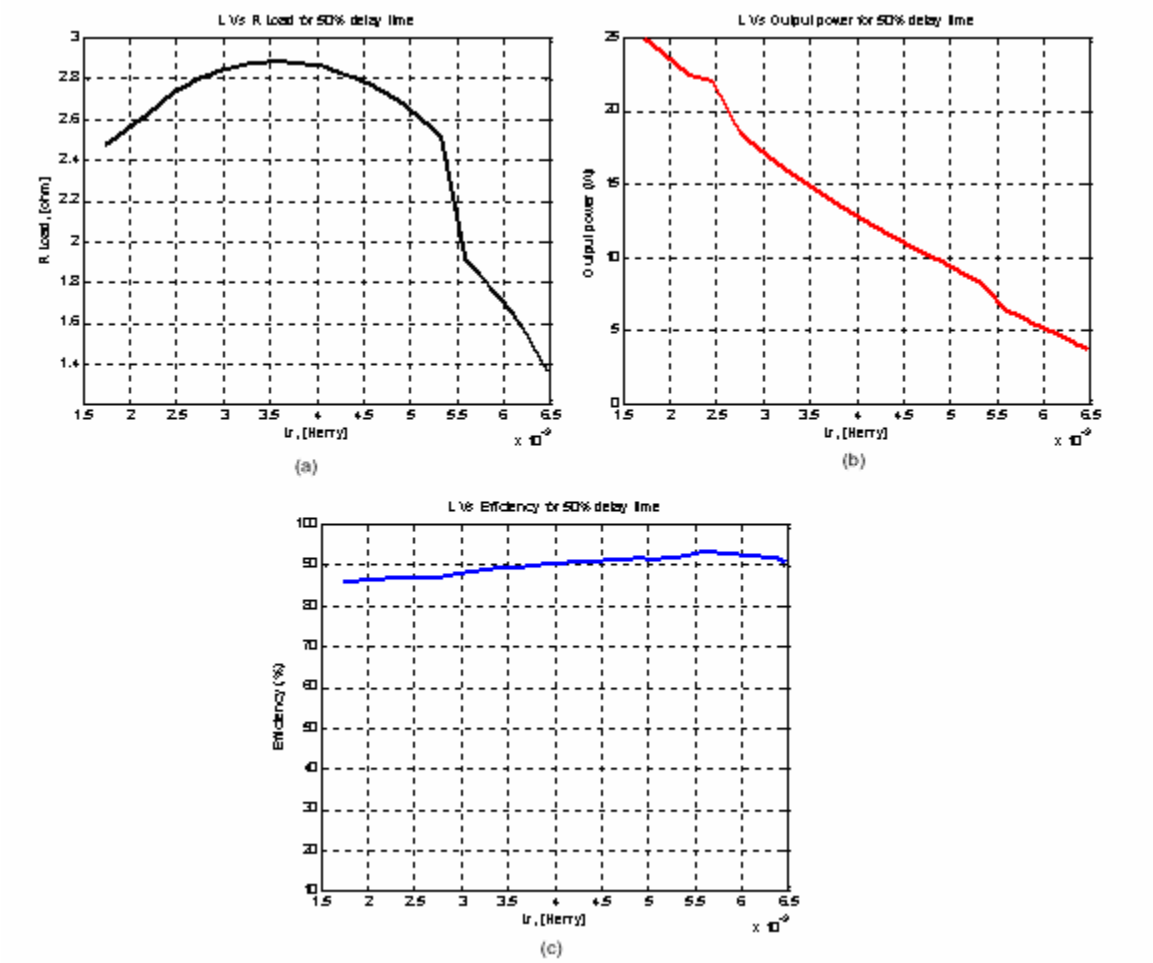


Fig 3.22: (a) Load resistance vs. inductance (L). (b) Output power vs. inductance (L). (c) Efficiency vs. inductance (L).

From figure 3.22 it is clear that a number of options can be made for the load resistance and the output power by varying the value of inductance while the efficiency can keep more or less same for all the choices.

Some interesting simulation is also done to see the impact on efficiencies if the delay time and the load resistance are changed while keeping all other parameters is constant. For example if a load network is designed for a particular delay time and for some reasons the value of the load resistance is changed or the delay time is altered then what will be the impact on efficiencies.

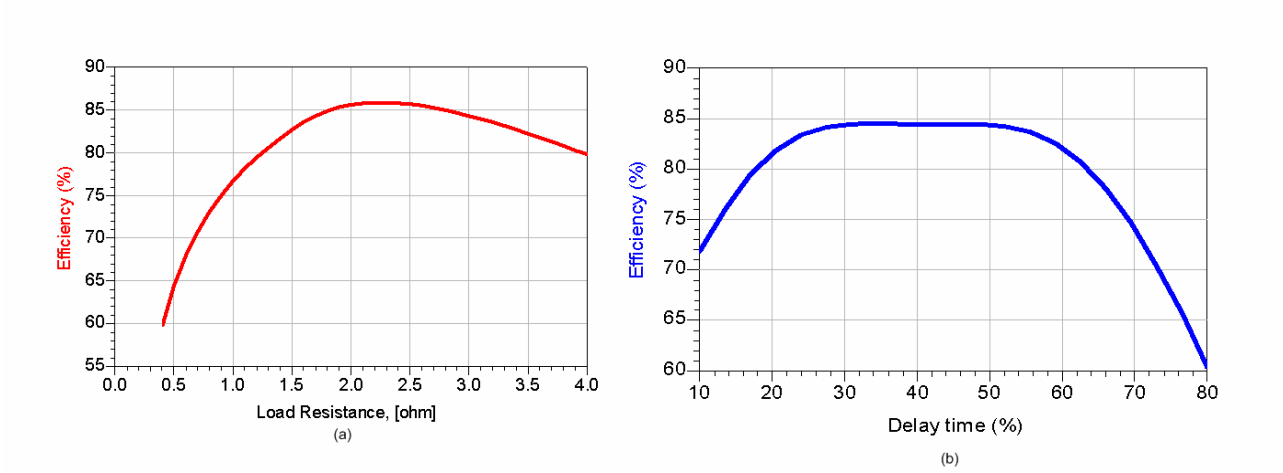


Fig. 3.23: (a) Efficiency vs. Load resistance (b) Efficiency vs. Delay time, for a fixed load network of particular delay time.

In figure 3.23 the optimum load for the delay time of 30% is considered. From table 3.5 the optimum load is about 2 ohm for 30% delay time. Now, this load resistance and the delay time is changed for few percent and observed the impact of efficiencies. The figure 3.23 shows that at the optimum point the highest efficiency is achieved (table. 3.5) and efficiency is degraded away from the optimum point. However, of course there are some flatness of efficiencies for plus or minus of few percent over the delay time and the load resistance but not for large variations.

Another interesting issue could be, to observe the frequency (switching frequency) selectivity over the efficiencies. Figure 3.24 shows that the efficiency is quite flat within a bandwidth of 100 MHz around the center frequency.

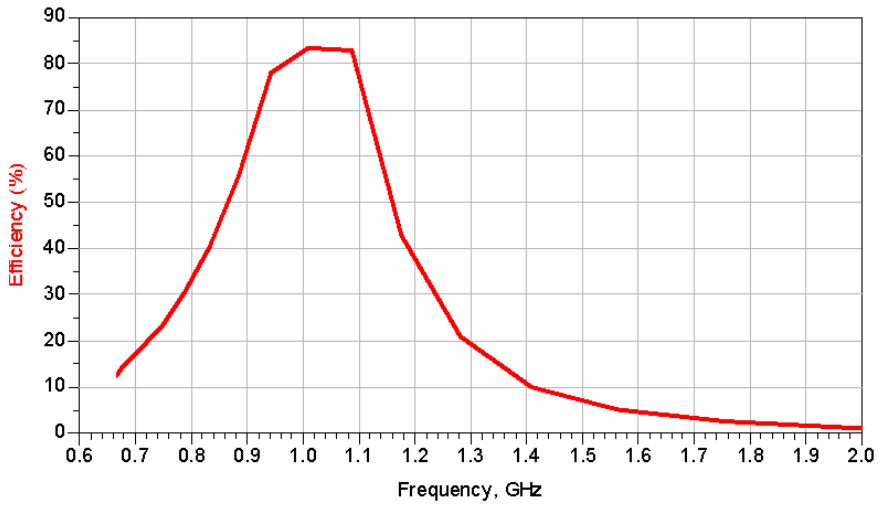


Fig 3.24: Frequency Vs Efficiency.

Up till now from all the results that we get from the Class DE amplifier, it seems that this circuit configuration could be used at high efficiency application. Therefore this class of amplifier is simulated also for the burst mode operation which was the main goal to investigate this configuration.

3.4.2 Class DE – Burst operation

The intention of investigating the Class DE circuit configuration for burst operation is mentioned in last portion of sec. 3.3 of this chapter. Therefore without having introduction only the results are discussed here. There are two types of driving condition are considered one is Case 1 (fig. 3.25 (a)) which is normal burst operation and another is Case 2 (fig. 3.25 (b)) where the lower switch is closed during the off period. Figure 3.25 shows the two types of driving signal.

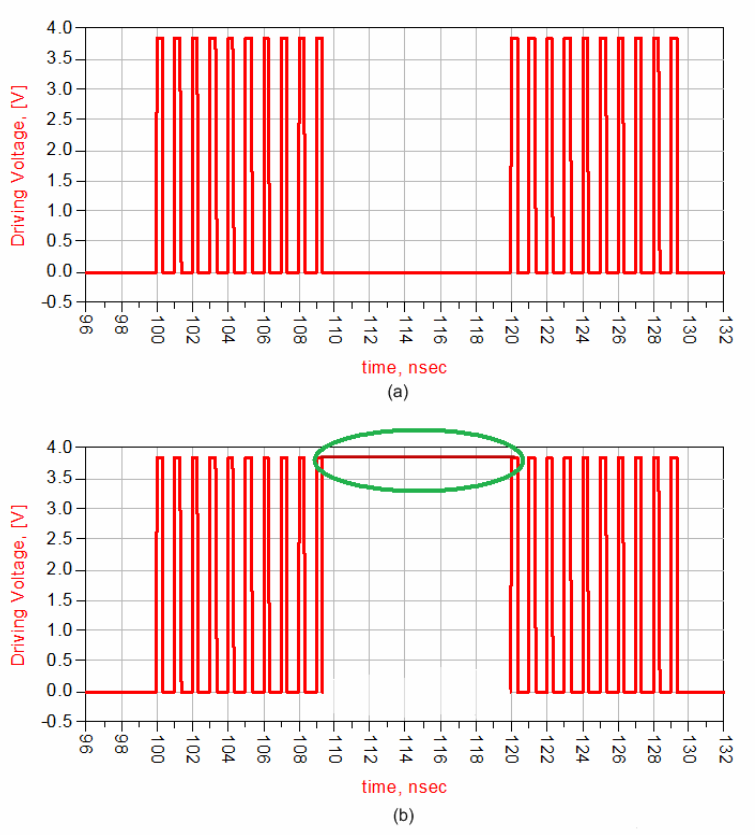


Fig 3.25: (a) Normal Burst operation. (b) The lower switch is on during the off period (green marked)

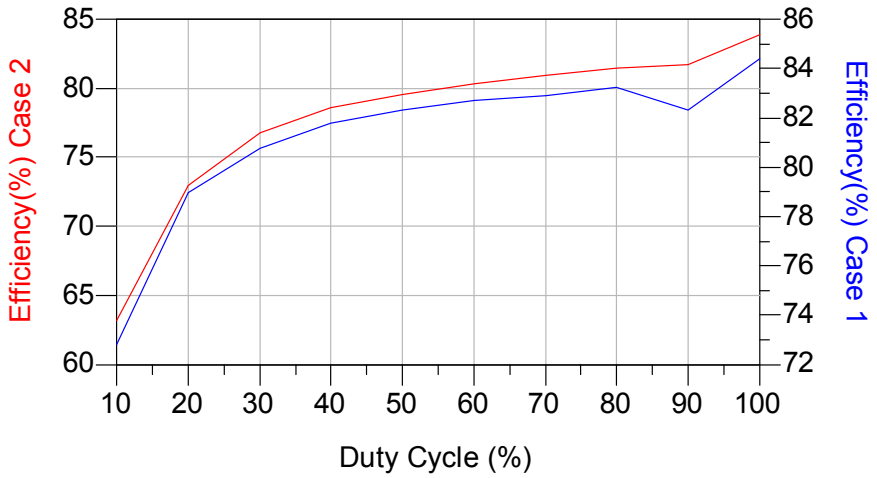


Fig 3.26: Comparison of Efficiency for two different driving signals.

Figure 3.26 depicts the efficiency over different duty cycles for two different switching configurations by considering the parameters of VDD=28V, R_on=0.5 Ω, RL=1.71 Ω, fc=1 GHz, delay time=15 ns (30%),fpwm=25 MHz, Ceq=23 pF, Lr=2.45 nH and Cf= 12.24 pF. The efficiencies over different duty cycles of the Case 2 are almost fit to efficiencies for the Case 1. This result could be interesting to investigate further with this circuit configuration for burst mode operation. However, the efficiency goes down compare to CMCD configuration (fig. 3.10) due to high current occurrence at the transitions of PWM frequency (fig. 3.27). Here the ZVS is not achieved in these transitions.

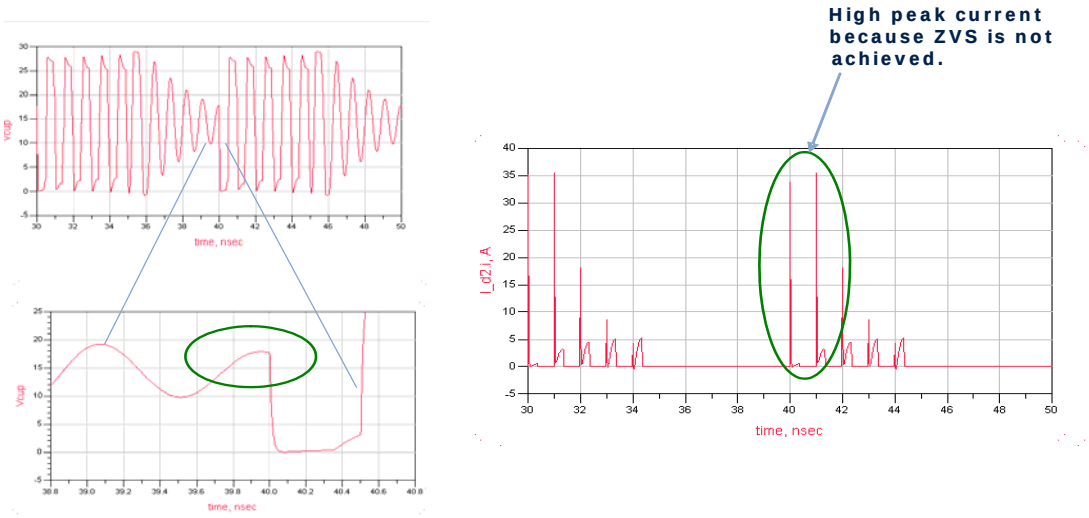


Fig. 3.27: The switch voltage and current and also the possible cause of losses for a Class DE circuit while driven with the RF burst signal

Figure 3.27 shows the switch voltage and current and also the possible cause of losses for a Class DE circuit while driven with the RF burst signal. However, from all the discussion of the Class DE configuration, conclusion can be made that this proposed class of amplifier could be an interesting candidate for a high efficient system; efficiency is above 80% within a reasonable bandwidth; very simple circuitry and possibility to increase linearity for burst mode operation. On the other hand, there are some disadvantages as well, *i.e.* really very low load resistance to make a real output matching network and suffering with high peak current at the drain in a burst operation.

Furthermore, a big problem associate with the circuit configuration of Class D (fig. 3.1) or Class DE which is not discussed yet that the availability of suitable devices for the upper switch. A **p-channel** device is required for the upper switch in order to operate the circuit in safe mode. But currently the available device which is for high frequency and high power application is only the **n-channel** LDMOS and there is no **p-channel** LDMOS. However, for a low frequency and low power application the CMOS could be used where both the p-channel and n-channel devices are available to implement for a class D type circuit configuration.

Chapter 4

Simulation Setups in Harmonic Balance

Now these days, circuit simulations by the software become basic requirement of any circuit design. Since this bust mode operation is a new technique for future transmitter architecture, hence a new simulation setup is required. Because, it is mentioned in previous chapter that there is no burst mode signal source palette in ADS or any other software thus to develop a simulation setup in harmonic balance is a key issue in this work. Harmonic balance is a highly accurate frequency domain analysis technique for obtain the steady-state solution of non-linear circuits and systems [21]. Therefore, it is more logical to analyze any RF and microwave circuits in Harmonic balance simulation rather than in transient simulation because these circuits are naturally handled in the frequency domain. To generate a burst signal, the simulation setup in transient analysis was not so difficult but in Harmonic balance it is much more complicated as it requires frequency domain multiplication.

4.1 The RF burst signal of Constant duty cycles:

As like time domain simulation setup here also need to multiply a pulse wave signal with a sinusoidal wave as a carrier to generate the RF burst signal. The simple multiplier which is used in transient analysis that can not be used in harmonic balance simulation since it cannot handle the frequency components. In ADS there are some nonlinear blocks. One of these blocks is used for multiplying two signal waves in order to generate the RF burst signal.

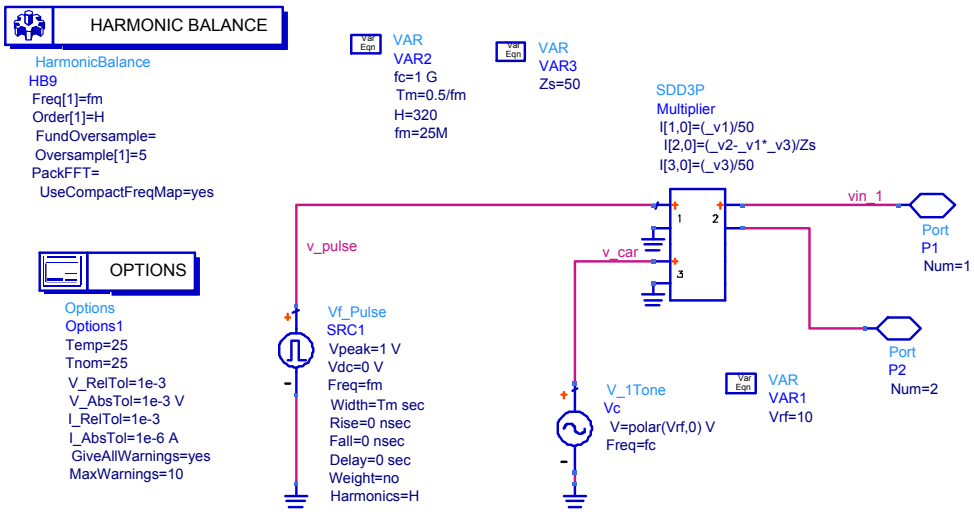


Fig. 4.1: Simulation Setup in ADS for generating the constant duty cycle RF burst signal

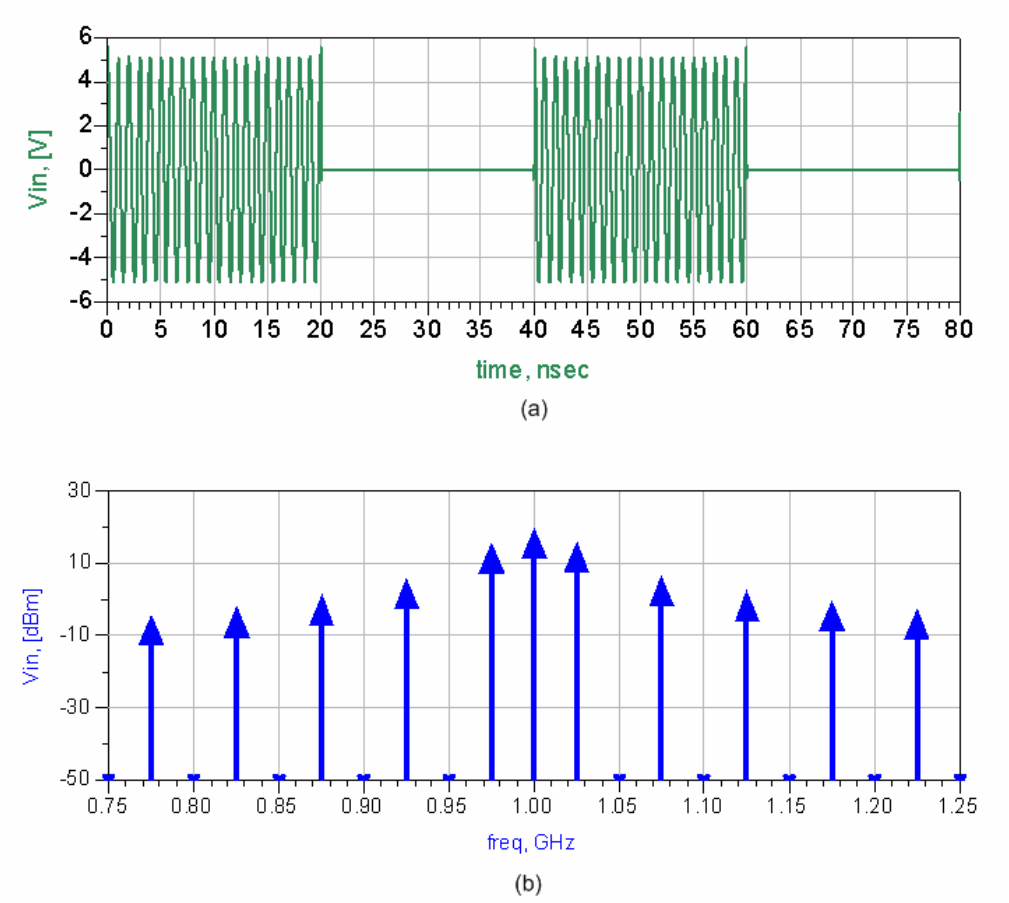


Fig. 4.2: The Constant duty cycle RF burst signal. (a) Time domain (b) Frequency domain

Figure 4.1 illustrates the simulation setup for generating a constant duty cycle RF burst signal and figure 4.2 depicts the output signals from the simulation setup. A RF burst signal with the duty cycle of 50% and the PWM rate of 25 MHz is generated in this setup. By varying the width and the frequency of the pulse wave we can change the duty cycle and the PWM rate respectively. Attention must be paid on voltage level of the carrier frequency ('Vrf' in figure 4.1) since it is determined the input RF power level for the Device Under Test (DUT).

Since there is only constant information in the constant duty cycle RF burst signal therefore it is worth to developed a two tone simulation setup to have feeling of the different output results (efficiency, nonlinear distortions etc.) from the PA while driven with a modulated signal.

4.2 Two-tone Burst signals:

To generate a two tone burst signal, the technique which is described in sec 2.2 is applied. In order to do this a triangular wave and a sinusoidal signal is considered. The sinusoidal wave is compared with the triangular wave to generate a pulse width modulated signal while the frequency of the triangular wave determines the PWM rate and the sinusoidal wave is considered as a baseband signal. To shift the pulse width modulated signal up to the desired carrier frequency, the PWM signal is multiplied with the corresponding carrier frequency.

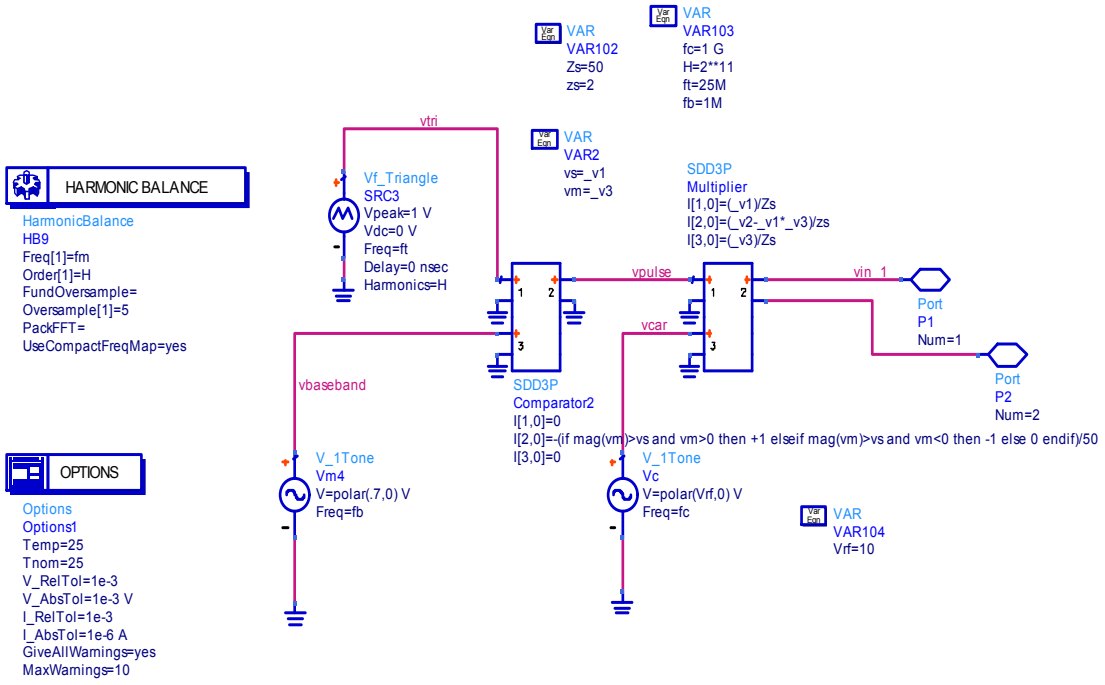


Fig 4.3: Simulation setup in ADS for generating a two-tone RF burst signal.

Figure 4.3 depicts the simulation setup in ADS for generating a two-tone RF burst signal where the PWM frequency and the baseband frequency are considered as 25 MHz and 1 MHz respectively. In order to avoid non-linear distortion around the band of interest which is produced by the PWM modulator, the PWM frequency is normally chosen between five to ten times higher than the bandwidth of the baseband signal. As like previous setup here also the voltage level of carrier frequency (Vrf) determined the input power level to the DUT. Figure 4.4 shows the output signals from the modulator which is shown in figure 4.3.

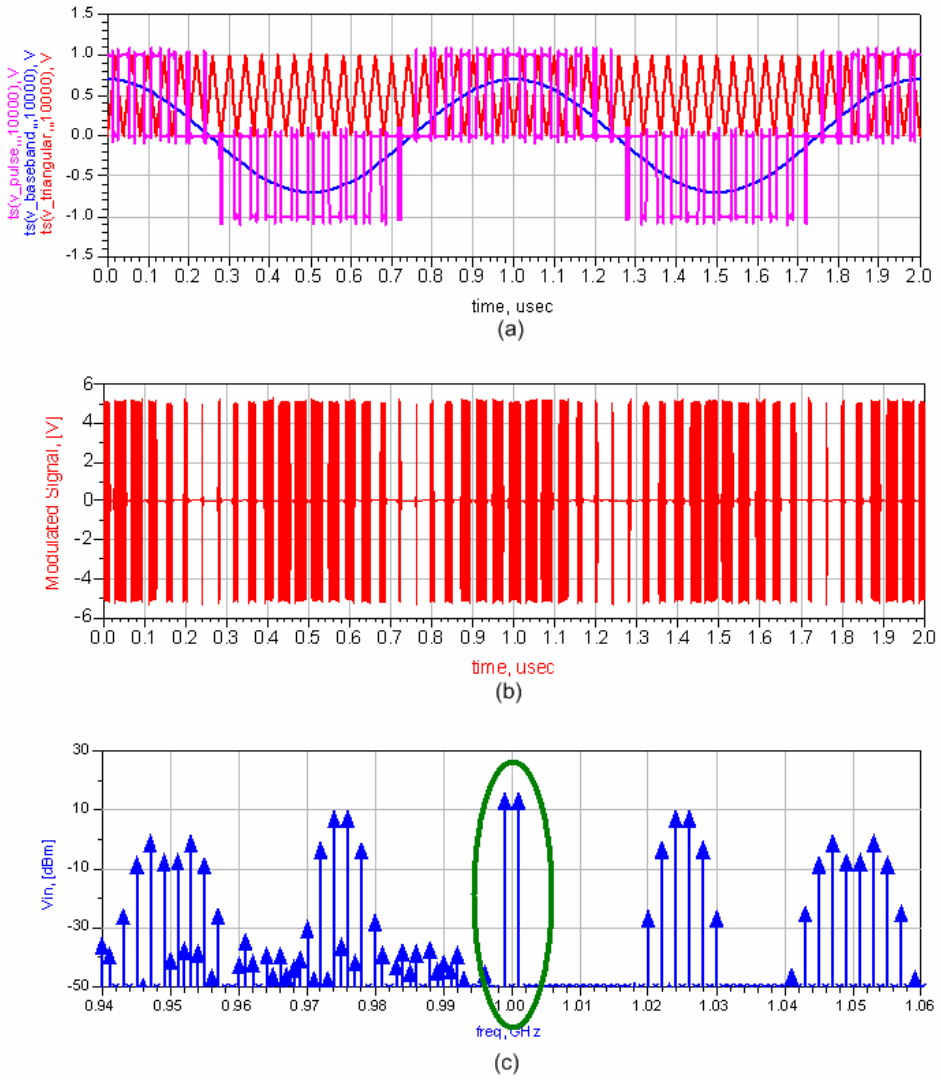


Fig 4.4: (a) Generation of the PWM Modulated signal. (b) Modulated RF burst signal in time domain. (c) Frequency domain representation of the RF burst signal.

Figure 4.4, (a) shows the way of generating a PWM signal and (b) shows the modulated RF burst signal which is obtained by multiplying the PWM signal (magenta curve fig. 4.4(a)) with the RF carrier. In figure 4.4 (c) the frequency domain signals of the modulated RF burst signals is presented where the spectral components which is marked with green oval is in the band of interest and rest of the frequency components are modulation products. It is also clear from this figure that the dynamic range is reasonably high and we can make some primary investigations of any desired DUT.

However, one question may be raised here that the considered base-band signal is a pure sinusoidal signal and which is simply one tone component in frequency domain but why it is

called two-tone burst signal. Basically, any signal in frequency domain can be represented in two ways one is as a single sided representation (considered only positive axis) and the other is double sided (considered also the negative axis). Therefore, when a baseband signal is up converted to the desired carrier frequency then the components from the negative axis came into the positive axis and this is how the considered single tone baseband signal ended up as a two-tone signal (fig. 4.4 (c)).

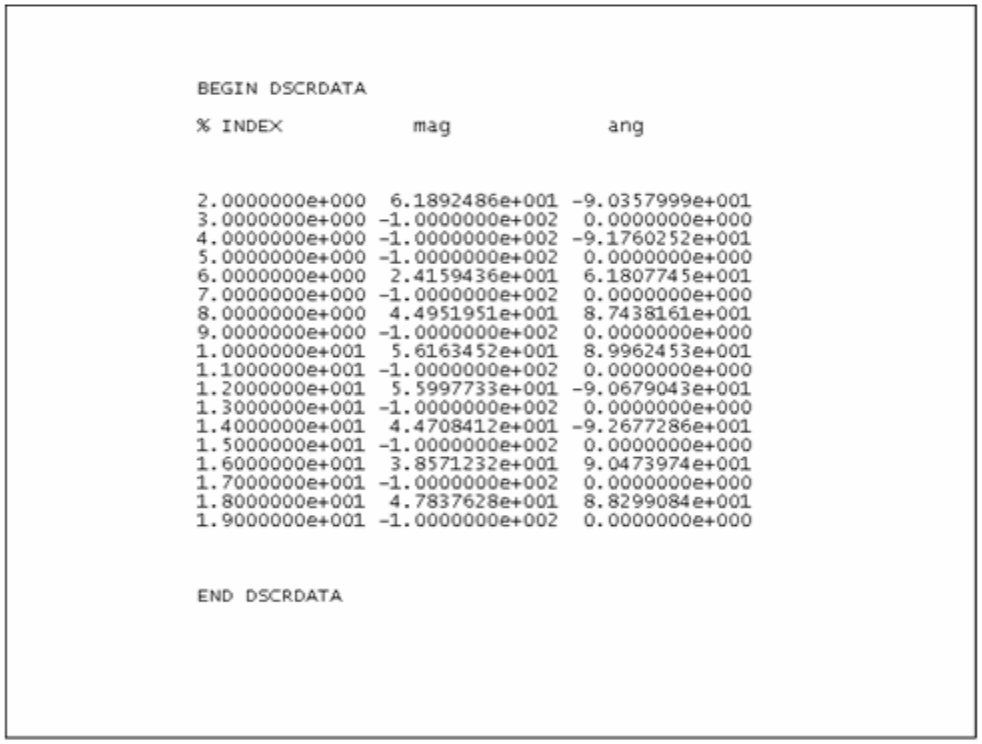
4.3 Data based Signal Source:

Apart from the method which is described earlier another methods can be applied to generate the RF burst signals. Data based signal source may be the useful candidate for this. By using the data based signal source any kind of signals can be constructed very easily.

In ADS there is one source palette called ‘P_Spectrum Dataset’ under frequency domain sources which can read the data from a dataset. If a file contains some meaningful information to represent a signal properly then it can be imported via mentioned source and easily be implemented in Harmonic balance simulation. The file must be a text file and should have adequate frequency components to represent the signal properly. The text file should have the following properties for generating the desired signal.

1. The spectrum of the signal must be single sided because the source palette ‘P_Spectrum Dataset’ starts counting from ‘0’ Hz to upper [21].
2. The first column of the file must be the index of the spectrums or frequency components.
3. The magnitude of the frequency components is expressed in **dBm** and is placed in the second column.
4. The phase of the frequency components is expressed in **degrees** and is placed in the third column.
5. Data may be in different formats but here discrete data type is selected.
6. At the beginning of the file, type of data and header of the column must be declared and at the end, statement of ending should also be declared.

A sample of possible text file which can be used in ADS is shown in figure 4.5. Only a few points are shown here for the reference, although these few points are not may be enough to present a signal properly.



```
BEGIN DSCRDATA

% INDEX           mag             ang


2.0000000e+000  6.1892486e+001 -9.0357999e+001
3.0000000e+000 -1.0000000e+002  0.0000000e+000
4.0000000e+000 -1.0000000e+002 -9.1760252e+001
5.0000000e+000 -1.0000000e+002  0.0000000e+000
6.0000000e+000  2.4159436e+001  6.1807745e+001
7.0000000e+000 -1.0000000e+002  0.0000000e+000
8.0000000e+000  4.4951951e+001  8.7438161e+001
9.0000000e+000 -1.0000000e+002  0.0000000e+000
1.0000000e+001  5.6163452e+001  8.9962453e+001
1.1000000e+001 -1.0000000e+002  0.0000000e+000
1.2000000e+001  5.5997733e+001 -9.0679043e+001
1.3000000e+001 -1.0000000e+002  0.0000000e+000
1.4000000e+001  4.4708412e+001 -9.2677286e+001
1.5000000e+001 -1.0000000e+002  0.0000000e+000
1.6000000e+001  3.8571232e+001  9.0473974e+001
1.7000000e+001 -1.0000000e+002  0.0000000e+000
1.8000000e+001  4.7837628e+001  8.8299084e+001
1.9000000e+001 -1.0000000e+002  0.0000000e+000


END DSCRDATA
```

Fig 4.5: Sample of a text file containing the particular information for generating a desired signal in ADS.

This type of file can be easily created in MATLAB environment. However, this text file cannot be read by the source ‘P_Spectrum Dataset’ directly. Therefore, at first this text file must be imported in a dataset of ADS. In order to do this, the text file must be copied in a data folder of the project and then it is very easy in ADS to make a dataset from the text file. Figure 4.6 illustrates how to read a text data file into a dataset. The procedure is described below by following the figure 4.6.

1. Select read data file in ‘dftool/mainWindow’.
2. Browse the text file from data folder.
3. Select file format as ‘MDIF’.
4. Select MDIF sub type ‘Discrete’.
5. Put a dataset name.
6. Press ‘Read File’ tab to read.

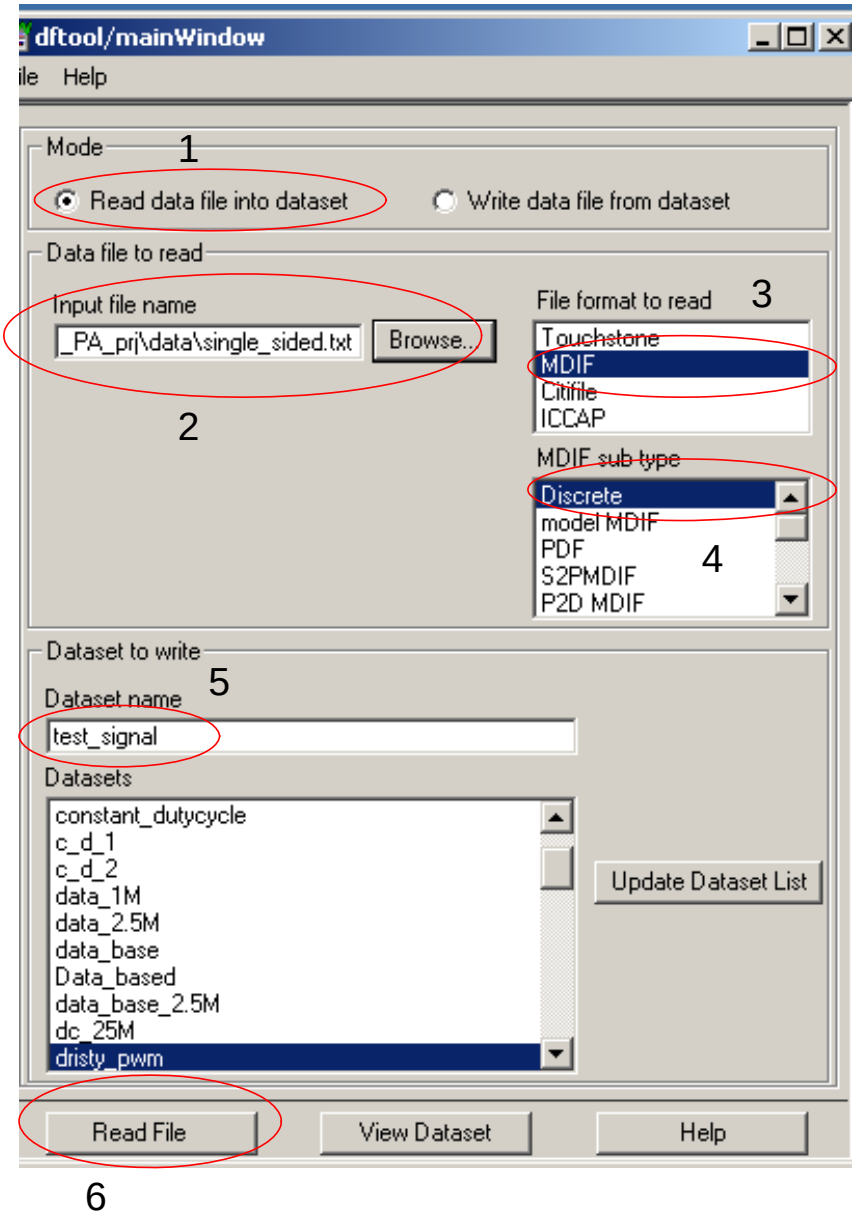


Fig 4.6: Procedure of reading a file into a Dataset of ADS

After reading the data from the text file a dataset will produce by the given file name and in the given location. Now the path of this dataset file has to set in the **'dataset'** option of the 'P_Spectrum Dataset' source. Power and angle of the frequency spectrums must be defined in the 'Expression' option of that source and also need to scale the magnitude of the spectral components depends on desired input power level to the DUT. Figure 4.7 shows how to define the 'expression' along with the full simulation setup for generating a RF burst signal from a data file.

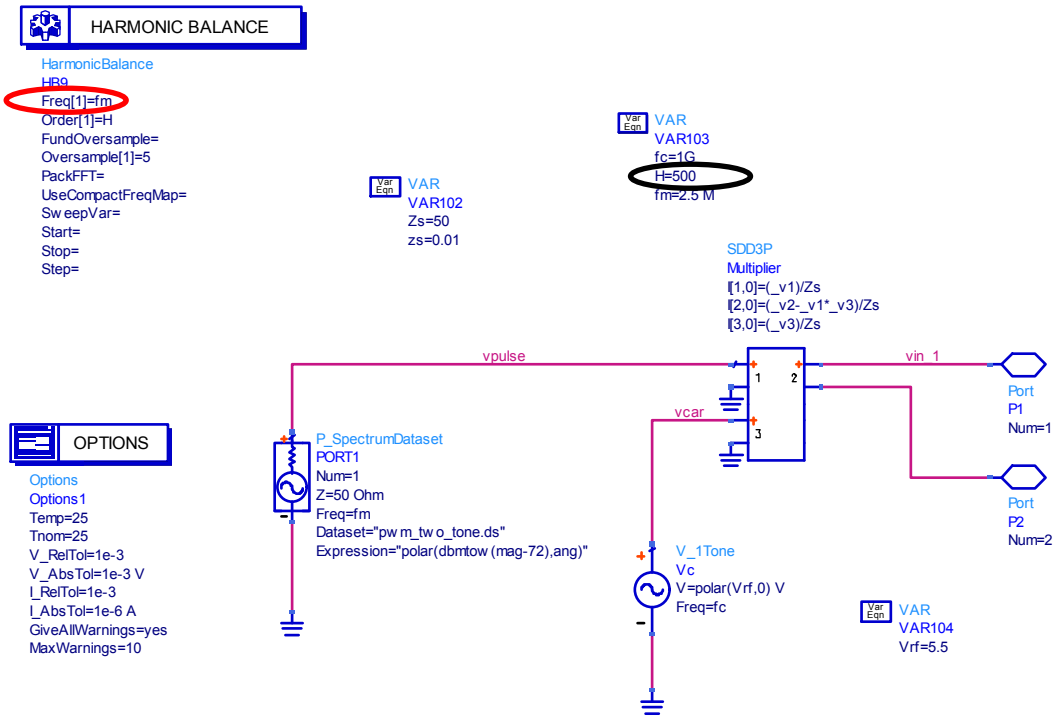


Fig 4.7: Simulation setup in ADS for generating a RF burst signal by using data file

Another vital issue for this technique is to set the harmonic frequency and the harmonics number. The Harmonic frequency must be the difference between two frequency components in the source file. As the simulator starts counting from the declared harmonic frequency (fig. 4.7 (red marked)) therefore in order to reach to the center frequency harmonics number should be high enough (fig. 4.7 (black marked)) to generate the signal correctly. In this point, one important issue may be worth to discuss that what is the reason to read the file which is containing only the baseband information, what's wrong if the data file is containing the information which is already up shifted to the carrier? One main reason for reading only the baseband information is, we have a flexibility to define any carrier frequency as desired very easily and also another reason is that a lot of harmonics have to declare during the simulation. Below figure 4.8 (a, b) showing the single sided frequency components which are read from the data file and the corresponding time domain signal. Figure 4.8 (c, d) representing the frequency spectrums and consequent time domain signal after shifted to the carrier frequency.

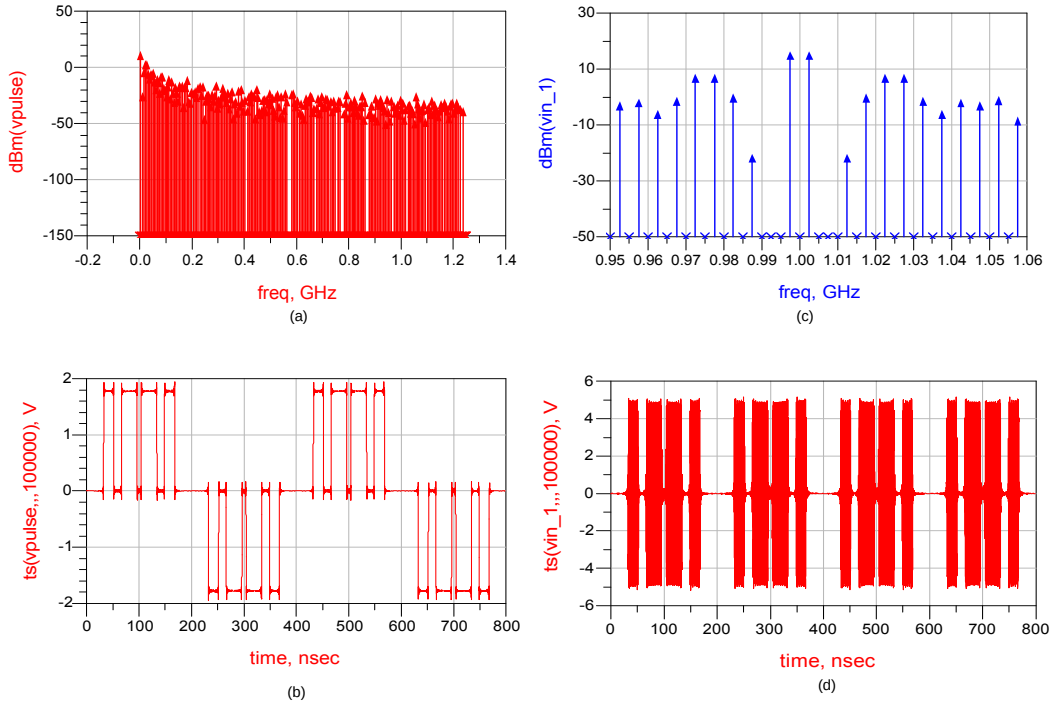


Fig 4.8: Output results of data based signal source.

4.4 Simulation setup in Microwave Office:

Now these days the software Microwave Office (MO) becomes very familiar to the designer for designing any RF/Microwave circuits. Therefore it is also significant to build a simulation setup in Harmonics balancer for the burst signals in Microwave Office. Also we have a power amplifier which is designed in Microwave Office.

It is very easy to build a setup for a burst signal in Microwave Office compare to the software ADS because it has already a defined port called **PORTMOD_F** which can handle modulated signal by means of data files. Moreover, in this simulator the center frequency can be defined in a system frequency therefore additional multiplication is not required for shifting up into the center frequency. However, here also some general procedures must be followed to construct a proper signal. Below some major procedures and key indications are given.

1. Target of the Port:

Microwave office ⟶ Element ⟶ Circuit Element ⟶ Ports ⟶ Signals ⟶ PORTMOD_F

2. File format:

The data file is a simple text file with particular formation.

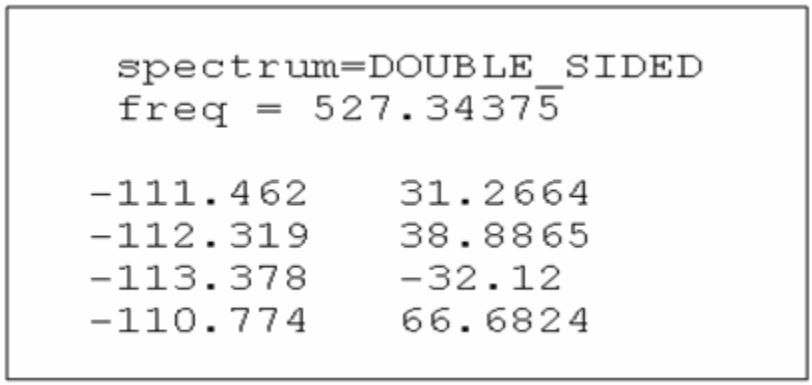


Fig 4.9: Sample of a text file containing the particular information for generating a desired signal in MO.

Figure 4.9 depicts the required arrangement of a data file suitable for the presentation of a modulated signal. At the beginning of the file, the type of the spectrum components have to mention whether it is double sided or single sided [22] and the difference between the two spectrums (in Hz) has to declare in 'freq'. However, this frequency can be mentioned in port under 'FRes'. As like ADS here also the first column is for magnitude in dBm and second column is for angle in degrees of the frequency components. After having correct format of file, that file has to copy in the data folder of a particular project.

3. Port setup:

How to setup the port is clearly written in help file of the port '**PORTMOD_F'** [22]. Here, the magnitude of the spectrums need not to scale manually. Once the power is set in the port, automatically it will assume that the defined power is the sum of all frequency components. Figure 4.10 shows the options and parameters of the port with modulated signal.

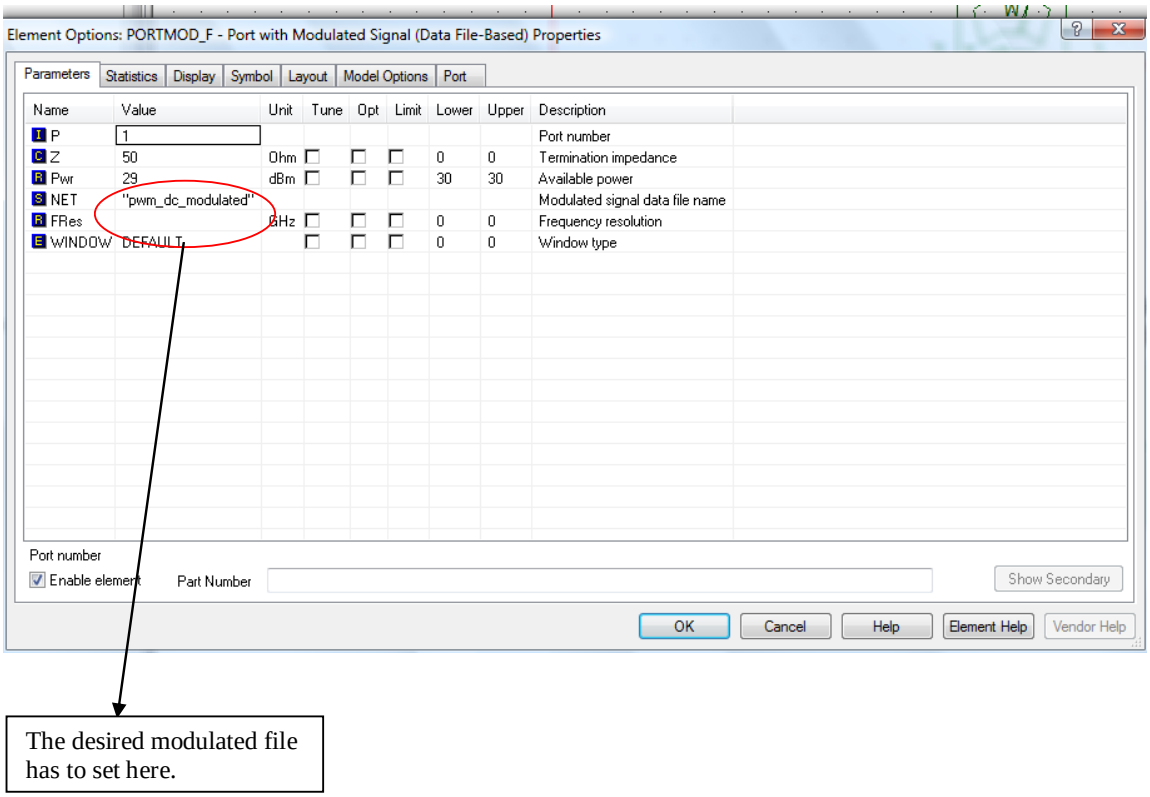


Fig 4.10: Port options.

4. Harmonic Balance setup:

Working Schematic ⟶ Options ⟶ Harmonic Balance

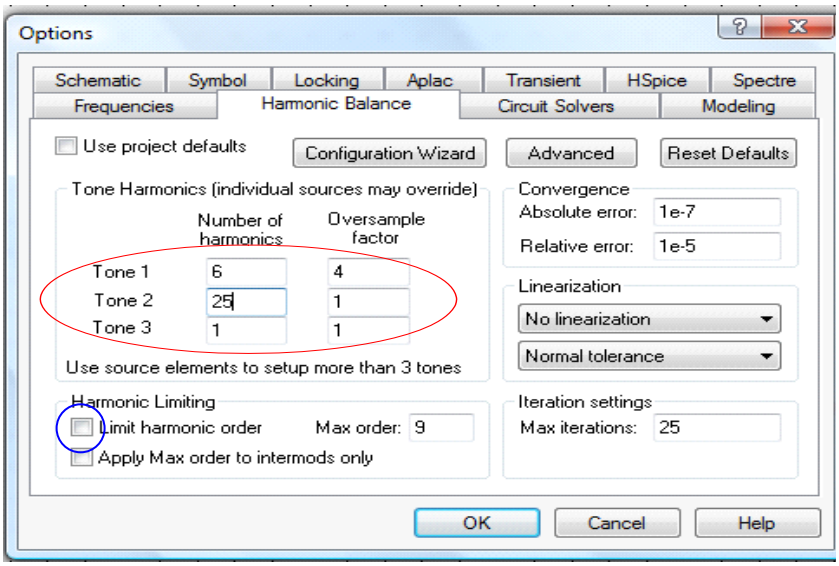


Fig 4.11: Harmonic balance setup.

In figure 4.11 the harmonics number in ‘Tone 1’ is the number of harmonic for the fundamental or carrier frequency. Here, the number of Harmonics is to set ‘6’ or above for accurate results. Also, the Oversampling factor should be four (4) in order to avoid *aliasing* effect in a highly nonlinear system.

The number of harmonics in ‘Tone 2’ defines how many spectral components from the data file will be considered. Here, a large number of harmonics is to define and the ‘**Limit harmonic order’** option has to off. Using too few harmonics will clip the spectrum around the carrier frequency. To know more about this setup please see the example project ‘Modulated_Signals’ under amplifier examples in Microwave Office.

With a complicated modulated signal where really a large number of tones have to define in ‘tone 2’, there it is hard to simulate a high non-linear system with a high number of fundamental harmonics in ‘Tone 1’. In that case, simulation can be done of a nonlinear system by reducing the number of harmonics in ‘Tone 1’ but obviously with less accurate results. Figure 4.12 shows the frequency domain and time domain output from the modulated port of the Microwave Office simulator.

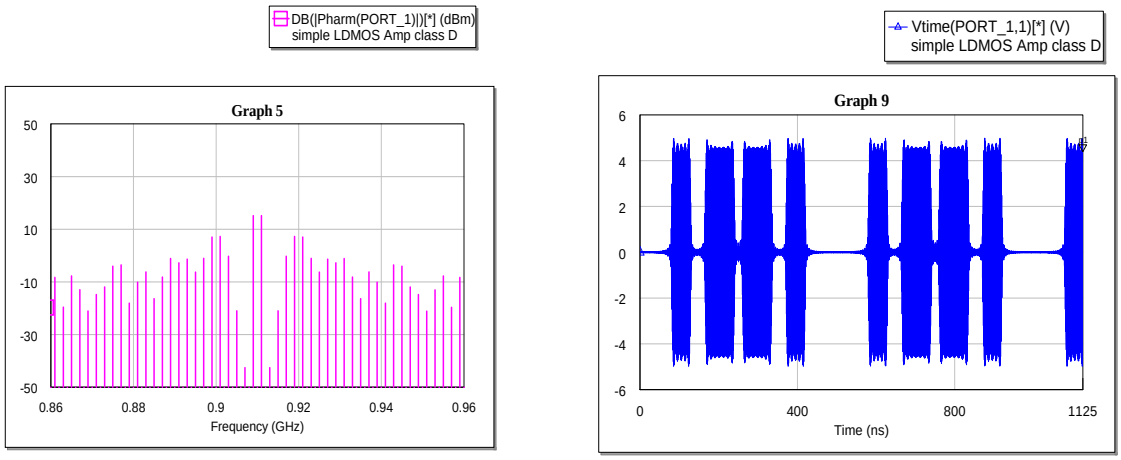


Fig 4.12: Modulated Signal (Two-tone). (a) Frequency domain. (b) Time domain.

4.5: Comparison between ADS and Microwave Office:

ADS and Microwave Office, both simulators have some advantages and disadvantages in sense of generating a RF burst signal. The main advantage of ADS is, a large number of harmonics can be defined while simulating a highly non-linear circuit whereas in Microwave office only a few numbers of harmonics can be defined. By a large number harmonics, Microwave office may run into problems with convergence. Apart from this problem also the Microwave office takes much simulation time for a high nonlinear circuit compare to the ADS.

On the other hand, the major advantages of Microwave office are it is very easy to implement, no need any additional multiplication to shift up into the carrier frequency like in the ADS and also the input RF power can be set directly in the port.

In fact, both simulators cannot handle the multi-tone simulation for complicated non-linear circuit or system. However, the developed simulation setup in both simulators for the burst operation gives good results. The results are well fitted to the measured results which are presented in the next chapter.

Chapter 5

Simulation and Measurement Results

Two Switched mode power amplifiers which are designed for the constant envelop signal are considered here for the simulation and measurement in the burst mode operation. One is 25-W, 900 MHz current mode class D Amplifier and the other one is 8-W, 1 GHz Class-J Amplifier [11]. The goal of this simulation and measurement was to compare the simulated result with the measured result and also to observe the behavior of the chosen power amplifiers in the burst mode operation.

5.1 Measurement Setup:

The modulated driving signal or the burst signal is generated in MATLAB and loaded up to an arbitrary waveform generator (Tektronix AWG 610). Since this generator cannot provide the desired driving power level a wideband pre-amplifier is used. In order to measure the correct input power a directional coupler is used to separate the input signal from the reflected signal caused by the PA. Some attenuators are used in different position of the setup chain to protect the measuring components and also to get the accurate results. A digital oscilloscope from Agilent is also used to observe the time domain input and output signals. Figure 5.1 shows the basic measurement setup of the SMPA for the burst mode operation.

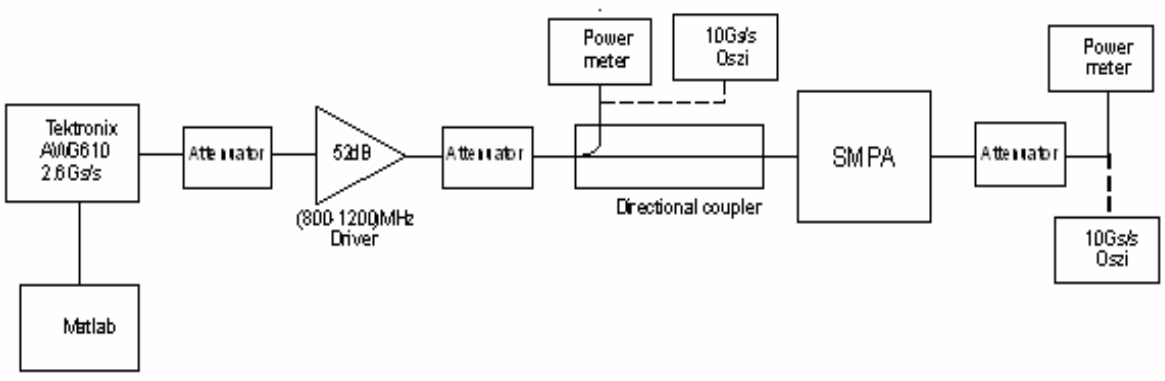


Fig 5.1: Measurement setup.

5.2 Current Mode Class-D Amplifier:

This amplifier was designed in Software (Microwave Office). Therefore, this amplifier is simulated in the burst mode operation by following the simulation setup in Microwave office depicted in the chapter 4. The simulated and measured results are shown in figure 5.2.

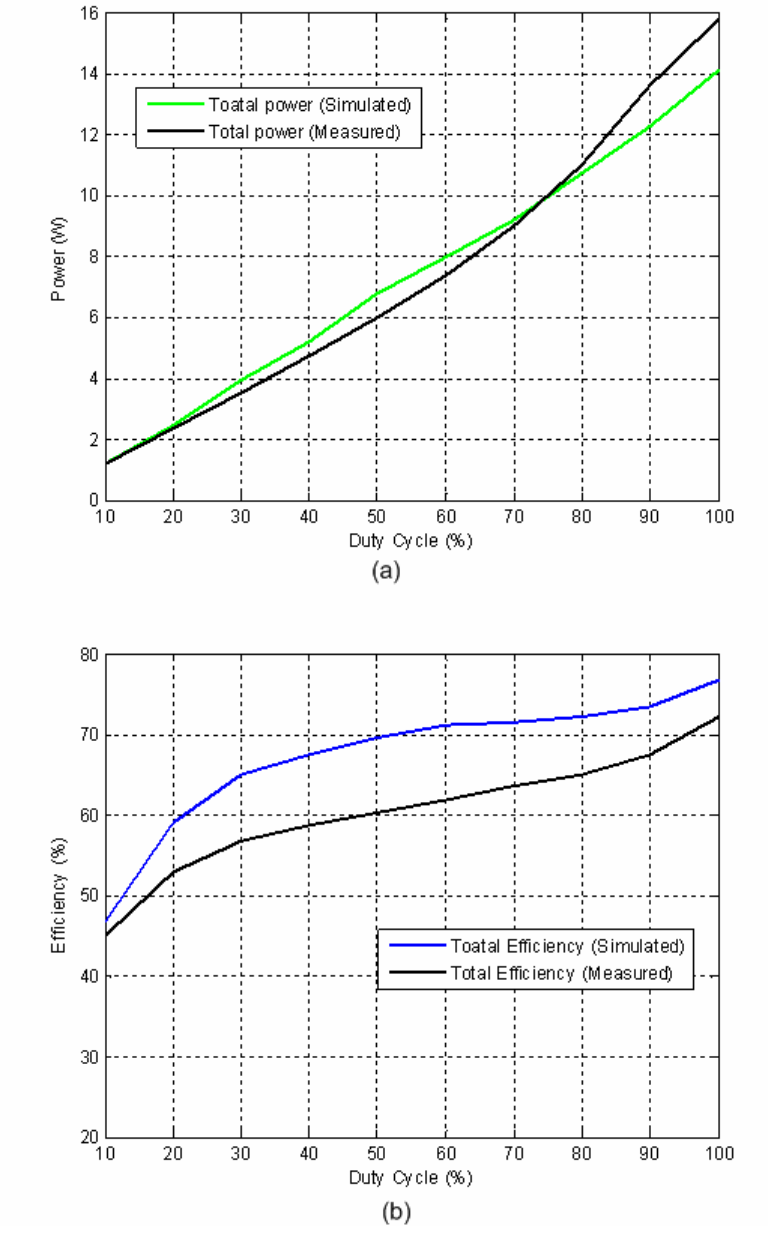
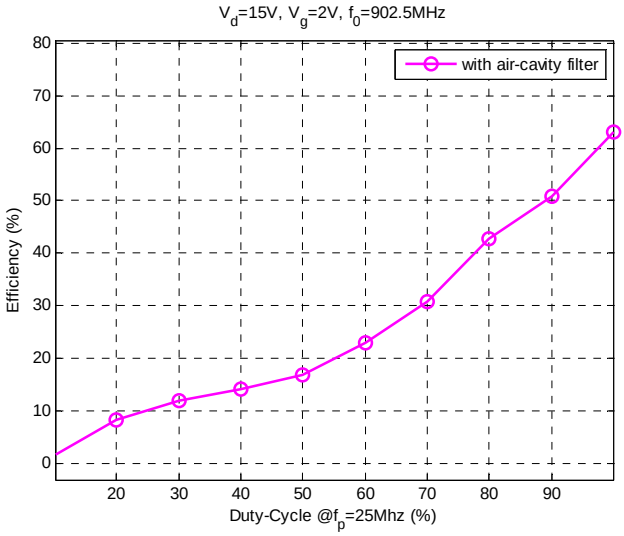


Fig 5.2: Comparison between Simulated and measured result with fc=909 MHz, VDD=15V, VGS=2V and fpwm=10 MHz. (a) Total power. (b) Efficiency.

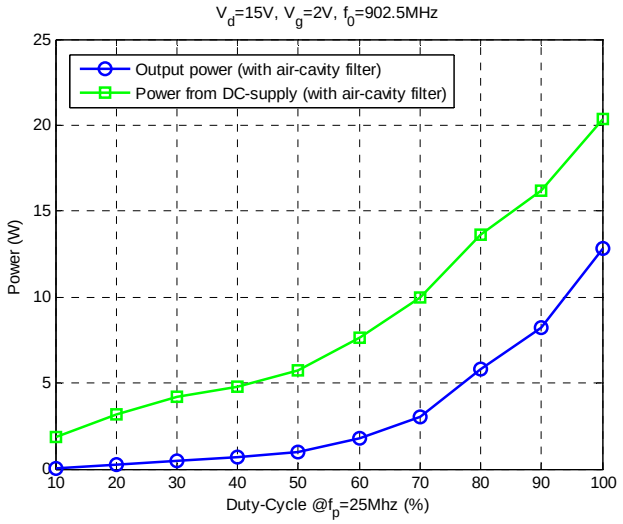
The measured and simulated output power shown in figure 5.2 (a) is quite fit to each other but the efficiency plot (fig. 5.2 (b)) does not fit properly between the two results. In simulation, the losses were not considered. However, the tendency is same in both results.

Now, from the above results it can be conclude that the simulator can give the correct result or at least it can give a reasonable indication of the output results. However, the vital issue is to observe the result after connecting the filter at the output of the PA.

The connected filter is approximately 35 MHz band pass air cavity filter centered at 900 MHz.



(b)



(a)

Fig 5.3: Output after connecting the filter. (a) Efficiency. (b) Output power.

Figure 5.3 shows the efficiency goes down quite a lot after connecting the filter. There are several reasons for this occurrence as stated in chapter 3. Among them the most vital reason is that the reflected signals change the current and voltage waveforms across the device in that way that the current and voltage will overlap. Attention must be paid here to find the solution for connecting the filter in an optimum way. Also, another limitation of the simulator Microwave office (MO) is found here that the simulator couldn't able to achieve convergence while simulating the SMPA in the burst mode operation after connecting the filter.

5.3 Class-J Amplifier:

Another amplifier is provided to simulate and measure in the burst mode operation. This amplifier has more efficiency than the other one but with less output power in the constant envelope operation. This amplifier was designed in ADS therefore simulation is conducted by the ADS simulation setup for the burst mode operation which is described in previous chapter [4]. Moreover, the measurement is performed in a same way as depicted earlier in sec. 5.1. Figure 5.4 shows the comparison of measured and simulated output power and efficiency in the burst mode operation.

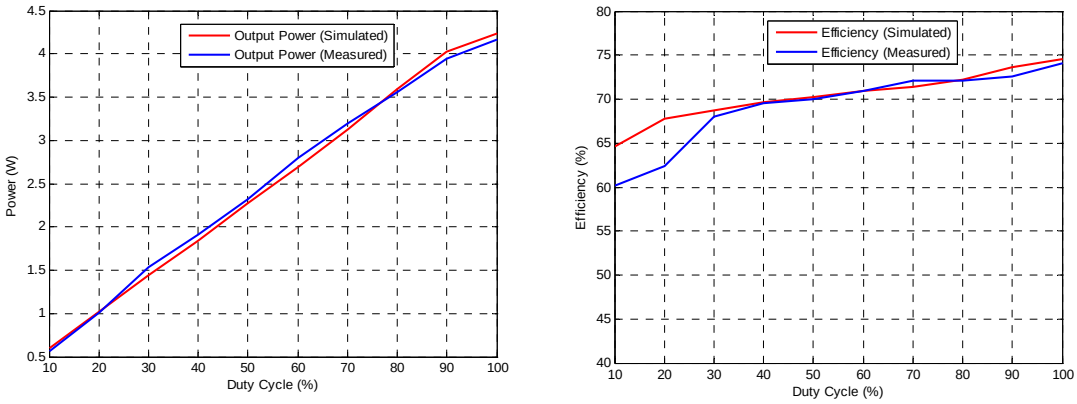


Fig 5.4: Simulated and Measured (a) Output power, (b) Efficiency.

The above figure is obtained with the parameters, VDD=15V, VGS=1.7V, Pin (RF) = 24 dBm (approximately at 100% duty cycle or constant envelop operation), fpwm = 25 MHz, fc = 1 GHz.

It is clear from the figure 5.4 that this amplifier has good efficiency compare to the other one. Also, the simulated and measured results are exactly fit to each other. The most noticeable thing for this amplifier is that the efficiency is almost flat over all duty cycle. In fact, when a signal having high backoff (7-10 dB) will be coded in burst mode operation then duty cycles of the pulse train will fall mostly likely in the range of 10% to 50 %. Therefore, it is important to provide high efficiency at the lower duty cycles to achieve overall good efficiency for real world signal i.e. multi-tone signal.

5.3.1 Two-tone and Multi-tone test:

Although the static PA tests can give the efficiencies of the PA for different duty-cycles, it would be interesting to observe the efficiency and linearity if the switched-mode PA is driven by more realistic multi-tone signals with a certain statistic. For this reason a simple two-tone signal (Fig. 5.5 and 5.6) with an RF bandwidth of 5-MHz and a multi-tone signal with 16 carriers (Fig. 5.7 and 5.8) with an RF bandwidth of 5MHz and a peak-to-average power ratio of 7dB are applied to the PA. Table 5.1 and 5.2 shows the measured and simulated results for these driving signals for the same measurement setup shown in figure 5.1.

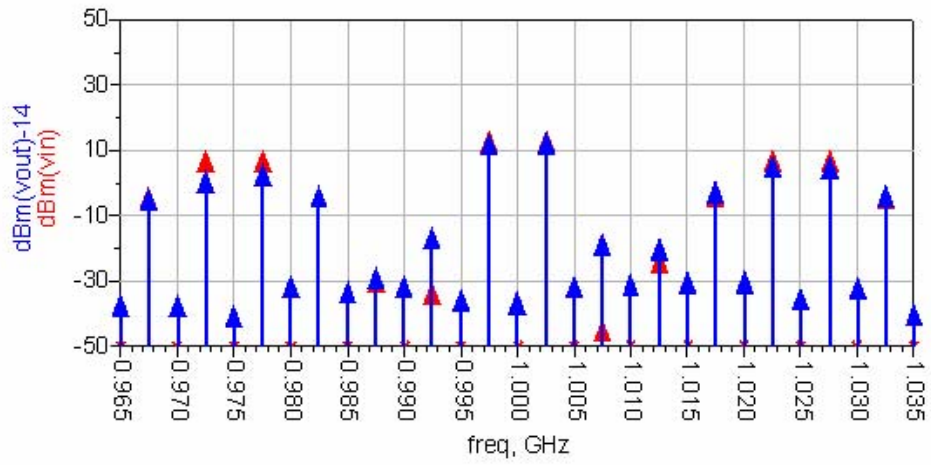
Results type	Pout [dBm]	Pout [W]	Pin [dBm]	Pin [W]	Pdc [W]	η [%]	PAE [%]
Simulated	33.47	2.23	19.97	0.099	3.077	72.30	70.02
Measured	33.73	2.36	20.61	0.115	3.375	69.93	66.52

Table 5.1: Measured and simulated results for a two-tone signal fc ± 2.5 MHz, VGS=1.7V, VDD=15V.

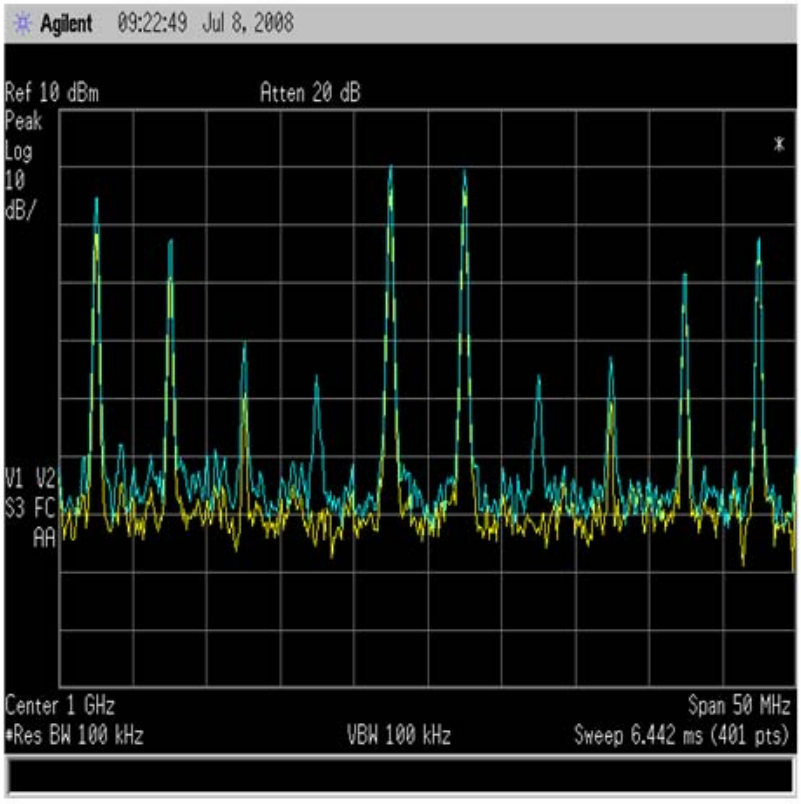
Results type	Pout [dBm]	Pout [W]	Pin [dBm]	Pin [W]	Pdc [W]	η [%]	PAE [%]
Simulated	-	-	-	-	-	-	-
Measured	33.17	2.08	19.95	0.09886	3.00	69.30	66.00

Table 5.2: Measurement results for a 5-MHz bandwidth multi-tone signal with PAP=7dB, VGS=1.7V, VDD=15V, fc = 1 GHz.

Since it was not possible to simulate the PA with the multi-tone signal in ADS therefore the simulation results are left open in table 5.2. The achieved efficiency is quite good both for two-tone and multi-tone input signals (Table 5.1 and 5.2). Figure 5.5 shows the input and output spectrum both for the simulated and measured case. From both results we have noticed the linearity in the range of ~35dBc. Also, in figure 5.6 the time domain output signal from PA driven by two-tone signal is shown.

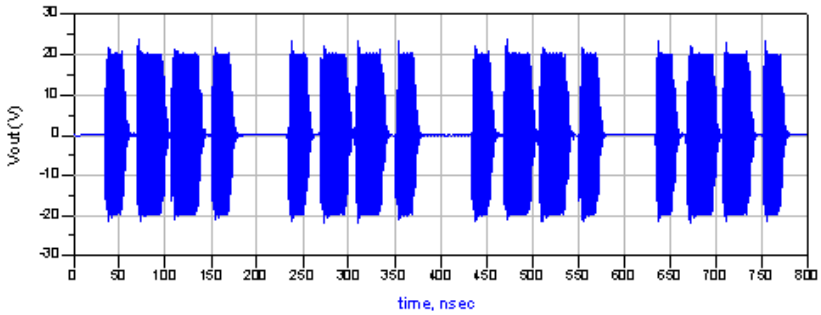


(a)

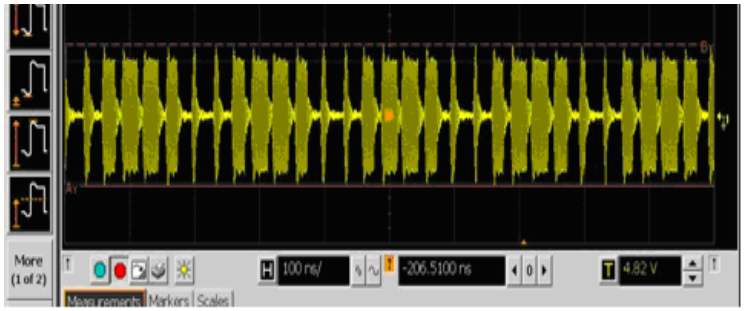


(b)

Fig 5.5: Frequency domain two-tone input and output signal by using the parameters mentioned in Table 5.1. (a) Simulated input signal (red), output signal (blue). (b) Measured input signal (yellow), output signal (blue).



(a)



(b)

Fig 5.6: Time domain output signal from PA driven by Two-tone signal by using the parameters mentioned in Table 5.1. (a) Simulated. (b) Measured.

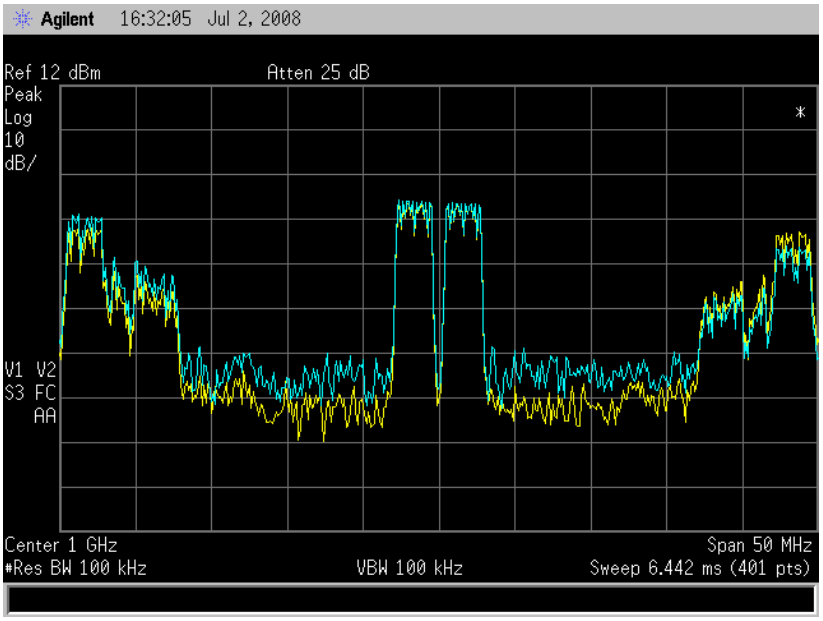


Fig 5.7: Frequency domain Multi-tone input (yellow) and output (blue) signal by using the parameters mentioned in Table 5.2.

Fig 5.8: Time domain input (purple) and output (yellow) signal from PA driven by Multi-tone signal by using the parameters mentioned in Table 5.2.

Figure 5.7 and 5.8 shows the frequency domain and time domain input and output signal from the PA driven by a multi-tone signal. Here also the output linearity is in the range of ~35dBc.

5.3.2 Measurement with Filter:

Before feeding the PA output signal to the antenna the RF bursts must be demodulated with a bandpass filter. In this case an air-cavity filter with a bandwidth of 35 MHz and with a center frequency of 946 MHz is connected to the SMPA to demodulate the RF bursts. The measurement setup is shown in figure 5.9.

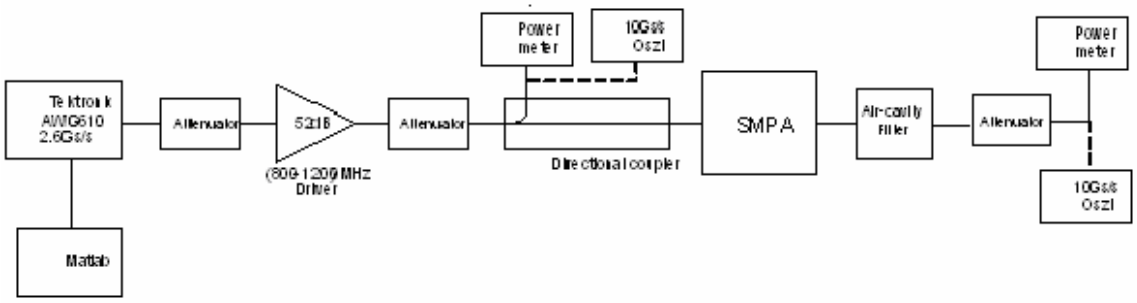


Fig 5.9: Measurement Setup with an air-cavity filter.

Although the Class-J PA is designed for a center frequency of 1GHz, the above measurements are also conducted at 946 MHz to be able to assess the performance of the PA together with available air-cavity filter which is centered at 946 MHz. However, the simulation file in ADS for this PA contains some blocks which are optimized for 1 GHz therefore the simulation results were far from the measured one. For this reason, only measured results are shown here. At first, the efficiency and output power over duty cycle is measured without the filter to observe the behavior of the PA at 946 MHz. Figure 5.10 shows the efficiency and output power over the duty cycles at 946 MHz.

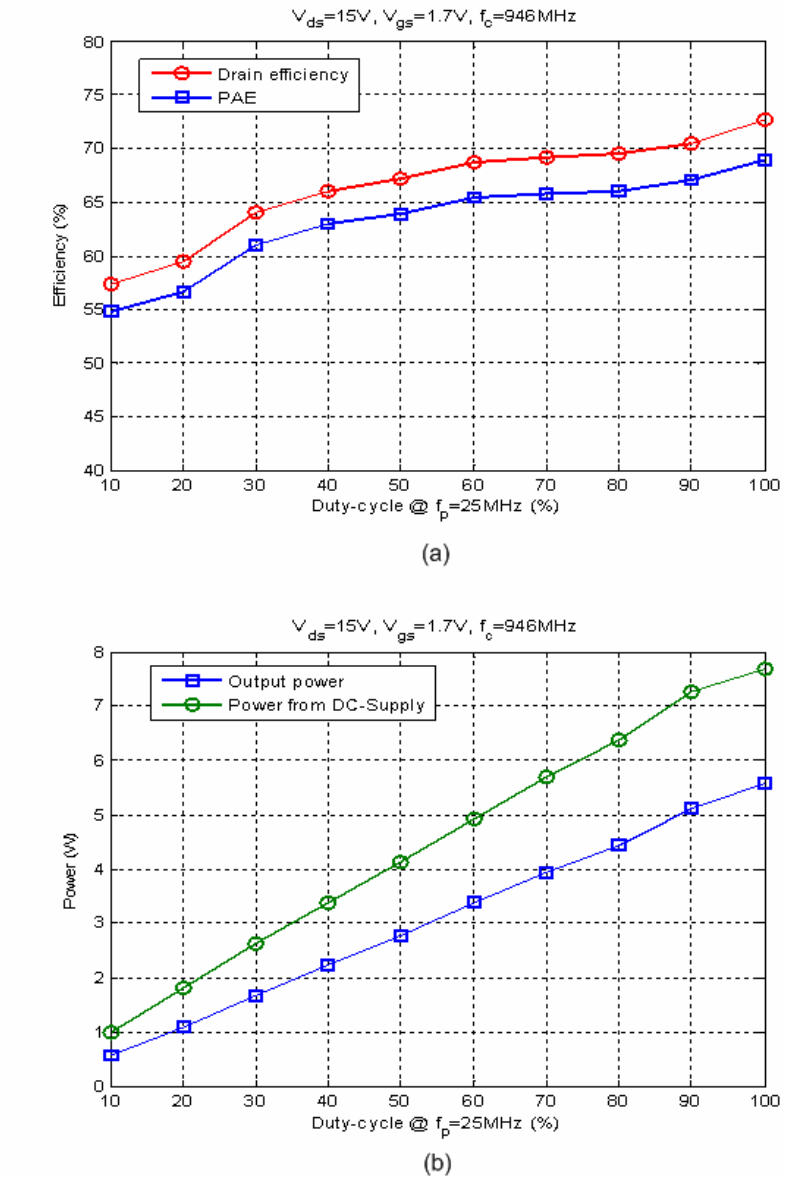


Fig 5.10: The SMPA performance @ 946 MHz (a) Efficiency vs. Duty Cycle (b) The output power vs. Duty Cycle.

From the above figure it is clear that the efficiency over the different duty cycles at 946 MHz is almost the same compared to the efficiencies over the duty cycle at 1 GHz. Now, the measurement is performed with the filter, connected at the output of the SMPA. This measurement setup is shown in figure 5.9. Figure 5.11 shows the efficiencies over the different duty cycles after connecting the filter.

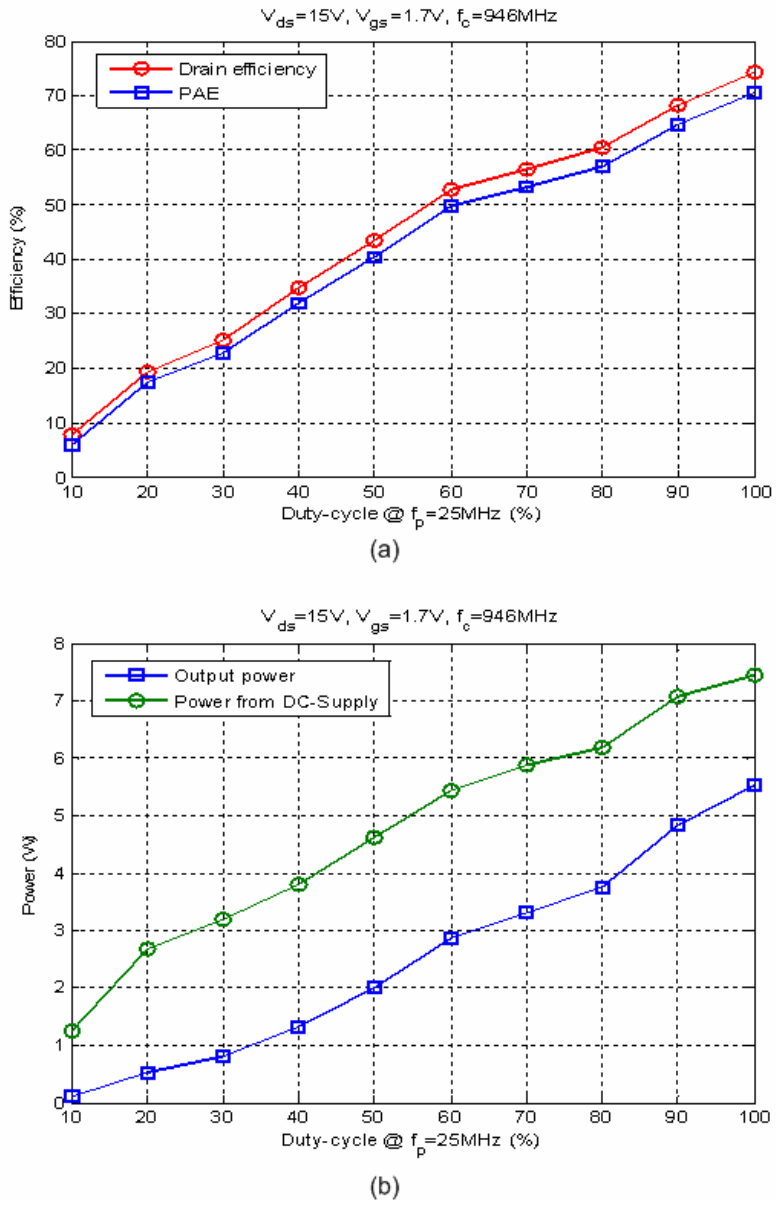


Fig 5.11: (a) Efficiency vs. Duty cycle. (b) Power vs. Duty Cycle. For the parameters, fc=946MHz, VGS=1.7V, VDD=15V.

The figure 5.11 shows that the efficiency goes down quite a lot after connecting the filter. There are lots of reasons behind this degradation. Some of the possible reasons are already been discussed in Chapter 3.

Because the main intention is to drive the PA with a real world signal and to feed the signal to the antenna therefore the multi-tone measurement is done by considering the filter at the output of the PA (fig. 5.9). Table 5.3 and figure 5.12 shows the results of the PA driven by 16-carrier Multi-tone signal following the measurement setup depicted in figure 5.9.

Pout dBm	Pout W	Pin dBm	Pin W	Pdc W	η %	PAE %
31.79	1.51	20.97	0.125	3.63	**41.6**	**38.15**

Table 5.3: Measurement results for a 5MHz bandwidth multi-tone signal with PAP=7dB, VGS=1.7V, VDD=15V, fpwm=25MHz, fc=946MHz.

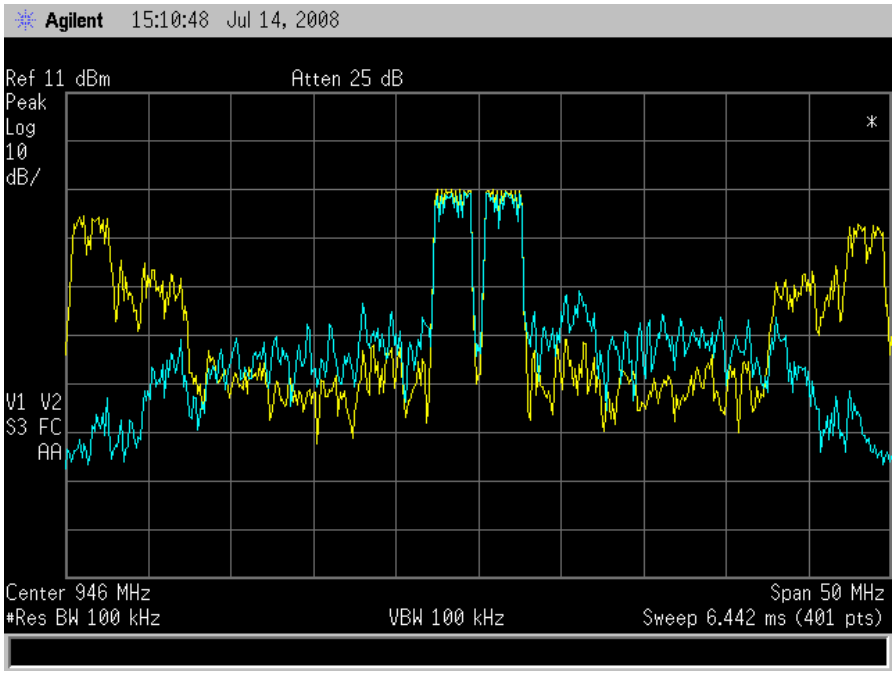


Figure 5.12: Frequency-domain output signal with air-cavity filter (blue) and without air-cavity filter (yellow) of the Class-J PA for a 16 carrier multi-tone signal, B=5MHz, PAP=7dB, fpwm=25MHz, fc=946MHz.

Figure 5.12 shows the linearity goes down by 10 dB after connecting the filter. In this section the filter is connected directly to the PA (with 50Ω cable) with the intention that the out-off-band spectral components (reflected at the filter input) will not be converted to energy. Because this PA was not optimized to work for this burst-mode operation together with the filter, the reflected wave comeback into the device and destroy the wave shapes of voltages and currents over the device. In order to prevent this reflection for this PA an attenuator is placed between the filter and the output of the PA. Figure 5.13 shows the new measurement setup to resist the reflected wave from the device.

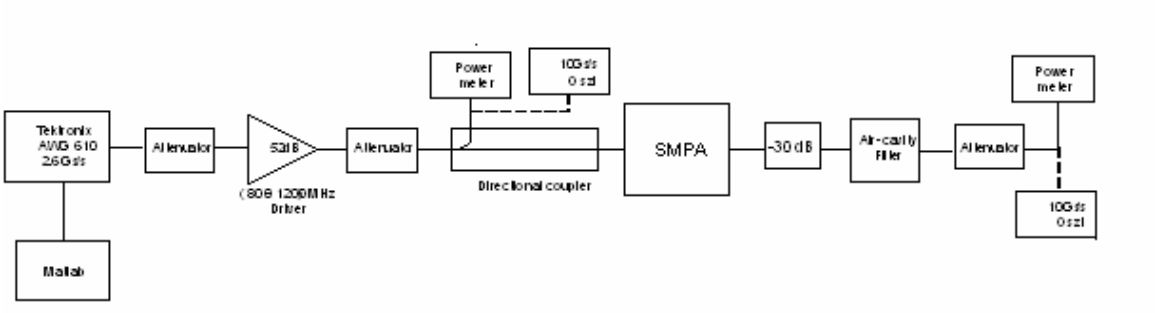


Fig 5.13: Measurement setup where the filter is isolated by the 30 dB attenuator.

By following the above measurement setup, the multi-tone measurement is performed and the measured efficiency was almost the same as in the previous measurement setup (fig. 5.9). In this concern, the most important result is observed that the linearity is improved (approximately 30 dBc) (fig 5.14) compare to the previous measurement where the filter was directly connected to the PA output. The result is shown in table 5.4 and the frequency domain input and output is shown in figure 5.14. Also, in figure 5.15 the time domain input and output signal from multi-tone measurement is presented.

Pout dBm	**Pout W**	**Pdc W**	**η %**
31.94	1.56	3.63	**42.97**

Table 5.4: Measurement results for a 5MHz bandwidth multi-tone signal with PAP=7dB, VGS=1.7V, VDD=15V, where the filter is isolated from the PA.

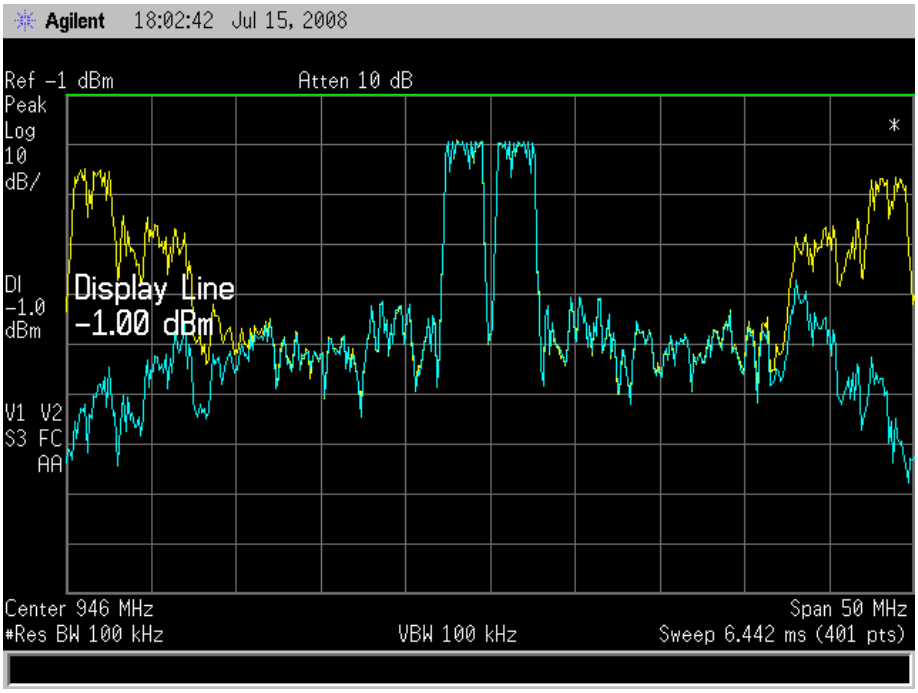


Figure 5.14: Frequency-domain output signal with air-cavity filter (blue) and without air-cavity filter (yellow) of the Class-J PA for a 16 carrier multi-tone signal, B=5Mhz, PAP=7dB, fp=25MHz, fc=946MHz.

Figure 5.15: Time-domain output signal with air-cavity filter (yellow) and input signal (blue) for a 16 carrier multi-tone signal, B=5Mhz, PAP=7dB, fp=25MHz, fc=946MHz.

In this measurement setup a certain length of cable is placed between the PA output and the filter input (fig. 5.16) but it was noticed that the efficiency of the PA has great impact on the length of that cable.

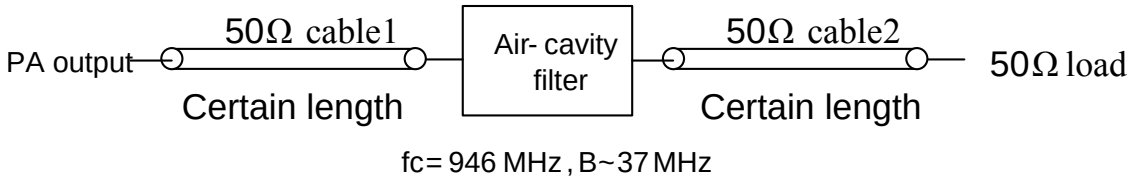


Fig 5.16: The filter connection with 50Ω cables from the PA output and the 50Ω load.

After observing this dependency of the cable length between the PA and the air-cavity filter, the length is adjusted and the optimum efficiency is obtained. The measured result is shown in table 5.5.

Pout dBm	**Pout W**	**Pdc W**	**Pin dBm**	**Pin W**	**η %**
32.856	1.93	3.87	19.7	0.0933	**49.87**

Table 5.5: Measurement results for a 5MHz bandwidth multi-tone signal with PAP=7dB, VGS=1.7V, VDD=15V, fpwm=30MHz, fc= 946 MHz where the filter is directly connected to the output of the PA (with an optimum length of transmission line whose length is set for optimum efficiency).

Finally, from the above measurement it can be conclude that the measured PA shows good linearity (approx. 30 dB) and gives quite high efficiency (approx. 50%) in burst mode operation compare to traditional transmission techniques for high PAP signal. However, the measured PA was not optimized for this burst mode operation.

Chapter 6

Conclusion and Future Research

6.1 Conclusion:

The burst mode operation, a new technique for transmitting high data rate modulated signals shows the promising results for the high efficient base station application. By using this technique, a 16 carrier multi-tone signal is implemented to a Class J amplifier and approximately 50% drain efficiency at 946 MHz and the linearity is in the range of -30 dBc is measured. The achieved results are fair enough in compare to the other proposed techniques which are also subjected to transmit the high peak to average power signals. However, these results are obtained from the SMPA which was not particularly designed for the burst mode operation. By an optimum SMPA which is designed for this burst operation and by implementing the digital pre-distortion technique very high efficiency and also the good linearity can be achieved. Due to the lack of time it was not possible to design an optimum PA for this operation.

However, in this thesis work, the theory of this burst mode operation is reviewed and comes into the conclusion that how to design a SMPA which will give very high efficiency in this burst mode operation. Also, for this new technique, the new simulation setups are developed and the simulated results are fit quite well to the measured results.

Furthermore, after reviewing the whole concept for this burst mode operation, one major drawback comes into mind that when a high peak to average power signal is coded as a PWM signal then usually the PA is operated in the range of 45% to 30% of the duty cycle. Therefore, the output power from the PA is degraded extensively compare with the output power produced by the PA while driven with a constant envelope signal i.e. 100% of duty cycle.

Finally, it can be said that the burst mode operation could be a very promising technique for the next generation high efficient base station application by means of operate the switched mode power amplifier efficiently at high peak to average power signals.

6.2 Future Research:

Because the burst mode operation is a completely new technique and it is an ongoing research topic therefore lot of investigations are required to achieve the high efficiency and good linearity. The following points are discussed about the future research that will help to realize the optimum operation.

- Connecting a band pass filter at the output of the PA (for demodulating the RF bursts) in an optimum way is the key research area which is still an unsolved problem in this burst mode operation. At present for this burst mode operation, the investigations on this filtering issue has the top research priority. Also this burst mode operation demands that this filter should have very narrow bandwidth around the center frequency with very sharp cutoff response and have extremely low insertion loss (close to zero). Therefore, to realize such a filter could also be a research topic for the future work.

- For achieving very high efficiency in burst mode operation a broadband input matching network of an SMPA is required. Therefore, to design an input matching network of an SMPA that has very wide bandwidth around the center frequency is one of the key issues to be investigated at high frequency applications. Apart from this input matching network, a wider bandwidth of the DC network at higher frequencies is also a future research subject.

- To process the baseband signal or to generate the RF burst signals in an optimum way is the vital part of this burst mode operation which requires more precise investigations.

- A deep analysis on Digital pre-distortion will facilitate to improve the linearity. To improve the linearity is one of the key research fields for this burst mode operation.

- To develop the P-Channel LDMOS could be a great revolution for this burst mode operation. In the burst mode operation, the time variant problem with the push-pull configured circuits can be avoidable by developing the P-Channel LDMOS. Also, we can achieve high output power by employed an H-bridge configured circuit once we have the P-Channel LDMOS.

- Finally, to design a switched mode power amplifier having extremely high output power with the high efficiency is also a vast research field.

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Appendix A – Class D amplifier

The class D amplifier or Voltage mode Class D amplifier is a switched mode amplifier. This amplifier is a push-pull configured circuit. Figure A1 shows the ideal circuit configuration and waveforms of Class D amplifier.

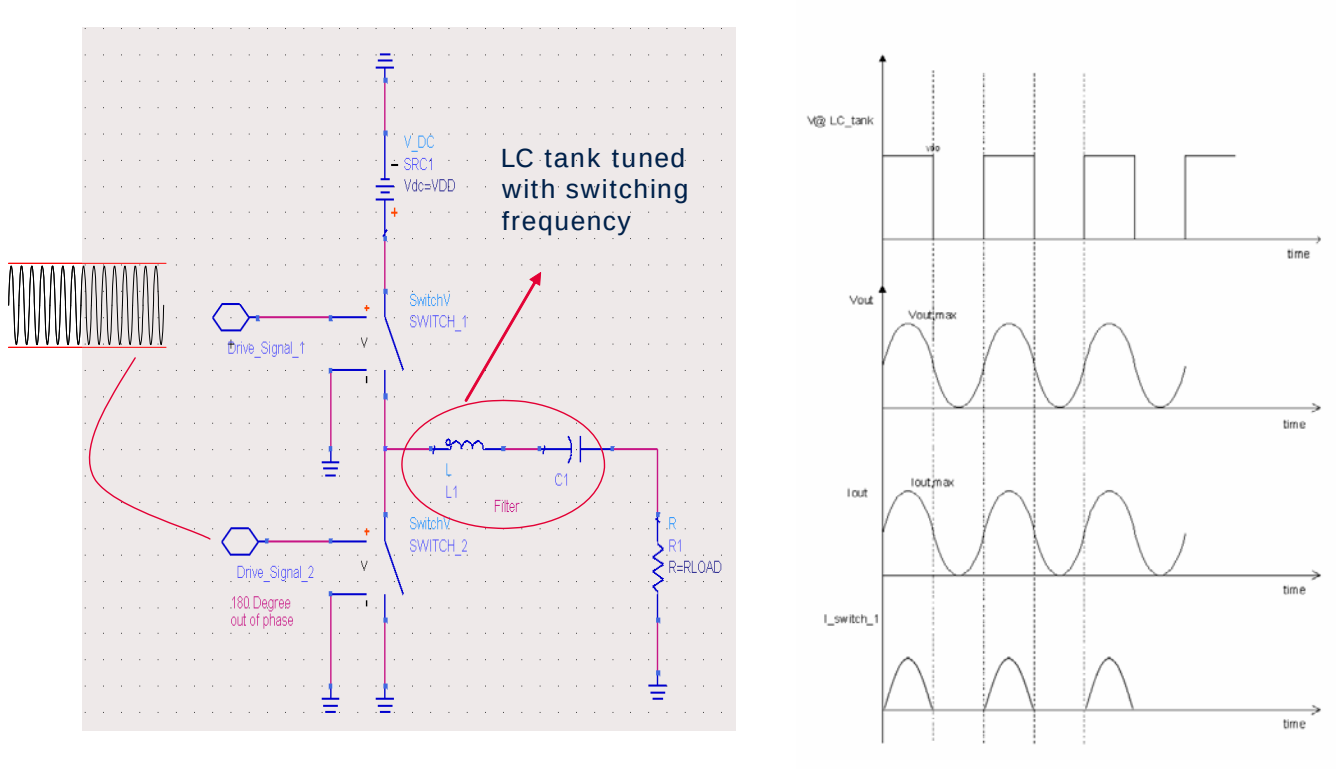

Fig. A1: Ideal Class D amplifier (a) Circuit configuration (b) Waveforms.

The RF inputs to the switches are driven 180 degrees out of phase and thus creates alternately switched between on and off to the circuit shown in figure A1 (a). When the switch_1 turned on, a half wave rectified sine current is pulled to the circuit and charges the capacitor C1 [24]. During this period of operation ideally there will be no voltage across the switch_1 and the potential at the LC tank will be equivalent to VDD. Again, when the switch_1 turned off and switch_2 turned on then the same current which has charged the capacitor C1 will flow back through the switch_2 and capacitor discharges. During this period the voltage at the LC tank will become zero. Therefore, due to this alternately switched on and off it is obvious that the signal at LC tank will become a square wave [fig. A1 (b)].

Now, if we make the Fourier series of that square wave then the following equation can be obtained.

$$V_{LC\_\tan k} = \frac{1}{2}V_{DD} + \frac{2V_{DD}}{\pi}\left(\sin(2\pi f_s t) + \frac{1}{3}\sin(6\pi f_s t) + ...\right) \quad \text{(A1)}$$

Therefore, from the equation A1 it is clear that the voltage at the output after passing through the LC tank will be a pure sinusoidal wave with switching frequency and the peak value of the output voltage can be expressed as:

$$V_{out,\max} = \frac{2V_{DD}}{\pi} \quad \text{(A2)}$$

Consequently, it is obvious that the output current will be also a sinusoidal wave and can be expressed as:

$$I_{out} = \frac{2V_{DD}}{\pi \times R_{load}}\sin(2\pi f_s t) \quad \text{(A3)}$$

Also the DC current over one switch will be the average value of the half wave rectified current, pulled to the particular switch.

$$I_{dc} = \frac{I_{out,\max}}{\pi} = \frac{2V_{DD}}{\pi^2 \times R_{load}} \quad \text{(A4)}$$

Appendix B – Current mode Class D amplifier

The Current mode Class D (CMCD) amplifier is also belongs to the family of Switched mode power amplifier. This is also a push-pull amplifier. The ideal circuit diagram of a current mode Class D amplifier is shown in figure B1 (a). The drain voltage and current waveform of this amplifier is half sinusoidal and square wave respectively [fig. B1 (b)] which are exactly opposite to a Class D amplifier waveforms. That is why, the CMCD amplifier also known as inverse Class D amplifier.

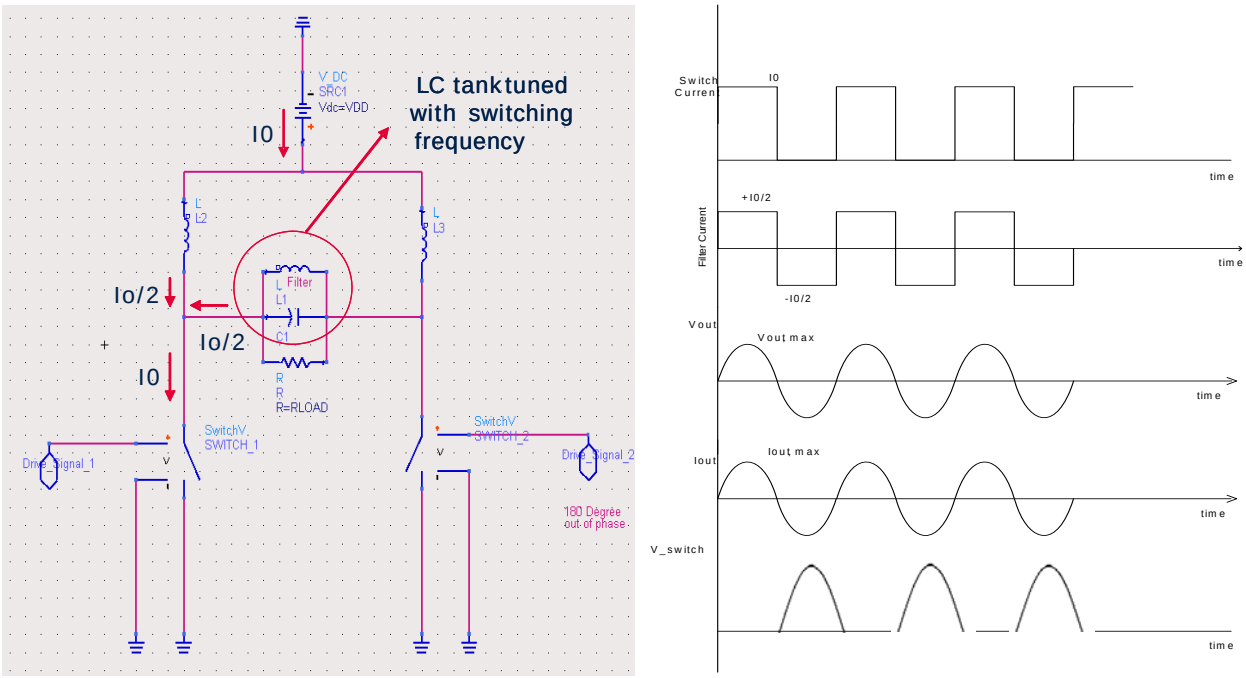

Fig. B1: Ideal Current mode Class D amplifier (a) circuit configuration (b) Waveforms

The two switches are driven 180 degrees out of phase by the RF driving signal and thus create the push-pull effect. The DC current *I0* flows to the circuit through two RF chokes. When switch_1 is turned on and switch_2 is turned off then half of the DC current (*I0*) pass through the resonator circuit to switch_1. The other half flows directly to the switch_1. A square shape current waveform is created by harmonic termination through the parallel resonator with amplitude of *I0/2* [fig. B1 (b)].

Since the harmonic components goes through the resonator therefore only the fundamental tones can reach to the load. The fundamental component can be found by the Fourier decomposition.

The Fourier series of a square wave with amplitude *I0/2* is

$$I_1 = \frac{4I_0}{2\pi}\left(\sin(2\pi f_s t) + \frac{1}{3}\sin(6\pi f_s t) + ...\right) \quad \text{(B1)}$$

Therefore, the amplitude of the fundamental current or output current is

$$I_{1,\max} = \frac{2I_0}{\pi} \quad \text{(B2)}$$

Thus, the voltage at the output is also a sinusoidal wave with the peak value of

$$V_{out,\max} = I_{1,\max} \times R_{load} = \frac{2I_0 R_{load}}{\pi} \quad \text{(B3)}$$

The voltage over one switch is half-wave rectified sinusoidal wave and the amplitude is

$$V_{Switch} = \pi V_{DD} \quad \text{(B4)}$$

From equations B3 and B4, the current *I0* can be deduced [24]

$$I_0 = \frac{\pi^2 V_{DD}}{2R_{load}} \quad \text{(B5)}$$