# RTx Controller Board Design Document

## I. Axis Position Feedback

### A. Analog-to-Digital Converters (ADC's) for Feedback circuits

#### 1. Component List

##### *a) ADC1*

| | | | |
|---|---|---|---|
| C1 | C4 | C5 | ADC1 |

##### *b) ADC2*

| | | | |
|---|---|---|---|
| C2 | C6 | C7 | ADC2 |

##### *c) ADC3*

| | | | | |
|---|---|---|---|---|
| C3 | C8 | C9 | R16 | ADC3 |

##### *d) ADC4*

| | | | | |
|---|---|---|---|---|
| C40 | C41 | C42 | R20 | ADC4 |

##### *e) Analog Reference Voltage Regulator*

| | | | |
|---|---|---|---|
| C23 | C24 | C25 | REF1 |

#### 2. Design Overview

##### *a) ADC Resolution*

The resolution of the axis position feedback ADC's corresponds to the resolution of measurement of the angular position of the axis. Assuming the potentiometer provides a resistance through the axis range of motion which is linear with angle and corresponds to a full-range output voltage sweep through a 360-degree rotation, we have:

$$Resolution_{\theta} = \frac{360^{o}}{2^{Resolution_{ADC}}} \Rightarrow Resolution_{ADC} = \log_2 \frac{2\pi\, rad}{Resolution_{\theta}}$$

The tracking precision required at full-range is then:

$$Resolution_{Range} = Sin(Resolution_{\theta}) * Range$$

$$\Rightarrow Resolution_{\theta} = \arcsin\left(\frac{Resolution_{Range}}{Range}\right)$$

$$\Rightarrow Resolution_{ADC} = \log_2 \frac{2\pi\, rad}{\arcsin\left(\frac{Resolution_{Range}}{Range}\right)}$$

We must track a ~2m length object at distances in excess of 18,000ft. However, we need not stay perfectly centered on the rocket at this distance, as video will not be at full zoom, and telemetry signals require less precision than video. Assuming we want to keep the rocket both in the frame and zoom such that the rocket length is 5% of the frame, the tracking resolution at this range becomes:

$$Resolution_{Range} = \frac{2m}{10\%} = 20m$$

$$Resolution_{ADC} = \log_2\left(\frac{2\pi\, rad}{\arcsin\left(\frac{20m}{5500m}\right)}\right) = 11 bits$$

However, the control system will not be capable of tracking to 1 LSb of the ADC, so as a rule of thumb we will assume tracking precision to within 30% of ADC resolution. Then we have:

$$Resolution_{ADC} = 11bits + 30\% * 11bits = 15\ bits$$

As ADC's are most commonly available in power-of-2 resolutions, a 16 bit ADC will be used.

### b) ADC Digital Interface

Given a sample rate of 2000Hz as described in section B.3.a below, we must have a data bandwidth of 2kSamples/sec, with a sample size of 16 bits or 2 Bytes. We must then have a data bandwidth of 4kB/s for each ADC, or 16kB/s if they are on a shared or daisy-chained bus. However, latency is of great concern in a control system, so it is not sufficient that the data transfer complete within the sample period.

A daisy-chain SPI interface allows a single sample command to be issued to all ADC's simultaneously, and allows a single data transfer from all axes to be performed with lower overhead as compared to a chip-select based SPI interface.

### c) ADC Choice

Common ADC data buses are I2C and SPI. The AD7685 is a 16-bit ADC supporting both SPI and daisy-chain serial interfaces at up to 55MHz, or more than 6.5MB/s. It also has a sample rate of up to 250kSamples/s, and a sample-to-data ready time of no more than 2.2us, minimizing latency and satisfying throughput requirements.

## 3. Summary of Parameters

$Resolution_{5500m} = 20m$

$Resolution_{ADC} = 16\ bits$

## B. Low-Pass Filters for Feedback ADC's

### 1. Component List

#### a) ADC1 Feedback LPF

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| R1 | R2 | R3 | C10 | C11 | C12 | C13 | OPAMP1-A |

#### b) ADC2 Feedback LPF

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| R4 | R5 | R6 | C14 | C15 | C16 | C17 | OPAMP1-B |

#### c) ADC3 Feedback LPF

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| R7 | R8 | R9 | C18 | C19 | C20 | C21 | OPAMP2-A |

#### d) ADC4 Feedback LPF

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| R17 | R18 | R19 | C36 | C37 | C38 | C39 | OPAMP2-B |

### 2. Design Overview/Component Choice

#### a) Control Bandwidth and Cutoff Frequency

The control bandwidth frequency $f_{CBW}$ for the closed-loop control system was chosen based on the requirement to track fast-moving objects with video during manual and automated control operation. The cutoff frequency $f_C$ for the ADC input LPF is specified to be one decade higher than $f_{CBW}$. This convention places $f_C$ far enough above the $f_{CBW}$ to prevent the LPF from limiting performance at the $f_{CBW}$, while still providing satisfactory noise filtering.

$$f_{CBW} = 2.5Hz$$

$$f_C = 2.5Hz * 10 = 25Hz$$

#### b) ADC 1-bit Frequency, desired noise level and Filter Order

The frequency of the ADC's LSB $f_{1bit}$ is the minimum frequency at which we will observe a change on the least significant bit. The maximum noise level desired at $f_{1bit}$ is -96dβ. $f_{1bit}$ must be a low enough frequency such that the Nyquist rate is reasonable given our choice of ADC's and microcontroller. With a 3$^{rd}$ Order LPF with our $f_C = 25Hz$, we have:

$$f_{-96d\beta} = 995Hz$$

The Nyquist rate, or minimum rate we must sample the ADC's is then $995Hz * 2 = 1090Hz$, which is a reasonable sample rate for the system.

#### c) Topology

A Sallen-Key topology Butterworth Low-Pass Filter was chosen due to its simplicity, and the ability to attain 3$^{rd}$-order filtering and a low $f_C$ with relatively low RLC values in combination.

#### d) Op-Amp

The AD861x Op-Amp was chosen to produce the Sallen-Key topology because it is recommended for use in conjunction with the chosen ADC's.

### 3. Consequences

#### a) Control Rate and ADC Sampling

A rule of thumb for minimum control rate is $f_{CR} \geq f_{CBW} * 40$, then:

$$f_{CR} \geq 2.5Hz * 40 \geq 100Hz$$

The Nyquist rate must also be satisfied, so the sample rate must be:

$$f_S \geq 1080Hz$$

Choosing $f_{CR} = 100Hz$ and $f_S = 2000Hz$ gives us 20 samples per control loop iteration.

### 4. Summary of Parameters

$f_{CBW} = 2.5Hz$

$f_C = 25Hz$

$f_S = 2000Hz$

$f_{CR} = 100Hz$

## II. Microcontroller

## III. Ethernet Port

## IV. USB Development/Debug Port

## V. Input Voltage Regulation/Filtering

## VI. Motor Driver Outputs