RTx Controller Board Design

I. Axis Position Feedback

A. Analog-to-Digital Converters (ADC's) for Feedback circuits

1. Component List

a) ADC1

C1	C4	C5	ADC1

b) ADC2

C2	C6	C7	ADC2

c) ADC3

C3	C8	C9	R16	ADC3

d) ADC4

C40	C41	C42	R20	ADC4

e) Analog Reference Voltage Regulator

C23	C24	C25	REF1

2. Design Overview

a) ADC Resolution

The resolution of the axis position feedback ADC's corresponds to the resolution of measurement of the angular position of the axis. Assuming the potentiometer provides a resistance through the axis range of motion which is linear with angle and corresponds to a full-range output voltage sweep through a 360-degree rotation, we have:

$$Resolution_\theta = \frac{360^o}{2^{Resolution_{ADC}}} \Rightarrow Resolution_{ADC} = \log_2 \frac{2\pi\ rad}{Resolution_\theta}$$

Comment [R1]: How does this measurement resolution correspond to desired control resolution?

B. Low-Pass Filters for Feedback ADC's

1. Component List

a) ADC1 Feedback LPF

R1	R2	R3	C10	C11	C12	C13	OPAMP1-A

b) ADC2 Feedback LPF

R4	R5	R6	C14	C15	C16	C17	OPAMP1-B

c) ADC3 Feedback LPF

R7	R8	R9	C18	C19	C20	C21	OPAMP2-A

d) ADC4 Feedback LPF

R17	R18	R19	C36	C37	C38	C39	OPAMP2-B

2. Design Overview/Component Choice

a) Control Bandwidth and Cutoff Frequency

The control bandwidth frequency f_{CBW} for the closed-loop control system was chosen based on the requirement to track fast-moving objects with video during manual and automated control operation. The cutoff frequency f_C for the ADC input LPF is specified to be one decade higher than f_{CBW}. This convention places f_C far enough above the f_{CBW} to prevent the LPF from limiting performance at the f_{CBW}, while still providing satisfactory noise filtering.

$$f_{CBW} = 2.5Hz$$

$$f_C = 2.5Hz * 10 = 25Hz$$

b) ADC 1-bit Frequency, desired noise level and Filter Order

The frequency of the ADC's LSB f_{1bit} is the minimum frequency at which we will observe a change on the least significant bit. The maximum noise level desired at f_{1bit} is -96dβ. f_{1bit} must be a low enough frequency such that the Nyquist rate is reasonable given our choice of ADC's and microcontroller. With a 3rd Order LPF with our $f_C = 25Hz$, we have:

$$f_{-96d\beta} = 995Hz$$

The Nyquist rate, or minimum rate we must sample the ADC's is then $995Hz * 2 = 1090Hz$, which is a reasonable sample rate for the system.

c) Topology

A Sallen-Key topology Butterworth Low-Pass Filter was chosen due to its simplicity, and the ability to attain 3rd-order filtering and a low f_C with relatively low RLC values in combination.

d) Op-Amp

The AD861x Op-Amp was chosen to produce the Sallen-Key topology because it is recommended for use in conjunction with the chosen ADC's.

3. Consequences

a) Control Rate and ADC Sampling

A rule of thumb for minimum control rate is $f_{CR} \geq f_{CBW} * 40$, then:

$$f_{CR} \geq 2.5Hz * 40 \geq 100Hz$$

The Nyquist rate must also be satisfied, so the sample rate must be:

$$f_S \geq 1080Hz$$

Choosing $f_{CR} = 100Hz$ and $f_S = 2000Hz$ gives us 20 samples per control loop iteration.

4. Summary of Parameters

$f_{CBW} = 2.5Hz$

$f_C = 25Hz$

$f_S = 2000Hz$

$f_{CR} = 100Hz$

II. Microcontroller

III. Ethernet Port

IV. USB Development/Debug Port

V. Input Voltage Regulation/Filtering

VI. Motor Driver Outputs