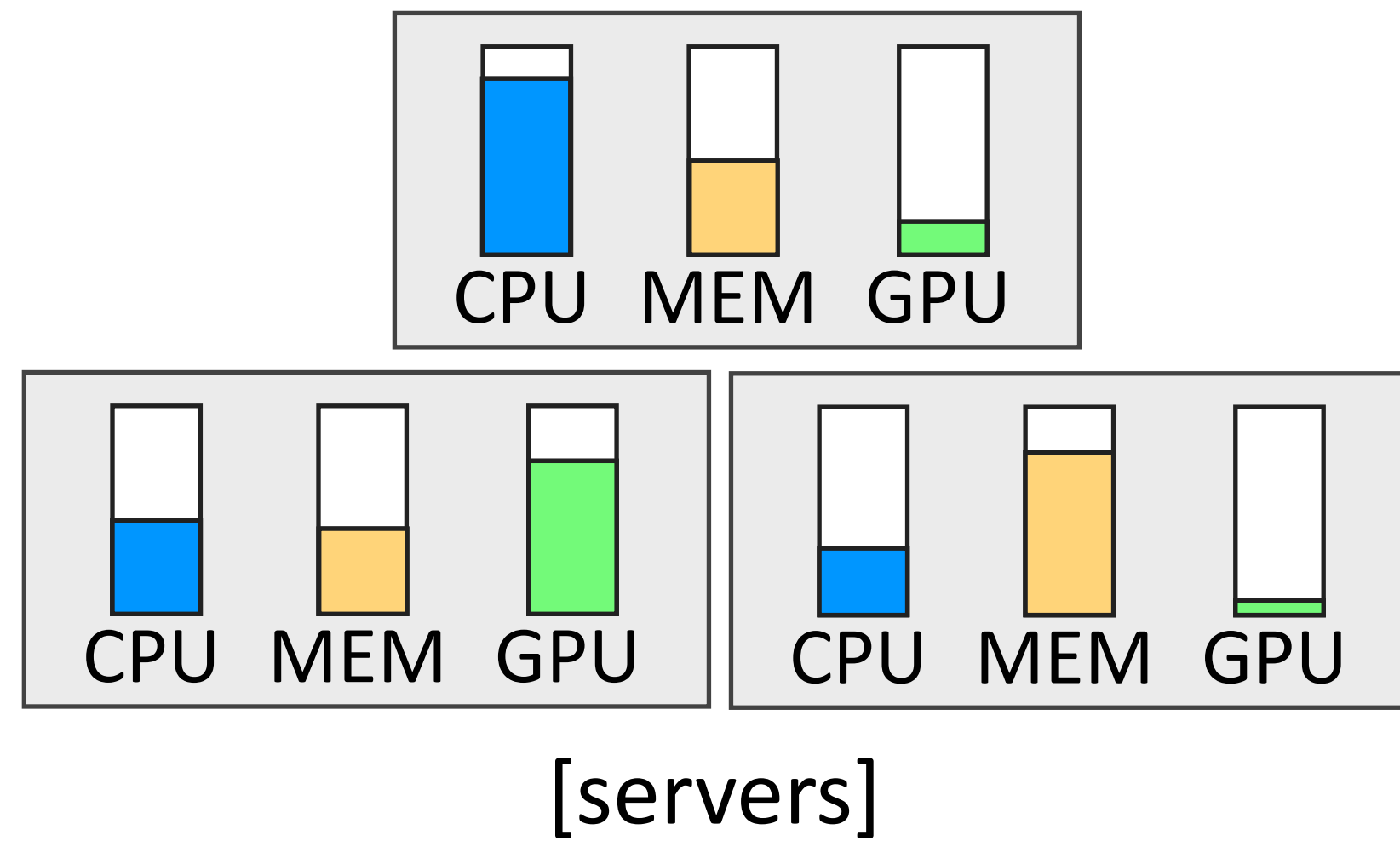


MIND: In-Network Memory Management for Disaggregated Data Centers

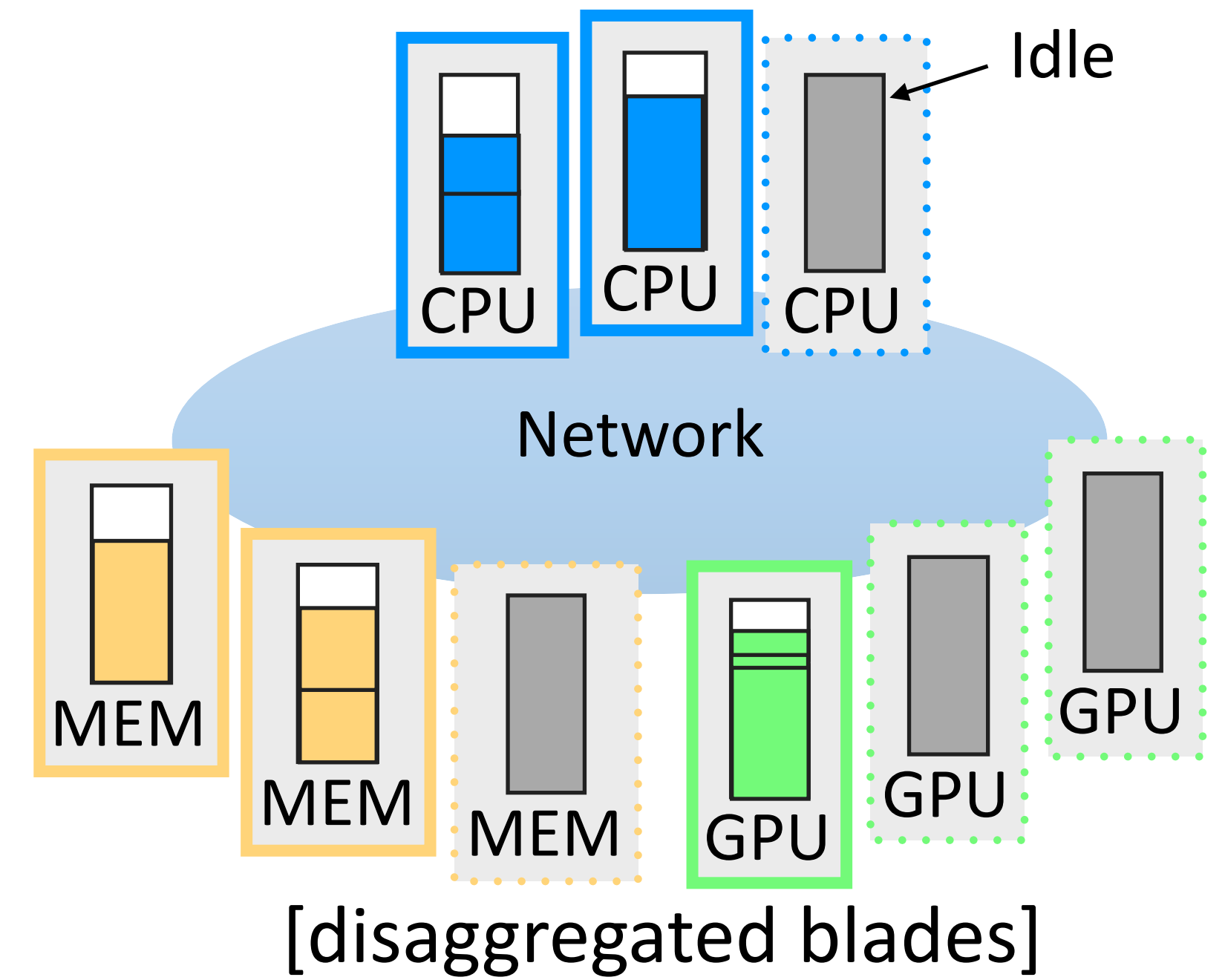
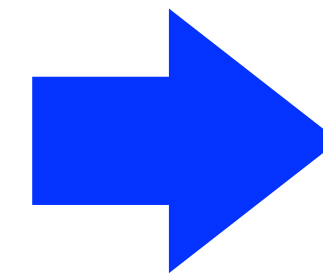
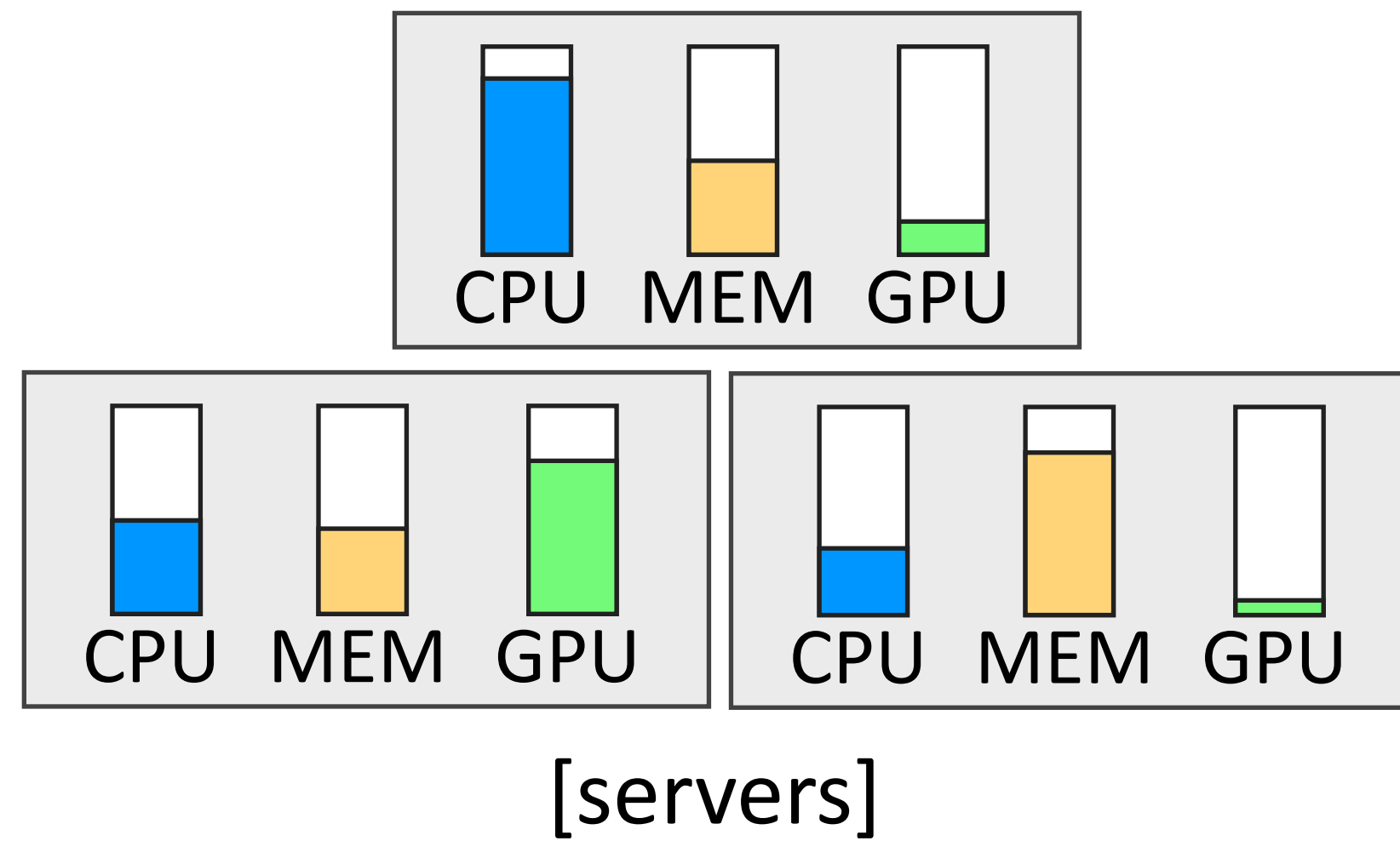
*Seung-seob Lee, Yanpeng Yu, Yupeng Tang,
Anurag Khandelwal, Lin Zhong, Abhishek Bhattacharjee*

Yale University

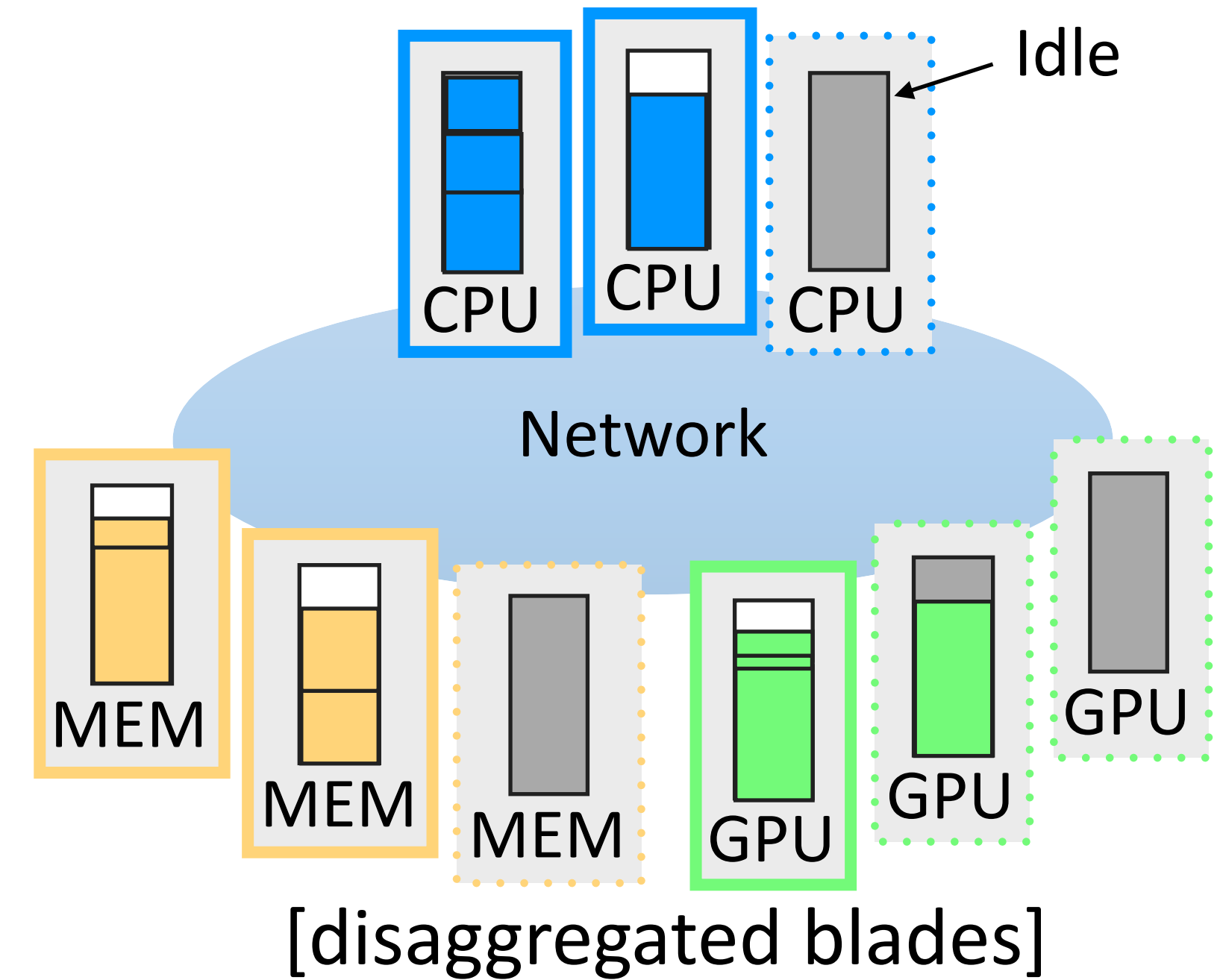
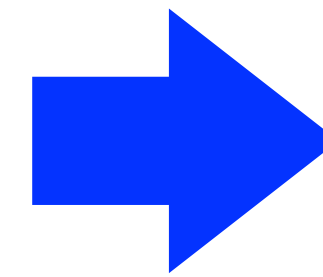
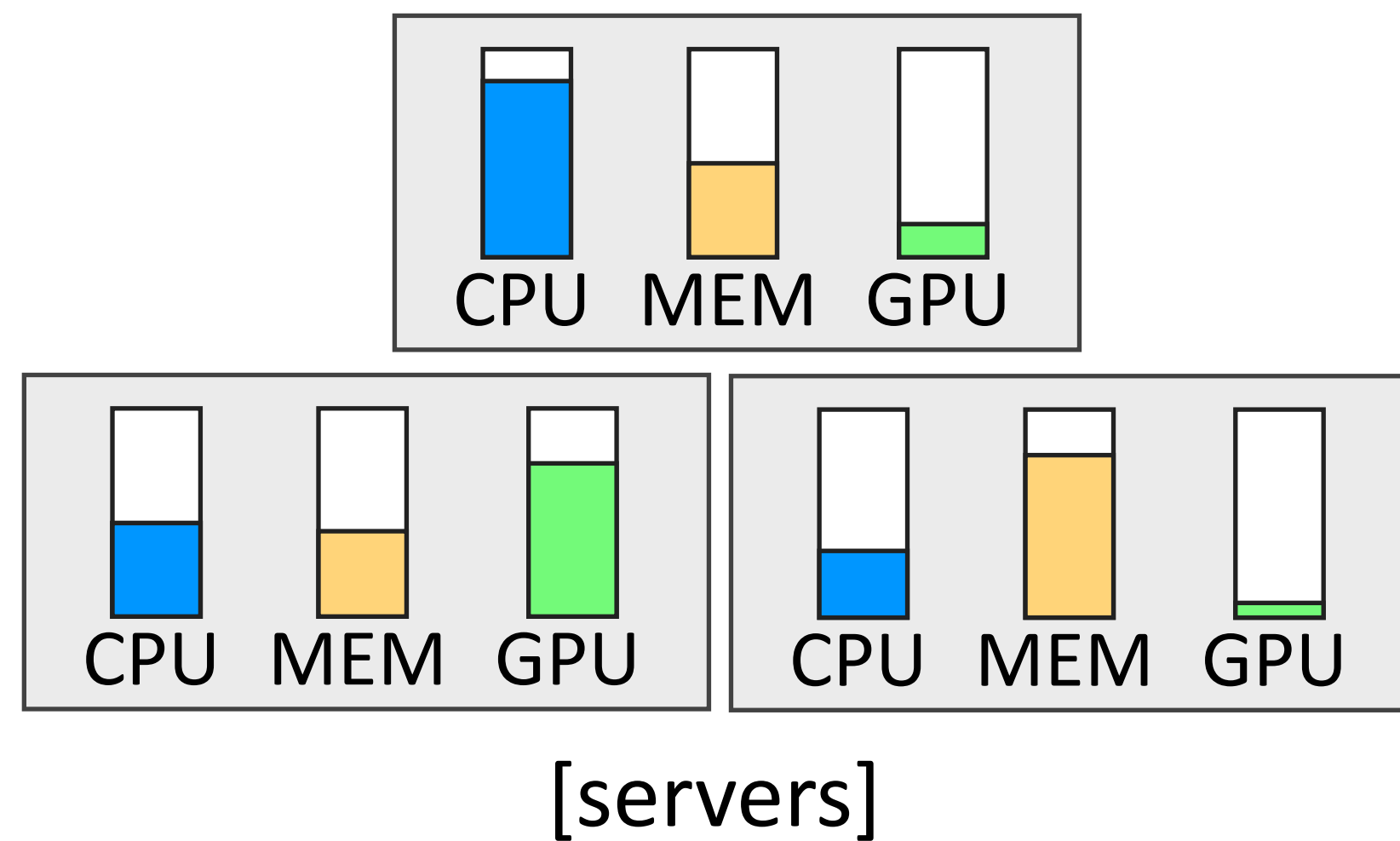
Resource Disaggregation



Resource Disaggregation

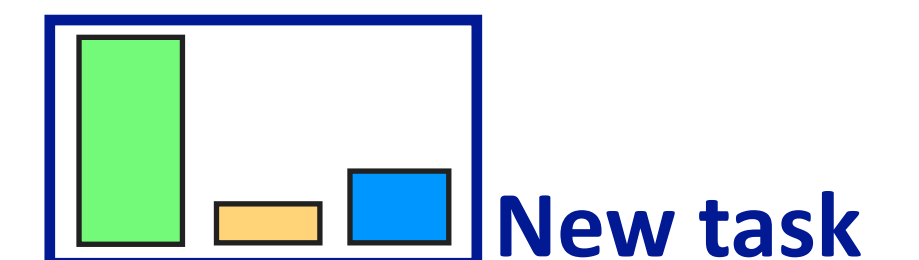


Resource Disaggregation



• Benefits of resource disaggregation

- High resource utilization
- Easy to manage (modularity)
- Elastic scalability



Memory Disaggregation

- **Need for memory disaggregation**

Low utilization

(as low as 30%)

Unbalanced usage

(> 70% of the time in clusters)

Energy consumption

(up to 46% of avg. system)

Memory Disaggregation

- Need for memory disaggregation
- Timely problem

Low utilization
(as low as 30%)

Unbalanced usage
(> 70% of the time in clusters)

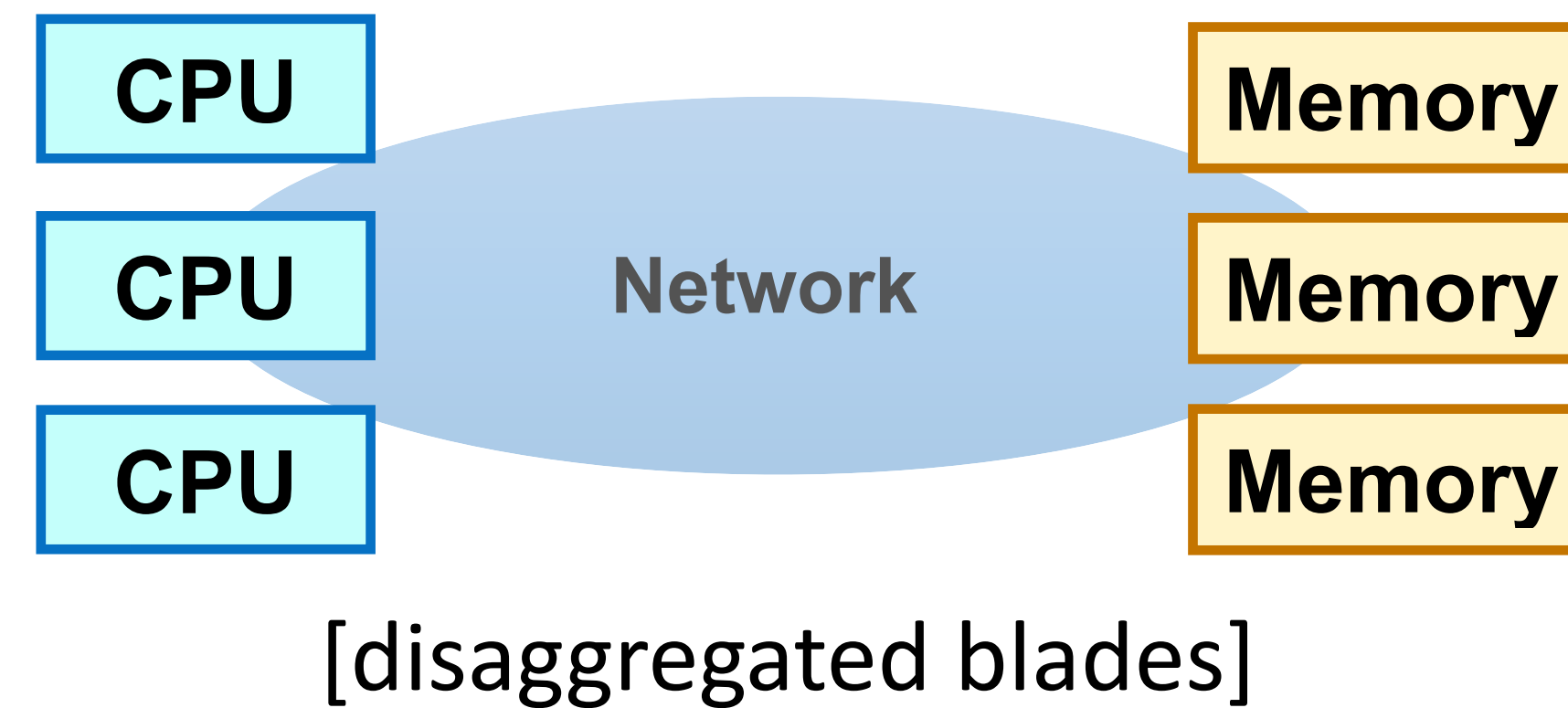
Energy consumption
(up to 46% of avg. system)

Faster & harder to disaggregate →

	Storage (NVMe SSD)	Network	Memory (DDR4)	L3 cache
Data rate	5 GB/s (PCIe 4.0)	25 GB/s (PCIe 4.0)	25.6 GB/s (per channel)	370 GB/s
Latency	45 / 450 μ s (R/W)	~5 μ s (4KB)	<50 ns	11 ns

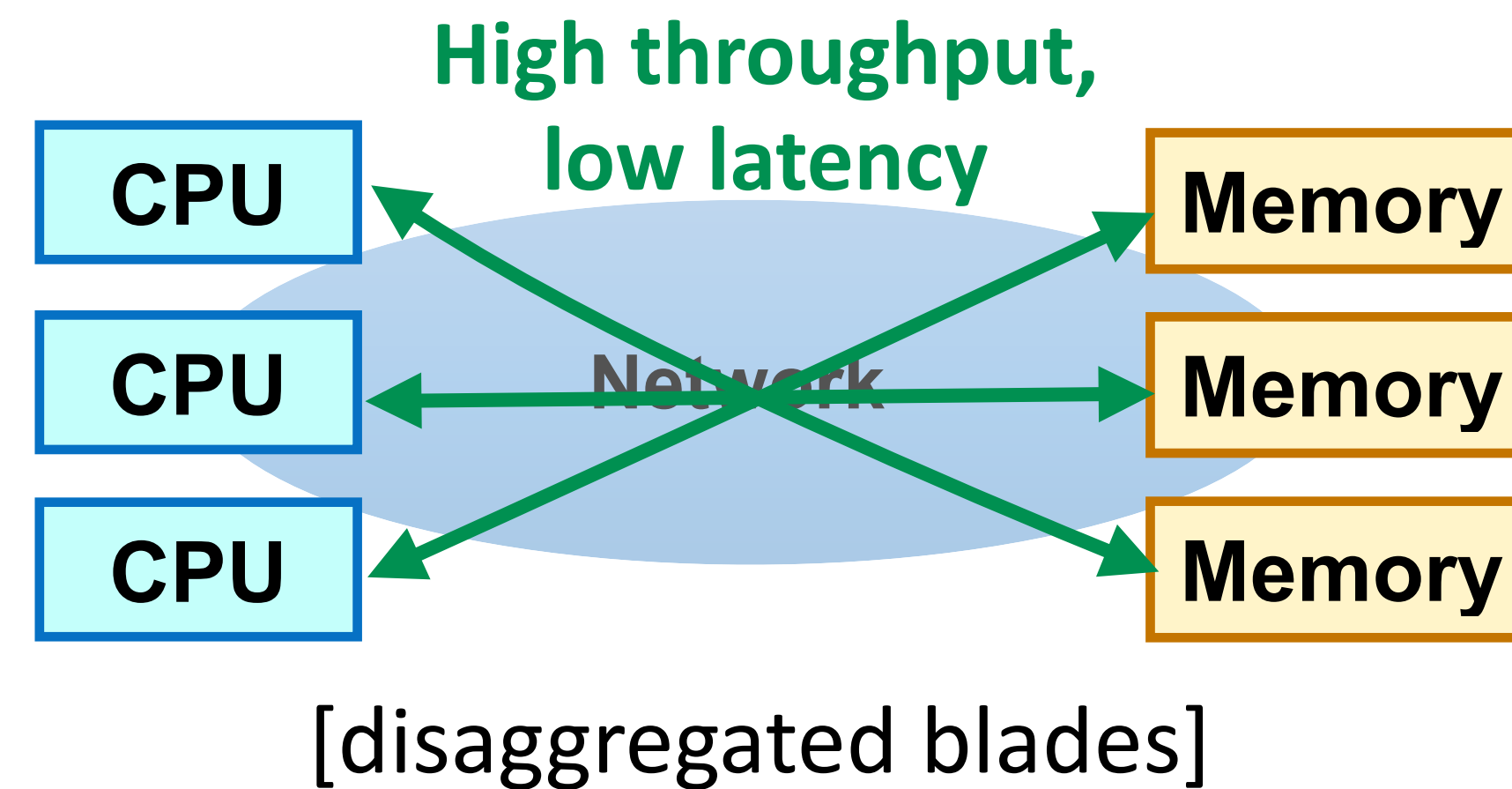
Storage disaggregation is already popular

Memory Disaggregation Goals



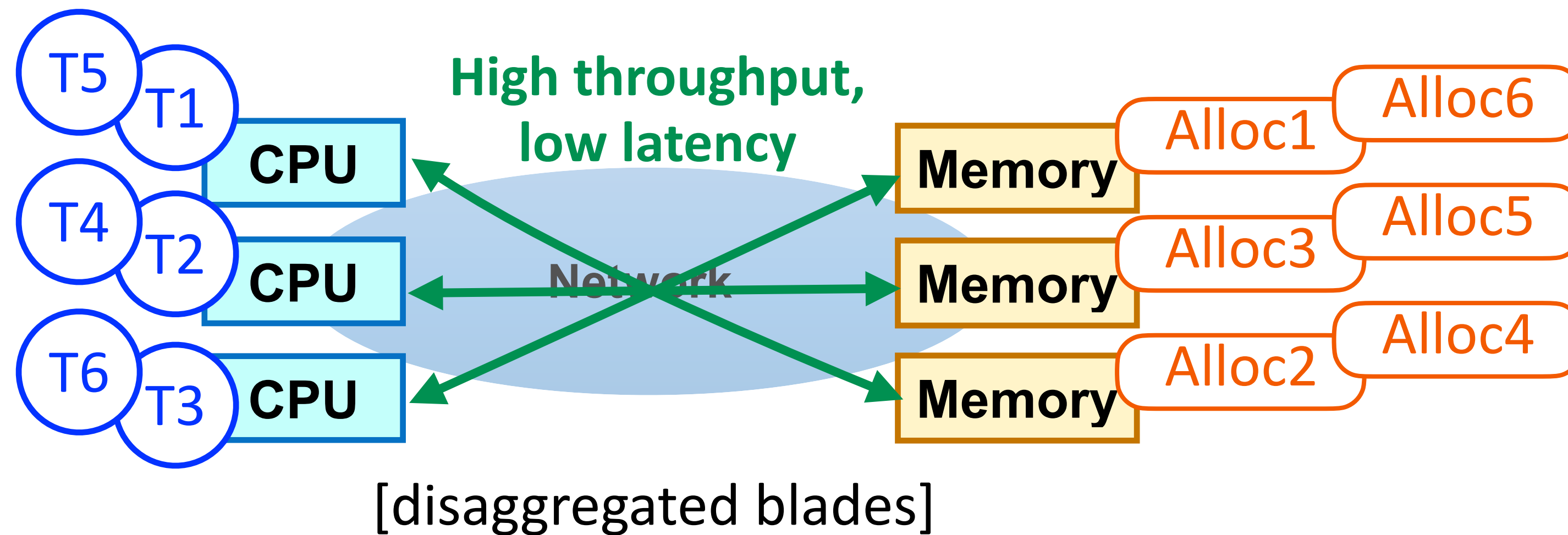
Memory Disaggregation Goals

- Performance (CPU \leftrightarrow memory): high throughput & low latency

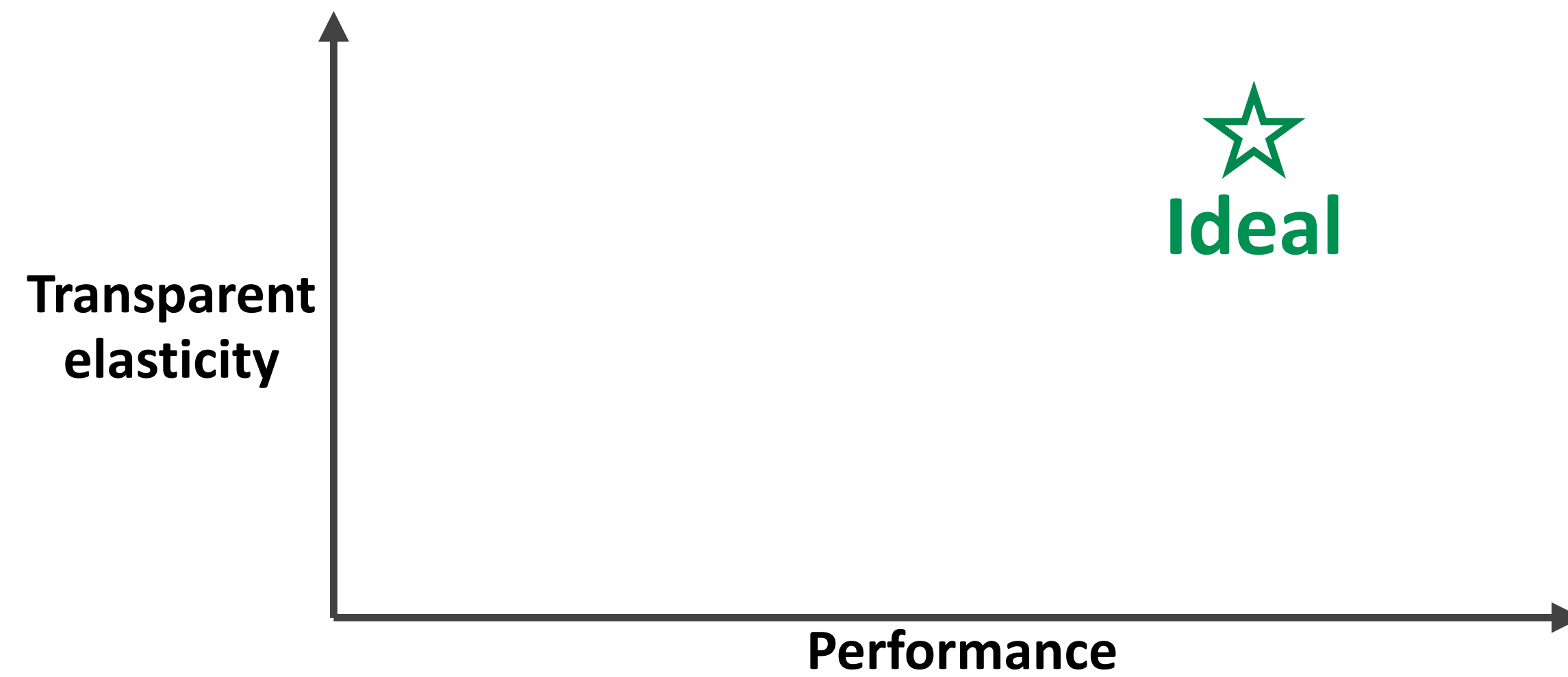


Memory Disaggregation Goals

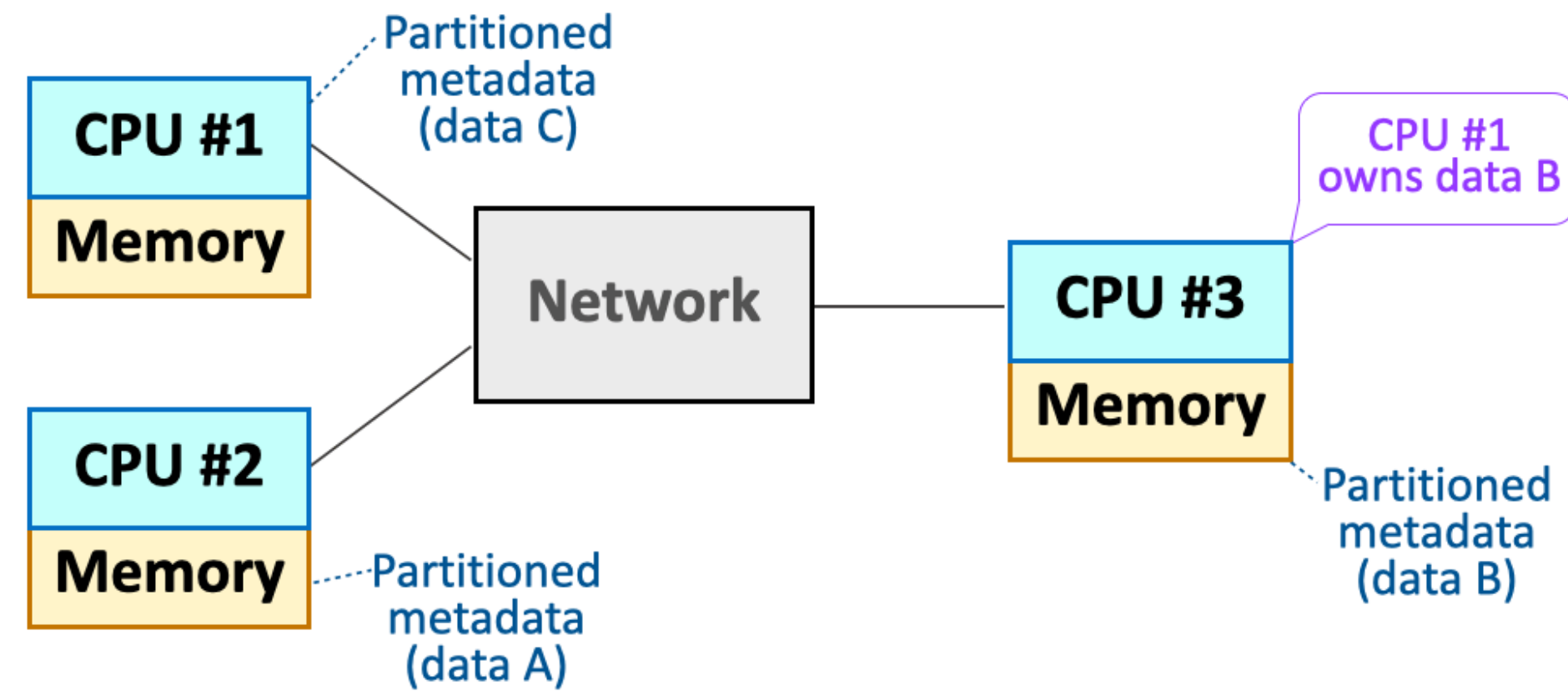
- **Performance (CPU \leftrightarrow memory):** high throughput & low latency
- **Transparent elasticity:** flexible resource allocation



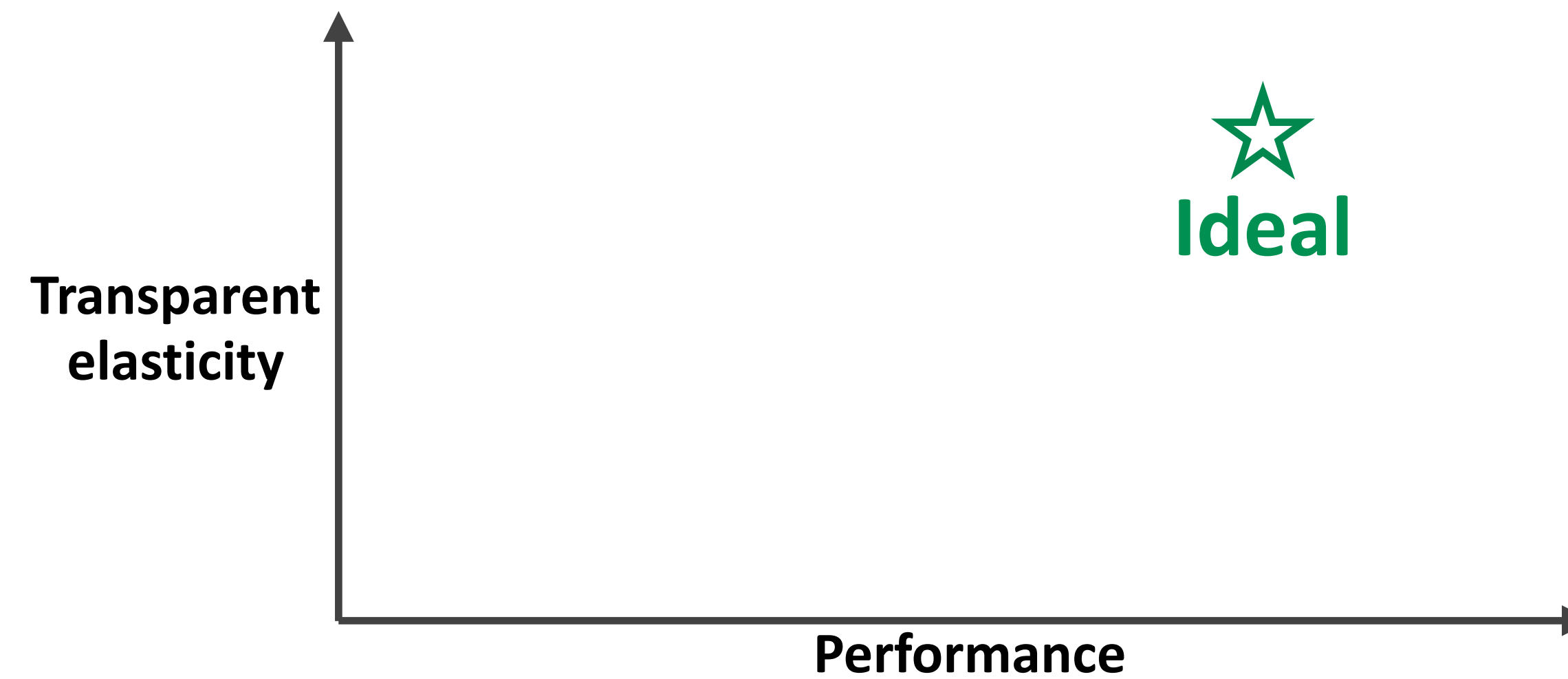
Existing Approaches



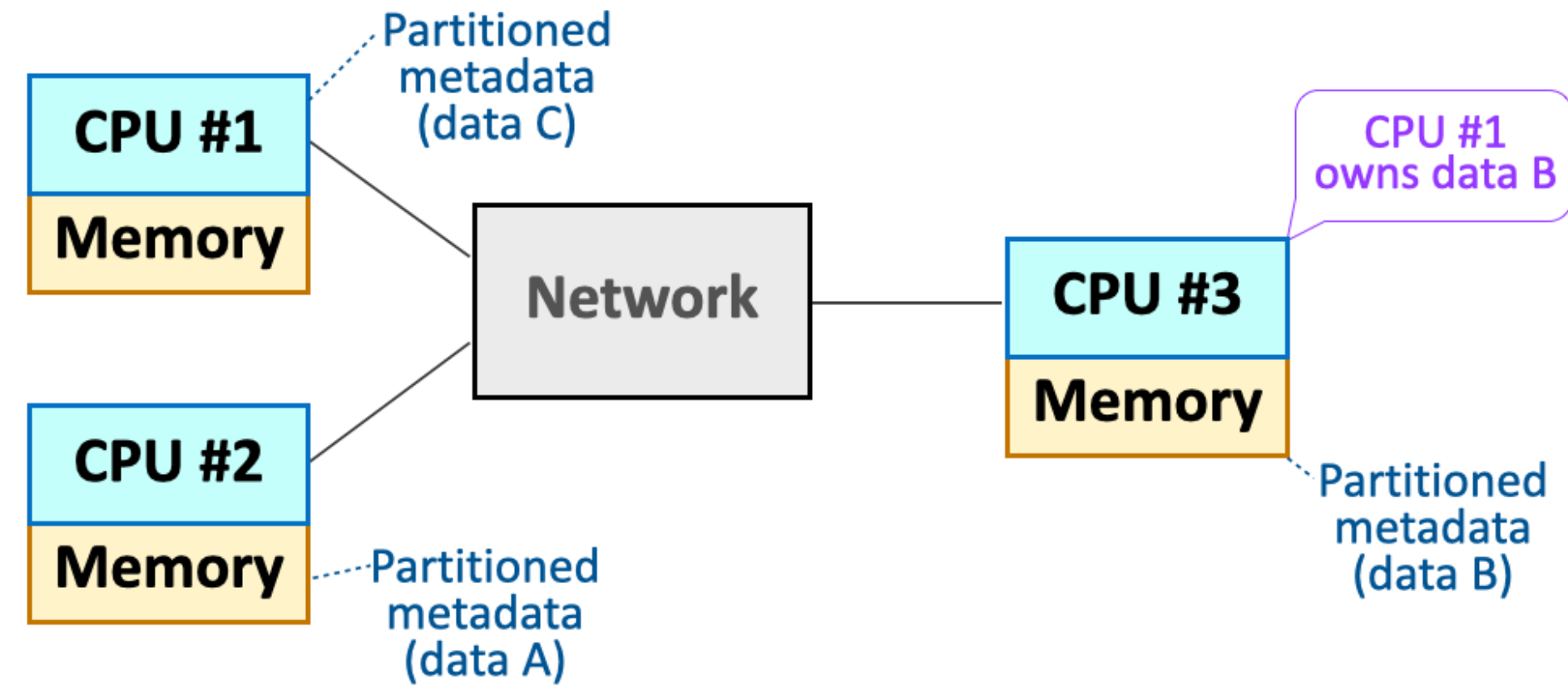
Existing Approaches



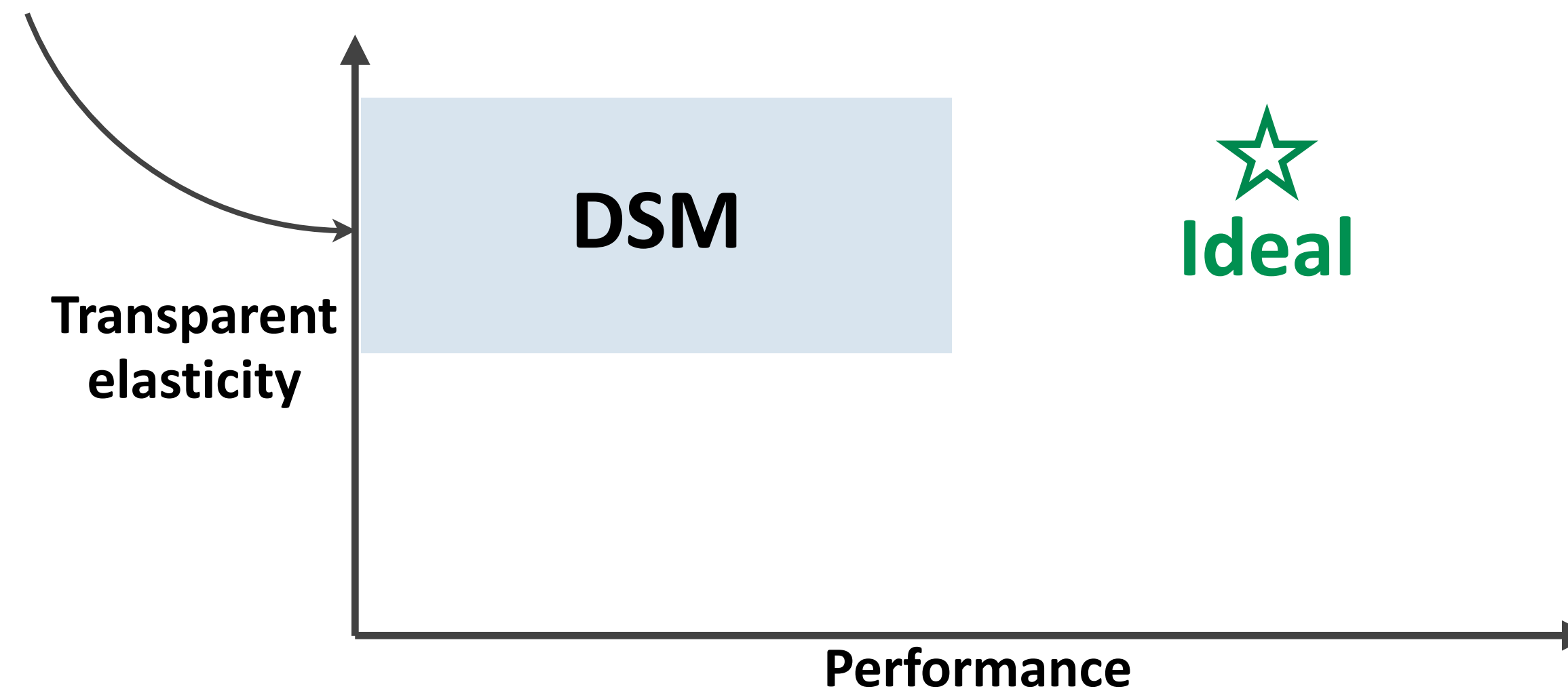
Distributed shared memory (DSM)



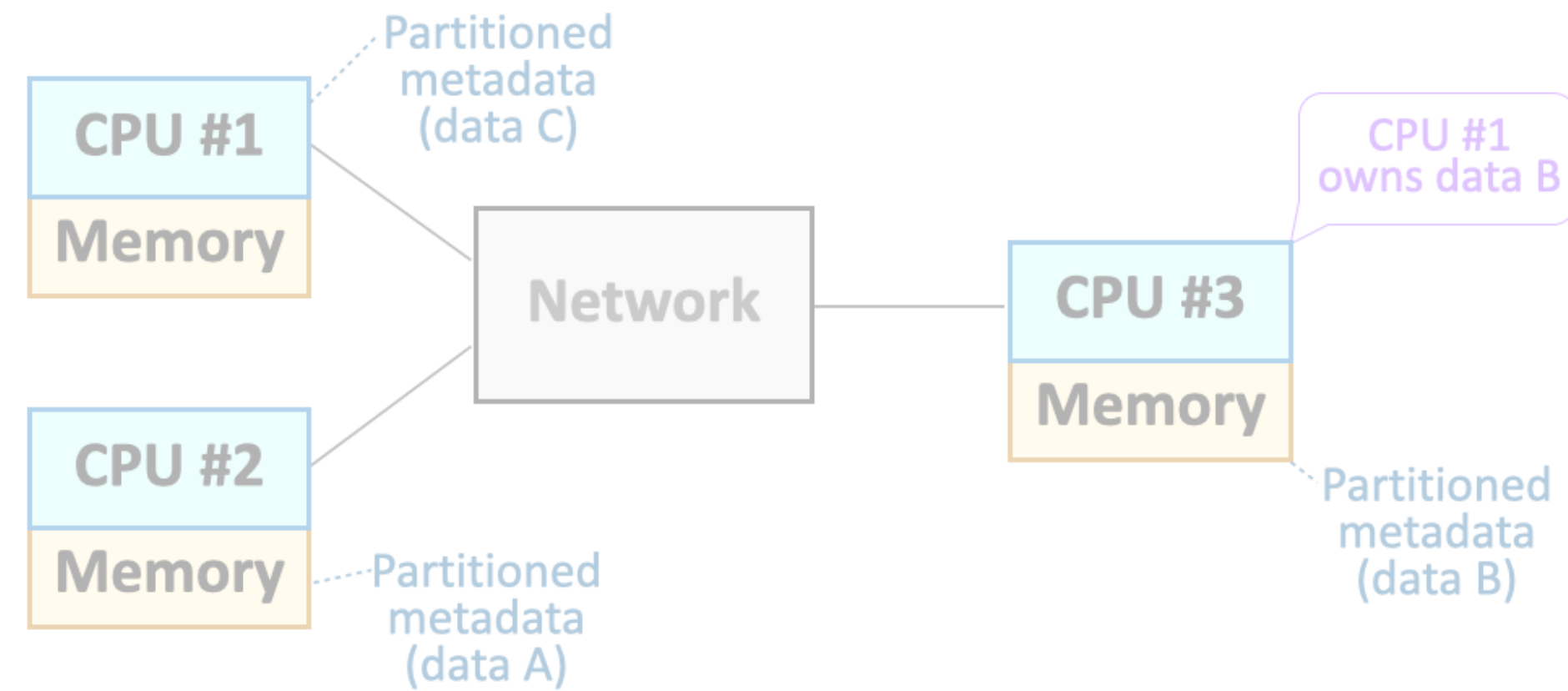
Existing Approaches



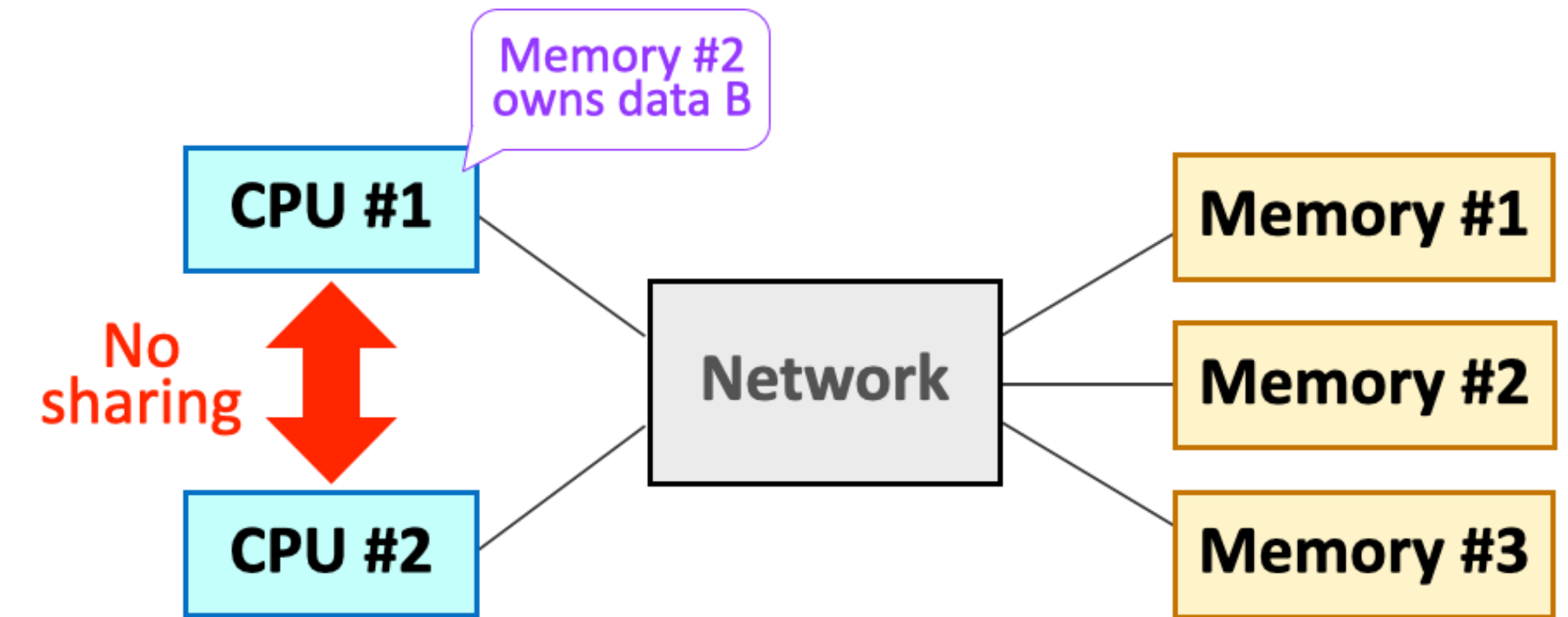
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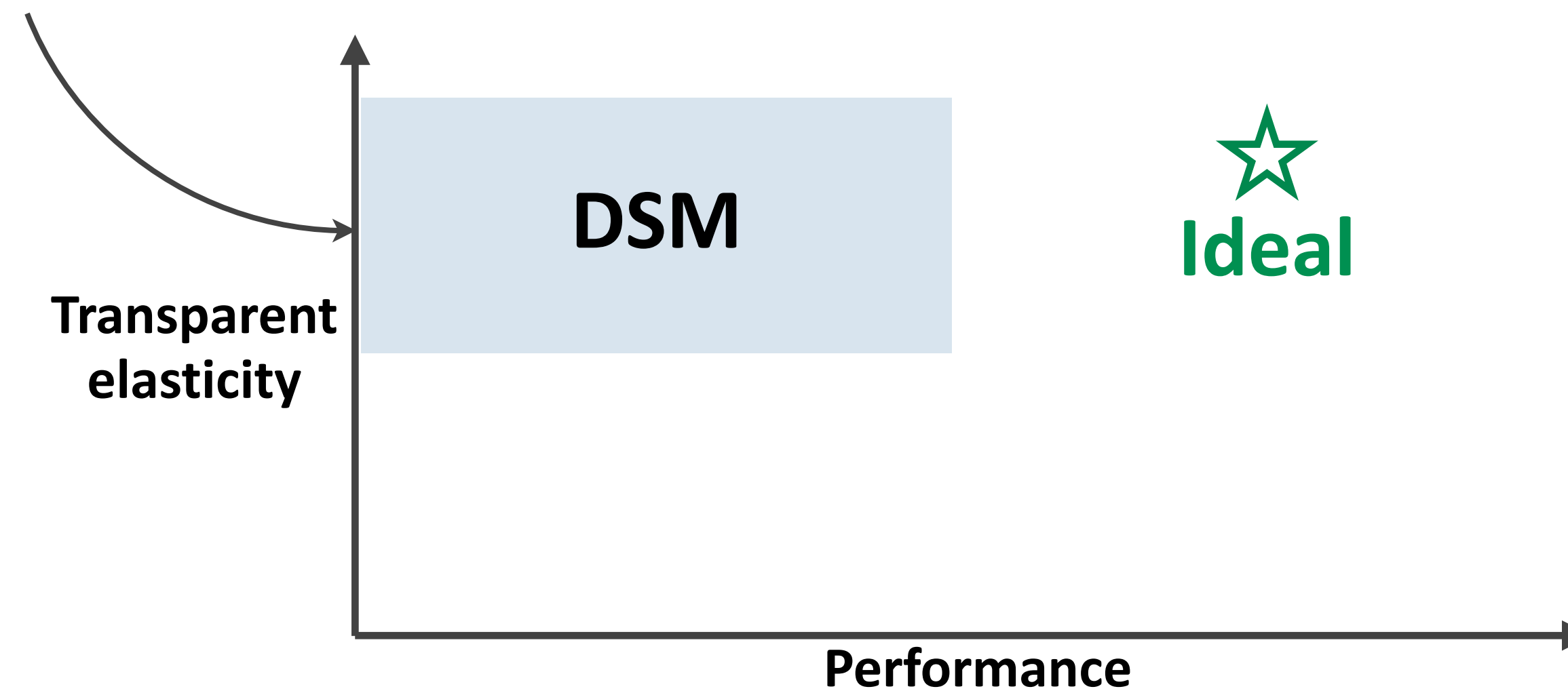
Existing Approaches



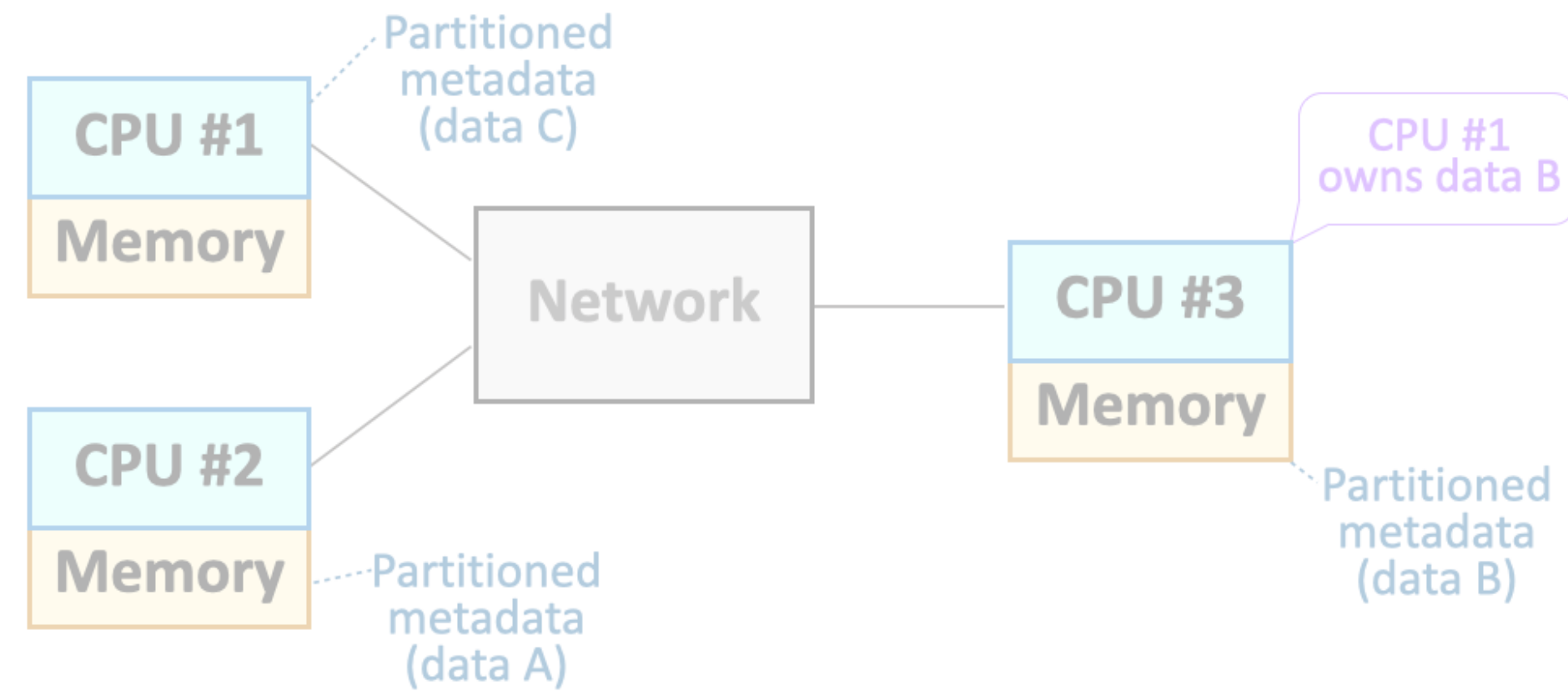
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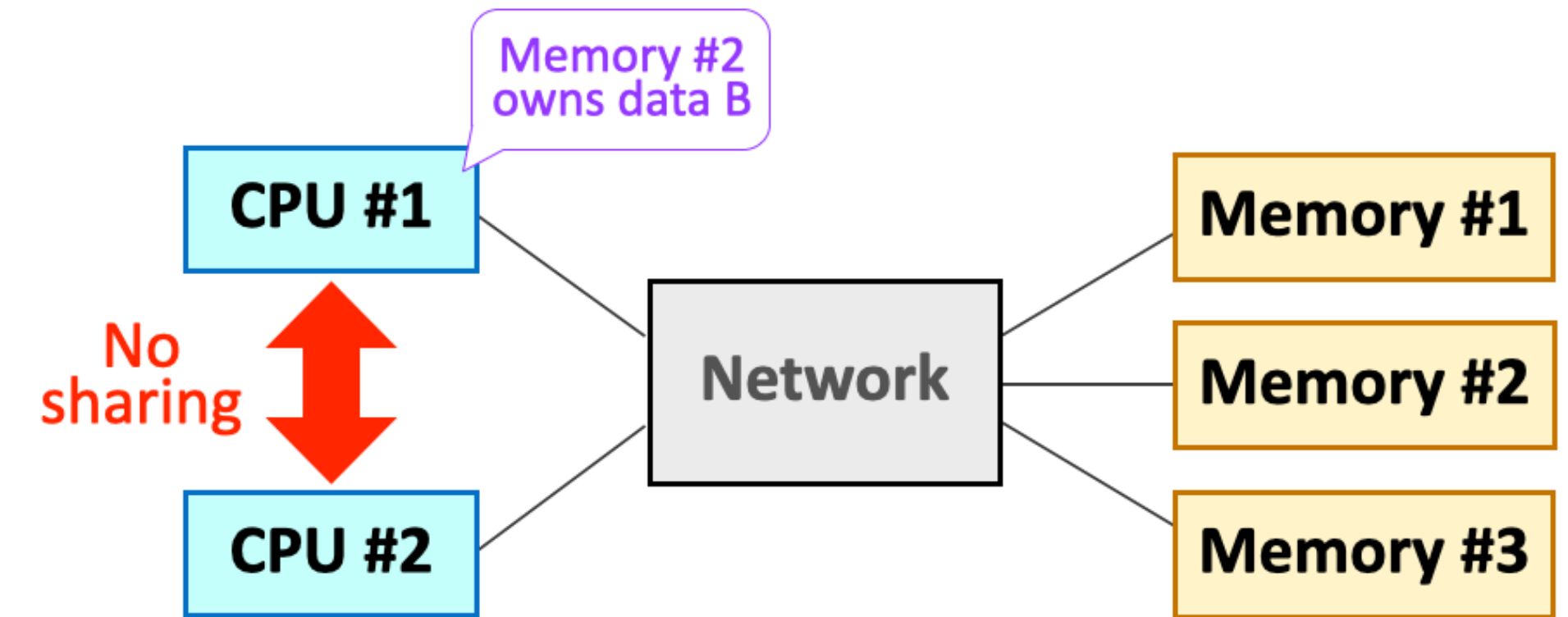
Recent disaggregated memory schemes



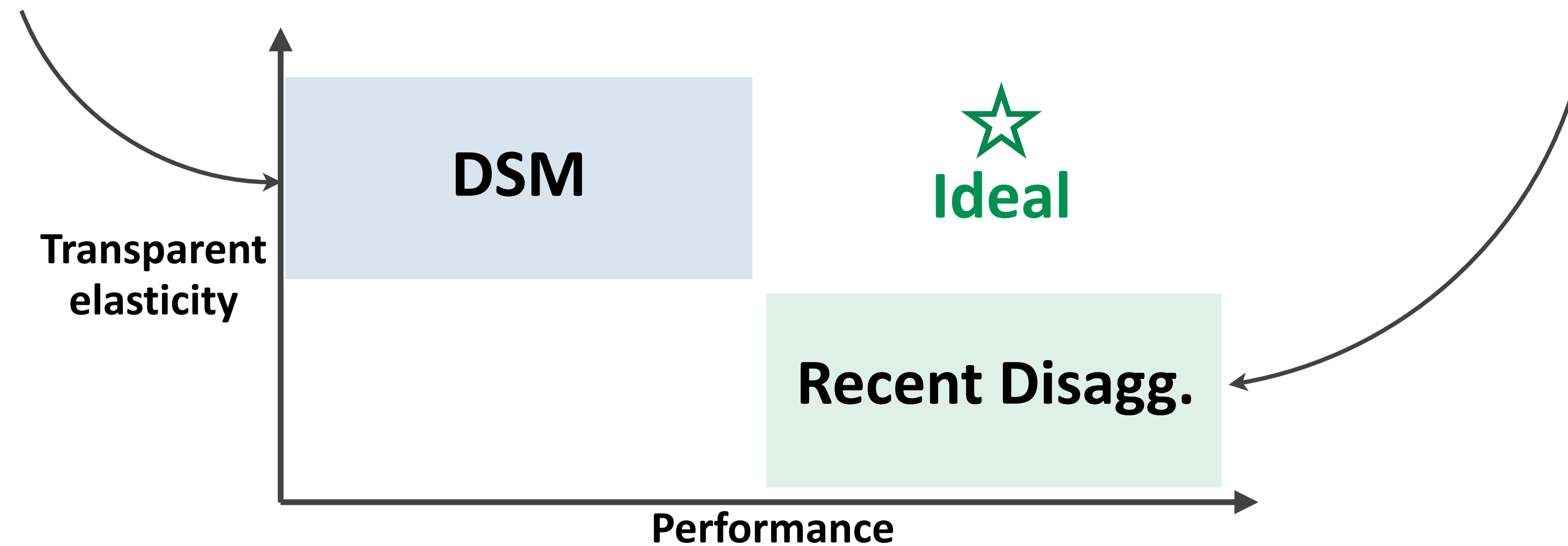
Existing Approaches



Distributed shared memory (DSM)

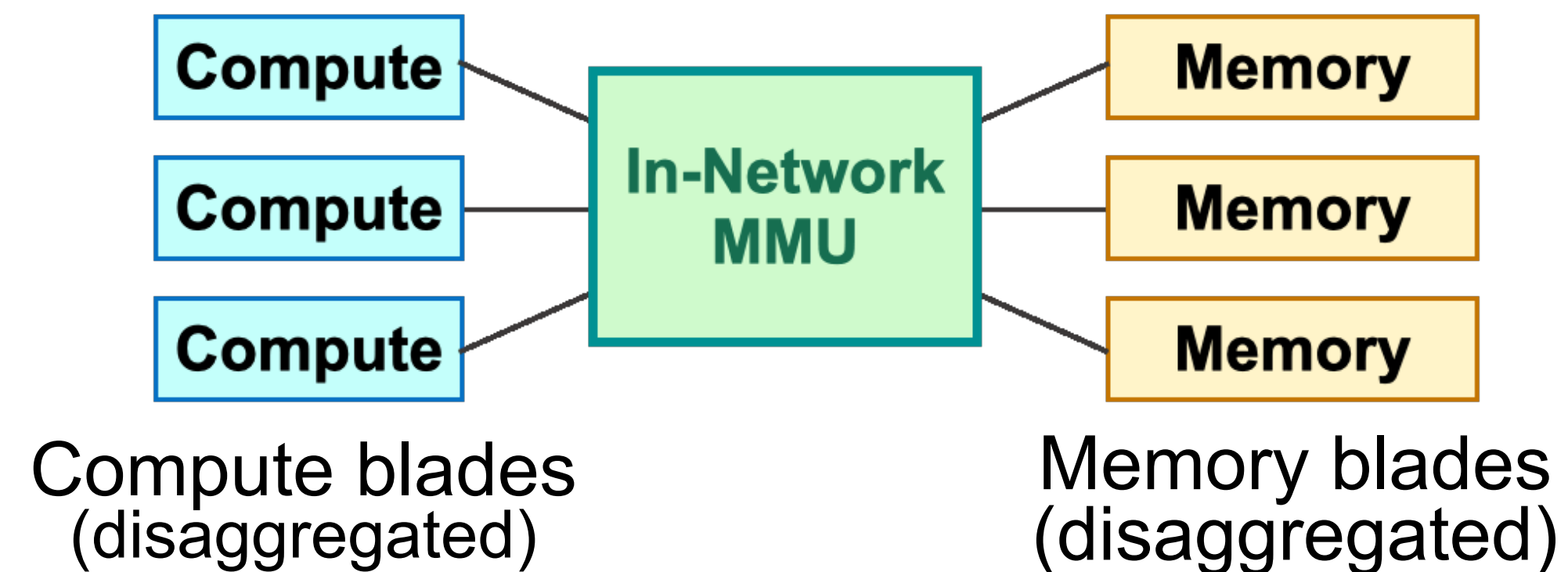


Recent disaggregated memory schemes



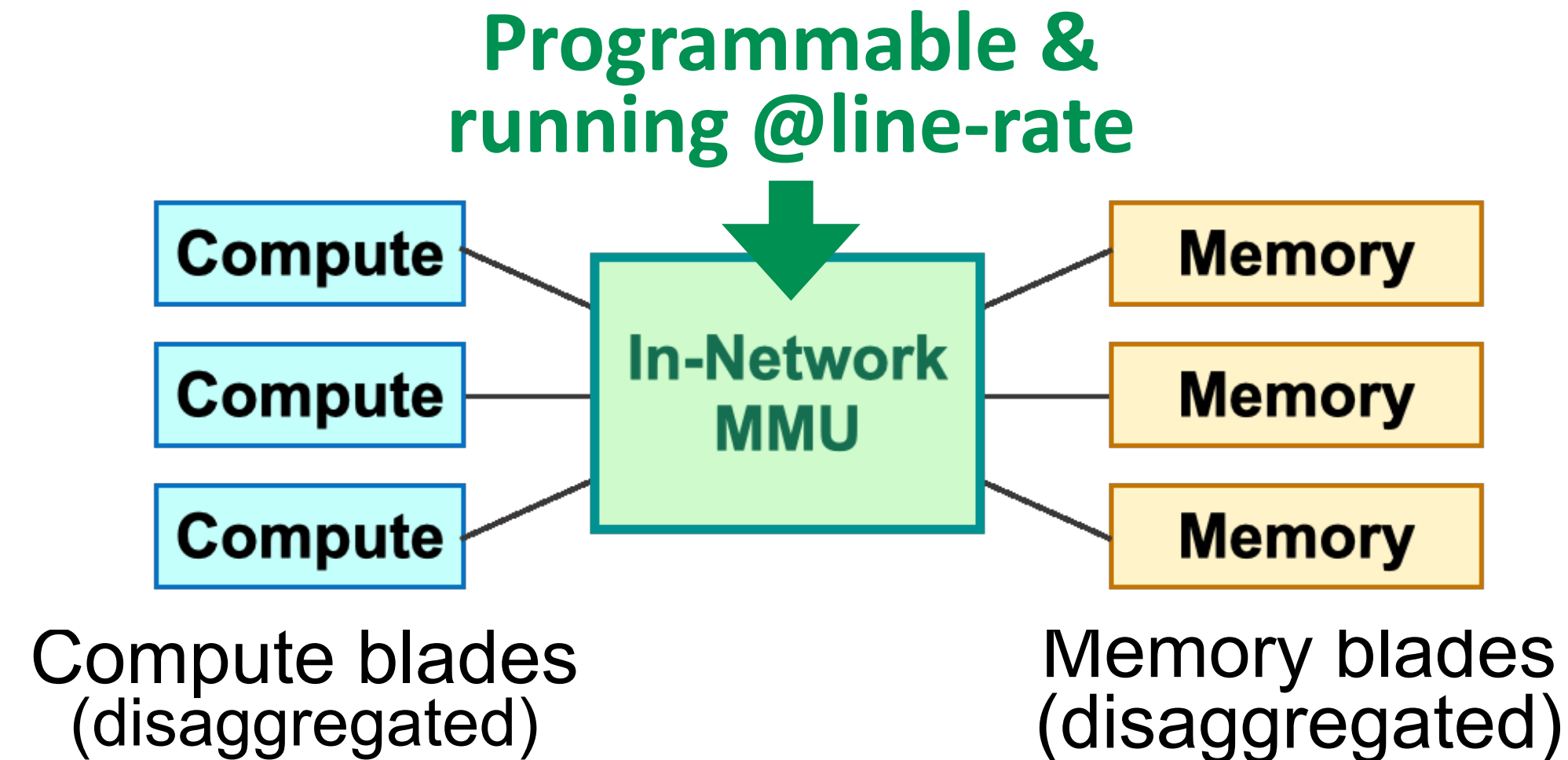
Key Insight — In-network Memory management

- **Central location:** global view & processing directly in the data path



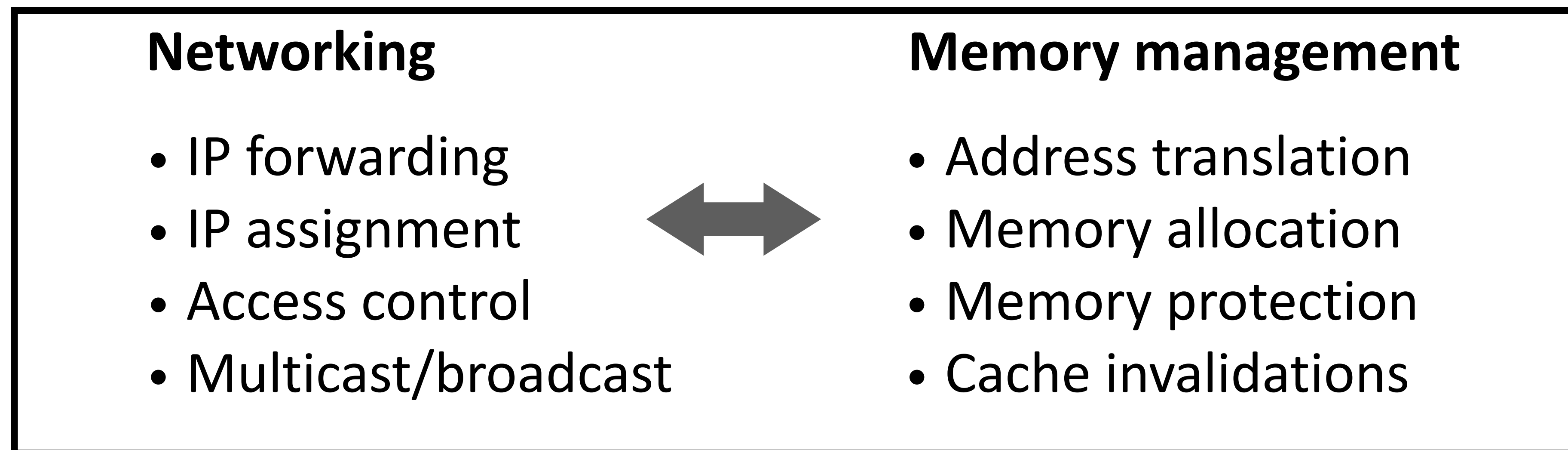
Key Insight — In-network Memory management

- **Central location:** global view & processing directly in the data path
- **Programmable switching ASIC:** flexible processing at line rate

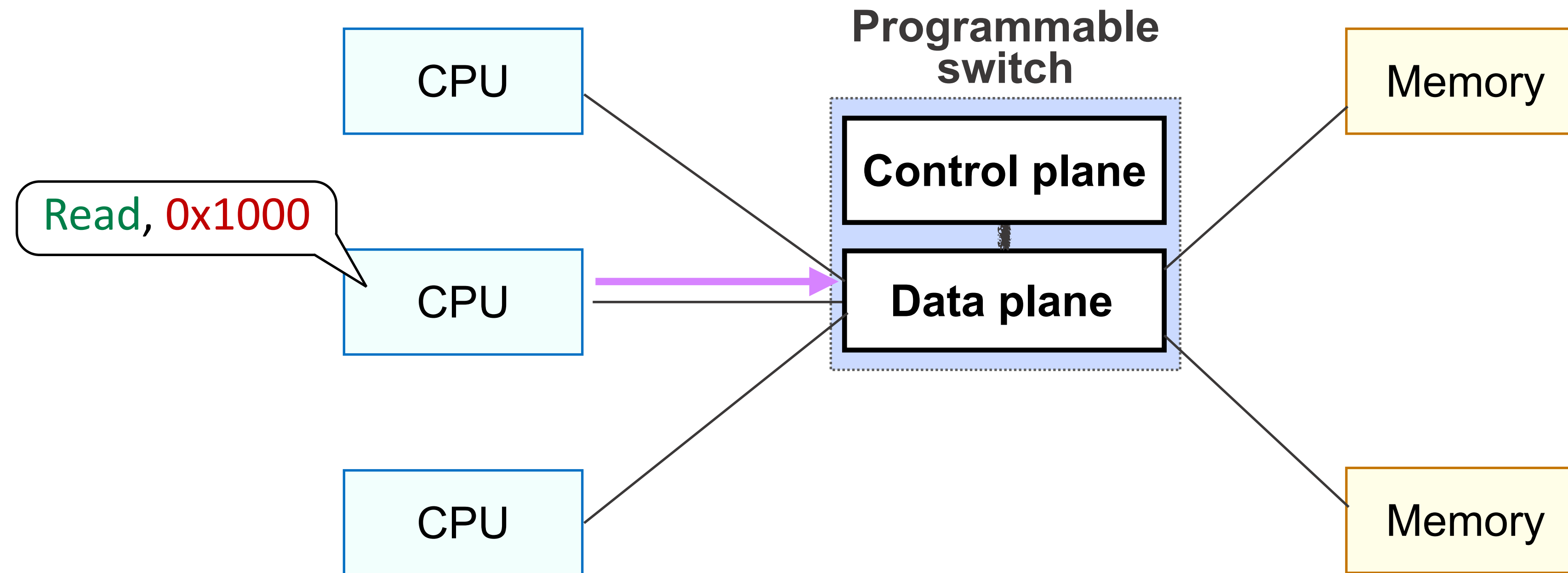


Key Insight — In-network Memory management

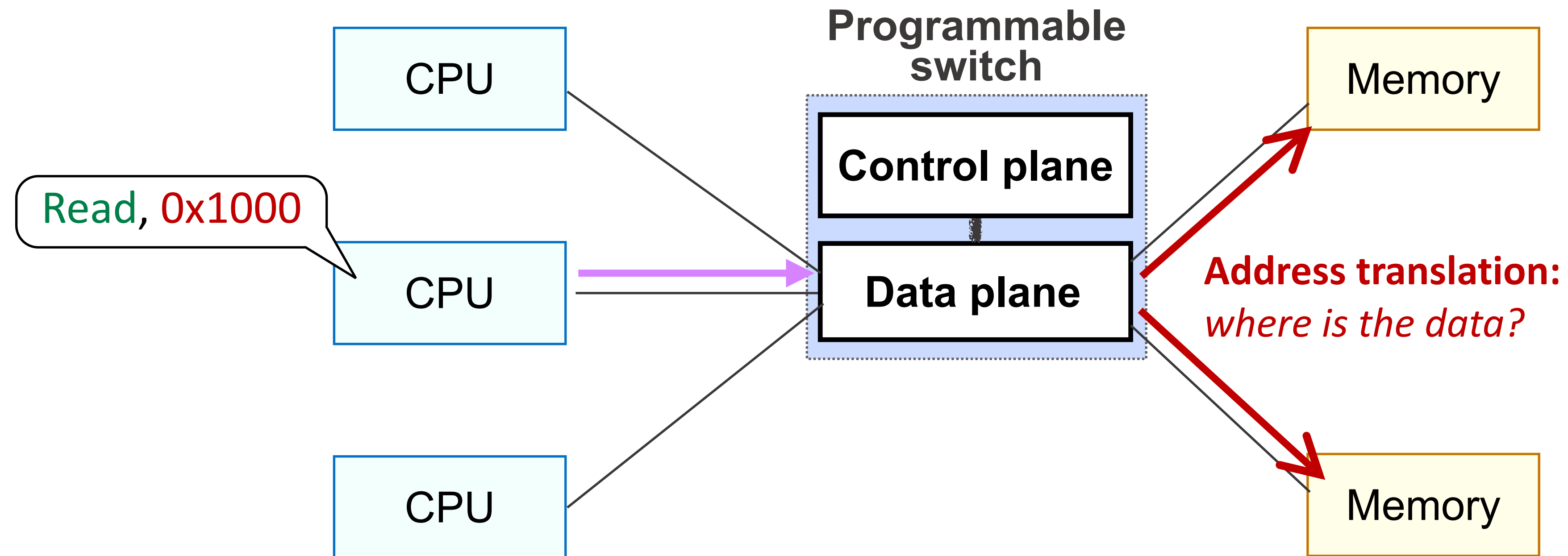
- **Central location:** global view & processing directly in the data path
- **Programmable switching ASIC:** flexible processing at line rate
- **Similarity between network functions and memory management**



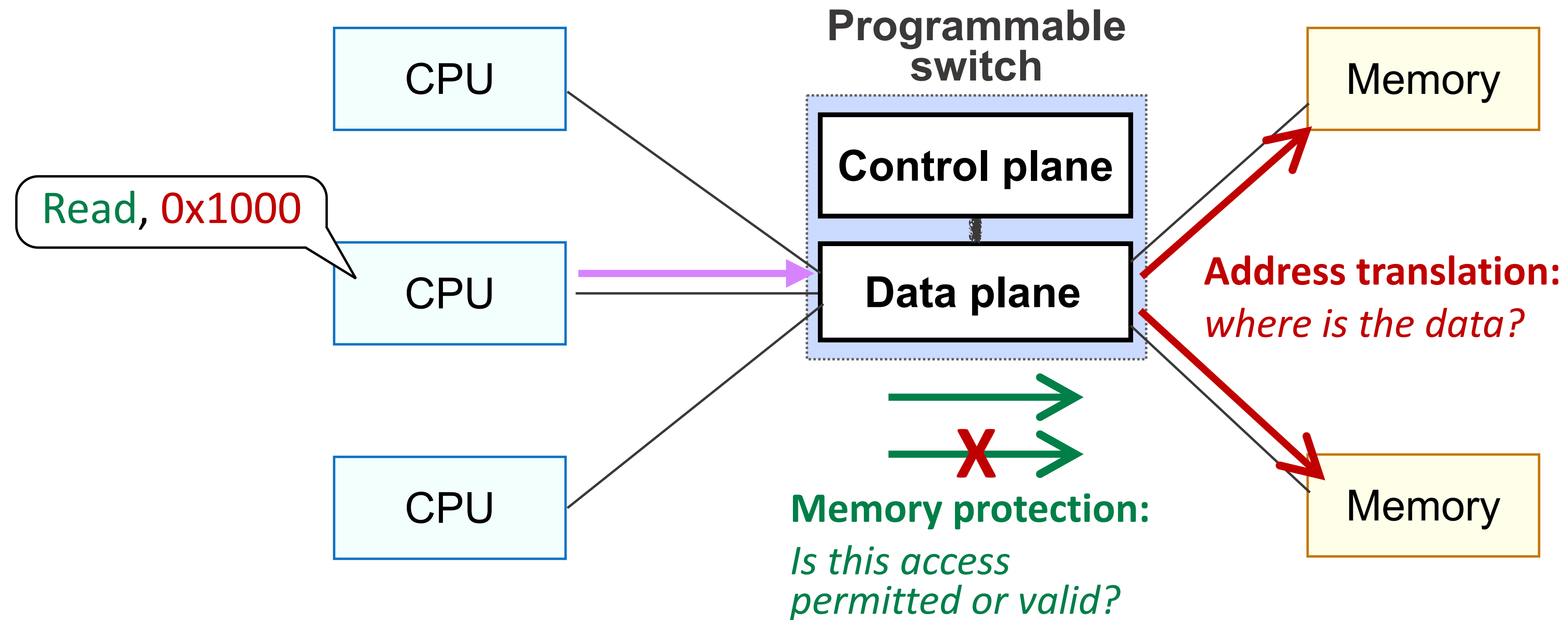
MIND: In-network Memory Management



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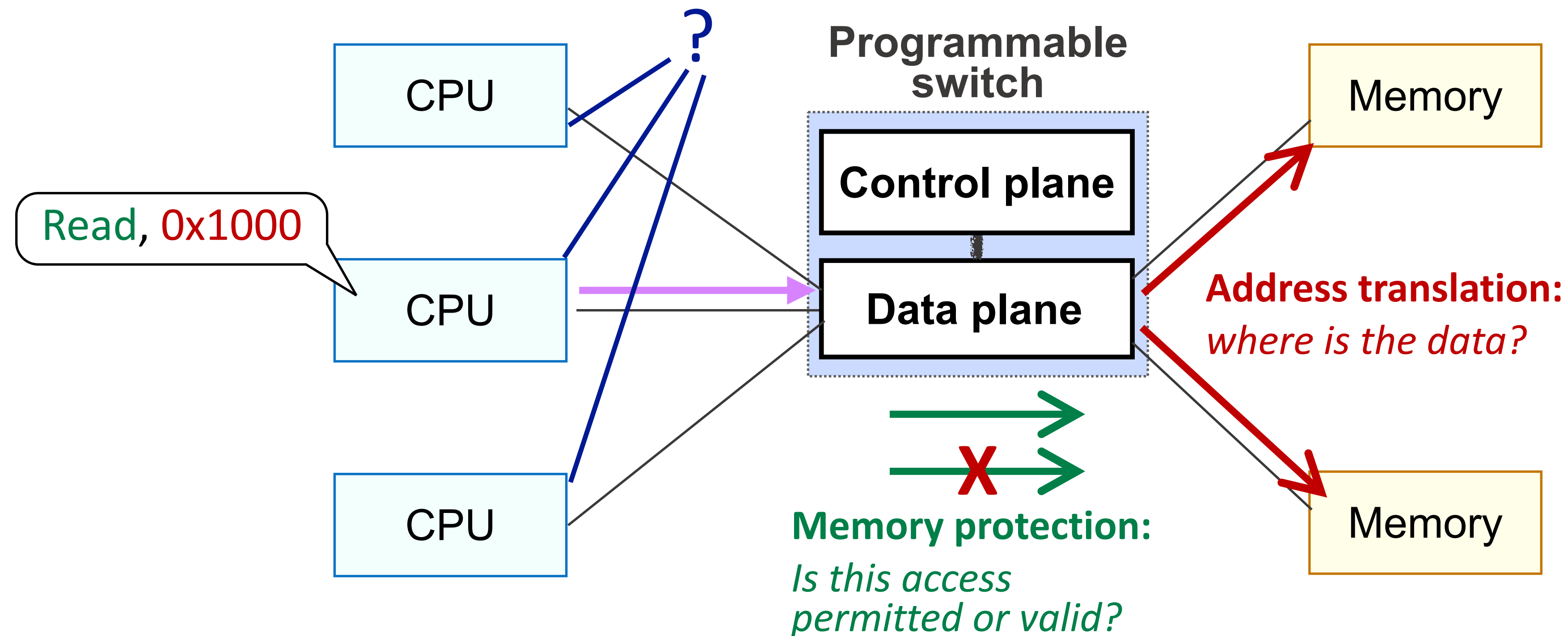


MIND: In-network Memory Management



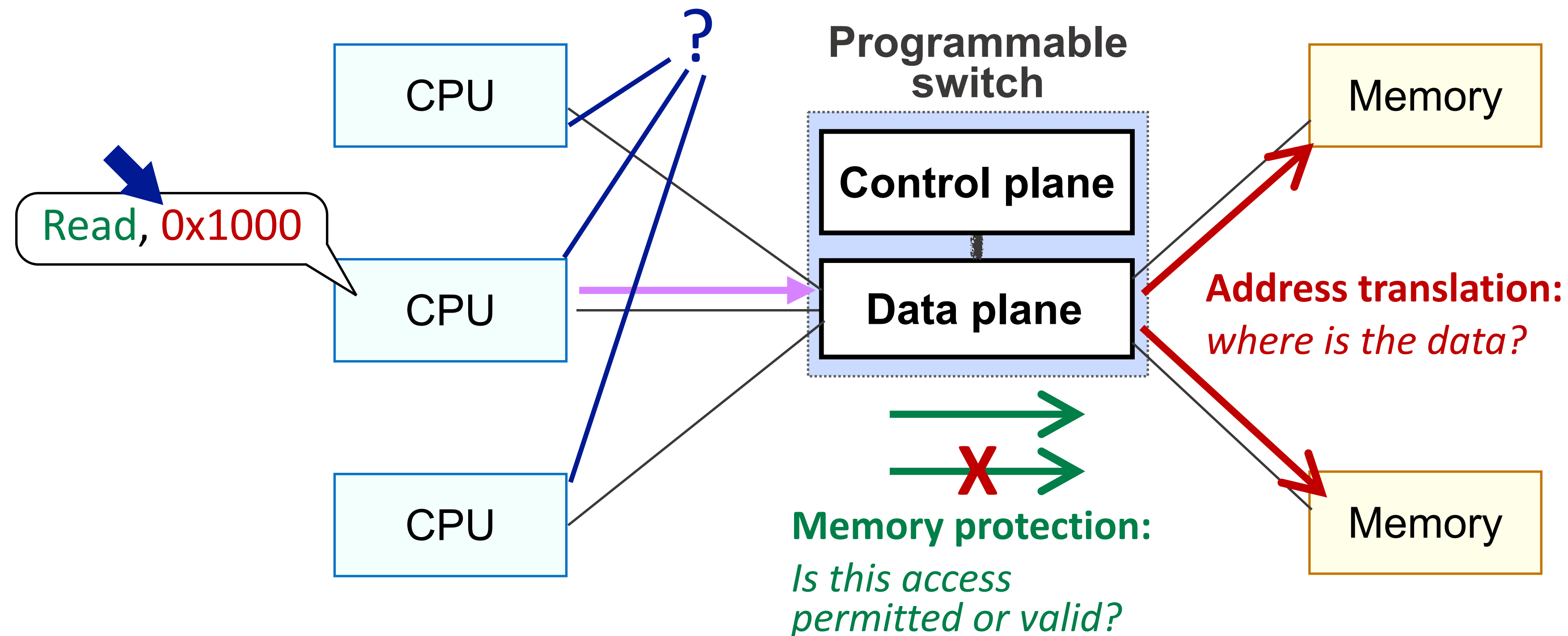
MIND: In-network Memory Management

Cache coherence protocol:
how to keep data synchronized?



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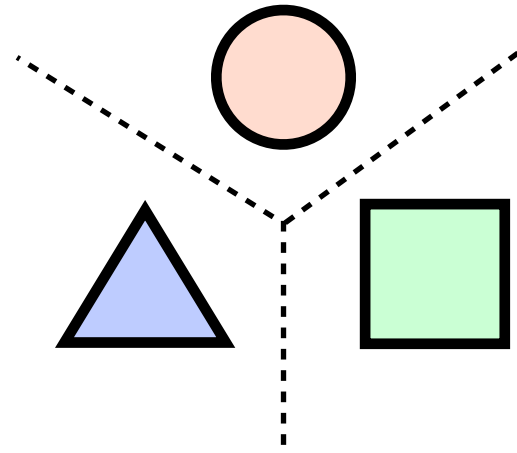
Challenges in Building In-network MMU

- Limited amount of in-network resources
 - *Limited size of in-network memory*
 - Tens of MB → not sufficient to store metadata in a traditional way
 - E.g., page table: 4 KB for 4GB of memory → 1M entries

Challenges in Building In-network MMU

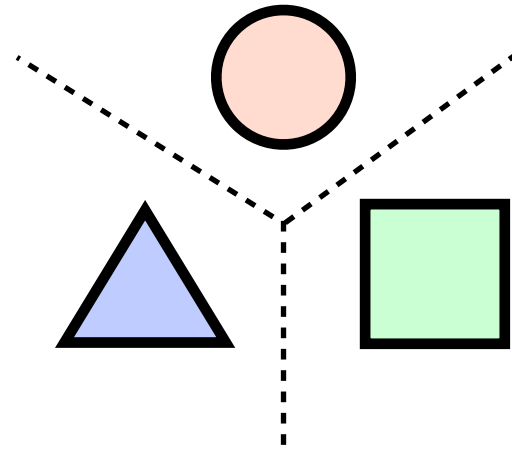
- Limited amount of in-network resources
 - *Limited size of in-network memory*
 - Tens of MB → not sufficient to store metadata in a traditional way
 - E.g., page table: 4 KB for 4GB of memory → 1M entries
 - *Limited computation capability*
 - Switching ASIC → not sufficient to directly port traditional MMU functions
 - E.g., limited number of operations for line rate processing
↔ complicated cache coherence protocol

3 Principles for System Design

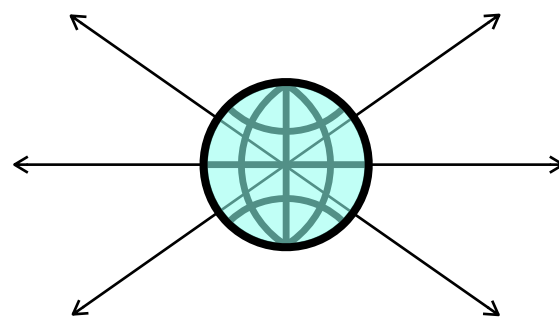


- **P1 - Decouple memory management functionalities**
→ *Each function has the data structure suitable to its purpose*

3 Principles for System Design

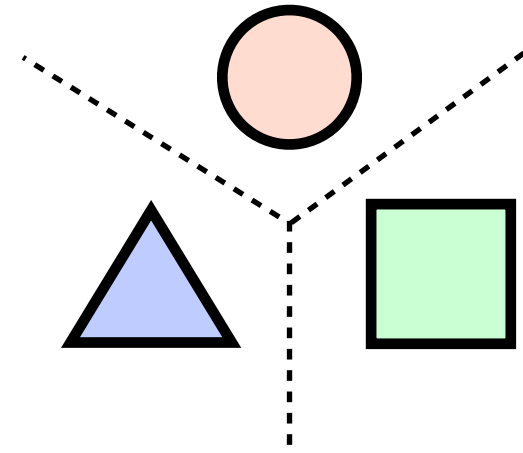


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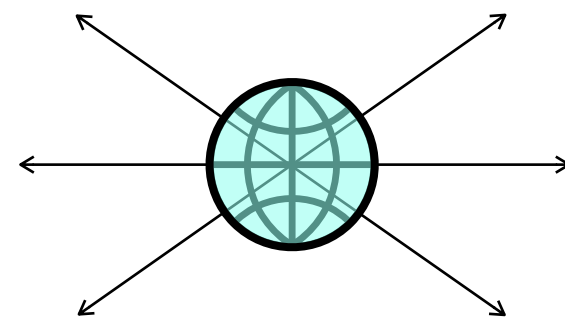


- **P2 - Leverage global view of network**
→ *Make better decisions for memory management*

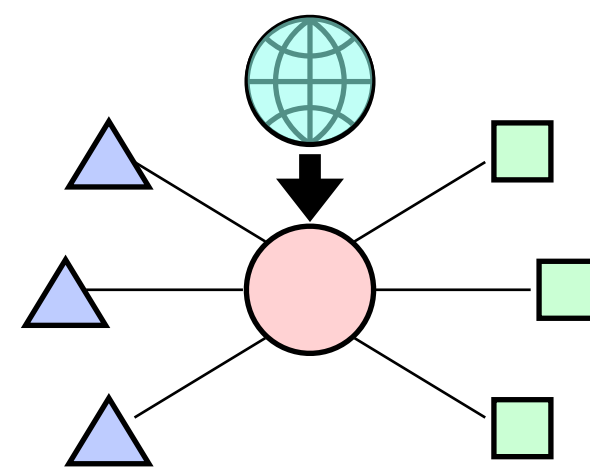
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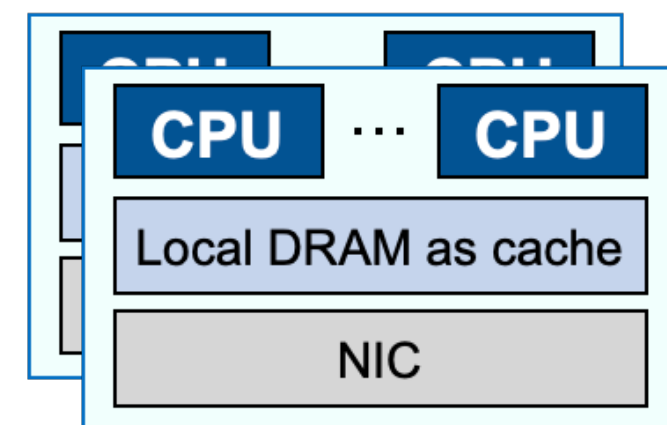
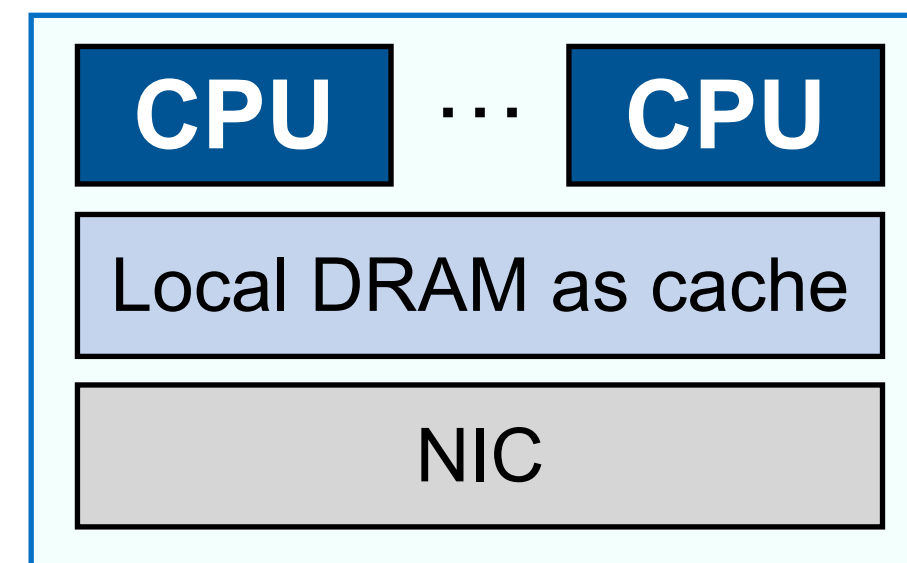


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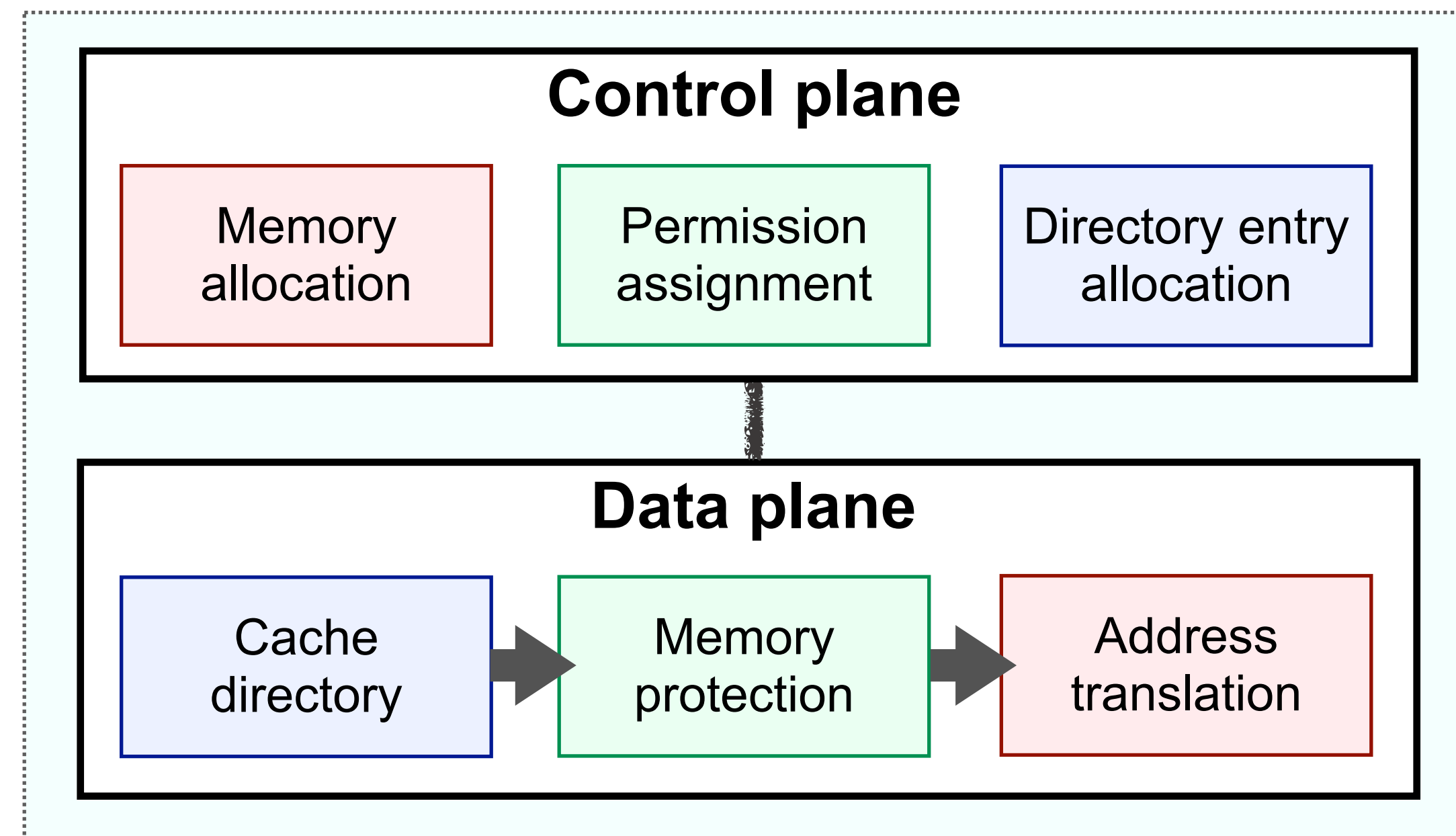


- **P3 - Exploit network-centric hardware primitives**
→ *Reuse network hardware highly optimized for network functions*

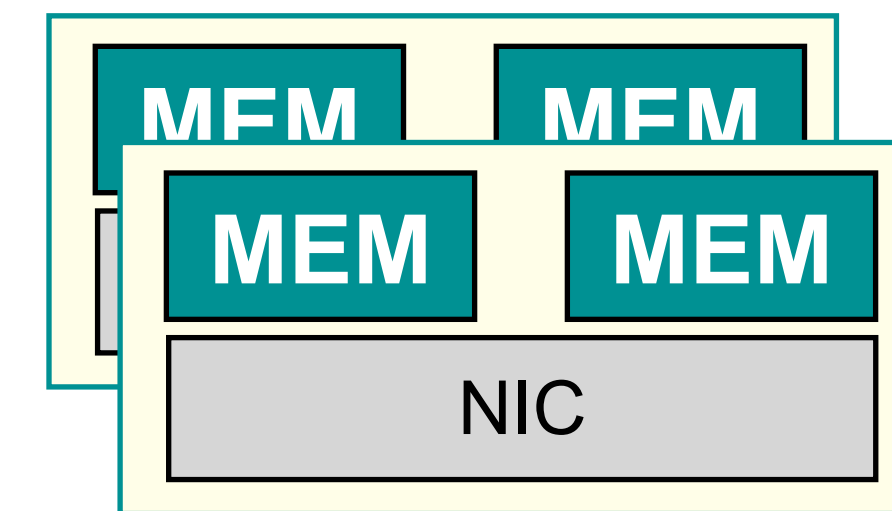
MIND overview: challenges and solutions



Compute blades

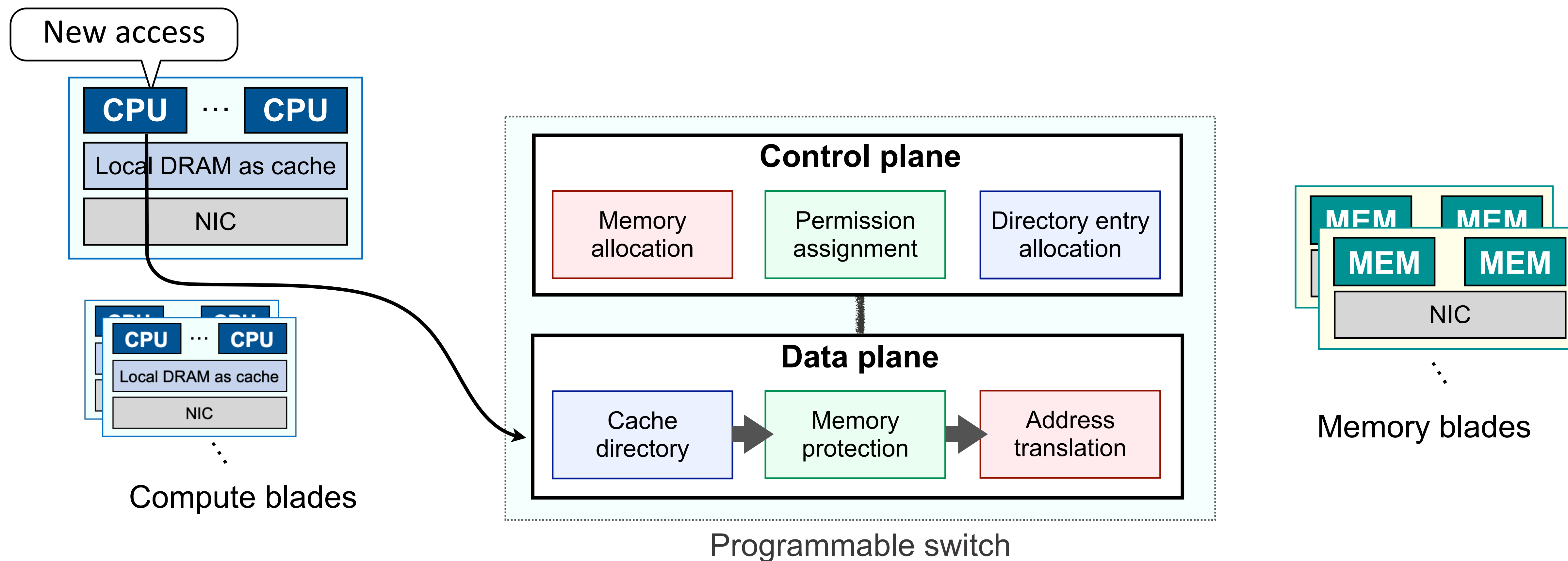


Programmable switch

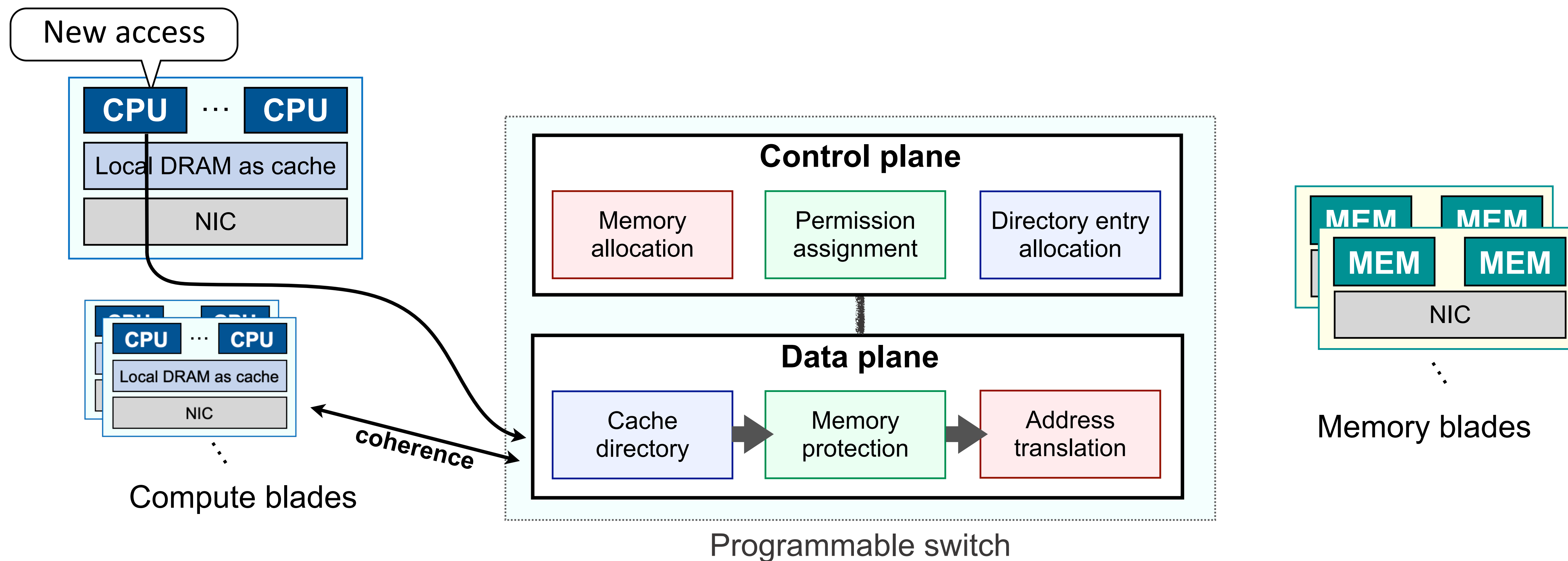


Memory blades

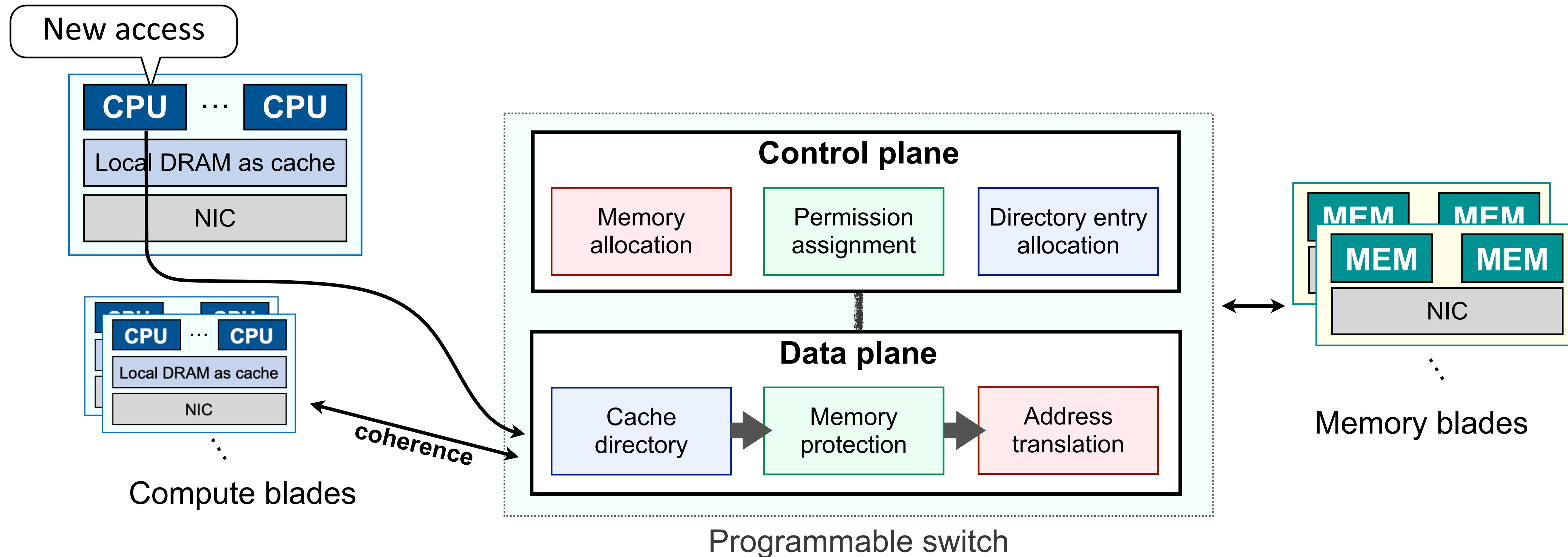
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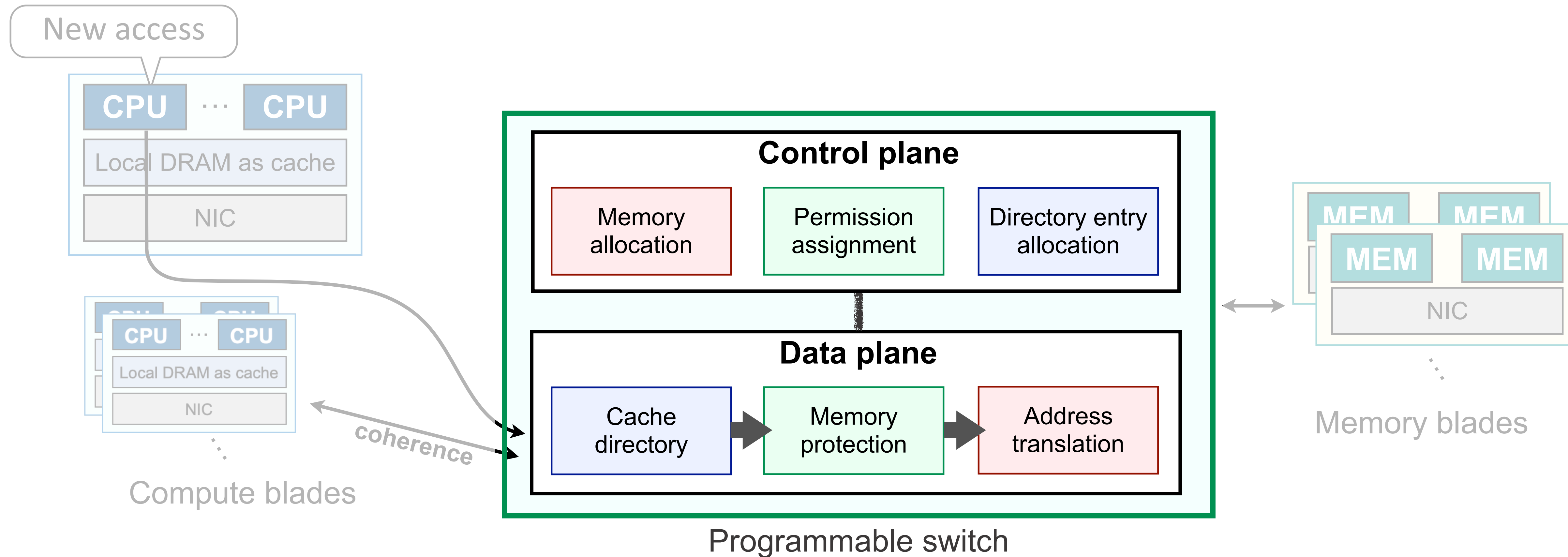
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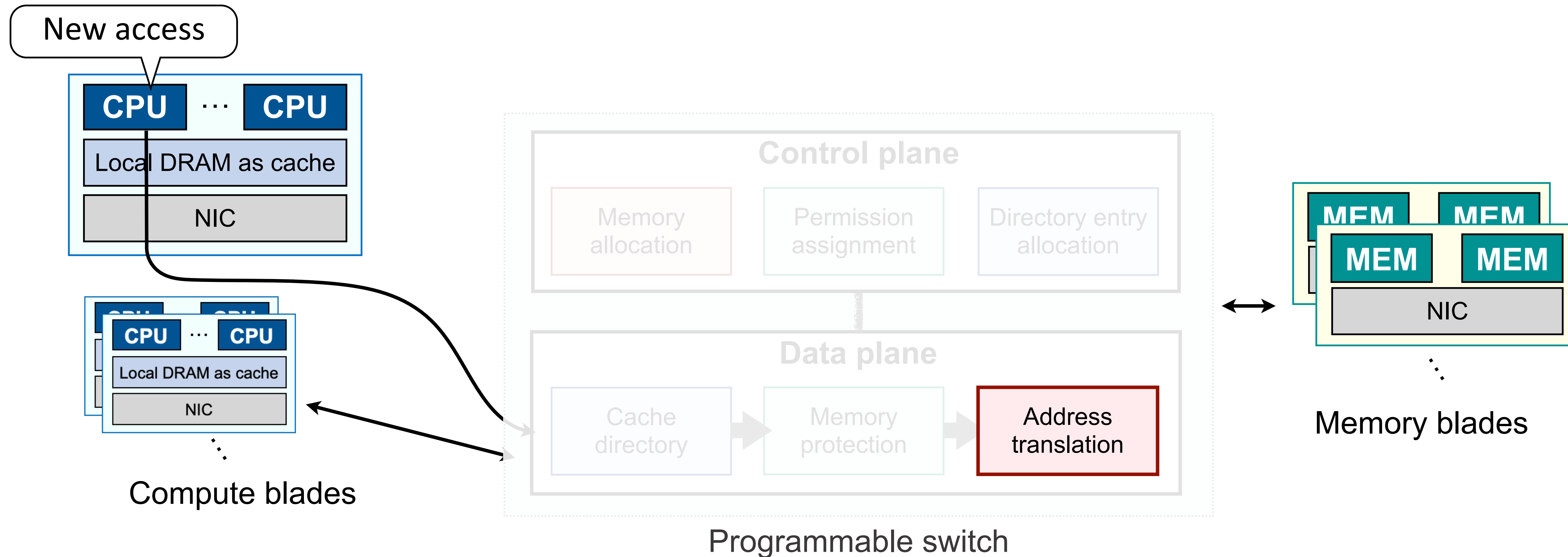
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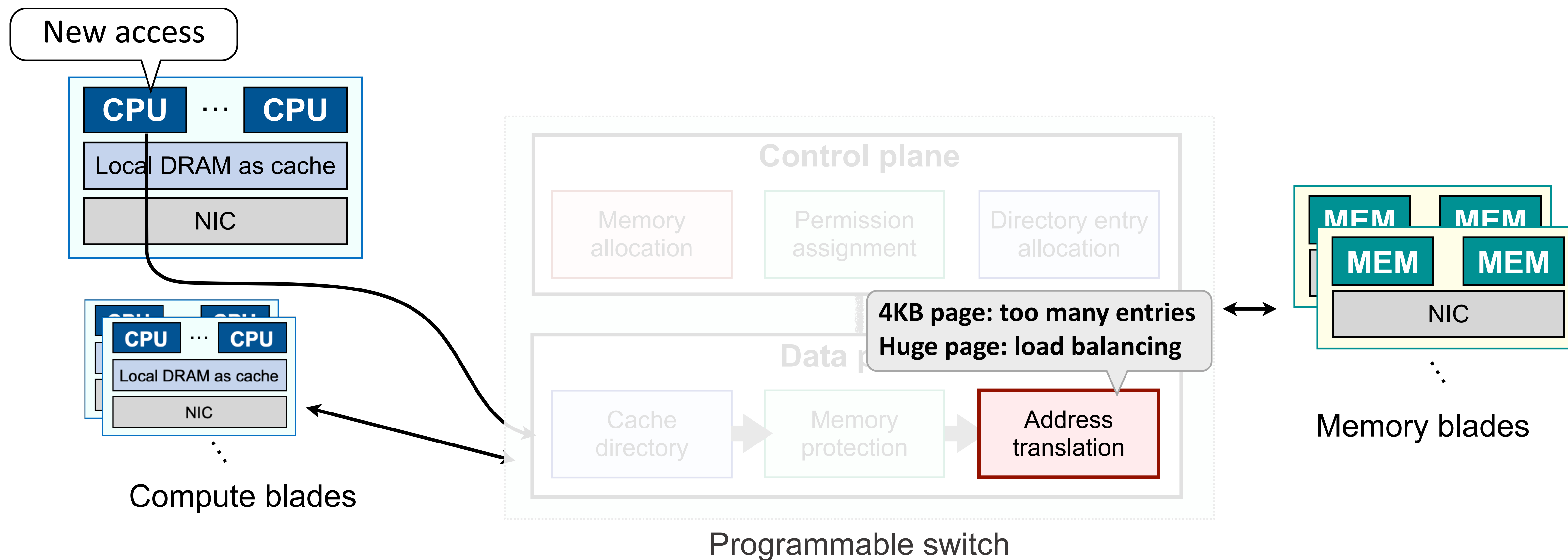
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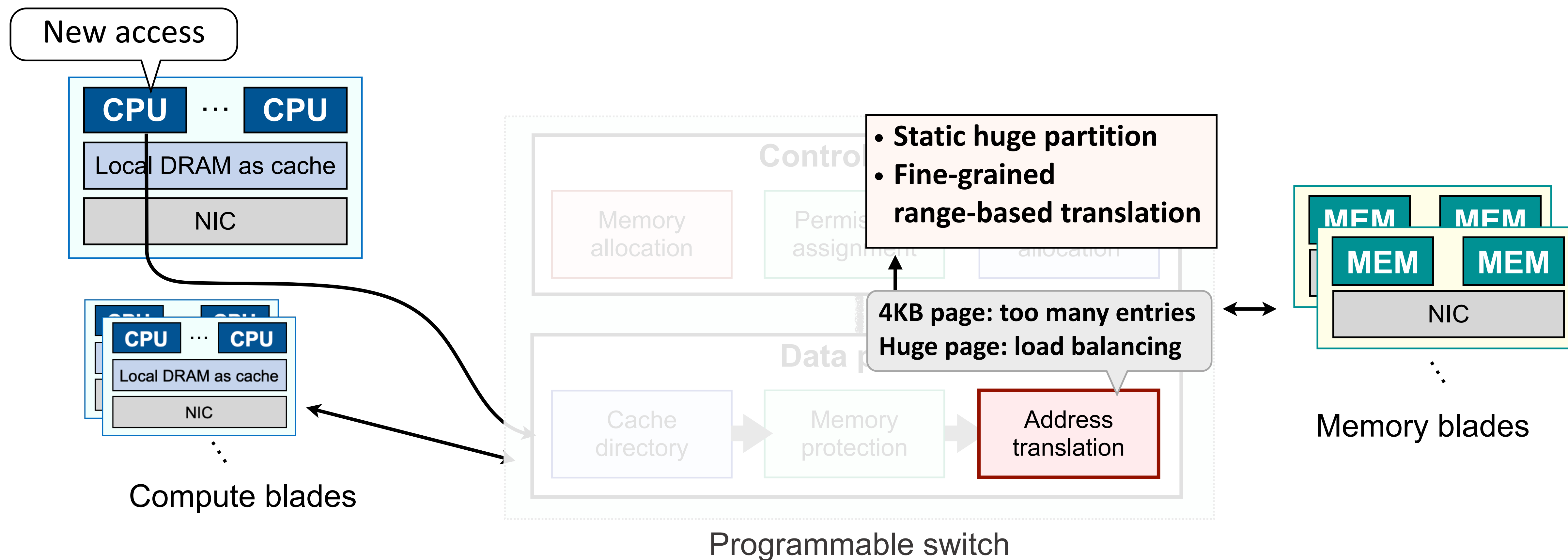
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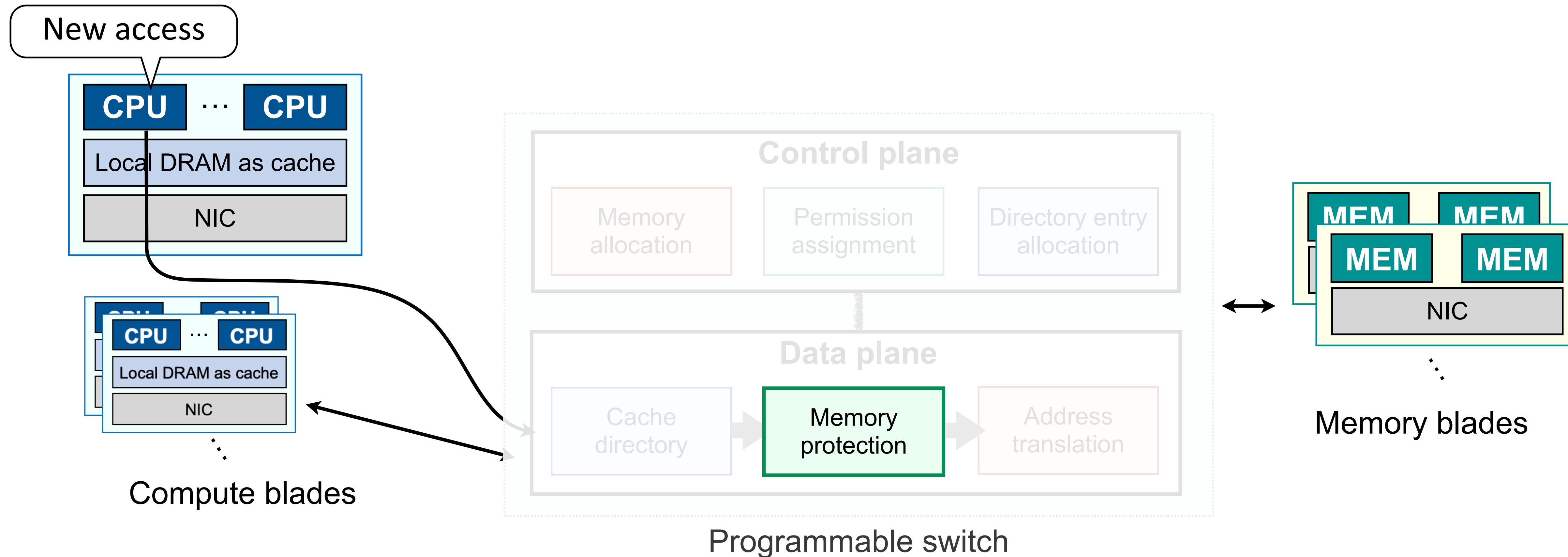
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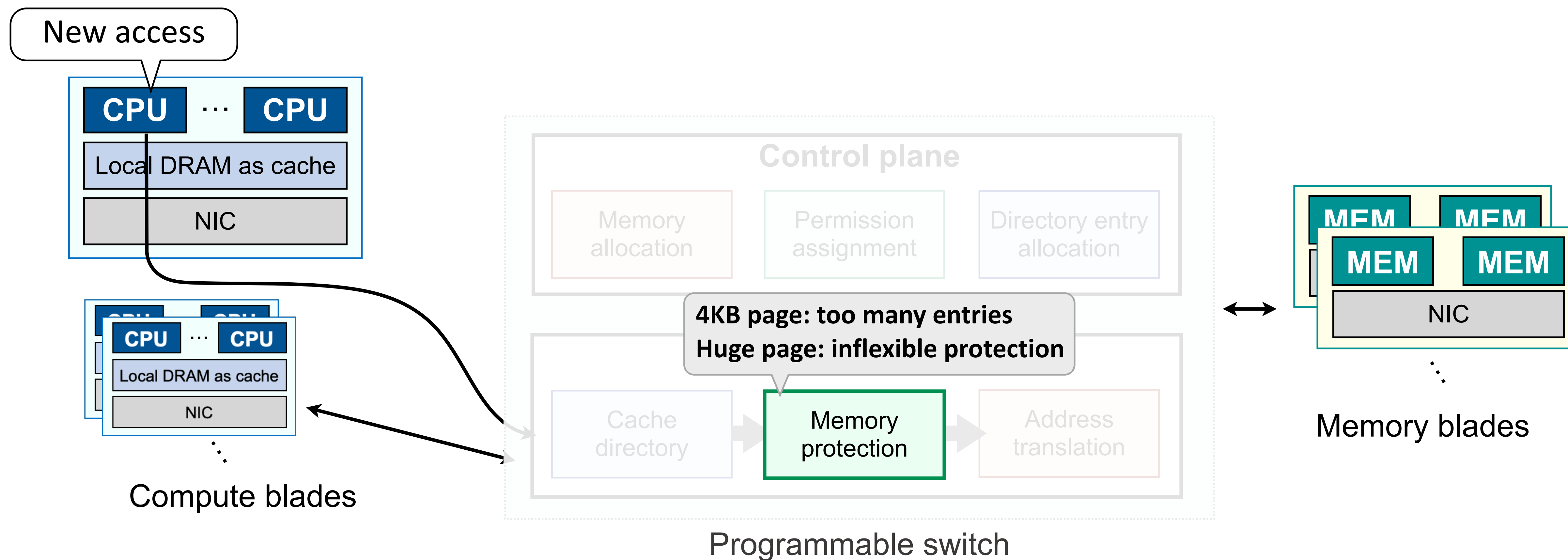
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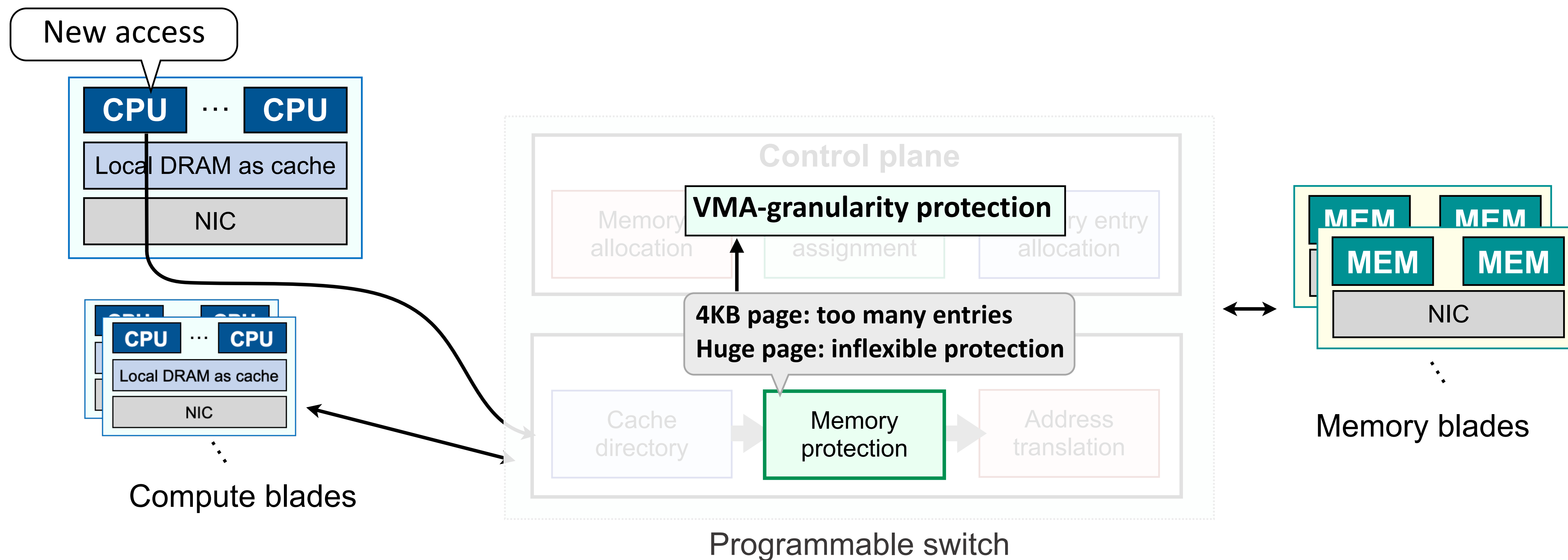
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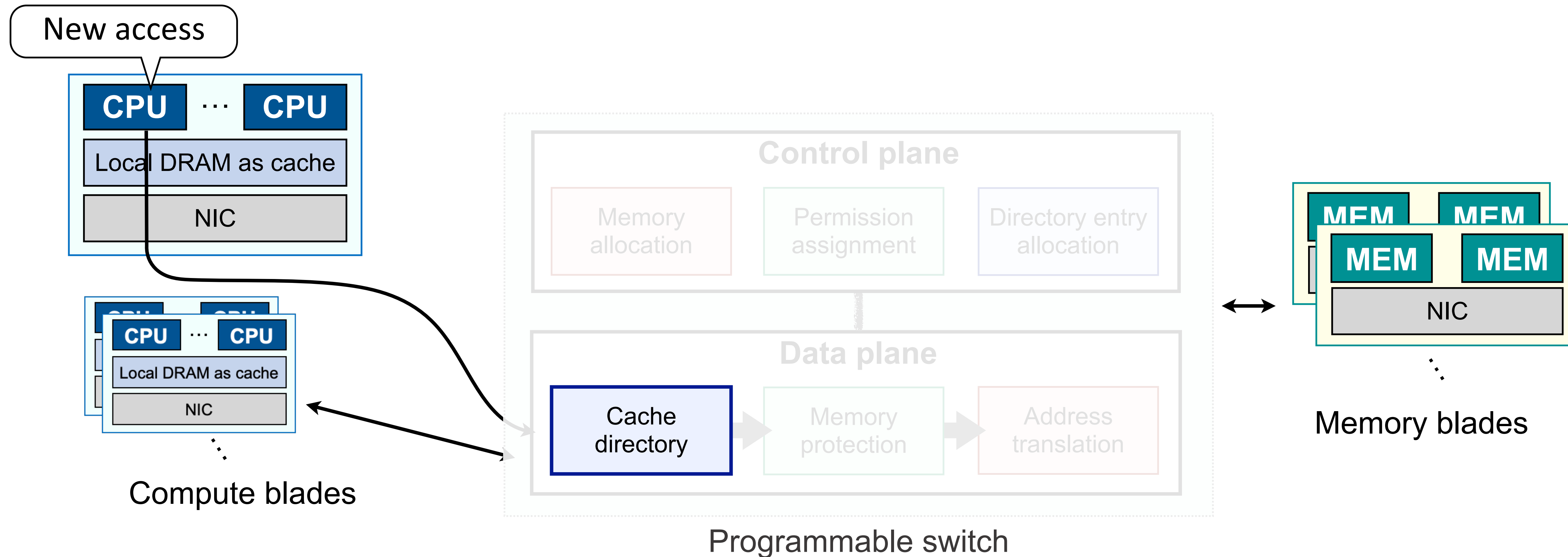
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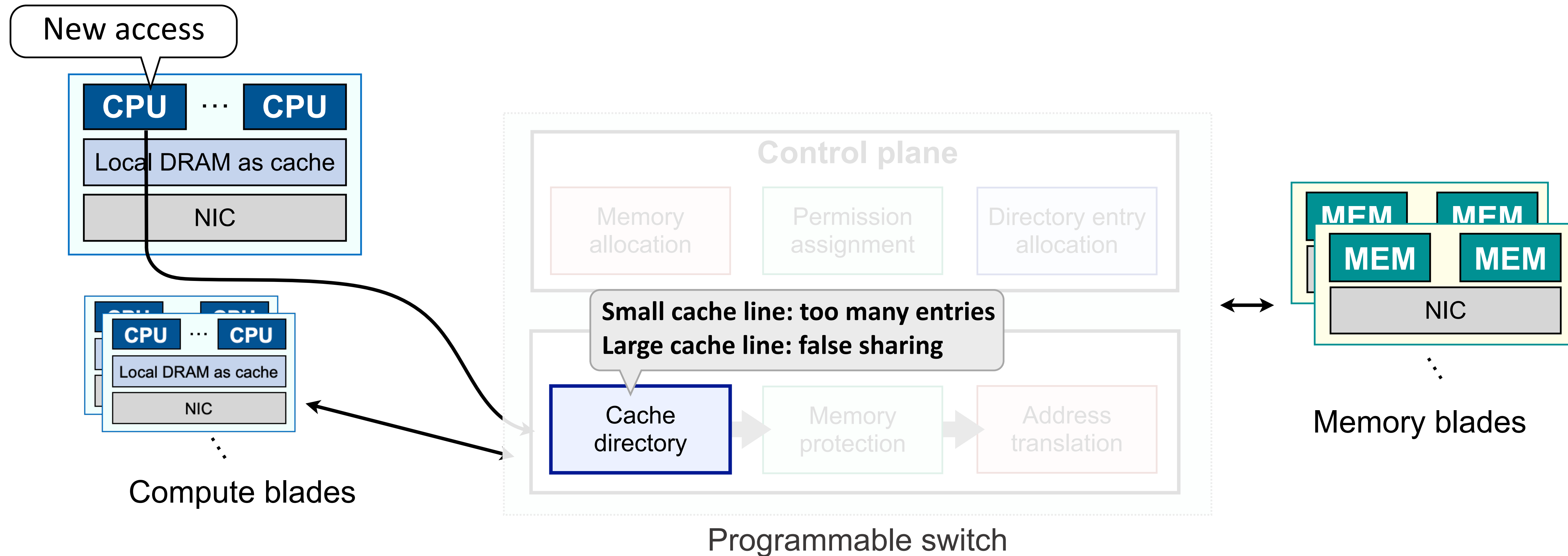
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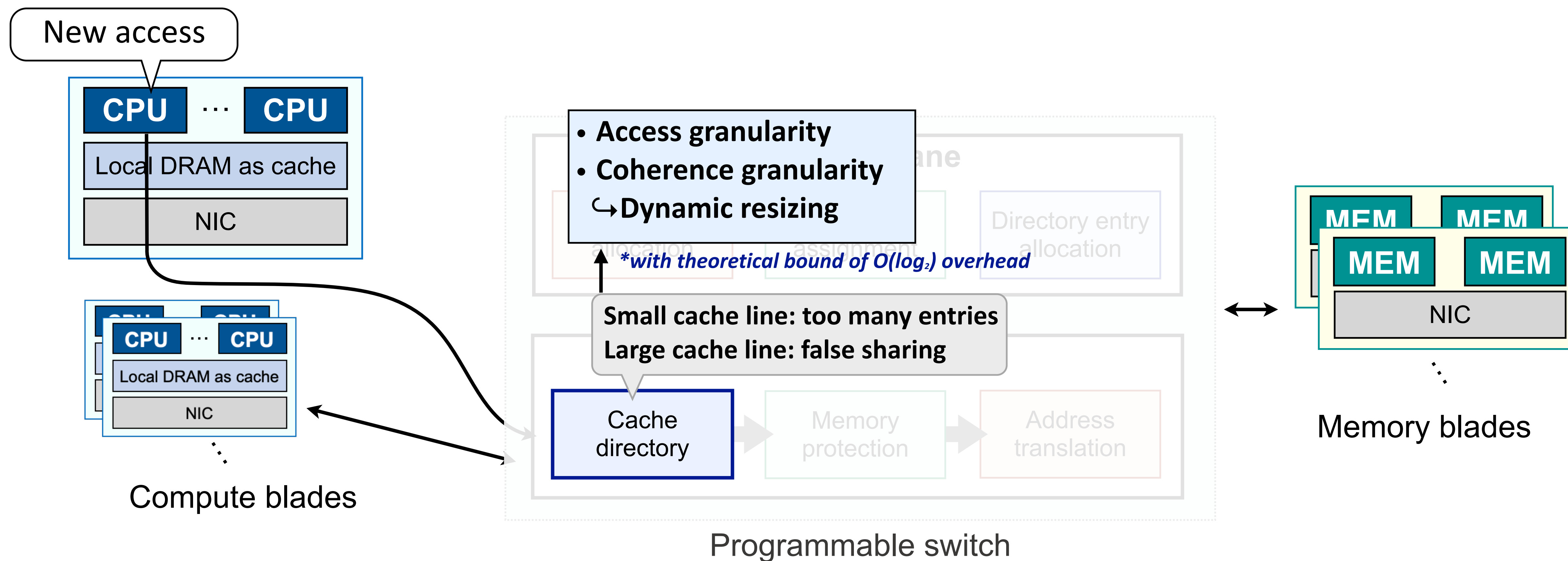
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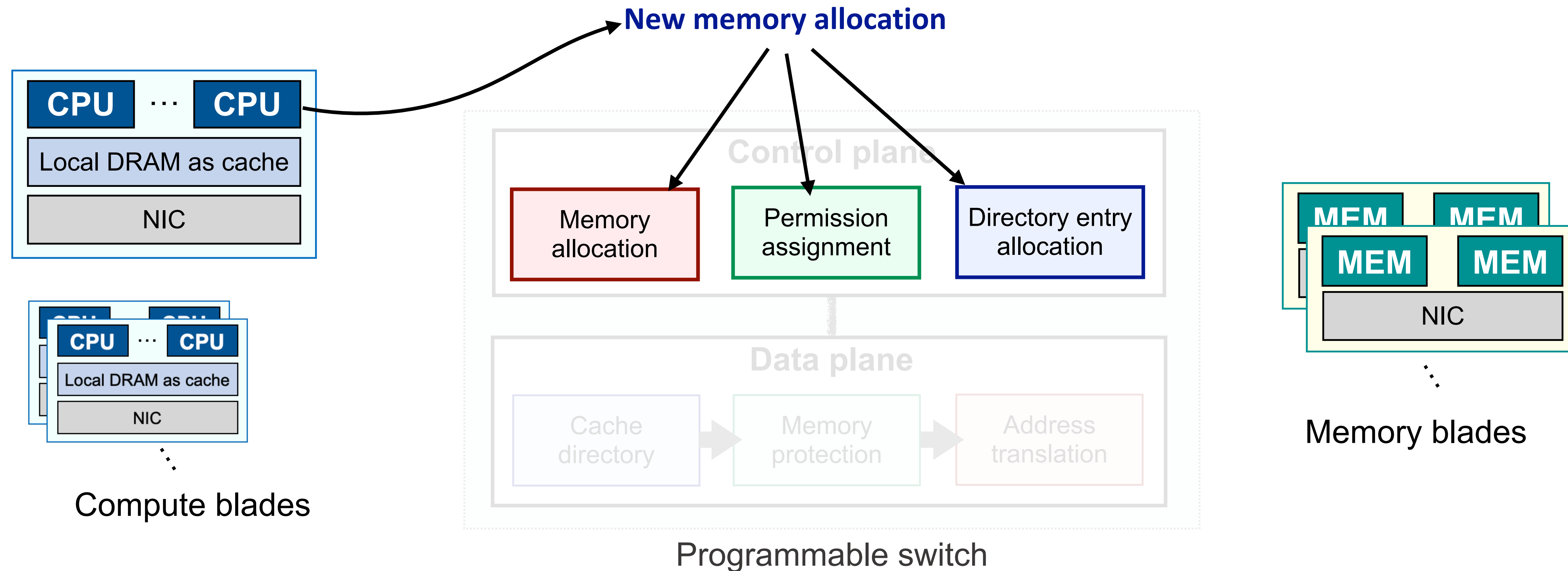
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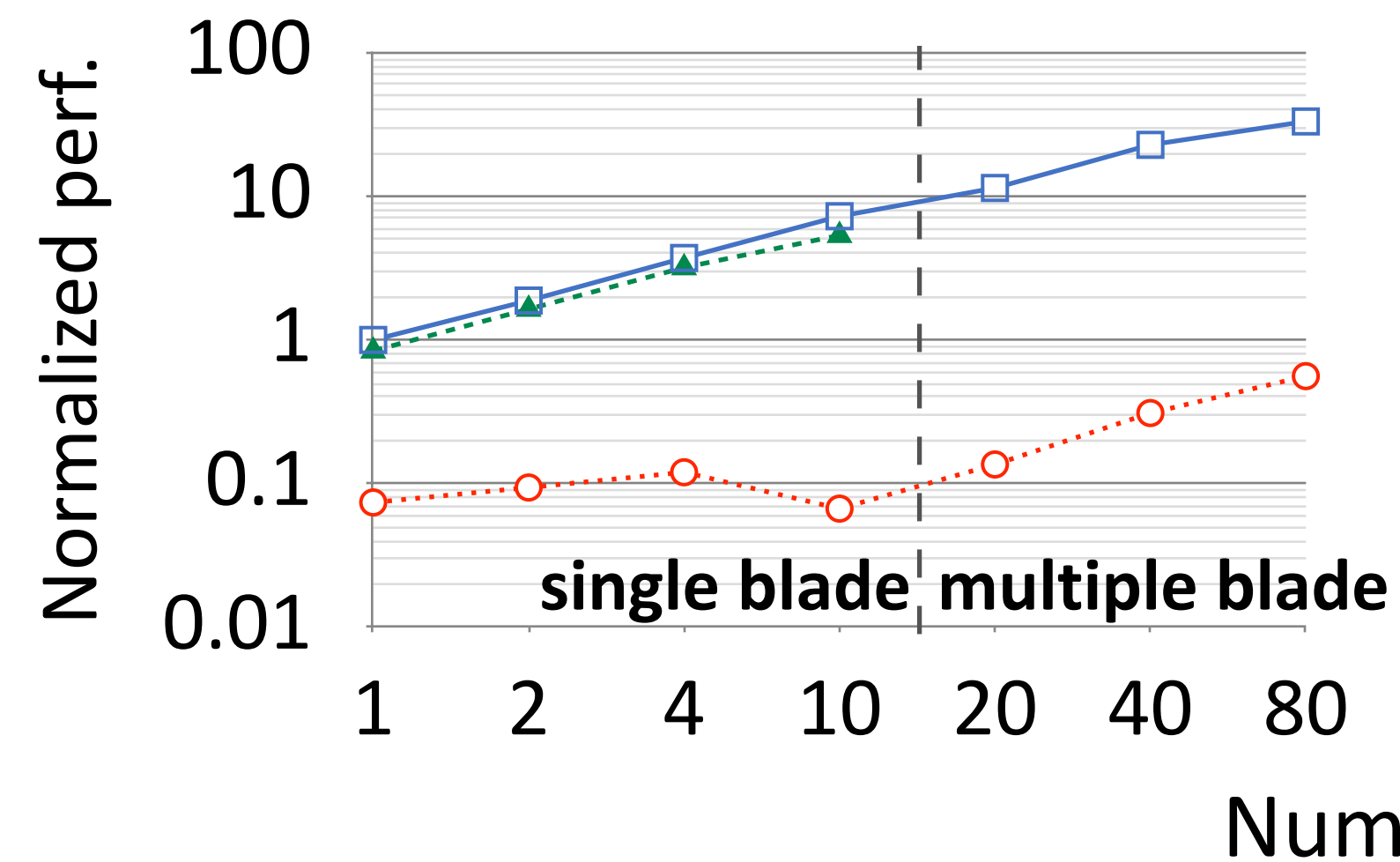
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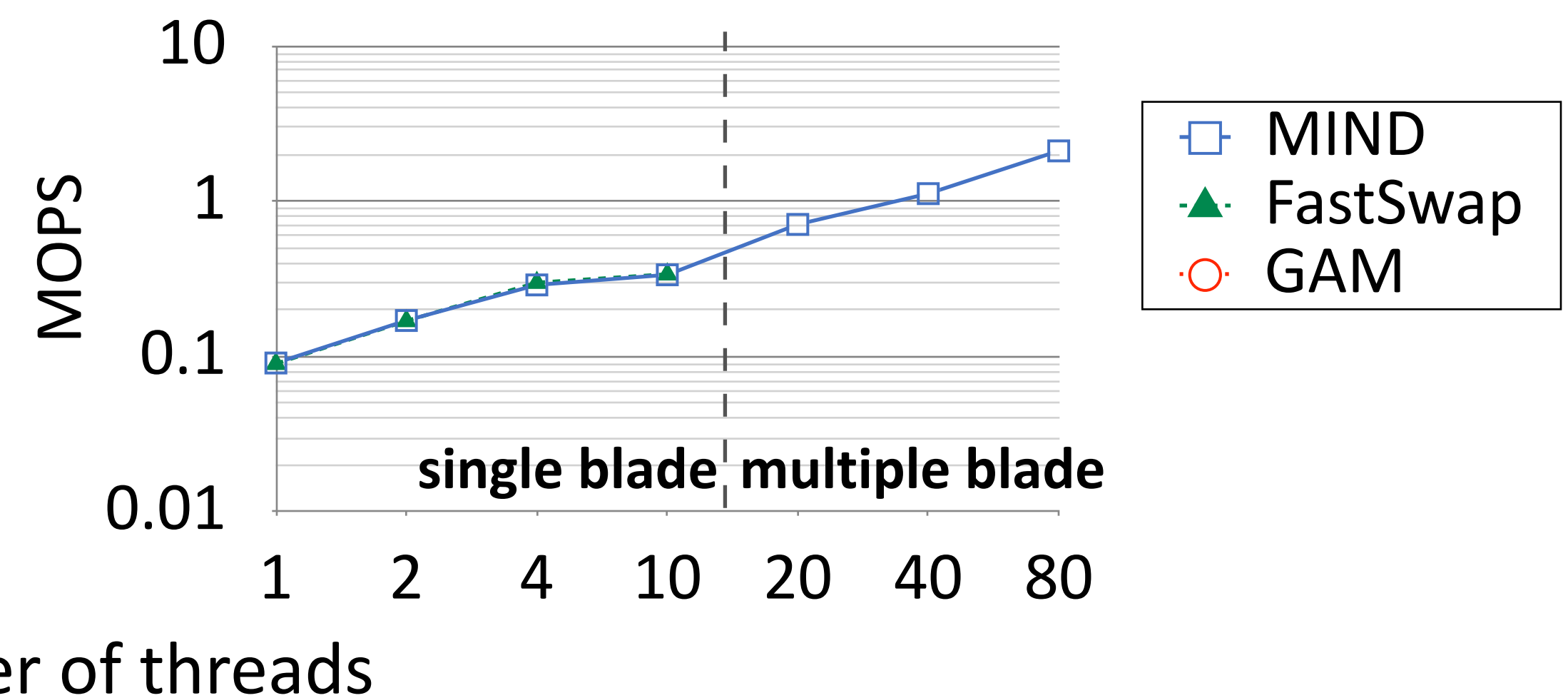
Performance Evaluation

- **Workloads with low contention**
 - TensorFlow (ResNet50), YCSB workload C (read only)

TensorFlow (trace-based for GAM)



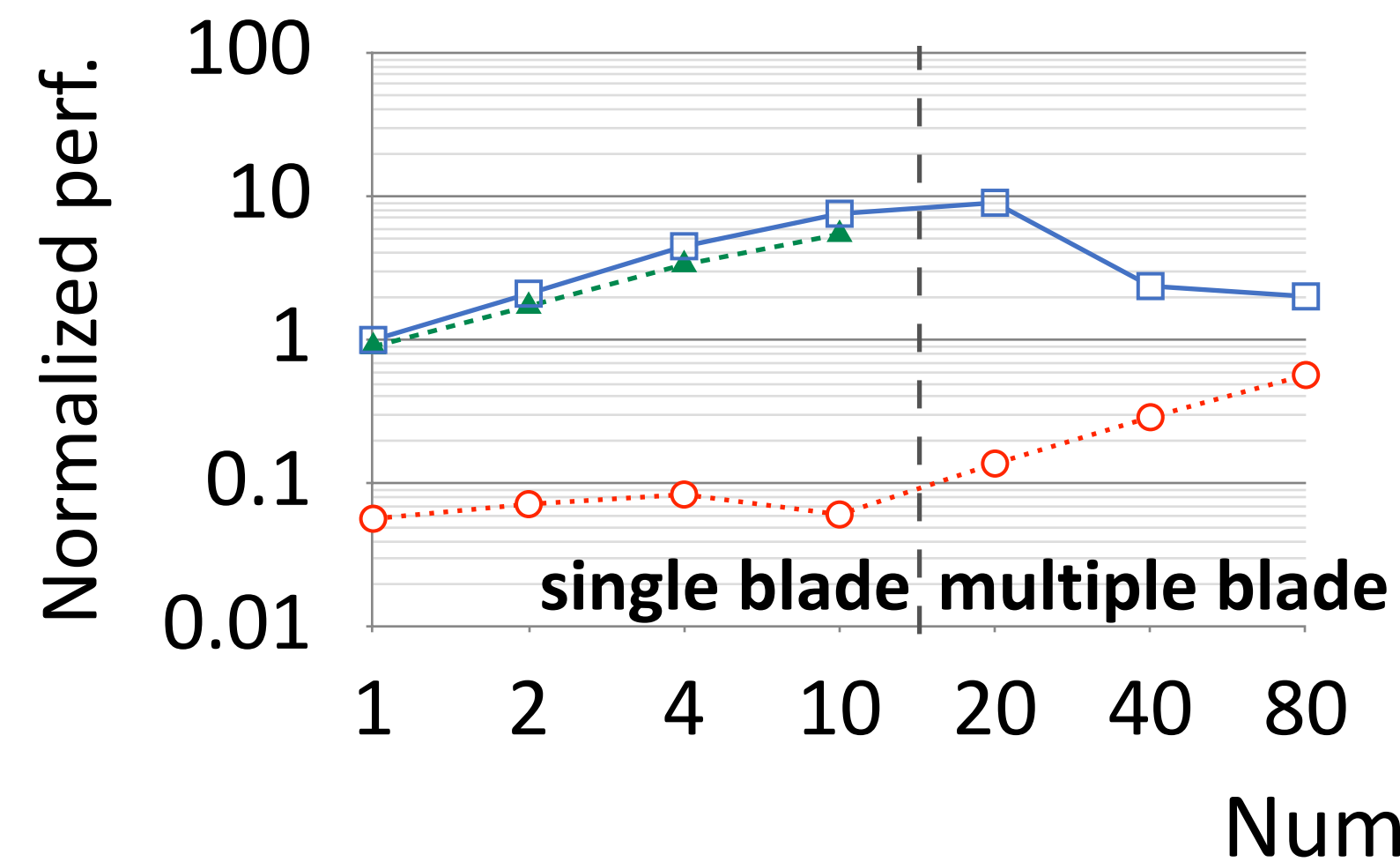
YCSB workload C (native)



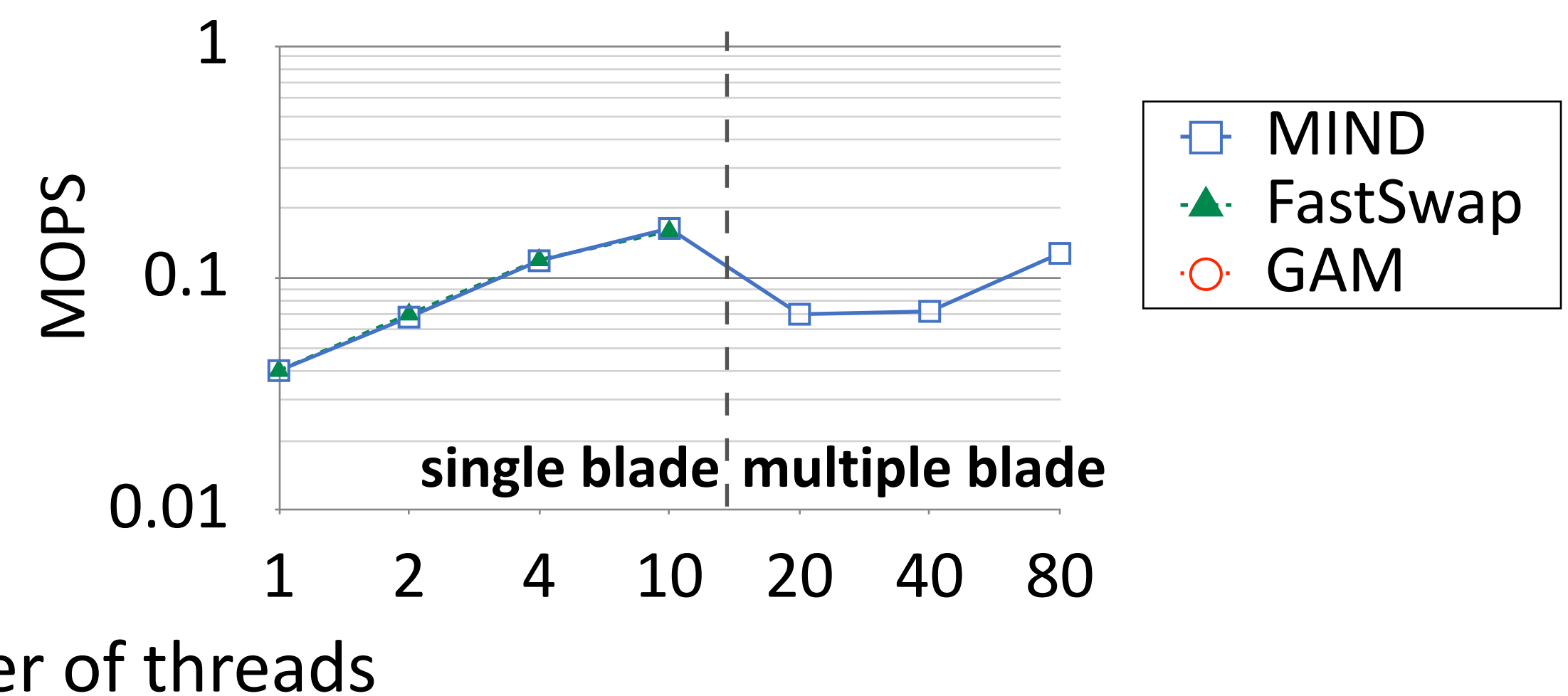
Performance Evaluation

- **Workloads with high contention**
 - GraphChi (PageRank), YCSB workload A (50 % update, 50 % read)

GraphChi (trace-based for GAM)



YCSB workload A (native)



Conclusion & Summary

- **Trade-off between resource elasticity and performance**
in memory disaggregation

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Conclusion & Summary

- **Trade-off between resource elasticity and performance** in memory disaggregation
- We designed MIND, an **in-network MMU** by leveraging programmable network
- Our prototype of MIND can **match the performance of prior proposals and provide transparent elasticity**