CSC230: Introduction to Computer Architecture

Course Dates

CRN(s):	Section A01 CRN: 20772 Section A02 CRN: 23816
Term:	Spring 2022
Course Start:	2022-01-10
Course End:	2022-04-29
Withdrawal with 100% reduction of tuition fees:	2022-01-30
Withdrawal with 50% reduction of tuition fees:	2022-02-13
Last day for withdrawal (no fees returned):	2022-02-28

Scheduled Meeting Times (M=Mon, T=Tue, W=Wed, R=Thu, F=Fri)

Section:	Location:	Classes Start:	Classes End:	Days of week:	Hours of day:	Instructor:
A01	BWC A104	2022-01-10	2022-04-07	TWF	12:30-13:20	Michael Zastre
A02	BWC A104	2022-01-10	2022-04-07	TWF	12:30-13:20	Michael Zastre
B01	ECS 249	2022-01-17	2022-04-07	M	11:30-12:50	
B02	ECS 249	2022-01-17	2022-04-07	M	13:00-14:20	
B03	ECS 249	2022-01-17	2022-04-07	T	09:30-10:50	
B04	ECS 249	2022-01-17	2022-04-07	T	11:00-12:20	
B05	ECS 249	2022-01-17	2022-04-07	T	13:30-14:50	
B06	ECS 249	2022-01-17	2022-04-07	W	11:00-12:20	

Instructor(s)

Name: **Michael Zastre**
Office: ECS 528
Phone: (250) 472-5771
Email: zastre at uvic dot ca

Office Hours:	Comments
Mon 02:00pm-04:00pm	
Wed 09:30am-11:30am	

Course Overview

This course approaches the topics related to computer organization and architecture in two ways: the "what", and the "how".

To answer the "what" question, the course presents the fundamental principles of computer organization and architecture. This leads to an introductory understanding of:

- the design of processors;
- the structure and operation of memory and virtual memory, cache, storage;
- pipelining;
- system integration;
- and peripherals.

The course also provides an introduction to issues of system performance evaluation and the relationship of architecture to system software.

Regarding the "how" question, the course provides an introduction to assembly language programming.

- This leads to a direct and practical understanding of the inner working stages of a processor in relation to the rest of the system.
- In addition, memory and cache management, interrupt processing and pipelining can be better understood.

Execution of software via assembly language and high level languages is explained in terms of system software tools which include assemblers, compilers, linkers, and loaders.

A word about course delivery

- This course will be delivered in-person. Therefore students are expected to be physically present in the lecture room and in the lab room for their registered lab.
- However, UVic requests students, staff, and faculty to remain at home if they are sick.
- **Therefore every attempt will be made to prepare video recordings of lectures using UVic's Echo 360 system so that isolating students may keep up with lectures.**
- (See UVic's information on COVID-19.)

Course Objectives And Learning Outcomes

Upon completion of this course, the student will be able to:

- Explain the concepts of RISC and CISC computer architecture, emphasizing RISC.
- Explain the elements of an instruction cycle.
- Summarize the instruction cycle.
- Write programs in assembly language using the AVR RISC architecture as a case study.
- Write small programs in the C language, using C as a cross compiler from a higher level language to an assembly language.
- Describe the function of compilers, linkers, loaders, and static and dynamic libraries
- Use the techniques of polling and interrupts to obtain input from peripheral devices
- Describe the characteristics of computer memory hierarchy systems, including performance issues of multiple memory levels
- Describe the concepts of cache and virtual memory
- Distinguish between memory mapping techniques
- Explain how instruction pipelining speeds up over program execution, including describing various pipeline hazards.
- Compare and contrast the various processors and architectures defined in the current literature

Textbooks

Recommended	**Some Assembly Required: Assembly Language Programming with the AVR Microcontroller**
	Timothy S. Margus
	CRC Press, 2012
	ISBN: 978-1-4398-2064-3

Recommended	**Computer Organization and Architecture: Designing for Performance (Tenth Edition)**
	William Stallings
	Pearson
	ISBN: 978-0-13-410161-3

Lab Topics

(Not in order of appearance):

- Arithmetic and logical operations using binary representation
- Assembly language programming using AVR Studio
- Use of Arduino board and attached peripherals
- Implementing assembly programs utilizing interrupts
- C programming tools (compiler, cross-compiler)
- Interface between high and low level languages

Lab participation accounts for 10% of the total course grade. More information about the nature of this participation will be given out during the first week of labs.

Assignments

This course includes four (4) major assignments. **The due dates may change as the course proceeds**; the official due date for an assignment will be given when the assignment is handed out. (Normally two weeks are provided for assignment completion.)

Assignment	Weight	Tentative Due Date
Assignment 1	10%	February 1
Assignment 2	10%	February 15
Assignment 3	10%	March 15
Assignment 4	10%	April 5

You should start assignments early enough to allow time to seek help if you encounter difficulties. **Late assignments will not be accepted.**

Students are encouraged to discuss assignment problems with each other and form study groups. However, final assignment submissions must be generated independently, and you will only receive credit for your own work. On some assignments, you may be permitted to use material from other sources **with proper attribution**. Submitting the work of others without proper acknowledgement will be considered a serious academic offense and may result in failure of the course.

Please consult the instructor if you are unsure whether or not you are following these guidelines when working on an assignment.

Exams

There will be three in-class exams only (*i.e.*, there is **no exam for this course during the final-exam period of the semester**).

Exam	Weight	Date
Exam A	17%	February 9 (Wednesday)
Exam B	18%	March 9 (Wednesday)
Exam C	15%	April 6 (Wednesday)

Missed exams:

- Normally a missed midterm exam will be given a zero grade.
- Accommodation for a missed midterm exam is granted in extenuating circumstances (ie. illness) **only if** the following is provided to the course instructor:
  - Notification by e-mail *from your uvic.ca e-mail account* sent to the instructor (zastre at uvic.ca) **before the date/time of the exam.**
  - Some form of documentation or concrete explanation to support the extenuating circumstances.
  - We understand that COVID-19 protocols may make this difficult (ie. individual decisions to self-isolate) and this will be taken into account by the teaching team.
- (Please note that normally at most one missed midterm exam can be accommodated.)

Grading

Coursework	Weight (out of 100%)
Assignments	40%
Labs (participation)	10%
Exams	50%

In order to pass the course, students must **obtain a passing grade on the weighted average of all assignments** and **obtain a passing grade on the weighted average of all three exams.**

The mark for labs is based on lab participation.

Grading System

The University of Victoria follows a percentage grading system in which the instructor will submit grades in percentages. The University will use the following Senate approved standardized grading scale to assign letter grades. Both the percentage mark and the letter grade will be recorded on the academic record and transcripts.

F	D	C	C+	B-	B	B+	A-	A	A+
0-49	50-59	60-64	65-69	70-72	73-76	77-79	80-84	85-89	90-100

Grades	Description
A+, A, A-	**Exceptional**, **outstanding** or **excellent** performance. Normally achieved by a minority of students. These grades indicate a student who is *self-initiating*, *exceeds expectation* and has an *insightful* grasp of the subject matter.
B+, B, B-	**Very good**, **good** or **solid** performance. Normally achieved by the largest number of students. These grades indicate a *good* grasp of the subject matter or *excellent grasp in one area balanced with satisfactory grasp in the other areas*.
C+, C	**Satisfactory**, or **minimally satisfactory**. These grades indicate a *satisfactory performance and knowledge* of the subject matter.
D	**Marginal Performance**. A student receiving this grade demonstrated a *superficial grasp* of the subject matter.

Grades	Description
F	**Unsatisfactory performance**. Wrote final examination and completed course requirements; no supplemental.

Posting of Grades

Typically marks for assignments, examinations, and provisional final grades, are made available through a Learning Management System (LMS) like Brightspace, where each student will be able to view only their own grades. Sometimes numerical marks/grades may be posted publicly to the entire class. In that case, full student numbers or names will not be included with the posted information.

Course Experience Survey (CES)

I value your feedback on this course. Towards the end of term you will have the opportunity to complete a confidential course experience survey (CES) regarding your learning experience. The survey is vital to providing feedback to me regarding the course and my teaching, as well as to help the department improve the overall program for students in the future. When it is time for you to complete the survey, you will receive an email inviting you to do so. If you do not receive an email invitation, you can go directly to the CES site

You will need to use your UVic NetLink ID to access the survey, which can be done on your laptop, tablet or mobile device. I will remind you closer to the time, but please be thinking about this important activity, especially the following three questions, during the course.

- What strengths did your instructor demonstrate that helped you learn in this course?
- Please provide specific suggestions as to how the instructor could have helped you learn more effectively.
- Please provide specific suggestions as to how this course could be improved.

Csc Student Groups

The Computer Science Course Union (https://onlineacademiccommunity.uvic.ca/cscu/) serves all students who are either in a computer science program or taking a class in computer science. Please sign yourself up on their mailing list if you would like to be informed about their social events and services.

The Engineering Students' Society (ESS) serves all students registered in an Engineering degree program, including Software Engineering (BSEng). For information on ESS activities, events and services navigate to http://www.engr.uvic.ca/~ess .

Course Policies And Guidelines

Late Assignments: No late assignments will be accepted unless prior arrangements have been made with the instructor **at least 48 hours before** the assignment due date.
Coursework Mark Appeals: All marks must be appealed **within 7 days** of the mark being posted.
Attendance: We expect students attend all lectures and labs. It is entirely the students' responsibility to recover any information or announcements presented in lectures from which they were absent.
Electronic devices in labs and lectures: No unauthorized *audio* or *video* recording of lectures is permitted.
Electronic devices in midterms and exams: Calculators are only permitted for examinations and tests if explicitly authorized and the type of calculator permitted may be restricted. No other electronic devices (e.g. cell phones, pagers, PDA, etc.) may be used during examinations or tests *unless explicitly authorized*.
Plagiarism: Submitted work may be checked using plagiarism detection software. Cheating, plagiarism and other forms of academic fraud are taken very seriously by both the University and the Department. You should consult the link given below for the UVic policy on academic integrity. Note that the university policy includes the statement that "A largely or fully plagiarized assignment should result in a grade of F for the course."

The Faculty of Engineering and Computer Science Standards for Professional Behaviour are at https://www.uvic.ca/engineering/assets/docs/professional-behaviour.pdf
U.Vic guidelines and policy concerning fraud and academic integrity are at http://web.uvic.ca/calendar/undergrad/info/regulations/academic-integrity.html
U. Vic Privacy Policy: If any student has concerns about their private information being stored or accessed outside of Canada, they are required to inform the course instructor about their concerns before the end of second week of classes.

Equality

This course aims to provide equal opportunities and access for all students to enjoy the benefits and privileges of the class and its curriculum and to meet the syllabus requirements. Reasonable and appropriate accommodation will be made available to students with documented disabilities (physical, mental, learning) in order to give them the opportunity to successfully meet the essential requirements of the course. The accommodation will not alter academic standards or learning outcomes, although the student may be allowed to demonstrate knowledge and skills in a different way. It is not necessary for you to reveal your disability and/or confidential medical information to the course instructor. If you believe that you may require accommodation, the course instructor can provide you with information about confidential resources on campus that can assist you in arranging for appropriate accommodation. Alternatively, you may want to contact the Centre for Accessible Learning located in the Campus Services Building.

The University of Victoria is committed to promoting, providing, and protecting a positive, and supportive and safe learning and working environment for all its members.

Copyright Statement

All course content and materials are made available by instructors for educational purposes and for the exclusive use of students registered in their class. The material is protected under copyright law, even if not marked with a ©. Any further use or distribution of materials to others requires the written permission of the instructor, except under fair dealing or another exception in the Copyright Act. Violations may result in disciplinary action under the Resolution of Non-Academic Misconduct Allegations policy (AC1300).