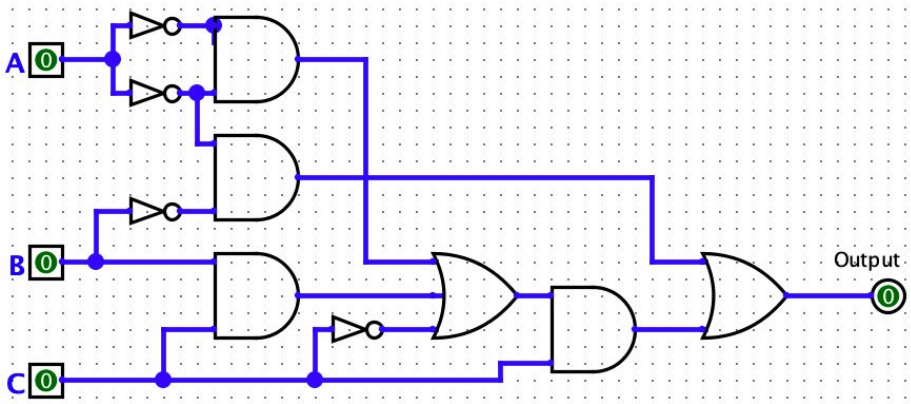
Computer Architecture Homework 4

Spring 2023, March

1 Boolean Algebra and Logic Gates

For the circuit shown below:



a. Write the Boolean Expression of the circuit and simplify it step by step (as simple as possible).(10 pts)

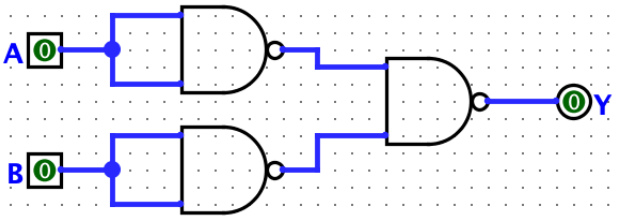
$$
\begin{aligned}
& (A\overline{A} + BC + \overline{C})C + \overline{A}\,\overline{B} \\
&= \overline{A}C + BC + \overline{C}C + \overline{A}\,\overline{B} \\
&= \overline{A}C + BC + \overline{A}\,\overline{B} \qquad \text{(5 pts)} \\
&= \overline{A}C(B + \overline{B}) + BC + \overline{A}\,\overline{B} \\
&= \overline{A}BC + \overline{A}\,\overline{B}C + BC + \overline{A}\,\overline{B} \\
&= (\overline{A} + 1)BC + \overline{A}\,\overline{B}(C + 1) \\
&= BC + \overline{A}\,\overline{B} \qquad \text{(5 pts)}
\end{aligned}
$$

b. Write the Truth Table of the simplified Boolean Expression.(10 pts)

A	B	C	Output
1	1	1	1
1	1	0	0
1	0	1	0
1	0	0	0
0	1	1	1
0	1	0	0
0	0	1	1
0	0	0	1

(-2 pts for each mistake)

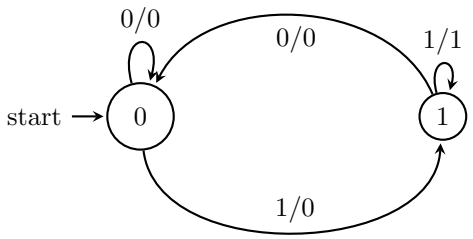
c. Create a circuit of Boolean Expression Y = A + B using only NAND gates.(10 pts)



(Consider $\overline{\overline{A}\,\overline{B}} = \overline{(\overline{A+B})} = A + B$)

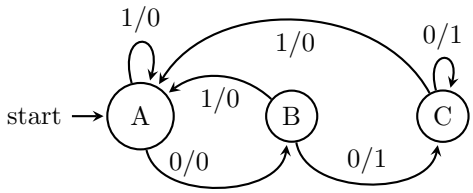
2 FSM

a.



(1) (5 pts)Start with the initial state, the FSM outputs a 1 if it detects the pattern (bitstring) :'11'
(2) (5 pts)What would it output for the input bitstring "011001110"?
The FSM would output : 001000110

b. Draw a FSM that outputs 1 when it receives two or more successive '0'. Complete the following graph.(20 pts)



(5 pts for each arrow)

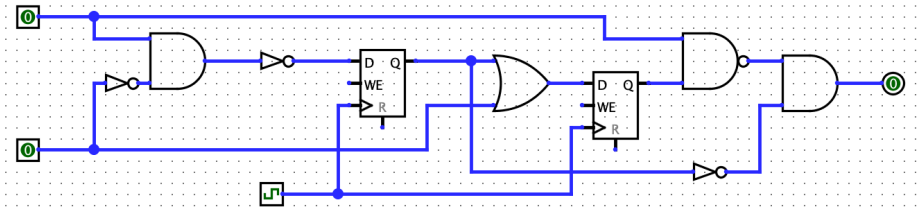
c. Fill out the remainder of the table for the FSM in (b).(10 pts)

Input	-	1	0	0	1	0	1	0	0
Next State	A	A	B	C	A	B	A	B	C
Output	-	0	0	1	0	0	0	0	1

(-2 pts for each mistake)

3 SDS

In the following circuit, NOT gates have a delay of 1ns, AND gates have a delay of 4ns, NAND gates have a delay of 6ns, OR gates have a delay of 3ns. The registers have a clk-to-q delay of 4ns and setup times of 6ns. Assume the inputs comes from registers and output is connected to a register. All the delays refer to propagation delay.



a. What is the minimum acceptable clock cycle time for this circuit? What clock frequency does it correspond to? (please include enough explanation)(20 pts)

Break this circuit into 3 paths between registers. The minimum clock cycle will be the maximum path delay, which is calculated by Clk-To-Q + Combinational Logic Delay + Setup Time.
Path1: Clk-To-Q + NOT + AND + NOT + Setup Time = 4ns + 1ns + 4ns + 1ns + 6ns = 16ns
Path2: Clk-To-Q + OR + Setup Time = 4ns + 3ns + 6ns = 13ns
Path3: Clk-To-Q + NAND + AND + Setup Time = 4ns + 6ns + 4ns + 6ns = 20ns (10 pts for the process)

So the minimum acceptable clock cycle time is 20ns. (5 pts)
20ns corresponds to a clock frequency of $\frac{1}{20\times10^{-9}s} = 50\,\text{MHz}$ (5 pts)

b. What is the maximum allowable hold time for the registers that allows this circuit run correctly? (please include enough explanation)(10 pts)

We need to ensure that Hold Time = Clk-To-Q + Combinational Logic Delay. The maximum allowable hold time for the three registers is how long it takes for any one of them to change its input, so we find the max hold time by looking at the shortest path, which is Path 2 in (a). (5 pts for the process)
maximum allowable hold time = Clk-To-Q + OR = 4ns + 3ns = 7ns (5 pts)