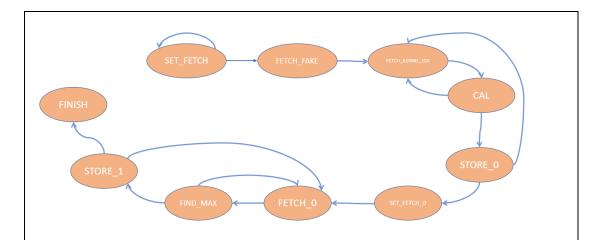
## 2023 Digital IC Design Homes

Simulation Result  Functional simulation  SUMMARY  Congratulations! Layer 0 data have been generated successfully! The result is BASS!!  Congratulations! Layer 1 data have been generated successfully! The result is BASS!!  terminate at 87048 cycle  Synthesis Result  Total logic elements  O  Embedded multiplier 9-bit elements  O  Gate-level simulation  SUMMARY  Congratulations! Layer 0 data have been generated successfully! The result is BASS!!  terminate at 87048 cycle  Total memory bits  O  Embedded multiplier 9-bit elements		黄彥承					
Functional simulation    SUBBART	Student ID	N2610	1185				
Simulation    STENDARY   STENDARY			Sim	ulatio	on Result		
simulation    SUBMARY	Functional			Gate-level			
Congratulations   Layer 0 data have been generated successfully   The result is PASS	simulation	simulation 100			simulation	100	
Cognetiations   Layer   data have been generated successfully! The result is FASS!!   Cognetiations! Layer   data have been generated successfully! The result is FASS!!	# S U M M A R Y						
Synthesis Result  Total logic elements 645  Total memory bits 0  Embedded multiplier 9-bit elements 0  Total cycle used 87048  Flow Summary  Cyclinery  Flow Status Successful - Wed May 17 20:11:01 2023  Quartus Prime Version 20.1.1 Build 720 11/11/2020 SJ Lite Edition  Revision Name ATCONV Family Cyclone IV E Device EP4CE55F23A7  Timing Models Final  Total logic elements 645 /55,856 (1 %) Total registers 113  Total pins 02 / 2.325 (25 %) Total virtual pins 0 Total memory bits 0 / 2,396,160 (0 %) Embedded Multiplier 9-bit elements 0 / 308 (0 %)  Embedded Multiplier 9-bit elements 0 / 308 (0 %)	# # Congratulations! Layer 0 data have been generated successfully! The result is PAS			SS!!			
Synthesis Result  Total logic elements 645  Total memory bits 0  Embedded multiplier 9-bit elements 0  Total cycle used 87048  Flow Summary  C <flitter>&gt; Flow Status Successful - Wed May 17 20:11:01 2023 Quartus Prine Version 20:1.1 Build 720 11/11/2020 SJ Lite Edition Revision Name ATCONV Top-level Entity Name ATCONV Family Cyclone IV E Device EP4E55F23A7 Timing Models Final Total logic elements 645 / 55,856 (1 %) Total registers 113 Total pins 62 / 325 (25 %) Total virtual pins 0 Total memory bits 0 / 2,396,160 (0 %) Embedded Multiplier 9-bit elements 0 / 308 (0 %)</flitter>	# # Congratulations! Layer 1 data	+			Congratulations! Layer 1 data have been ge	enerated successfully! The result is PASS!!	
Synthesis Result  Total logic elements 645  Total memory bits 0  Embedded multiplier 9-bit elements 0  Total cycle used 87048  Flow Summary  Control Status Successful - Wed May 17 20:11:01 2023  Quartus Prime Version 20:1.1 Build 720 11/11/2020 SJ Lite Edition  Revision Name ATCONV  Top-level Entity Name ATCONV  Family Cyclone IV E  Device EP4CE55F23A7  Timing Models Final  Total logic elements 645 / 55,856 (1 %)  Total registers 113  Total pins 82/325 (25 %)  Total virual pins 0  Total memory bits 0 / 2,396,160 (0 %)  Embedded Multiplier 9-bit elements 0/308 (0 %)	# # terminate at 87048 cycle				terminate at 87048 cycle		
Total logic elements  Total memory bits  Dembedded multiplier 9-bit elements  Total cycle used  87048  Flow Summary  Constitution  Flow Status  Guartus Prime Version  Revision Name  ATCONV  Top-level Entity Name  ATCONV  Top-level Entity Name  ATCONV  Family  Cyclone IV E  Device  EP4CE55F23A7  Timing Models  Total logic elements  645 / 55,856 (1 %)  Total pins  Revisions  113  Total pins  82 / 325 (25 %)  Total wirtual pins  0 / 2,396,160 (0 %)  Embedded Multiplier 9-bit elements  0 / 308 (0 %)							
Total logic elements  Total memory bits  Embedded multiplier 9-bit elements  Total cycle used  87048  Flow Summary			Syn	ıthesi	s Result		
Embedded multiplier 9-bit elements 0  Total cycle used 87048  Flow Summary	Total logic eler	<del>-</del>					
Embedded multiplier 9-bit elements 0  Total cycle used 87048  Flow Summary				0			
Total cycle used   87048			9-bit elements	0			
Flow Summary     C < <filter>&gt;  Flow Status Successful - Wed May 17 20:11:01 2023  Quartus Prime Version 20.1.1 Build 720 11/11/2020 SJ Lite Edition  Revision Name ATCONV  Top-level Entity Name ATCONV  Family Cyclone IV E  Device EP4CE55F23A7  Timing Models Final  Total logic elements 645 / 55,856 (1 %)  Total registers 113  Total pins 82/325 (25 %)  Total virtual pins 0 / 2,396,160 (0 %)  Embedded Multiplier 9-bit elements 0 / 308 (0 %)</filter>	<del>-</del>			870	48		
Flow Status         Successful - Wed May 17 20:11:01 2023           Quartus Prime Version         20.1.1 Build 720 11/11/2020 SJ Lite Edition           Revision Name         ATCONV           Top-level Entity Name         ATCONV           Family         Cyclone IV E           Device         EP4CE55F23A7           Timing Models         Final           Total logic elements         645 / 55,856 (1 %)           Total registers         113           Total pins         82 / 325 (25 %)           Total virtual pins         0           Total memory bits         0 / 2,396,160 (0 %)           Embedded Multiplier 9-bit elements         0 / 308 (0 %)	Flow Summary						
Quartus Prime Version         20.1.1 Build 720 11/11/2020 SJ Lite Edition           Revision Name         ATCONV           Top-level Entity Name         ATCONV           Family         Cyclone IV E           Device         EP4CE55F23A7           Timing Models         Final           Total logic elements         645 / 55,856 (1 %)           Total registers         113           Total pins         82 / 325 (25 %)           Total virtual pins         0           Total memory bits         0 / 2,396,160 (0 %)           Embedded Multiplier 9-bit elements         0 / 308 (0 %)	< <filter>&gt;</filter>						
Revision Name         ATCONV           Top-level Entity Name         ATCONV           Family         Cyclone IV E           Device         EP4CE55F23A7           Timing Models         Final           Total logic elements         645 / 55,856 (1%)           Total registers         113           Total pins         82 / 325 (25 %)           Total virtual pins         0           Total memory bits         0 / 2,396,160 (0%)           Embedded Multiplier 9-bit elements         0 / 308 (0%)			-				
Top-level Entity Name         ATCONV           Family         Cyclone IV E           Device         EP4CE55F23A7           Timing Models         Final           Total logic elements         645 / 55,856 (1 %)           Total registers         113           Total pins         82 / 325 (25 %)           Total virtual pins         0           Total memory bits         0 / 2,396,160 (0 %)           Embedded Multiplier 9-bit elements         0 / 308 (0 %)					dition		
Family         Cyclone IV E           Device         EP4CE55F23A7           Timing Models         Final           Total logic elements         645 / 55,856 (1 %)           Total registers         113           Total pins         82 / 325 (25 %)           Total virtual pins         0           Total memory bits         0 / 2,396,160 (0 %)           Embedded Multiplier 9-bit elements         0 / 308 (0 %)							
Device         EP4CE55F23A7           Timing Models         Final           Total logic elements         645 / 55,856 (1 %)           Total registers         113           Total pins         82 / 325 (25 %)           Total virtual pins         0           Total memory bits         0 / 2,396,160 (0 %)           Embedded Multiplier 9-bit elements         0 / 308 (0 %)							
Timing Models         Final           Total logic elements         645 / 55,856 (1 %)           Total registers         113           Total pins         82 / 325 (25 %)           Total virtual pins         0           Total memory bits         0 / 2,396,160 (0 %)           Embedded Multiplier 9-bit elements         0 / 308 (0 %)			•				
Total logic elements       645 / 55,856 (1 %)         Total registers       113         Total pins       82 / 325 (25 %)         Total virtual pins       0         Total memory bits       0 / 2,396,160 (0 %)         Embedded Multiplier 9-bit elements       0 / 308 (0 %)							
Total registers         113           Total pins         82 / 325 (25 %)           Total virtual pins         0           Total memory bits         0 / 2,396,160 (0 %)           Embedded Multiplier 9-bit elements         0 / 308 (0 %)							
Total pins         82 / 325 (25 %)           Total virtual pins         0           Total memory bits         0 / 2,396,160 (0 %)           Embedded Multiplier 9-bit elements         0 / 308 (0 %)	_						
Total virtual pins 0  Total memory bits 0 / 2,396,160 (0 %)  Embedded Multiplier 9-bit elements 0 / 308 (0 %)	_		/·······				
Total memory bits 0 / 2,396,160 (0 % ) Embedded Multiplier 9-bit elements 0 / 308 (0 % )	·		***************************************				
Embedded Multiplier 9-bit elements 0 / 308 (0 % )							
	-	t elements					
		Celements					
Description of your design			Descrint	ion o	f vour design		
1 0					•	(ECM) that is	
The proposed work is implemented using a finite state machine (FSM) that is	The man and m	1- :-			a linile state machine		
divided into ten states. The state diagram is described below:	The proposed v	work is	s implemented u	sing	a minte state macmine	(I'SIVI) mat is	



SET FETCH: Sets all parameters' initial value.

FETCH FAKE: Updates layer 0 index.

FETCH KERNEL IDX: Gets 3\*3 kernel's corresponding index.

CAL: Calculates the convolutional value.

STORE 0: Stores convolutional value to layer 0 according to layer 0 index.

SET FETCH 0: Sets value to get layer 0 value.

FETCH 0: Gets layer 0 according to layer 0 index.

FIND MAX: Finds the maximum value.

STORE\_1: Stores the maximum value to layer 1 according to layer 1 index.

FINISH: Finish by setting the busy signal to 0.

 $Scoring = (Total\ logic\ elements + Total\ memory\ bits + 9*Embedded\ multipliers\ 9-bit\ elements)\ X\ Total\ cycle\ used$ 

\* Total logic elements must not exceed 1000.