數位IC設計

Introduction

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Outline

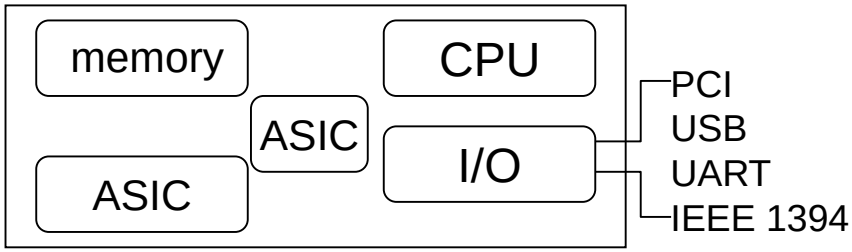
- **Chapter 1**: Introduction
- **Chapter 2**: Semi Custom Design Flow
- **Chapter 3**: RTL Coding-Part I
- **Chapter 4**: RTL Coding-Part II
- **Chapter 5**: Digital System Design
- **Chapter 6**: Control Unit
- **Chapter 7**: Datapath
- **Chapter 8**: Case Study
- **Chapter 9**: System on a Chip
- **Chapter 10**: Low-Power Design

Hardware Implementation

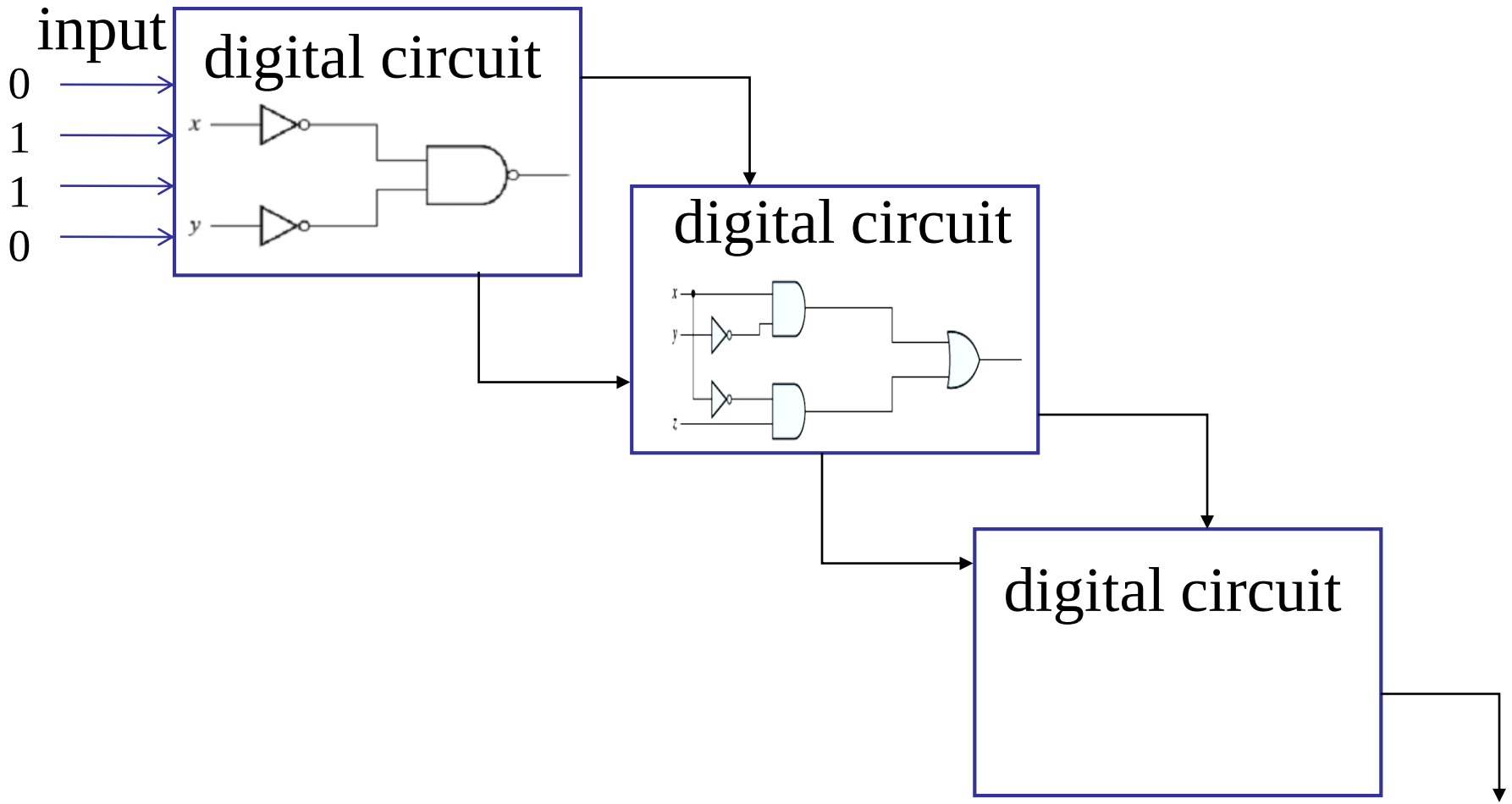
Methods and Algorithms are used to solve some specific problems.

Methods or Algorithms can be implemented with

1. Hardware processor + suitable software programs (flexibility)
   a. Pentium IV + suitable software programs (high-level language)
   b. TI-DSP + suitable software programs
   c. MCU(8051) + suitable software programs (low-level language)
2. Dedicated hardware circuits (faster)
   a. old_PCBs (TTL SSI, MSI chips and wires)
   b. new_PCBs(some devices, application specific integrated circuit-ASIC, wires)
3. Some hardware circuits + software programs (to solve more complex problems)
   a. System on a board (memory, processor, ASIC, I/O, other devices)
   b. System on a chip (SoC)
      current and future work
      RISC-ARM



Digital System



digital circuit === IC (integrated circuit)

semiconductor

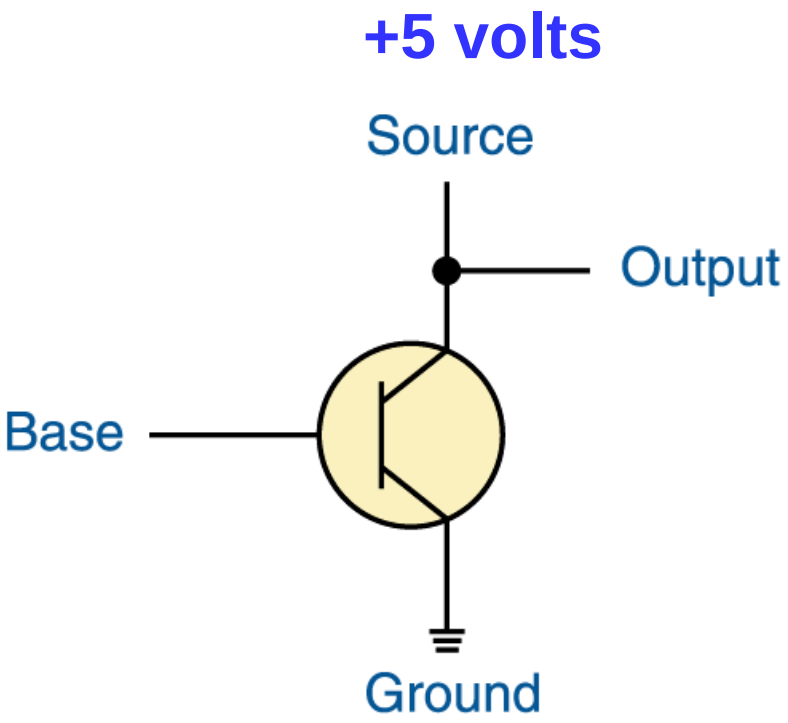
Circuits

- **Transistor**
- **Gate (1 gate ~= 2~14 transistors)**

  A combination of interacting transistors
- **Circuit**

  A combination of interacting gates designed to accomplish a specific logical function
- **IC (Integrated Circuit)**
- **System➔ PCB (printed circuit board)**
- **SoC (system on a chip)**

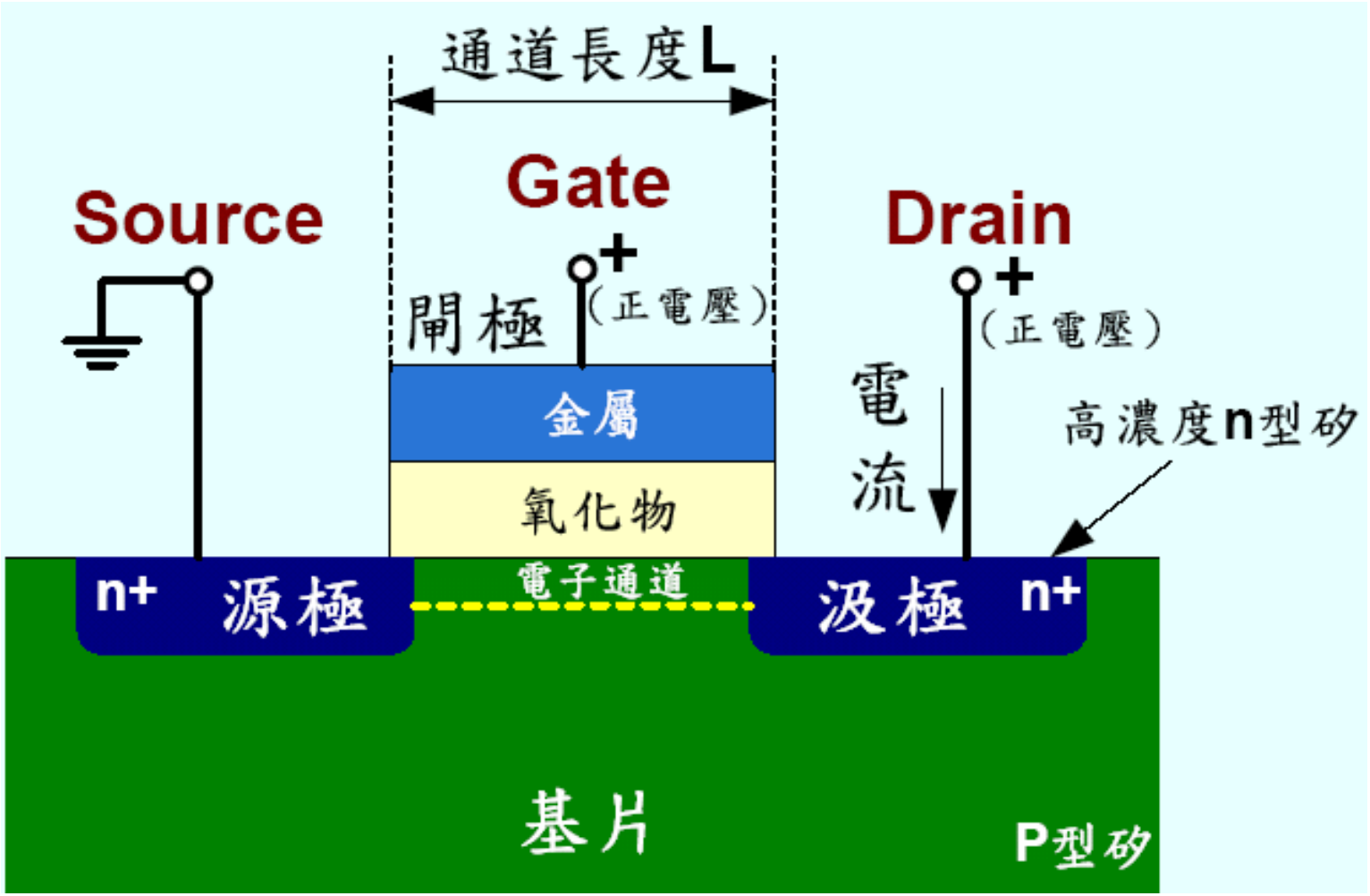
Transistor(電晶體)



- A transistor has three terminals
  - A source (feed with 5 volts)
  - A base
  - An emitter, typically connected to a ground wire
- If the base signal is high (close to +5 volts), the source signal is grounded and the output signal is low (0). If the base signal is low (close to 0 volts), the source signal stays high and the output signal is high (1)

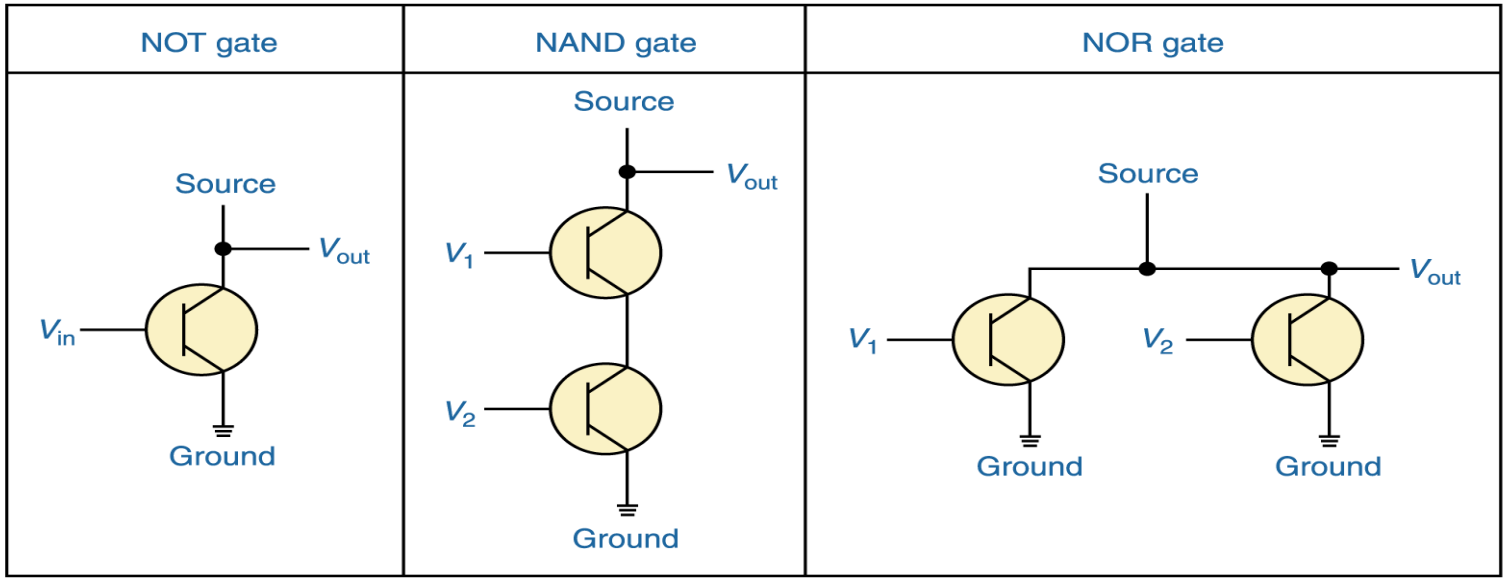
N-channel MOS Transistor

Transistor (電晶體)– **Semiconductor(半導體)**



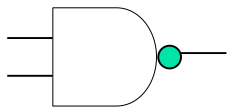
Constructing Gates (semiconductor)

- It turns out that, because the way a transistor works, the easiest gates to create are the NOT, NAND, and NOR gates

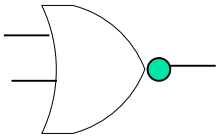


V_{in}	V_{out}
0	1
1	0

V_1	V_2	V_{out}
0	0	1
0	1	1
1	0	1
1	1	0

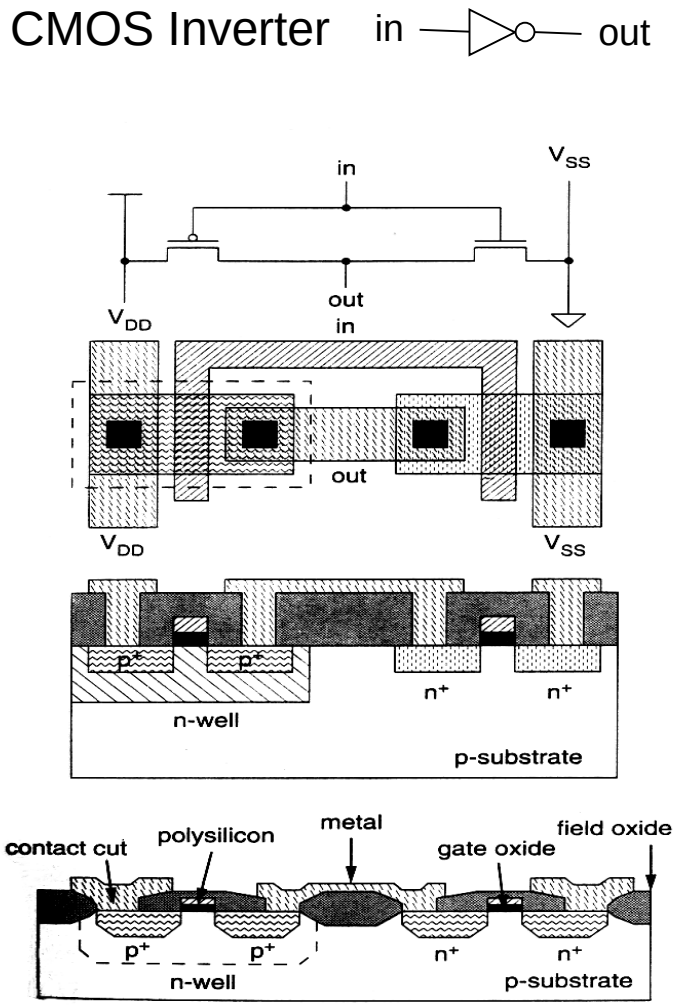


V_1	V_2	V_{out}
0	0	1
0	1	0
1	0	0
1	1	0



IC Design (with CMOS)

One npn transistor and one pnp transistor are used to construct one inverter.



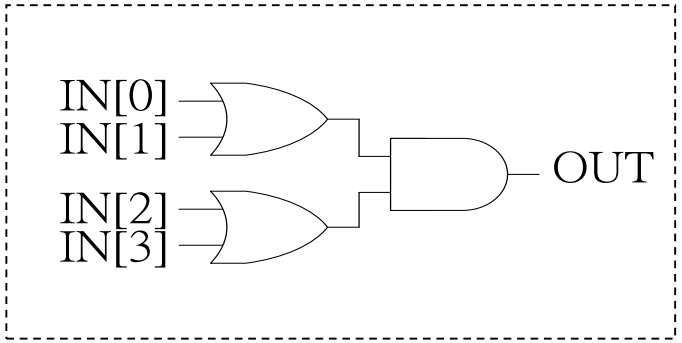
done by chip designer

masking

done by TSMC, UMC

Design Entry for VLSI System

Choose the design entry method:



Schematic

Gate level design

Intuitive & easy to debug

HDL (Hardware Description Language)

Descriptive & portable

Easy to modify

Mixed HDL & Schematic

…

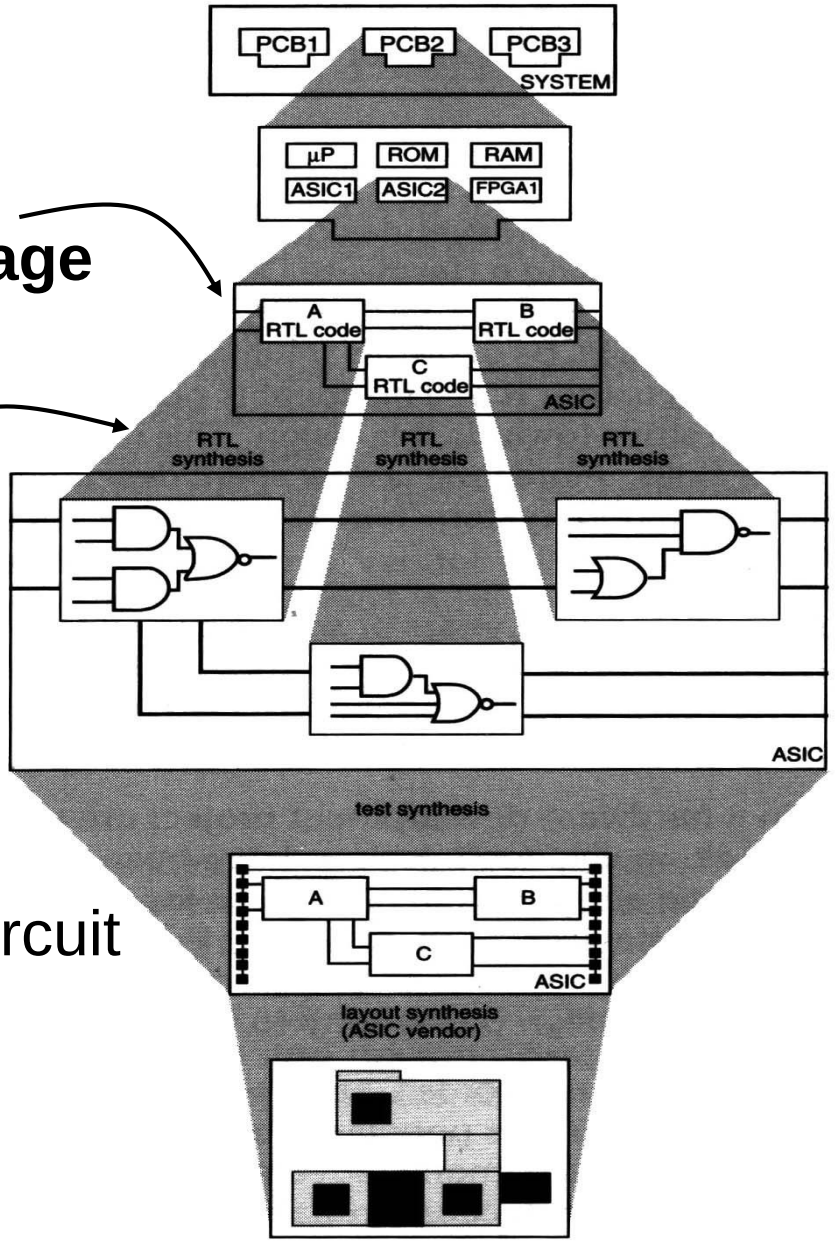
```
always @(IN)
begin
  OUT = (IN[0] | IN[1]) &
     (IN[2] | IN[3]);
end
```

Hierarchical Components in PCB

1. **Describe the circuits with Hardware Description Language (HDL硬體描述語言)**

2. **Synthesis (合成) the circuits**

….



application specific integrated circuit (ASIC晶片)

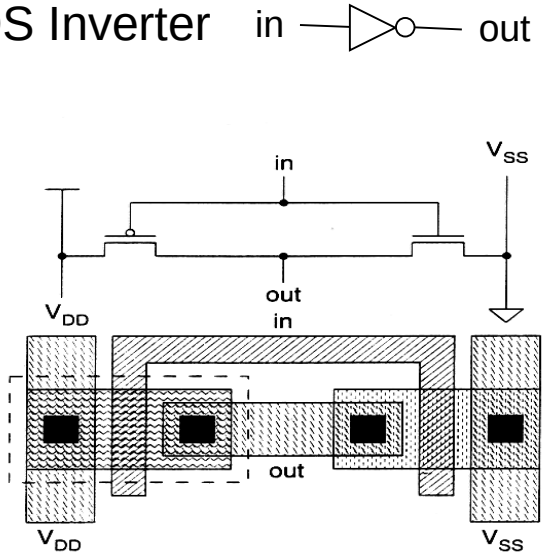
IC or chip

IC Design (with CMOS)

done by
chip designer
(半客戶設計)
+
Related software tools

Semi-custom design
Cell-based design

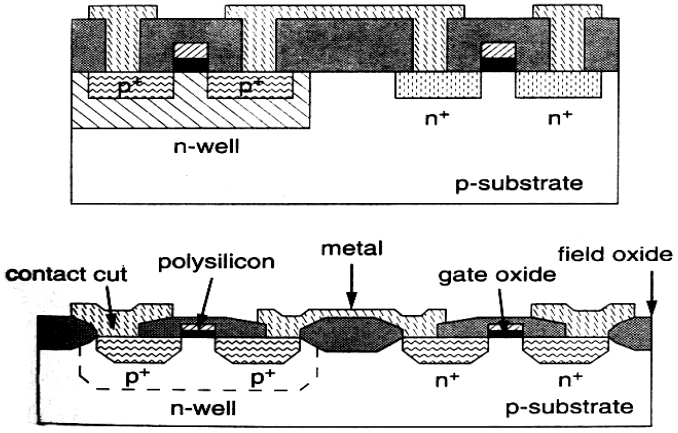
CMOS Inverter



done by
chip designer
(全客戶設計)
Full-custom design

masking

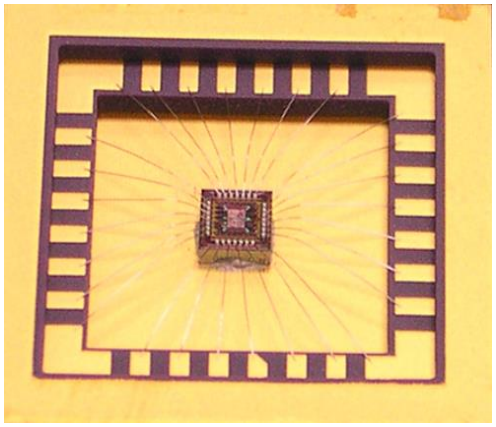
One npn transistor
and one pnp transistor
are used to construct
one inverter.

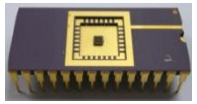


done by
TSMC, UMC

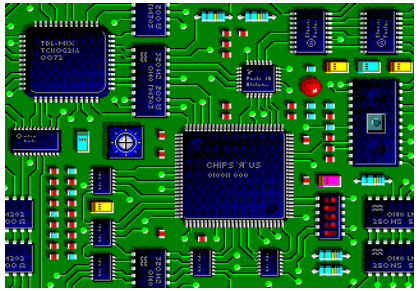
Packing, Testing

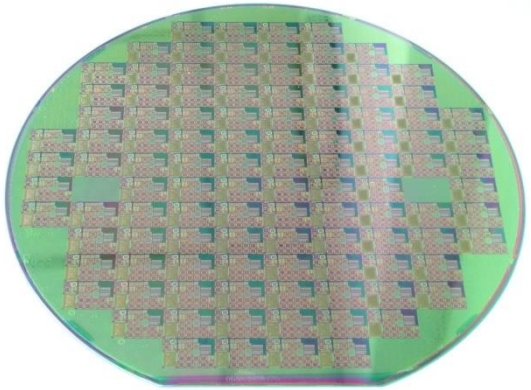
Chip/Circuit Everywhere!

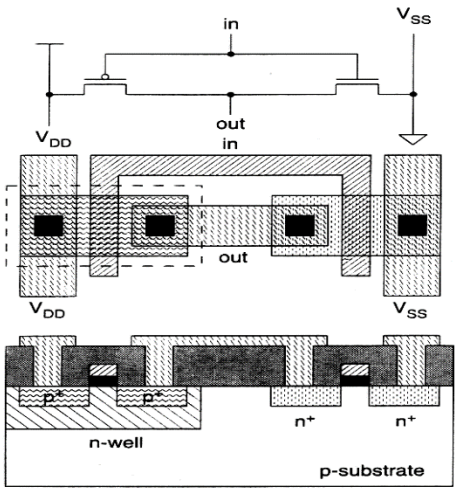


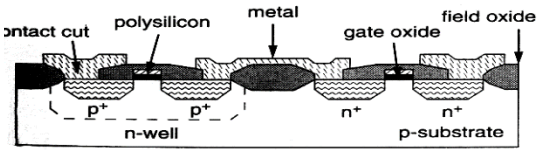


Applications

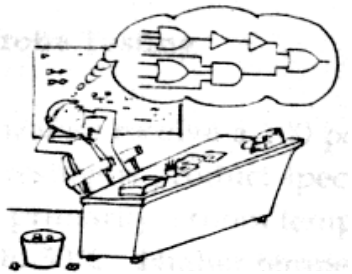




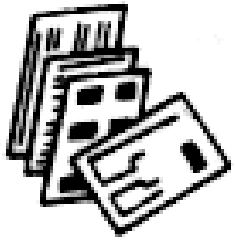




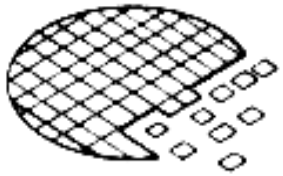
IC Industry in Taiwan



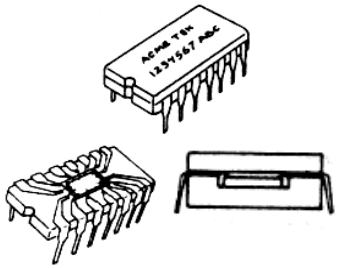
邏輯設計



光罩設計



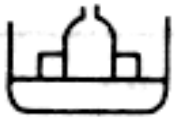
晶粒測試及切割



封　裝

成品測試

設計 → 光罩 → 製造 → 封裝 → 測試

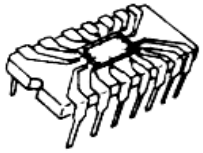


長晶

晶圓切割

晶圓

化學品



導線架

Historical Perspective

- Evolution of IC
  - 1958: Single transistor 1
  - 1962+: SSI 10
  - 1967: MSI (Medium) 100
  - 1972: LSI 1000
  - 1978: VLSI 10^5-10^6
  - 1990: ULSI (Ultra) $>10^6$
  - 2000: SOC (System on Chip)

積體電路 (IC) 分類

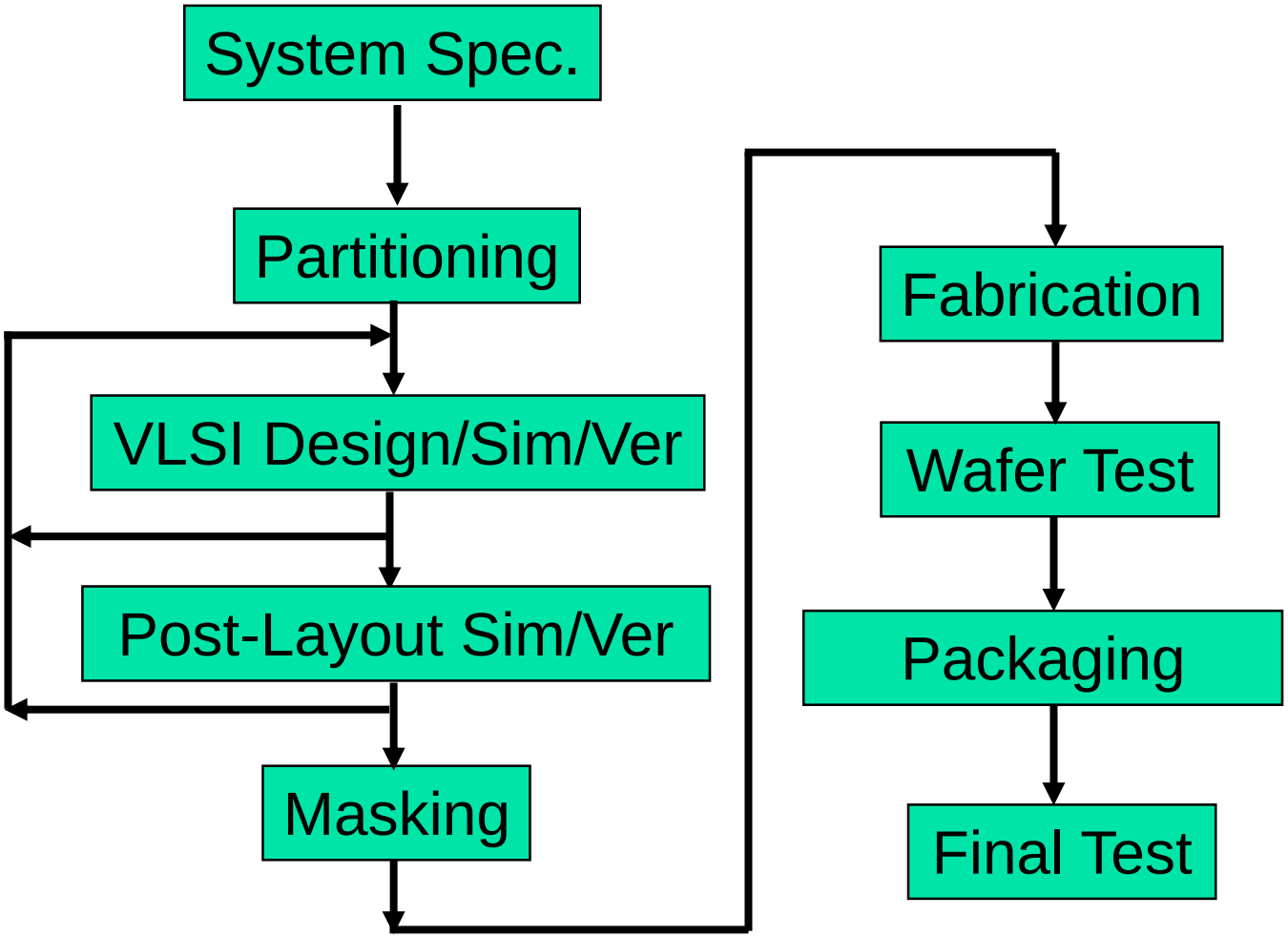
- SSI (Small-Scaled Integrated Circuits)
  - 小型積體電路→含數十個元件 (1970s)
- MSI (Medium-Scaled IC)
  - 中型積體電路→含數百個元件
- LSI (Large-Scaled IC)
  - 大型積體電路→含數千個元件 (1980s)
- VLSI (Very Large Scaled IC)
  - 超大型積體電路→含數萬個元件 (1990s)
- SoC (System on a Chip)
  - 單晶片系統→含數百萬個元件 (2000s)

SIA Roadmap 1997

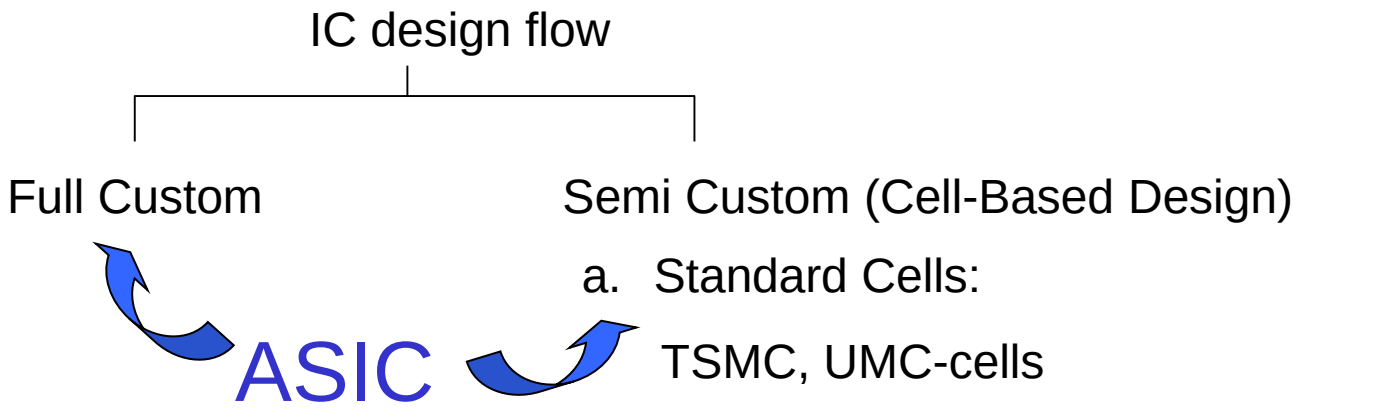
Technology (um)	0.25	0.18	0.15	0.13	0.10	0.07
Year	1997	1999	2001	2003	2006	2009
Transistors	11M	21M	40M	76M	200M	520M
On-chip clock (MHz)	750	1200	1400	1600	2000	2500
Area (mm^2)	300	340	385	430	520	620
Wiring layers	6	6-7	7	7	7-8	8-9

SIA : Semiconductor Industry

Circuit Design Process



IC Design flow



Full (Fully) Custom Design:

a. For analog circuits and digital circuits requiring custom optimization
b. Gates, transistors and layout are designed and optimized by the engineer

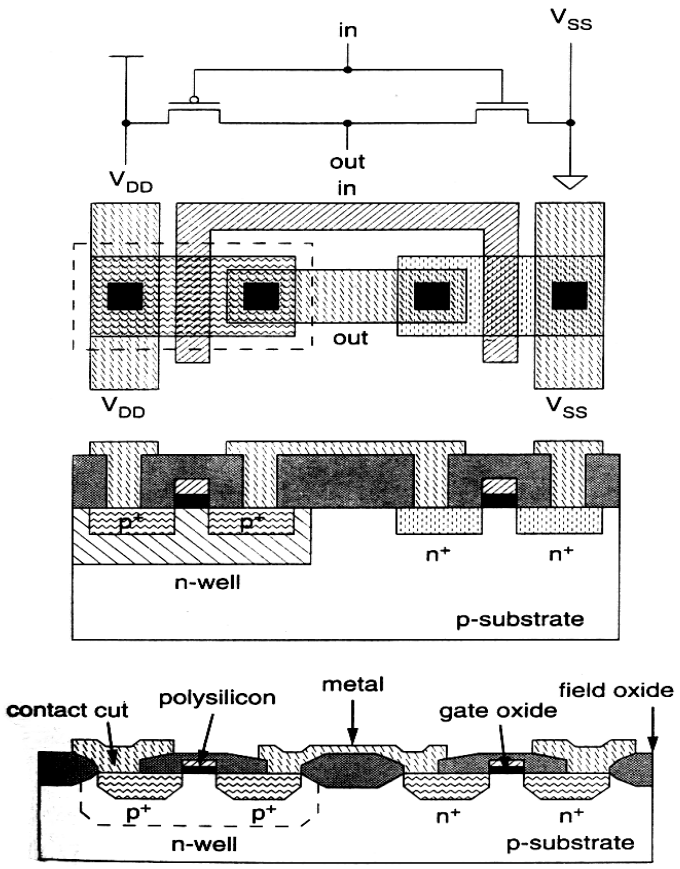
Semi Custom Design:

a. For larger digital circuits
b. Real gates, transistors and layout are synthesized and optimized by related software tools
c. Realization with hardware description language (HDL) such as VHDL and Verilog

Full Custom Design (全客戶式設計)

a. Digital circuits requiring custom optimization (smaller system)
b. Analog circuits
c. Long design cycle (transistors and wires)
d. No CPLD or FPGA solutions

CMOS Inverter in out



done by chip designer

masking

done by TSMC, UMC

Packing, Testing

Semi Custom Design (半客戶式設計)

Semi Custom Design

a. Product specification

b. Modeling with HDL

c. Synthesis (by using suitable standard cell)

d. Simulation and verification

e. Physical placement and layout

-- implemented with suitable tools

f. Tape-out (real chip) -- implemented by suitable Fab companies

g. Testing -- implemented by suitable tools and mechanisms

more flexible, shorter design cycle, suitable for smaller production

Two different solutions :

PLD → FPGA or CPLD — Xilinx, Altera

Standard cell → Real ASIC chip — Fab (TSMC, UMC, ..)

less flexible, long design cycle, larger-scale production to reduce price

Standard Cells

Standard Cell

- Cells are characterized and stored in library
- Need update when technology advance
- Need technology mapping before layout for each design

Macro Cells

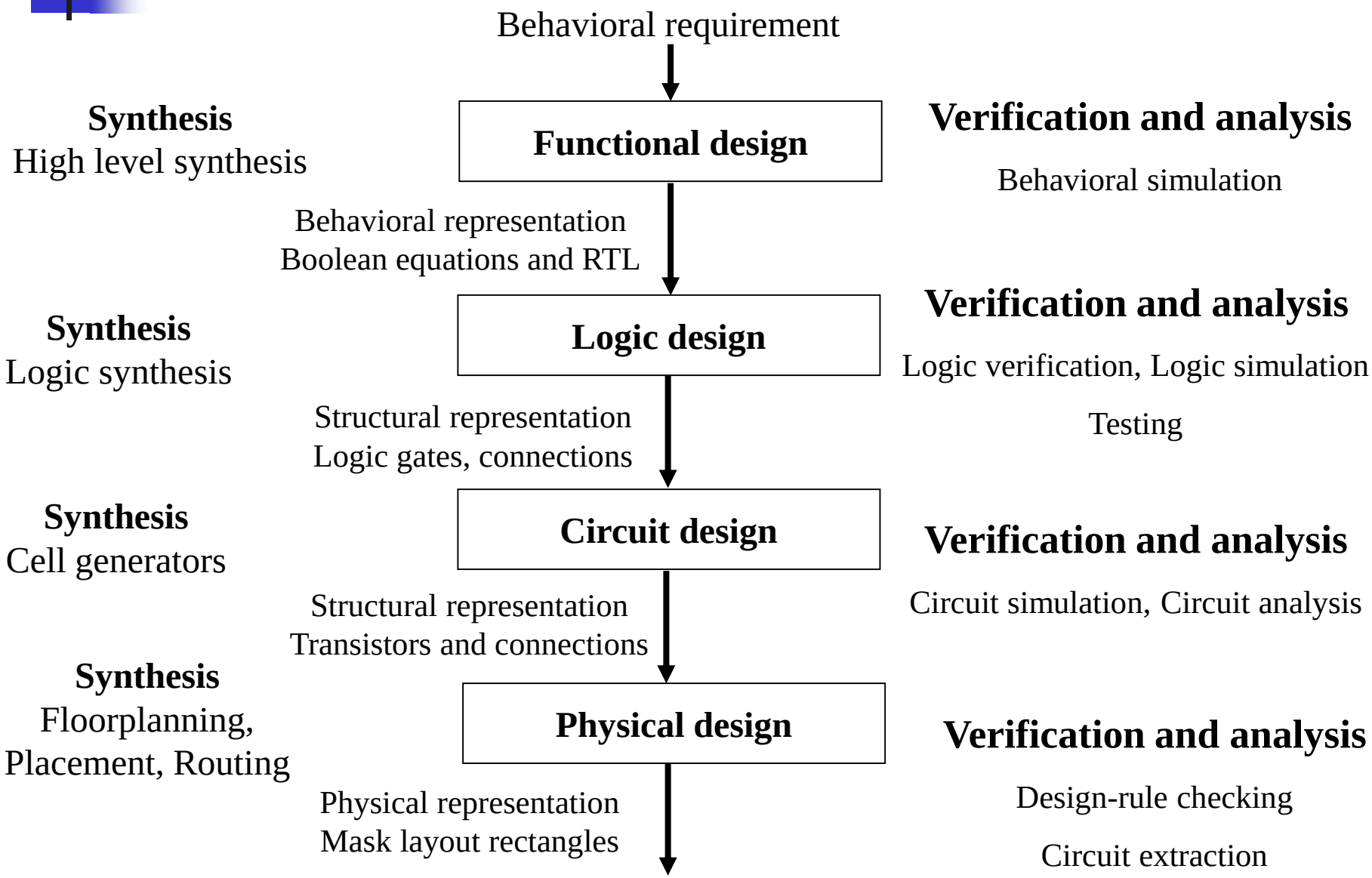
- Need parametrized capability in terms of speed and layout
- Examples : FARADAY Memory Compile

  User Interface : memaker

  Single port RAM, Dual port RAM, ROM

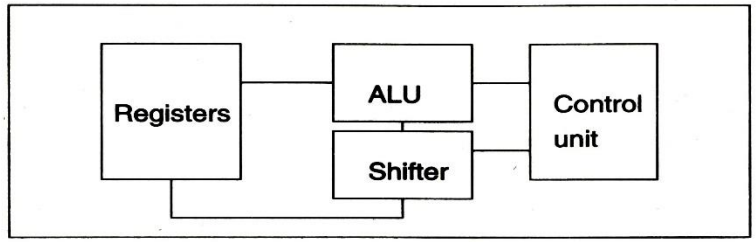
  Data sheet, Verilog simulation module, netlist simulation timing

Synthesis Flow of Semi Custom design (1/2)

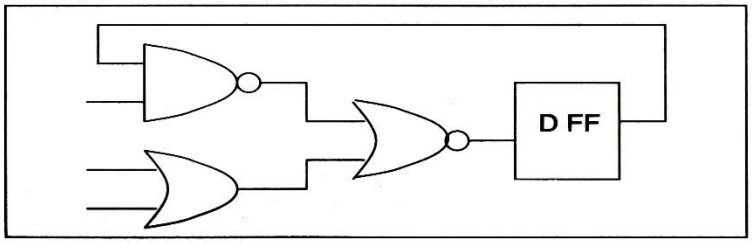


Synthesis Flow of Semi Custom design (2/2)

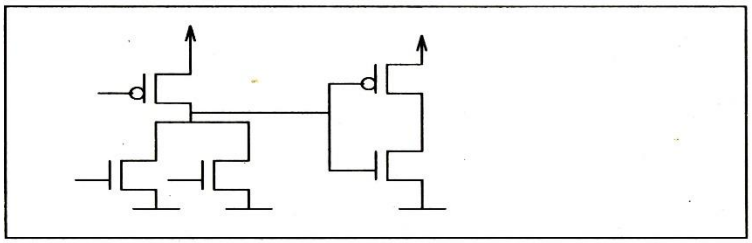
Functional design



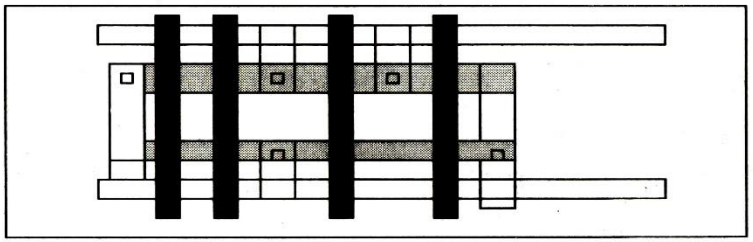
Logic design



Circuit design



Physical design



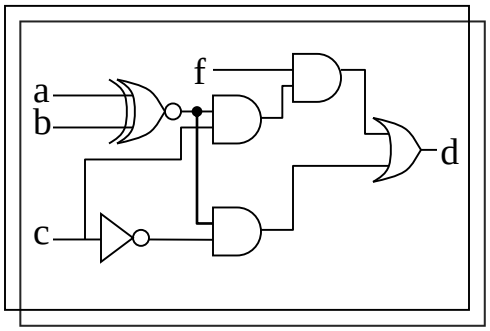
Synthesis (1/3)

- *Synthesis = Translation+Optimization+Mapping*

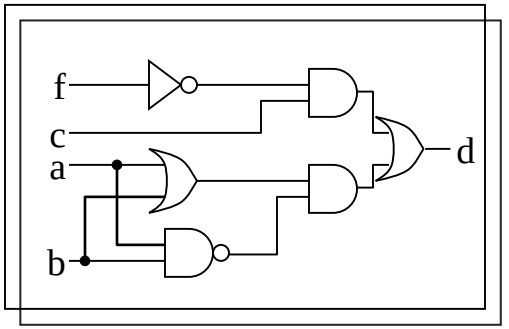
```
always @(…)
   if (a==b)
      if (c==1)
         d=f;
      else
         d=1;
   else
      d=0;
```

HDL Source

Translate into Boolean Representation



Optimize + Map

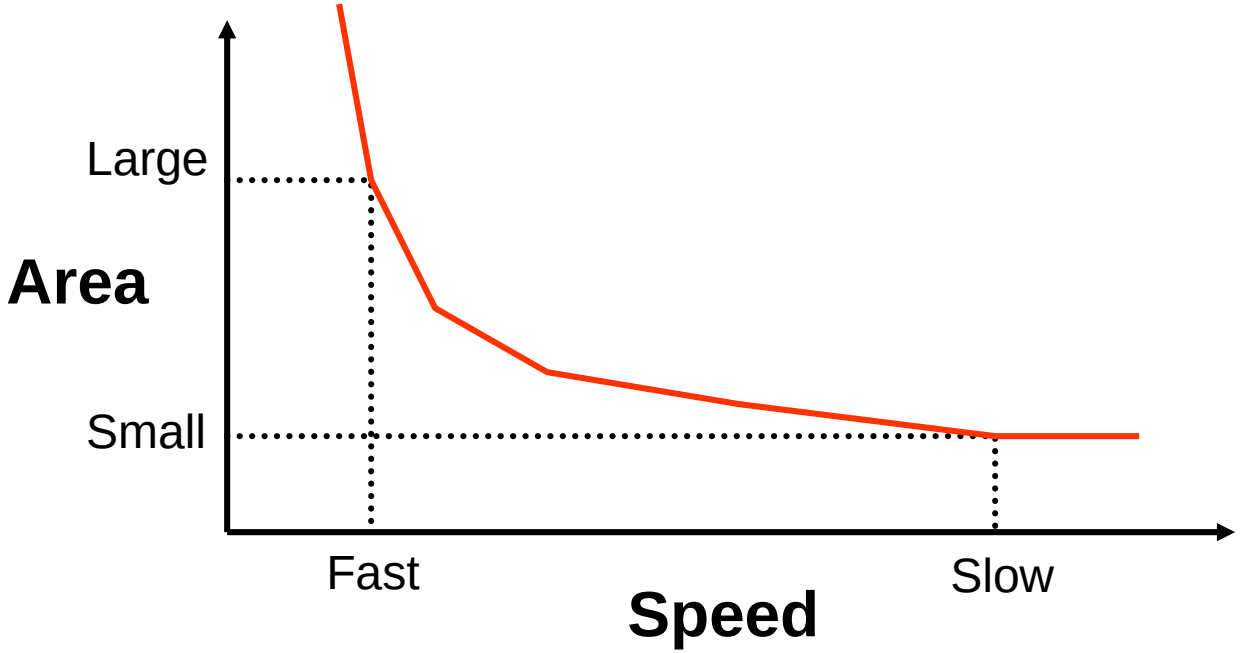


Target Technology

Process of logic synthesis

Synthesis (2/3)

- Synthesis is **constraint-driven**
  - You set the goals. Design Compiler optimizes design toward goals.



Synthesis (3/3)

- Providing an environment and various tools for the designers to produce circuits automatically and efficiently to meet the requirements of
  - **performance**
  - **area**
  - **testability**