2023 Digital IC Design Homework 3

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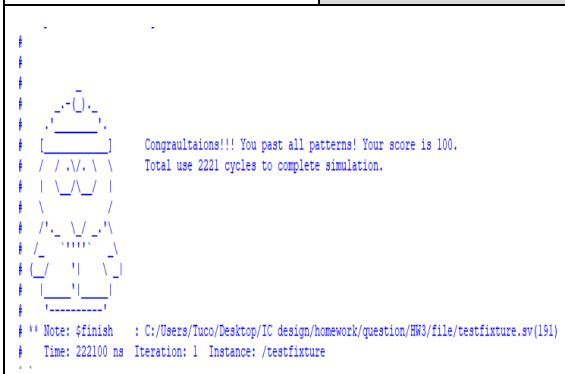
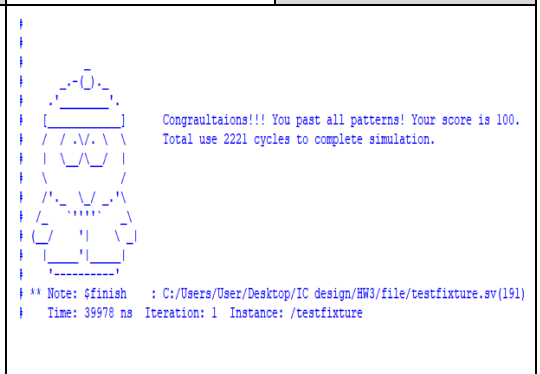
Simulation Result

Functional simulation	100	Gate-level simulation	100

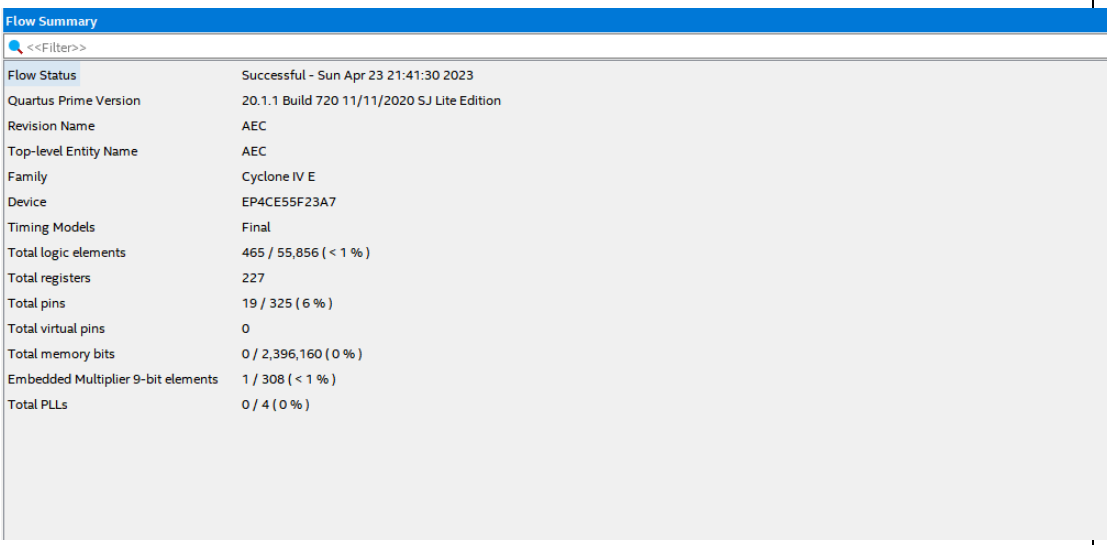




Synthesis Result

Total logic elements	465
Total memory bits	0
Embedded multiplier 9-bit elements	1
Total cycle used	2221
Clock width	40 ns

(your flow summary)



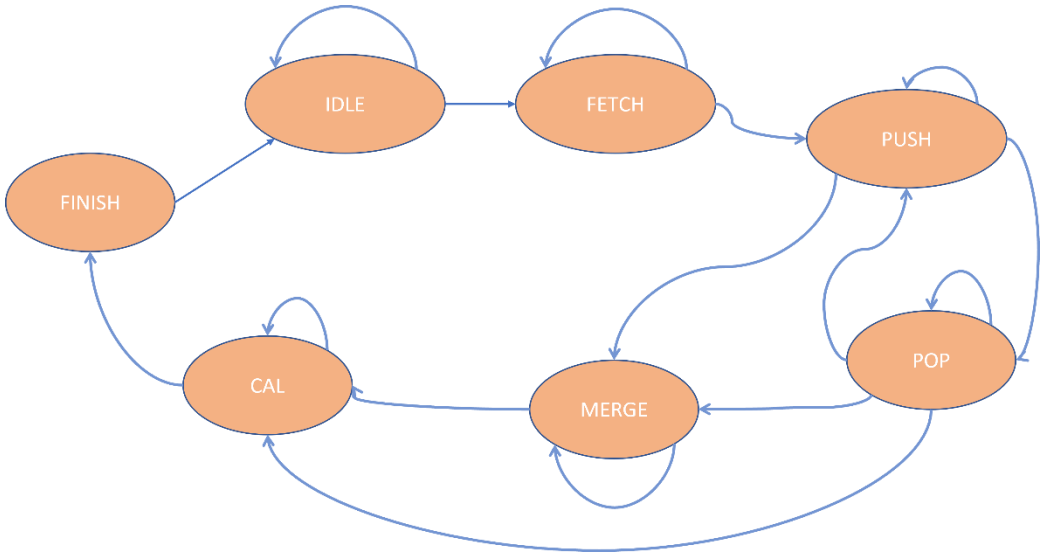
Flow Summary

<<Filter>>

Flow Status	Successful - Sun Apr 23 21:41:30 2023
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	AEC
Top-level Entity Name	AEC
Family	Cyclone IV E
Device	EP4CE55F23A7
Timing Models	Final
Total logic elements	465 / 55,856 (< 1 %)
Total registers	227
Total pins	19 / 325 (6 %)
Total virtual pins	0
Total memory bits	0 / 2,396,160 (0 %)
Embedded Multiplier 9-bit elements	1 / 308 (< 1 %)
Total PLLs	0 / 4 (0 %)

Description of your design

The proposed work is implemented using a finite state machine (FSM) that is divided into seven states. The state diagram is described below:



Given that interaction between the state is too complicated. We will give the brief description to the seven states.

IDLE: Resets all params and waits till the data inputs.
FETCH: Gets the input values and stores them into a predefined array.
PUSH: Pushes the input into the output array or operator stack.
POP: Pops the operator out to output array.
MERGE: Merges the operator stack and output array if the input all be scanned.
CAL: calculates the output array and returns the result.
FINISH: Rises the valid flag to outputs the result.

*Scoring = Area cost * Timing cost*

*Area cost = Total logic elements + Total memory bits + 9*Embedded multipliers 9-bit elements*

*Timing cost = Total cycle used * Clock width*

*** Total logic elements must not exceed 1500.**