DIGITAL DESIGN

ASSIGNMENTREPORT

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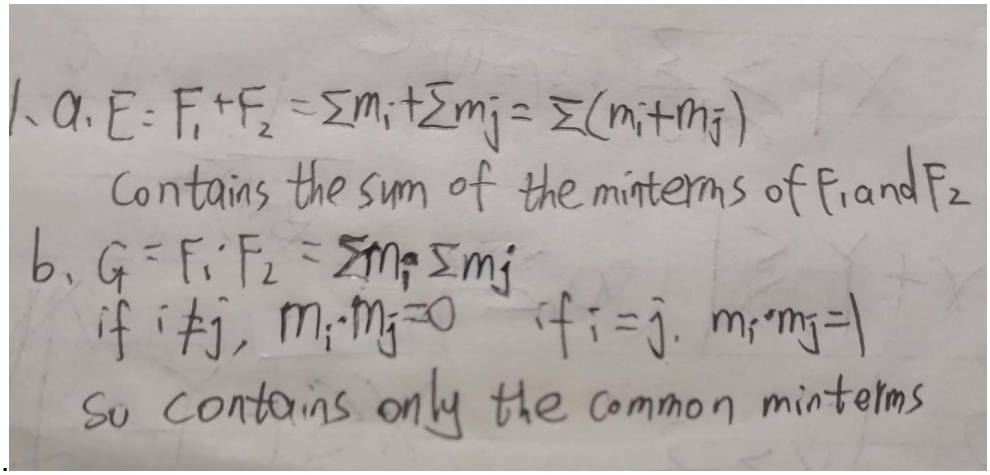
PART 1: DIGITAL DESIGN THEORY

Provide your answers here:

1.



2.a. $\prod(0, 2, 4, 5, 6)$ b. $\sum(0, 2, 4, 6, 7, 9, 10, 12, 14)$

3.a. $\sum(2, 3, 7, 8, 9, 10, 11, 15)$ a'b'cd'+a'b'cd+a'bcd+ab'c'd'+ab'c'd+ab'cd'+ab'cd+abcd

b. $\prod(1, 4, 5)$ abc'+a'bc'+a'b'c'+abc+a'bc=m6+m2+m0+m7+m3=(m1+m4+m5)'=M1*M4*M5

=(a+b+c')*(a'+b+c)*(a'+b+c')

4.a. y'z' + yz' + x'z = z'+x'z=(x'+x)z'+x'z=x'z'+xz'+x'z=x'+xz' ≠ x'z' false

b. x'y'+ x'z'+ yz =x'y'(z'+z)+x'z'(y'+y)+yz(x'+x)=x'y'z'+x'y'z+x'yz'+x'yz+xyz=x'z+x'z'+xyz=x'+xyz

false

5.a.

m0			m2
	m5	m7	
	m13	m15	
m8			m10

=BD+B'D'

b.

	m1	m3	
m4	m5	m7	m6

	m13	m15	
	m9	m11	

=w’x+z

c.A’BCD+ABCD+ABCD’+A’B’CD+A’B’C’D+AB’CD+AB’C’D

	m1	m3	
		m7	
		m15	m14
	m9	m11	

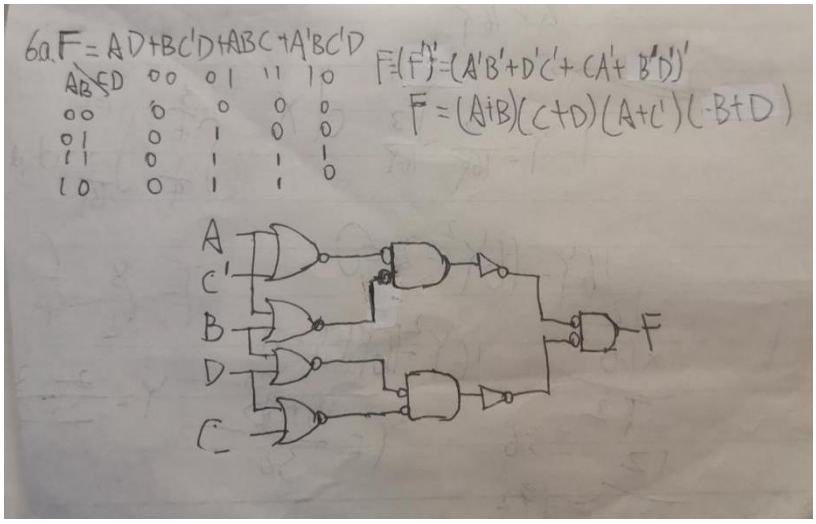
=ABC+CD+B’D

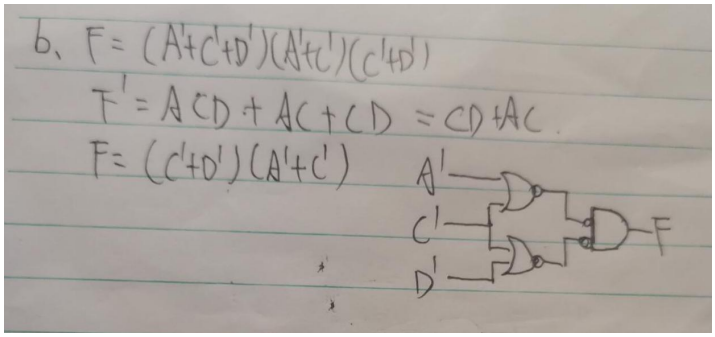
d.A’B’C’D’+ABC’D+A’BC’D+A’B’C’D+A’BCD+ABCD+AB’CD

m0	m1		
	m5	m7	
	m13	m15	
		m11	

=A’B’C’+BD+ACD

6.





7.a.

	00	01	11	10
0	m0 1	m1 1	X	X
1	m4 1	m5 1	X	m6 1

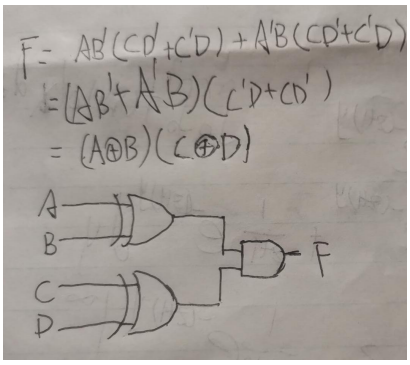
When m2=m3=m7=1,it is the most simplified function

F(x, y, z)=∑ (0, 1, 2, 3, 4, 5, 6, 7)=1

b.can not producefour grids to simplify F

0	0	X	0
0	m5 1	m7 1	m6 1
m12 1	0	0	m14 1
0	X	X	0

X can not produce four grids to simplify F, so X=0. F=A'BD+A'BC+ABD'

8. 

PART 2: DIGITAL DESIGN LAB (TASK1)

DESIGN

Describe the design of your system by providing the following information:

- *Verilog design (provide the Verilog code)*
- *Truth-table*

SIMULATION

Describe how you build the test bench and do the simulation.

- *Using Verilog(provide the Verilog code)*
- *Wave form of simulation result (provide screen shots)*
- *The description on whether the simulation result is same as the truth-table, is the function of the design meet the expectation.*

CONSTRAINT FILE AND THE TESTING

Describe how you test your design on the Minisys Practice platform.

- *Constraint file (provide the screen shots on the feature of a pin and the binding info between pins and the input /output ports)*
- *The testing result (provide the screen shots (at least 3 testing scene) to show state of inputs and outputs along with the related descriptions.*

THE DESCRIPTION OF OPERATION

Describe the problem occurred while in the lab and your solution. Any suggestions are welcomed.

- *Problems and solutions*

PART 2: DIGITAL DESIGN LAB (TASK2)

DESIGN

Describe the design of your system by providing the following information:

- *Verilog design while using data flow (provide the Verilog code)*
- *Verilog design while using structured design (provide the Verilog code)*
- *Block design (provide screen shots)*
- *Truth-table*

SIMULATION

Describe how you build the test bench and do the simulation.

- *Using Verilog (provide the Verilog code)*
- *Wave form of simulation result (provide screen shots)*
- *The description on whether the simulation result is same as the truth-table, is the function of the design meet the expectation*

CONSTRAINT FILE AND THE TESTING

Describe how you test your design on the Minisys Practice platform.

- *Constraint file (provide the screen shots on the feature of a pin and the binding info between pins and the input /output ports)*
- *The testing result (provide the screen shots (at least 3 testing scene)) to show state of inputs and outputs along with the related descriptions.*

THE DESCRIPTION OF OPERATION

Describe the problem occurred while in the lab and your solution. Any suggestions are welcomed.

- *Problems and solutions*