通过非线性ADC在模拟信号上进行gamma矫正

CMOS Image Sensor with Analog Gamma Correction using Nonlinear Single-Slope ADC

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***Abstract*—A human eye has the logarithmic response over wide range of light intensity. Although the gain can be set high to identify details in darker area on the image, this results in saturation in brighter area. The gamma correction is essential to fit the human eye. However, the digital gamma correction degrades image quality especially for darker area on the image due to the limited ADC resolution and the dynamic range. This paper proposes a CMOS image sensor (CIS) with nonlinear analog-to-digital converter (ADC) which performs analog gamma correction. The CIS with the proposed nonlinear ADC conversion scheme was fabricated with a 0.35-μm CMOS process. The test results show the improved image quality than digital gamma correction.**

I. Introduction

Recently, CIS has been rapidly replaced the charge coupled device (CCD) sensor due to its high speed imaging and on-chip system integration capability [1]-[3]. The image signal processing (ISP) block controls the gain to accommodate wide dynamic range of the natural scenes [4]. However, the gain control is not effective for ill-illuminated scene because the high gain to improve the brightness of darker area on the image result in saturation in brighter area as illustrated in Fig. 1(b). The gamma correction that realizes high gain for lower signal level and low gain for high signal level as shown in Fig. 1(c) is required to fit the logarithmic response of the human eye. Conventional CIS performs this gamma correction in digital domain. The major problem in a digital gamma correction is the fact that it amplifies the quantization noise for lower signal level and result in image quality degradation [5]. 数字gain会增大量化噪音

Although a analog gamma correction scheme is reported in [6], it does not utilize the maximum dynamic range. This paper proposes a nonlinear single slope ADC that utilizes full dynamic range as shown in Fig. 1(c).

Section II describes the architecture of the conventional single slope ADC used in CIS. Section III proposes the nonlinear single slope ADC. Section IV and V present its simulation results and experimental results, respectively.

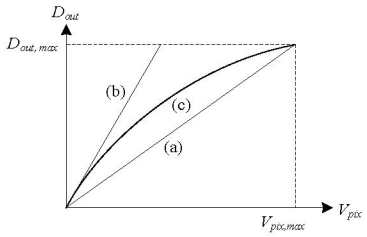

Figure 1. Gain and dynamic range: (a) normal gain, (b) high gain, and (c) gamma correction gain.

The conclusion is provided in section VI.

II. Operation Of The Single-Slope ADC

Fig. 2 shows the operation principle of the single-slope ADC used in CIS. The ADC has a comparator and an N-bit latch, a ramp generator and a counter. The comparator generates the *latch* signal by comparing the pixel signal with the ramp signal. The latch stores the counter value when the comparator generates the *latch* signal.

At the first phase, the ramp generator and the counter are reset and the pixel reset level, ramp offset and the comparator offset are sampled. At the second phase, all the offsets are canceled out. This offset cancellation is called

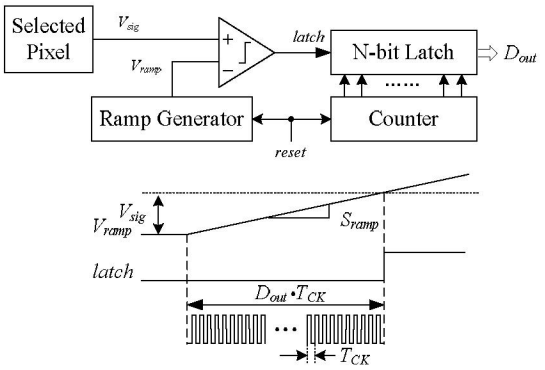

Figure 2. Operation principal of the single-slope ADC with comparator.

correlated double sampling (CDS). At the third phase, the ramp signal, V_{ramp} starts to increase and the comparator changes its output, *latch* when V_{ramp} exceeds the V_{sig} as shown in Fig. 2. The counter counts up while the ramp signal is increasing. The latch stores the counter value when the comparator changes its output logic. Then, the content of the latch represents the duration time until the V_{ramp} reaches to V_{sig} and it corresponds to ADC result for V_{sig}. Therefore, the ADC result is dependent on the ramp slope, S_{ramp} and the clock frequency, f_{CK} as follows.

$$D_{out} = V_{sig} \frac{f_{CK}}{S_{ramp}}. \tag{1}$$

III. The Proposed Nonlinear Single-Slope ADC

Fig. 3 shows the principle of the proposed nonlinear single slope ADC. Since the time elapse until the ramp signal reaches to input signal level represents the ADC result, the ADC behavior shown in Fig. 3(a) can be implemented by use of nonlinear ramp as shown in Fig. 3(b).

The ramp signal should reach V_{max} at T_{max}, which is the maximum ADC time to utilize the full dynamic range because T_{max} corresponds to the maximum digital output, D_{max}. This ramp signal can be implemented with an integrator that has a constant current input and a time dependent current input as shown in Fig. 4.

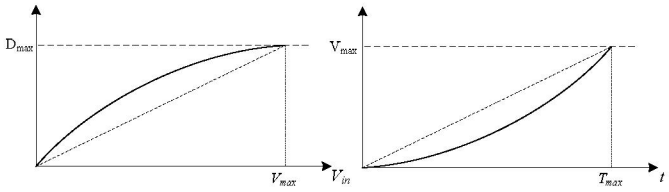

Figure 3. Principle of nonlinear single slope ADC: (a) desired ADC behavior, (b) required ramp signal.

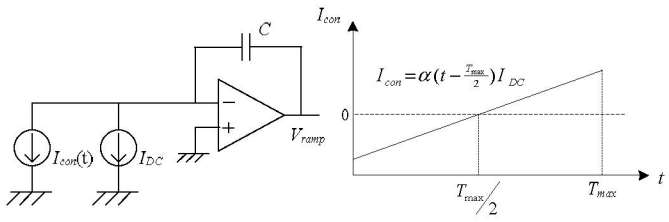

Figure 4. Nonlinear ramp generator: (a) schematic diagram, (b) control current for the nonlinear ramp generator.

The output voltage of the ramp generator shown in Fig. 4 can be obtained as follows.

$$V_{ramp}(t) = \frac{1}{C}\int_0^t [I_{DC} + I_{con}(\tau)]d\tau = \frac{I_{DC}}{C}\left[\left(1 - \frac{\alpha T_{max}}{2}\right)t + \frac{\alpha}{2}t^2\right] \tag{2}$$

Equation (2) contains the second order term that realizes the wave form as shown in Fig. 3(b). As the slope of the time dependent current source, α controls the relative weight of the second order term, higher α provides larger curvature. The ramp reaches V_{max} at T_{max} regardless of the α as follows.

$$V_{ramp}(T_{max}) = \frac{1}{C} I_{DC} T_{max} = V_{max}. \tag{3}$$

This condition is satisfied as long as the integral of I_{con}(t) over T_{max} is equal to zero.

Fig. 5 shows the block diagram of the proposed nonlinear ramp generator.

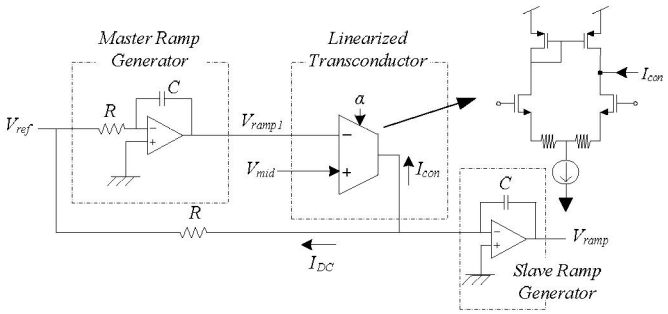

Figure 5. Block diagram of the proposed nonlinear ramp generator.

The time dependant current source is realized with an additional ramp generator and a linearized transconductor. The output of the master ramp generator, V_{ramp1} corresponds to the time elapse from the beginning of the ramping. Then, V_{ramp1} is converted into current by the transconductor. Since I_{con}(t) should change its polarity at $T_{max}/2$, as shown in Fig. 4(b) the operational transconductor is biased with a reference voltage, Vmid that is half of the maximum V_{ramp1} at T_{max}. The transconductance of the transconductor corresponds to α in (2) and it can be controlled by either the transistor size of the differential pair, source degeneration resistor or the tail current.

The proposed nonlinear ADC corresponds to an analog gamma correction that provides higher SNR for lower signal level than the digital gamma correction. The input signal and the output of the linear ADC can be expressed as

$$\begin{aligned} P &= S + n_c \\ D_{out} &= S + n_c + n_q, \end{aligned} \tag{4}$$

where P is the pixel value, S is the signal, n_c is the circuit noise, D_{out} is the output of linear ADC and n_q is quantization

noise. Equation (4) represents that the linear ADC output includes the quantization noise in addition to pixel signal. The output of the digital gamma correction, G_{dig} can be expressed as

$$G_{dig} = A(S)\cdot D_{out} + n_D = A(S)\cdot(S + n_c) + A(S)\cdot n_q + n_D \quad (5)$$

where $A(S)$ is the gamma correction curve and n_D is the truncation error in digital gamma correction. The output of the nonlinear ADC, G_{ana} can be expressed as follows.

$$G_{ana} = A(S)\cdot P + n_q = A(S)\cdot(S + n_c) + n_q \cdot \quad (6)$$

Equation (5) and (6) show that the analog gamma correction has a constant quantization noise over the entire signal range while the digital gamma correction has amplified quantization noise at the low signal level because $A(S) > 1$ for lower signal level.

IV. Simulation Results

Fig. 6 shows the transistor level simulation result of the proposed ramp generator. The transconductance of the source degenerated OTA is controlled by selecting the size of transistors in the differential pair.

Fig. 7 shows the quantization error simulation result of the conventional digital gamma correction with linear ADC and the analog gamma correction using the proposed nonlinear ADC. The gamma correction curves for both cases are set identical. It shows that the analog gamma correction does not amplify the quantization noise while the digital gamma correction amplifies the quantization noise at low input signal level.

V. Experimental Results

The proposed nonlinear ramp generator is embedded in a CIS with 4-TR pixel and fabricated using 0.35-μm CMOS process. Fig. 8 shows the microphotograph of the fabricated chip. The fabricated CIS is capable to change ramp slope and the transconductance of the linearized transconductor.

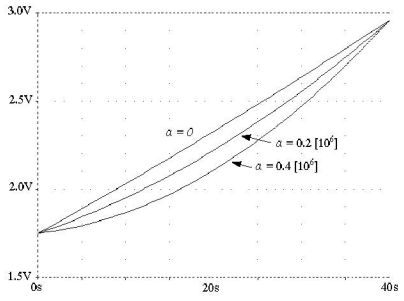

Figure 6. Transistor level Simulation results of proposed ramp generation.

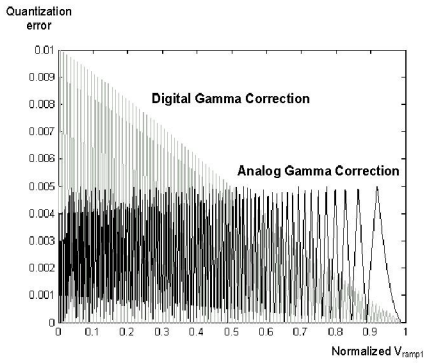

Figure 7. Quantization error simulation results for α=0.3x106 and 10bit ADC resolution of analog gamma correction using the proposed nonlinear ADC and conventional digital gamma correction with linear ADC.

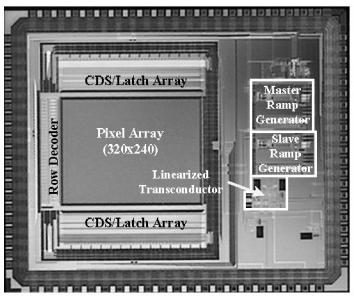

Figure 8. Die photograph of the fabricated CIS (4,800x 4,000μm^2).

Fig. 9 shows the measurement result of the proposed ramp generator for various α. The ramp signal reaches V_{max} at T_{max} regardless of the α.

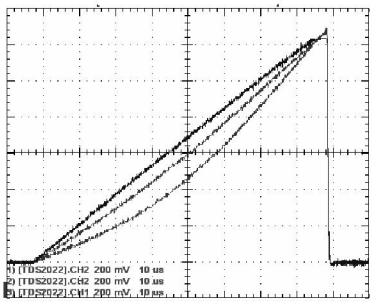

Figure 9. The measurement result of the proposed ramp generator.

Fig. 10 shows images from the fabricated CIS. The image obtained with normal gain can not see the details in lowly illuminated area as shown in Fig. 10(a) (enclosed area with white box on the image). Although the details in dark area can be observable with high gain, the brighter area is saturated as shown in Fig. 10(b). The image with nonlinear ADC not only provides details in darker area but also avoids saturation in brighter area as shown in Fig. 10(c).

Fig. 11(a) shows the result image of the digital gamma correction with the image obtained from the normal gain linear ADC. Fig. 11(b) is the image obtained from the proposed CIS. The gamma correction curves for both cases

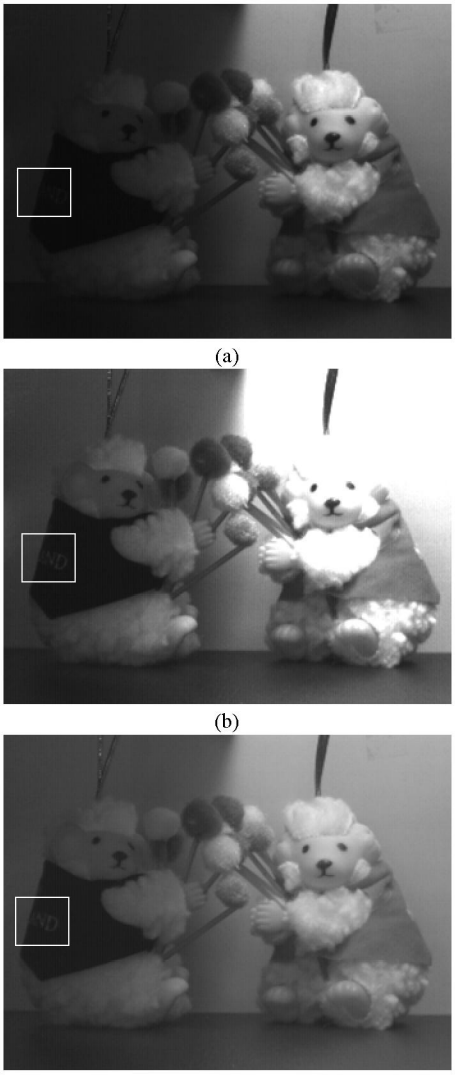

Figure 10. CIS image. (a) With normal gain linear ADC. (b) With high gain linear ADC (gain=5). (c) With the nonlinear ADC (α=0.4x106).

are set identical. The analog gamma correction provides better image quality than the digital gamma correction for darker area as marked with white box on the image.

The measured performances of fabricated CIS are summarized in table I.

TABLE I. PERFORMANCE SUMMARY

Technology	0.35-μm CMOS
Pixel Pitch	5.6 μm^2
Resolution	320 x 240 (QVGA)
Frame Rate	15 fps (typical)
Clock Frequency	12 MHz (typical)
ADC Resolution	10 bit (typical)
Supply Voltage	3.3 V
Power Consumption	30 mW

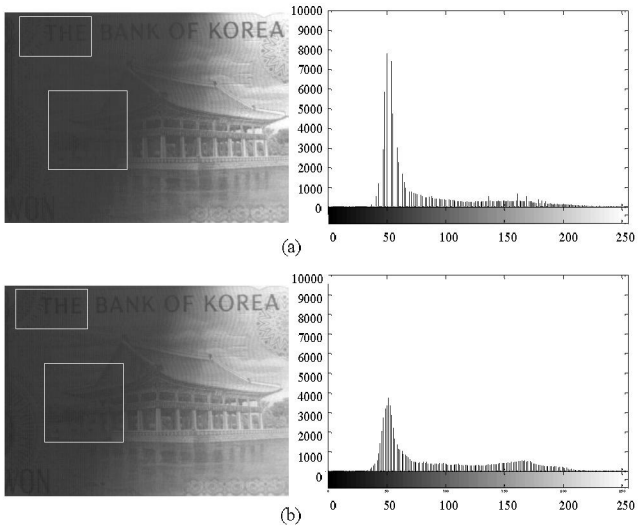

Figure 11. Comparison between the digital gamma correction and the analog gamma correction. (a) Image and its histogram after digital gamma correction with the linear normal gain ADC. (b) Image captured with the proposed nonlinear ramp generator and its histogram.

VI. CONCLUSION

This paper presented a nonlinear single slope ADC for analog gamma correction in a CIS. The images from the fabricated CIS showed that the analog gamma correction using nonlinear ADC provides more improved image quality than conventional approach.

ACKNOWLEDGMENT

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