

Team11 Lab1 Report

2025/3/7

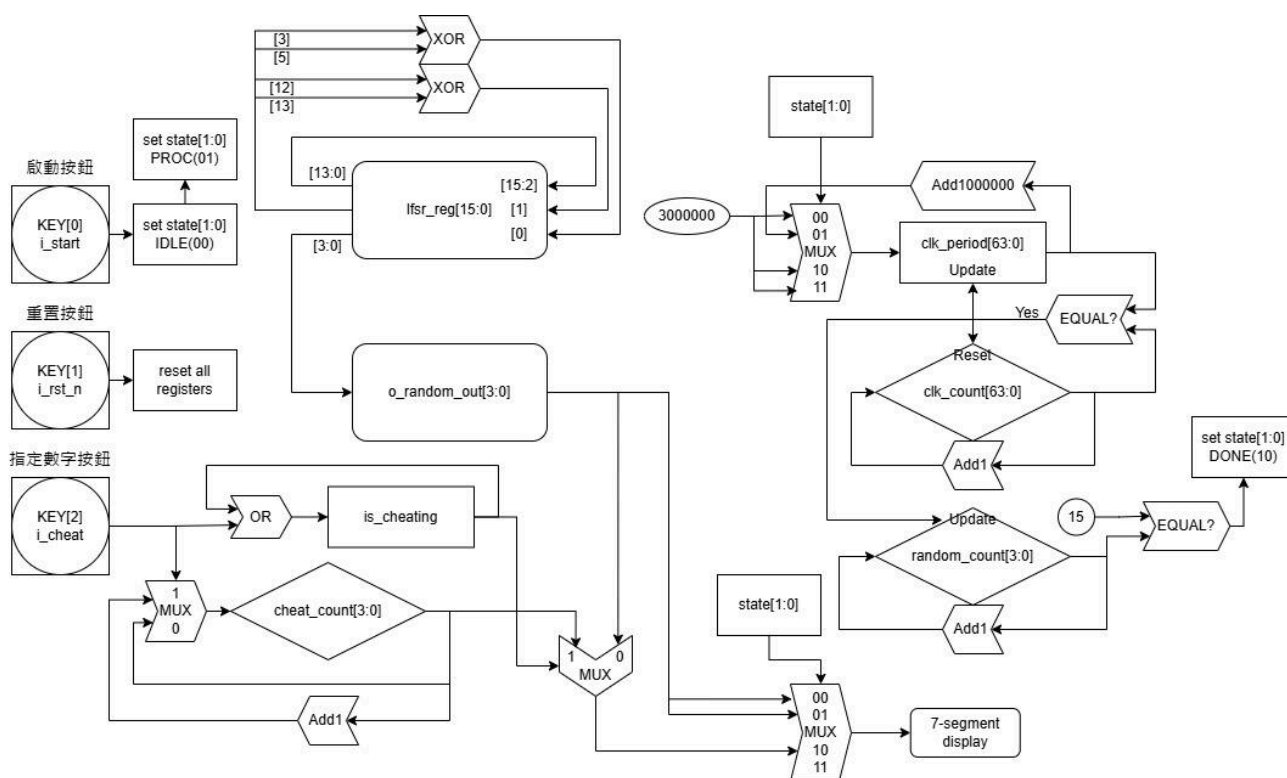
I. File Structure

team11_lab1

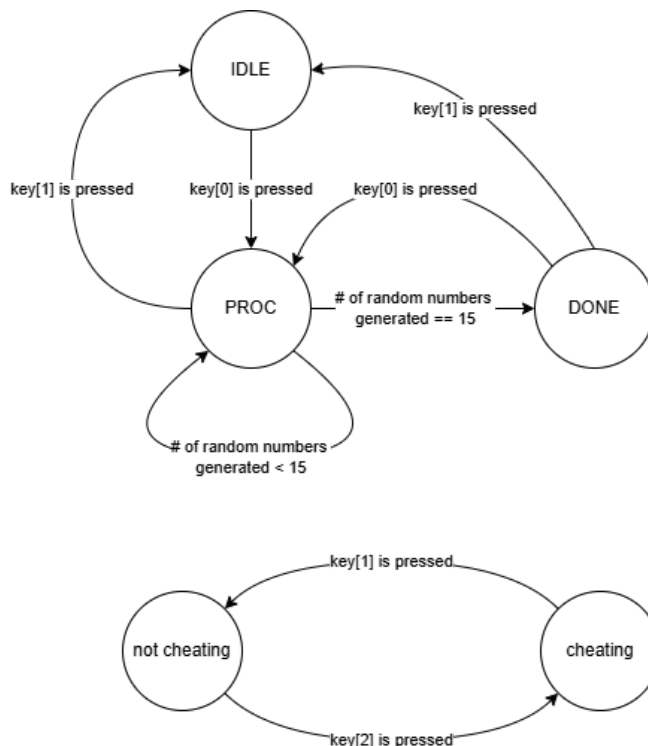
- team11_lab1_report.pdf
- src
 - Top_0307.sv
 - DE2_115
 - DE2_115.sv

*note that because we added a new function when we push the key2 button, DE2_115.sv has been modified to load the stimulation of the key2 button.

II. System Architecture



III. Hardware Scheduling



IV. Problems & Thought

In the beginning, we built the FSM using sequential blocks, and it worked correctly. However, when we developed the bonus functionality, it didn't behave as expected due to the design of the FSM. Additionally, we encountered multiple synthesis errors while adjusting our code.

After resolving the synthesis errors, we faced an issue where the FSM couldn't transition to the DONE state and instead always returned to the IDLE state. After extensive debugging, we finally discovered that our "state" variable had only one bit, which was a mistake that did not cause a compilation error.

//B10901023: This was my first time using an FPGA board; I think it was fun.

//B10901010: B10901023 is GOD.

//B10901062: I don't know. The homework was already finished before I arrived.

V. Fitter Summary

Table of Contents		Fitter Summary	
Flow OS Summary		Fitter Status	Successful - Fri Mar 07 17:47:40 2025
Flow Log		Quartus II 64-Bit Version	15.0.0 Build 145 04/22/2015 SJ Full Version
Analysis & Synthesis		Revision Name	DE2_115
▼ Fitter		Top-level Entity Name	DE2_115
Summary		Family	Cyclone IV E
Settings		Device	EP4CE115F29C7
Parallel Compilation		Timing Models	Final
I/O Assignment Warnings		Total logic elements	224 / 114,480 (< 1 %)
Ignored Assignments		Total combinational functions	219 / 114,480 (< 1 %)
Incremental Compilation Section		Dedicated logic registers	166 / 114,480 (< 1 %)
Pin-Out File		Total registers	166
Resource Section		Total pins	518 / 529 (98 %)
I/O Rules Section		Total virtual pins	0
Device Options		Total memory bits	0 / 3,981,312 (0 %)
Operating Settings and Conditions		Embedded Multiplier 9-bit elements	0 / 532 (0 %)
Messages		Total PLLs	0 / 4 (0 %)
Suppressed Messages			
Flow Messages			
Flow Suppressed Messages			
Assembler			

VI. Timing Analyzer

Table of Contents		Unconstrained Paths		
Incremental Compilation Section			Property	Setup
Pin-Out File				Hold
Resource Section		1	Illegal Clocks	0
I/O Rules Section		2	Unconstrained Clocks	0
Device Options		3	Unconstrained Input Ports	3
Operating Settings and Conditions		4	Unconstrained Input Port Paths	172
Messages		5	Unconstrained Output Ports	11
Suppressed Messages		6	Unconstrained Output Port Paths	40
Flow Messages				
Flow Suppressed Messages				
Assembler				
▼ TimeQuest Timing Analyzer				
Summary				
Parallel Compilation				
SDC File List				
Clocks				
Slow 1200mV 85C Model				
Slow 1200mV 0C Model				
Fast 1200mV 0C Model				
Multicorner Timing Analysis Summary				
Multicorner Datasheet Report Summ				
Advanced I/O Timing				
Clock Transfers				
Report TCCS				
Report RSKM				
Unconstrained Paths				
Messages				