Team11 Lab1 Report

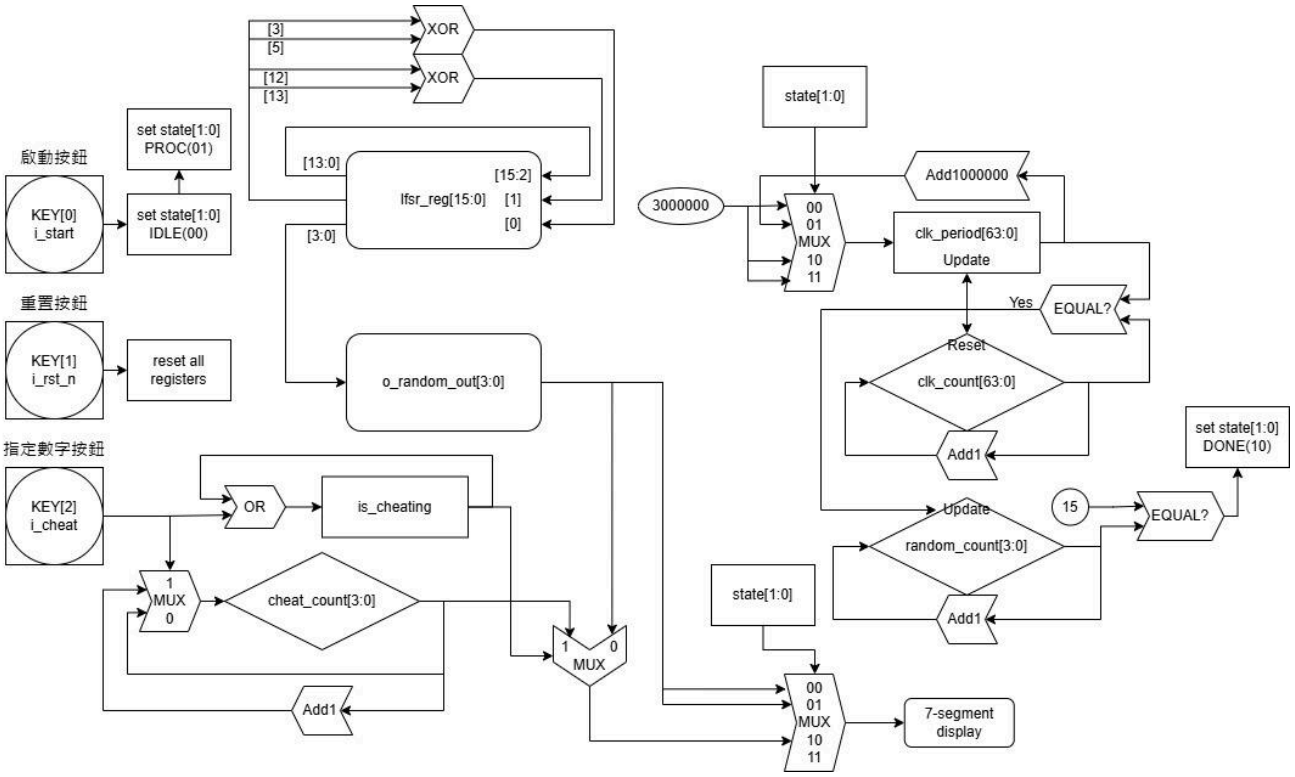
2025/3/7

I. File Structure

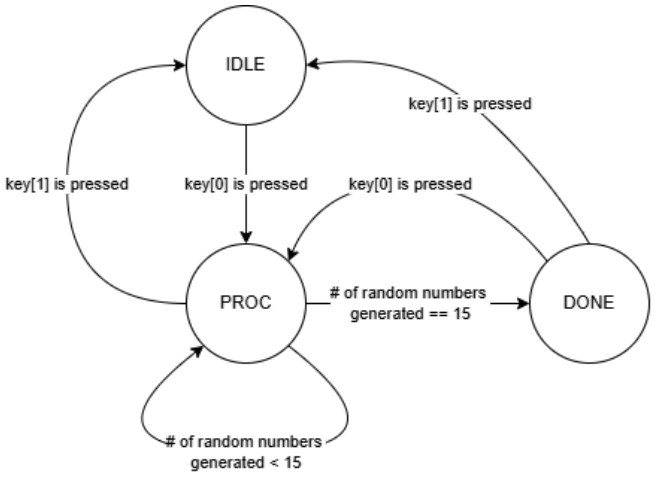
team11_lab1
- team11_lab1_report.pdf
- src
  - Top_0307.sv
  - DE2_115
    - DE2_115.sv

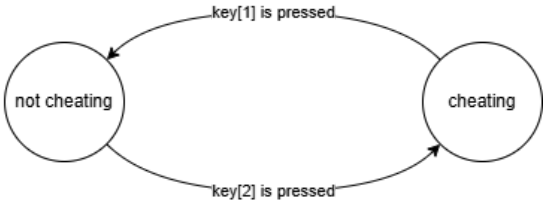
*note that because we added a new function when we push the key2 button, DE2_115.sv has been modified to load the stimulation of the key2 button.

II. System Architecture



III. Hardware Scheduling





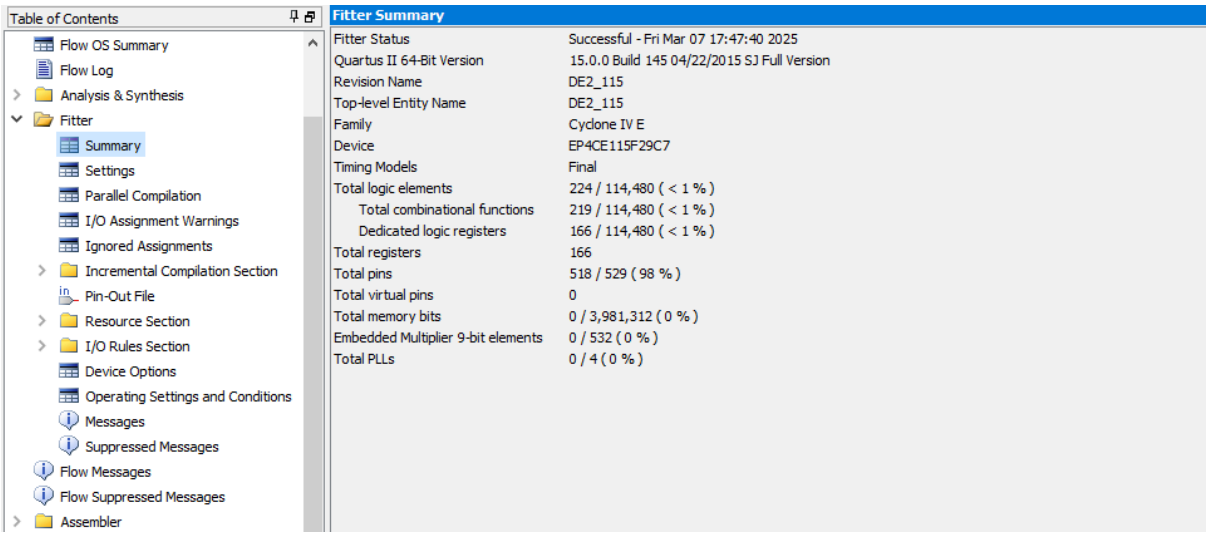
IV. Problems & Thought

In the beginning, we built the FSM using sequential blocks, and it worked correctly. However, when we developed the bonus functionality, it didn't behave as expected due to the design of the FSM. Additionally, we encountered multiple synthesis errors while adjusting our code.

After resolving the synthesis errors, we faced an issue where the FSM couldn't transition to the DONE state and instead always returned to the IDLE state. After extensive debugging, we finally discovered that our "state" variable had only one bit, which was a mistake that did not cause a compilation error.

//B10901023: This was my first time using an FPGA board; I think it was fun.
//B10901010: B10901023 is GOD.
//B10901062: I don't know. The homework was already finished before I arrived.

V. Fitter Summary



VI. Timing Analyzer