Title:

Predictable Routing of Network-On-Chip for Real-Time computing on

Multi-Processor Systems-on-Chip

\* Abstract

We propose a

\* Introduction

Improvements in semiconductor technology along with an increasing concern for energy efficiency have led to an industry wide shift toward a design paradigm which leverages parallelism in order to meet performance. Network-On-Chip (NoCs) has been proposed [4][5] as an attractive

alternative to traditional dedicated wires in order to achieve

performance and modularity while connecting

Multi-Processor Systems-on-Chip **(MPSoC).**

Embedded systems are often required to meet stringent performance requirements in order to meet real time computing constraints while still keeping size and cost attractive.

A common paradigm in network design as well as NoCs is the usage of dynamic routing and virtual channels however such architecture is sensitive to changes in traffic from multiple sources and can't assure latency, as such designing a real time MPSoC is difficult using this approach.

Contributions

\* Problem definition - (real time tasks on single chip,mapping)

Application model is a task communication graph (TCG)

A directed graph *Gt* = (*V*, *E*), where *V* is the set of computation tasks,

and *E* is the set of communication links between tasks. A task *v* has

an execution time *t*, which is a function of task executions. A directed

edge *e* = (*vs*, *vd*, *w*) has a source task *vs*, a destination task *vd* and the

amount of data *w* that sends from *vs* to *vd*. *w* is a function of

communication transactions

\* Algorithm

  \* Routing (MCF / LP , rounding)

  \* Scheduling

\* Experimental Results

  \* Simulator

  \* MCSL Benchmark

\* Conclusions

\* References

NoC Synthesis Flow for Customized Domain

Specific Multiprocessor Systems-on-Chip

Davide Bertozzi, Antoine Jalabert, Srinivasan Murali, Student Member, IEEE,

Rutuparna Tamhankar, Student Member, IEEE, Stergios Stergiou, Student Member, IEEE,

Luca Benini, Member, IEEE, and Giovanni De Micheli, Fellow, IEEE

[4] W. J. Dally and B. Towles, "Route Packets, Not Wires:

On-Chip Interconnection Networks," ACM/IEEE Deszgn

Automation Conf., pp. 684-689, June 2001.

[5] C. Seitz, "Let's Route Packets Instead of Wires", Advanced

Research in VLSI: Proceedings of the Sixth MIT Conference, pp. 133-138, 1990.

[6]  “Weichen Liu, Jiang Xu, Xiaowen Wu, Yaoyao Ye, Xuan Wang, Wei Zhang, Mahdi Nikdast, Zhehui Wang, “A NoC Traffic Suite Based on Real Applications,” *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*, July 2011”

[7] Investigating Performance Advantages of Random Topologies on Network-on-Chip

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[8] **NoCs Simulation Framework for OMNeT++**

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L. Benini and G. De Micheli, "Networks on chip: a new SoC paradigm", IEEE Computer, vol. 35, no. 1, Jan. 2002

J. Kim, J. Balfour, and W. Dally, “Flattened Butterfly Topology

for On-Chip Networks,” in International Symposium on

Microarchitecture, December 2007, pp. 172–182.

Communication Latency Aware Low Power NoC Synthesis

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