Yanjun Wang

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Last Updated on 7th October 2020

EDUCATION

PURDUE UNIVERSITY

Ph.D. in Electrical and Computer Engineering
West Lafayette, Indiana
Aug 2016 - May 2022 (Expected)
Advised by **Prof. Xiaokang Qiu**
GPA: 3.80 / 4.00

Research Interest:
Programming Languages
Program Synthesis
Program Verification
Formal Methods
Program Analysis
Program Logics

HUAZHONG UNIVERSITY OF SCIENCE AND TECHNOLOGY

B.E. in Electrical Engineering
Wuhan, Hubei, China
Aug 2012 - Jun 2016
Excellent Student at HUST
GPA: 3.85 / 4.00

SKILLS

PROGRAMMING

Proficient:
Java • Python

Familiar:
C/C++ • Shell • Coq

TECHNICAL TOPICS

Well Experienced:
Programming Languages
Formal Methods
Compilers

Familiar With:
Software Analysis
Computer Network

AWARDS

CAV '19 Student Travel Grant
PLDI '19 Student Travel Grant
Silver Medal in ACM Student Research Competition (SRC) at POPL '18.

LINKS

LinkedIn:// **yjw**

EXPERIENCE

FACEBOOK, INC. | Software Engineer Intern

May 2020 - Aug 2020 | Systems and Infrastructures

- internship project on intent-based networking
- worked on improving a network design & config generation tool that provisions, migrates data-center networks based on high-level network specifications

RESEARCH

PURDUE UNIVERSITY | Graduate Research Assistant

Aug 2017 - Present | Purdue Computer-Aided Programming Lab

Comparative Synthesis on Network Design | 2019 - Present

- proposed a quantitative synthesis framework, called **comparative synthesis**
- generate network design automatically by making comparative quires to user, with design objectives conjectured

Retreet: Reasoning About Recursive Tree Traversals of Fine-grained | 2018 - Present

- proposed a stack-based, fine-grained representation of dynamic instances in a tree traversal
- encoded dependence analysis problems to Monadic Second-Order (MSO) logic over trees

DryadSynth: A Syntax-Guided Synthesizer | 2017 - 2020

- developed a novel **cooperative synthesis** framework **DryadSynth**
- exploits several divide-and-conquer strategies to split a synthesis problem to smaller subproblems that are solved by either a pure deductive component or a height-based enumeration algorithm
- got 2nd Place in INV Track of SyGuS-Comp'17
- won 1st Place in CLIA Track of SyGuS-Comp'18 and SyGuS-Comp'19

Dryad$_{dec}$: A Decidable Logic for Tree Data-structures with Measurements | 2017 - 2018

- proposed a decidable logic that supports user-defined recursive measure functions based on Max or Sum, and recursive predicates based on these measure functions, such as AVL trees or red-black trees
- proved **decidability** by small model property

PUBLICATIONS

Reconciling Enumerative and Deductive Program Synthesis[1]
Kangjing Huang, Xiaokang Qiu, Peiyuan Shen, and **Yanjun Wang**.
In Proc. of 41st ACM SIGPLAN Conference on Programming Language Design and Implementation (**PLDI '20**).

Learning Network Design Objectives Using A Program Synthesis Approach
Yanjun Wang, Chuan Jiang, Xiaokang Qiu, and Sanjay G. Rao.
In Proc. of 18th ACM Workshop on Hot Topics in Networks (**HotNets '19**).

A Decidable Logic for Tree Data-Structures with Measurements[1]
Xiaokang Qiu, **Yanjun Wang**.
In Proc. of 20th International Conference on Verification, Model Checking, and Abstract Interpretation (**VMCAI '19**).

[1] Authors are ordered alphabetically.