四川大学期末考试试题（闭卷）

（2021——2022 学年第 1 学期）　A 卷

课程号：304131030　课序号：　课程名称：数字逻辑（双语）　任课教师：　成绩：

适用专业年级：2021 级　学生人数：　印题份数：　学号：　姓名：

考 生 承 诺

我已认真阅读并知晓《四川大学考场规则》和《四川大学本科学生考试违纪作弊处分规定（修订）》，郑重承诺：

1、已按要求将考试禁止携带的文具用品或与考试有关的物品放置在指定地点；

2、不带手机进入考场；

3、考试期间遵守以上两项规定，若有违规行为，同意按照有关条款接受处理。

考生签名：

1. Choose the best answer from the four choices(20 points, 2 points per question).

(1) The output of an XOR gate is LOW when (　　).

A. no inputs are LOW　　B. all inputs are LOW

C. any input is LOW　　D. Both (A) and (B)

(2) The Boolean expression　A + A'B　is equal to. (　　)

A. A+B　　B. A　　C. A+B'　　D. A'B

(3) The OR operation can be produced with (　　)

A. two NAND gates　　B. three NOR gates

C. two NOR gate　　D. one NOR gates

(4) The waveforms of input A, B and output Y of a two-variable input logic gate are known as follows, which is the function of the logic gate. (　　)

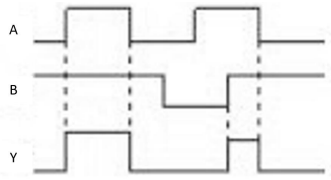


Figure 1(4)

A. AND　　B. NAND

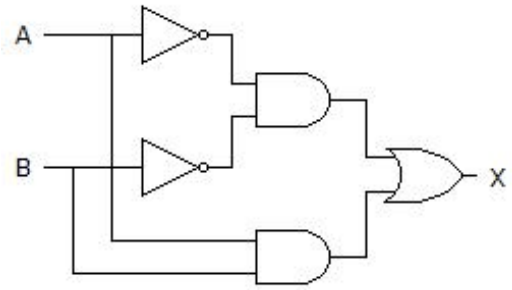
C. NOR　　D. XOR

(5) If we want to use an XNOR gate as an Inverter (NOT gate), then the two inputs of it should connect as the (　　).

A. One of the inputs should be connect to "1"　　B. Connect the inputs together

C. One of the inputs should be connect to "0"　　D. Can't realize

(6) Which of the following logic expressions represents the logic diagram shown? （ ）



A. X=AB'+A'B
B. X=(AB)'+AB
C. X=(AB)'+A'B'
D. X=A'B'+AB

Figure 1(6)

(7) The following figure is a block diagram of a seven-segment LED display with a common anode. If the character "5" is to be displayed, the output (a ～ g) of the decoder should be ( ).

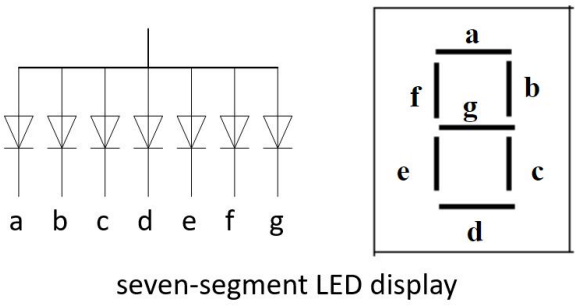


Figure 1(7)

A. 0100100 B. 1100011 C. 1011011 D. 0011011

(8) For synchronous RS flip-flops, if S=R', the logic function of the（ ）flip-flop can be completed.

A. JK B. D C. T D. None of the above

(9) Assume Q0 is LOW. The next clock pulse will cause（ ）.

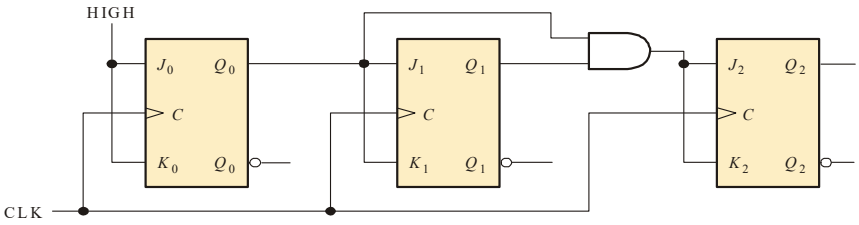


Figure 1(9)

A. FF1 and FF2 to both toggle B. FF1 and FF2 to both latch
C. FF1 to latch; FF2 to toggle D. FF1 to toggle; FF2 to latch

(10) The modulus of a counter is ( ).

A. the number of flip-flops B. the actual number of states in its sequence
C. the maximum possible number of states

D. the number of times it recycles in a second

2. Fill in the blanks with the correct answer (20 points, 2 points per blank).

(1) The 2's complement of (_____)$_{10}$ is 101101001.

(2) If a logic function F=∏M(1, 3, 7), then its inverse function F'=∑m(_____).

(3) The following waveform pattern is for a(n) _____ gate.

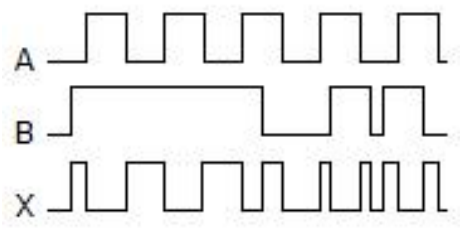


Figure 2(3)

(4) A simple decoder can detect the presence of the binary code 0011 with an active-HIGH output. Design it with the basic gates(AND, OR, NOT) only _____.

(5) An 8-bit comparator using 74LS85 is shown. If A_7~A_0=11110101 and B_7~B_0=00001010, the three output of the lowest order comparator should be $F_{A>B}$=_____, $F_{A=B}$=_____, $F_{A<B}$=_____.

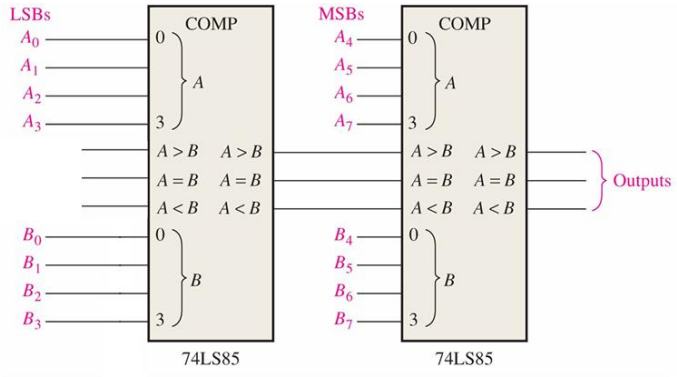


Figure 2(5)

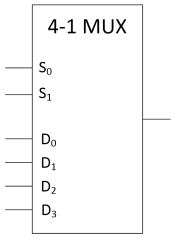


Figure 3(1)

(6) If an octal-to-binary priority encoder has its 0, 2, 5, and 6 inputs at the active level, the active HIGH binary output is _____. If more than one input is active, the one with the highest order decimal digit will be active.

(7) A 8-bit shift register can be used to delay serial data by _____clock periods.

(8) To cause a D flip-flop to toggle, connect the _____ to the D input

3. Answer the questions (40 points, 8 points per question).

(1) Please list the truth table of a 1-bit full adder, and implement it ***only using two*** 4-1 multiplexers. The 4-1 multiplexer is shown as figure 3(1).

(2) For the parallel adder in Figure 3(2), Write out the logic function of $\sum_1$ and $\sum_2$, and simplify $\sum_1$ and $\sum_2$ with Karnaugh maps. The inputs are A_1, A_0 and B_1, B_0.

(3) Please design a logic diagram to build the logic function F=CB'+ A'CD' with 3-8 binary decoder(74LS138) and some gates. (open answer)

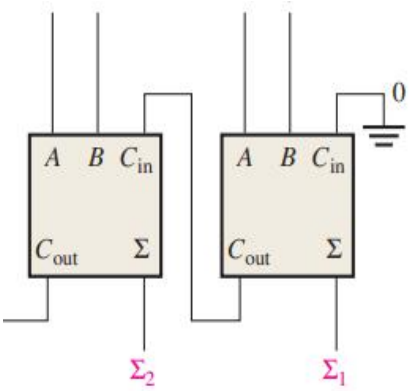


Figure 3(2)

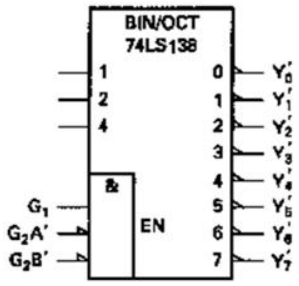


Figure 3(3)

(4) Given the logic diagram shown as Figure 3(4), draw the State Diagram.

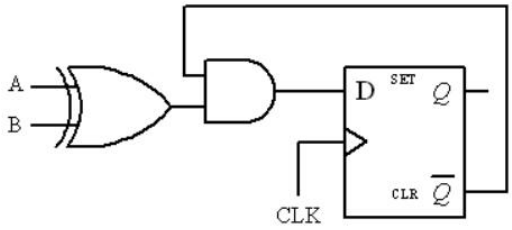
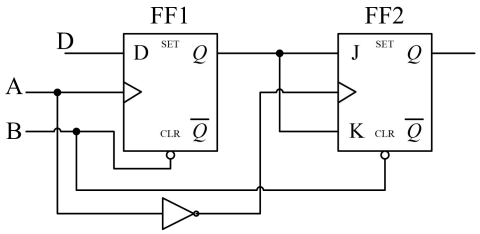


Figure 3(4)

Figure 4(2)

(5) Given the sequential circuit as Figure 3(5). Draw the output waveforms of FF1 and FF2 in proper relation to these inputs.



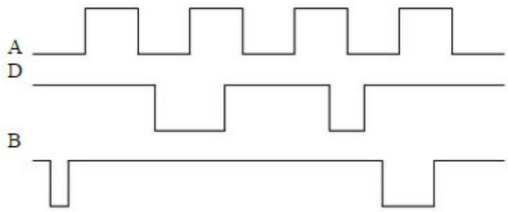


Figure 3(5)

4. Comprehensive questions(20 points, 10 points per question).

(1) Design a logic circuit to produce a HIGH output only if the input, represented by a 4-bit binary number, is greater than twelve or less than three. Give the details. (open answer)

(2) Design a logic circuit to simulate traffic lights. The green light is on for 4 seconds, then the yellow light for 2 seconds and then the red light for 4 seconds. A LOW signal can turn on the lights. Assume you can get a 1HZ clock. (open answer)