四川大学期末考试试题（2018-2019 学年第 1 学期）A 卷

参考答案与评分标准

1. Choose the best answer from the four choices. (20points)

1) In the 2's complement form, the binary number 10010101 is equal to the decimal number (d).
(a) -21 (b) -106 (c) +141 (d) -107

2) The 8421BCD number for decimal 397 is (b).
(a) 110001101 (b) 001110010111 (c) 1110010111 (d) 110001101000

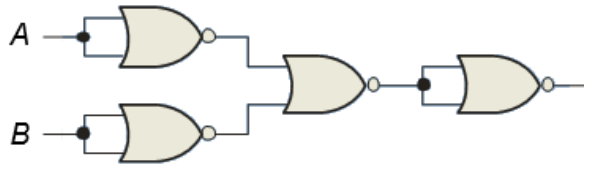
3) The same is "0", the difference is "1, what is its logical relationship? (c)
(a) AND (b) OR (c) XOR (d) XNOR

4) Apply DeMorgan's theorems to the expression $\overline{(A+\overline{\overline{B}C}+D)}+\overline{ABC\overline{D}}$. The answer is (a)

(a) $\overline{A}+\overline{B}+\overline{C}+D$ (b) $\overline{A\overline{B}C\overline{D}}$ (c) $\overline{A}+\overline{B}+C+\overline{D}$ (d) $\overline{A}\overline{B}\overline{C}D$

5) Which of the following is a standard SOP(sum-of-product) expression.(c)
(a) A(B+C)+ABC (b) (A+B)(A+C) (c) $\bar{A}B+A\bar{B}$ (d) All above.

6) The circuit shown is equivalent to (d)
(a) AND gate (b) XOR gate (c) OR gate (d) NAND gates



7) The output of JK flip-flop is set to 1 when (d)
(a) J=0, K=1 (b) J=0, K=0 (c) J=1, K=1 (d) J=1, K=0

8) In general, a multiplexer has (d)
(a) One data input, several data outputs, and select inputs
(b) One data input, one data output, and select inputs
(c) several data input, several data outputs, and select inputs
(d) several data input, one data outputs, and select inputs

9) A modulus-8 ring counter requires (c)
(a) 3 flip-flops (b) 5 flip-flops (c) 8 flip-flops (d) 12 flip-flops

10) The group of bits 11001 is serially shifted (right-most bit first) into a 5-bit parallel output shift register with an initial state 01110. After three clock pulses, the register contains (c)
(a) 01110 (b) 00001 (c) 00101 (d) 00110

2. Fill in the blanks with the correct answer. (20 points)

1) $(27.4)_8=(\underline{10111.1})_2=(\underline{17.8})_{16}=(\underline{23.5})_{10}=(\underline{00100011.0101})_{8421BCD}$

2) 与非门 and 或非门 are called universal gates.

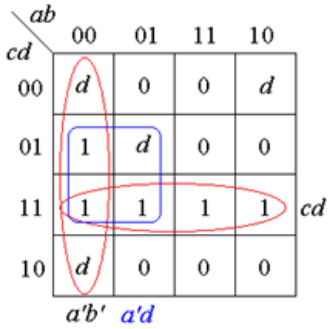
3) A circuit with 10 flip-flops can store (10) bits binary numbers, that is, include (1024) states at most.

4) A J-K flip-flop with J = 1 and K = 1 has a 10 kHZ clock input.The Q input is a 5 kHZ square wave.

5) A modulus-12 counter must have 4 flip-flops.

3. Answer the questions briefly. (30 points)

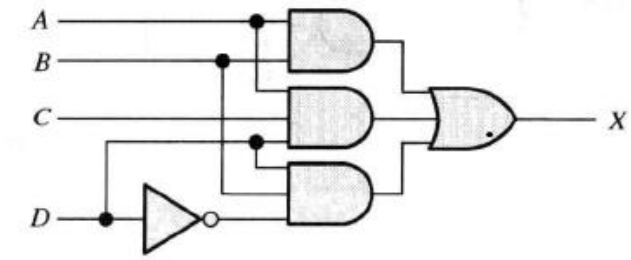
1) (6p) Optimize the functions $f(a,b,c,d) = \Sigma m(1,3,7,11,15) + \Sigma d(0,2,5,8)$ in a minimum sum-of-products expression using a Karnaugh map.

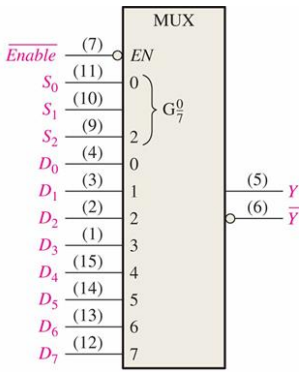


（卡诺图正确4分；逻辑表达式正确2分）

$f(a,b,c,d)= a'd+cd$ 或 $a'b'+cd$

2) (8p) Write the equivalent form of the following circuit, and implement it by a 8-to-1 MUX. Suggest using ABC as $S_2S_1S_0$.





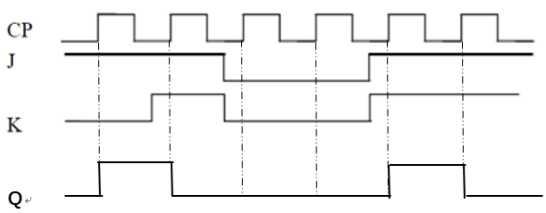
解：

1）读图正确得到布尔表达式：AB+ACD（2 分）

2）建议用 ABC 作为选择信号，找出输出和 D 之间的关系（4 分：D0-D4 接低电平，D5 接 D，D6，D7 接高电平）；在图中正确标出变量并有效使能信号（2 分）。

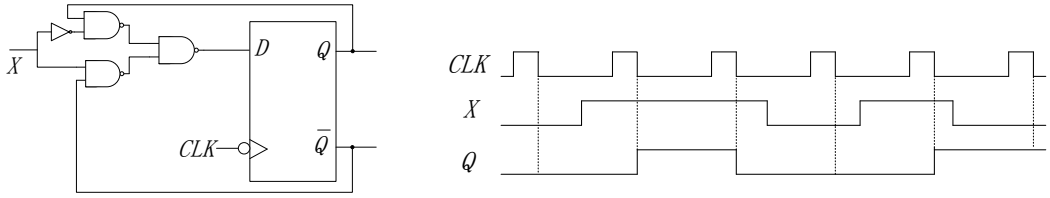
* 随意 3 个变量作为选择信号，找出输出和余下一个变量之间的关系。得分参照 2）

3) (6p) Assuming a rising edge triggered J-K flip-flop as input, the output associated with the clock is determined, and try to draw the working waveform of the Q terminal of the trigger. Suppose Q starts at low level.



各时钟周期的状态正确得 1 分。

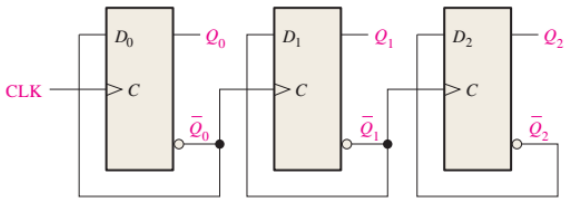
4) (5p)Given the logic diagram for this problem, complete the partial timing diagram (assume the initial state is Q = 0).

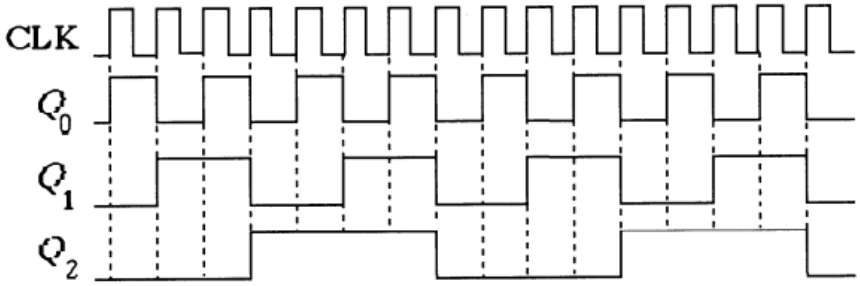


写出方程 2 分，画出波形图 3 分 (注意是下降沿触发)。

$Q^{n+1} = \mathrm{D} = \overline{\overline{X}Q^n \cdot X\overline{Q^n}} = \bar{X}Q^n + X\overline{Q^n} = X \oplus Q^n$

5) (5p) For the ripple counter, show the complete timing diagram for **SIXTEEN** clock pulses. Show the clock, *Q*0, *Q*1, and *Q*2 waveforms. Assume that *Q*0*Q*1*Q*2 are initially LOW.

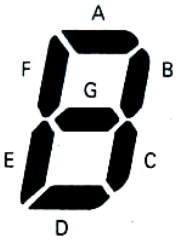


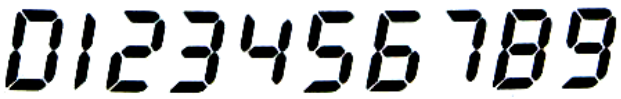


4. Complete the Designs. (30 points)

1) (10p) Design a combinational circuit that will accept 4-bit EX-3 code and drive a 7-segment display. The segments are turned on with a LOW (0) logic level and turned off with a HIGH (1) logic level.

Decimal	EX-3
0	0011
1	0100
2	0101
3	0110
4	0111
5	1000
6	1001
7	1010
8	1011
9	1100





解：真值表正确 3 分，表达式正确 3 分，逻辑图实现 4 分。

余3码	最小-最大项	输入				输出						
十进制	下标	w	x	y	z	A	B	C	D	E	F	G
0	3	0	0	1	1	0	0	0	0	0	0	1
1	4	0	1	0	0	1	0	0	1	1	1	1
2	5	0	1	0	1	0	0	1	0	0	1	0
3	6	0	1	1	0	0	0	0	0	1	1	0
4	7	0	1	1	1	1	0	0	1	1	0	0
5	8	1	0	0	0	0	1	0	0	1	0	0
6	9	1	0	0	1	0	1	0	0	0	0	0
7	10	1	0	1	0	0	0	0	1	1	1	1
8	11	1	0	1	1	0	0	0	0	0	0	0
9	12	1	1	0	0	0	0	0	0	1	0	0

$$A = \sum m(4,7) + \sum d(0,1,2) = w'y'z' + w'xyz$$

$$B = \sum m(8,9) + \sum d(0,1,2) = x'y'$$

$$C = m5 + \sum d(0,1,2) = w'y'z$$

则可得到 $D = \sum m(4,7,10) + \sum d(0,1,2) = w'y'z' + w'xyz + x'yz'$

$$E = \sum m(4,6,7,8,10,12) + \sum d(0,1,2) = y'z' + w'xy + x'z'$$

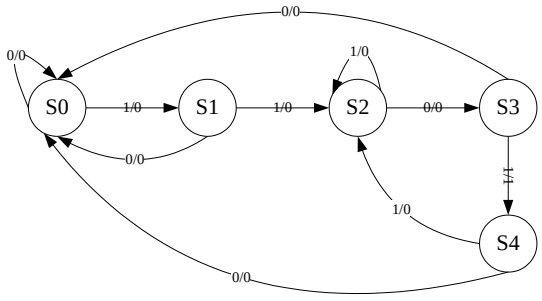
$$F = \sum m(4,5,6,10) + \sum d(0,1,2) = w'y' + w'z' + x'yz'$$

$$G = \sum m(3,4,10) + \sum d(0,1,2) = w'x' + w'y'z' + x'yz'$$

最后一步无标准答案，可通过卡诺图化简后完成逻辑图，亦可通过译码器、数字多路器等直接设计完成。

2) (10p) Design a modulus-7 binary counter. (open answer)

3) (10p) Create a state diagram for a sequence detector that outputs a 1 when it detects the final bit in the serial data stream 1101(the sequence can be overlapped).



（各状态的输入输出正确各给2分）