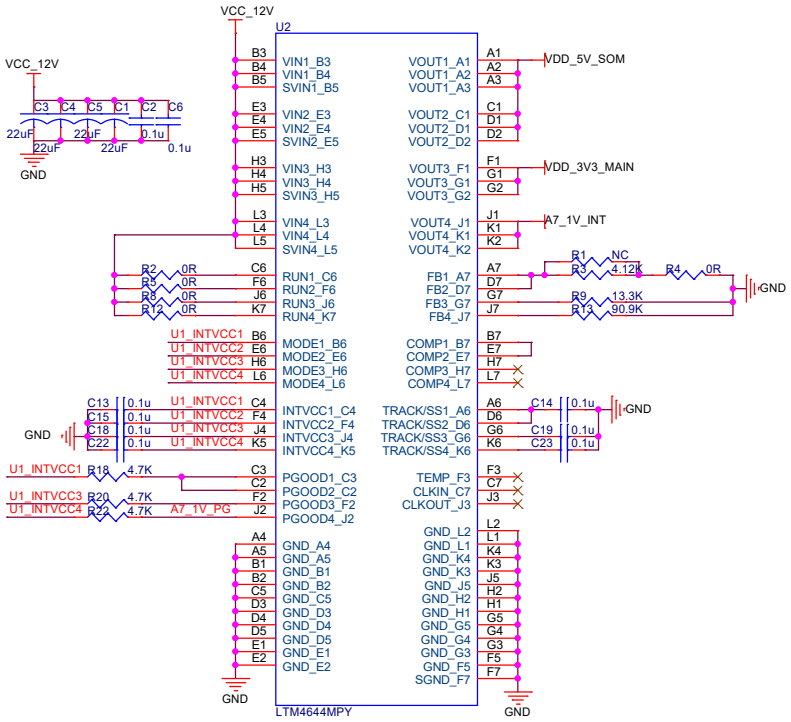
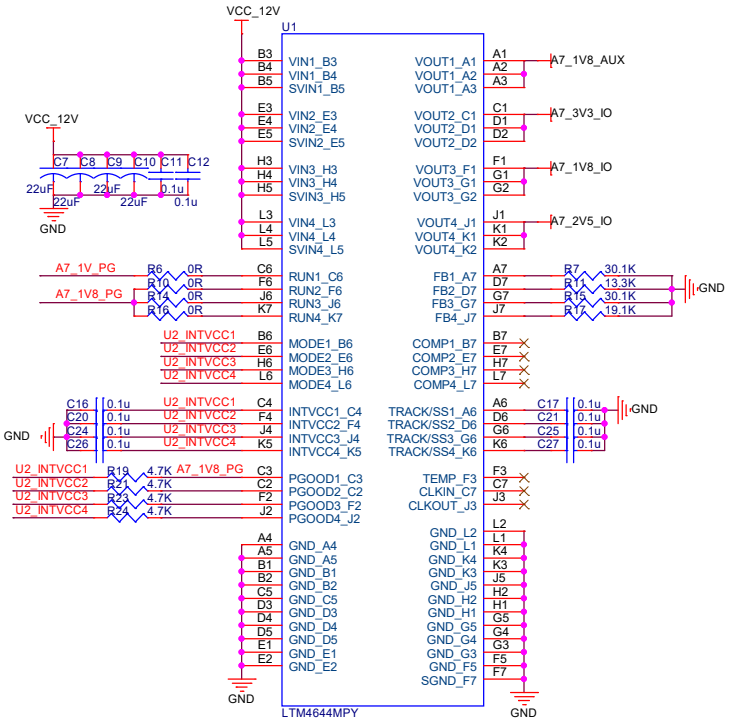
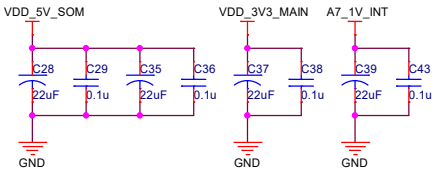
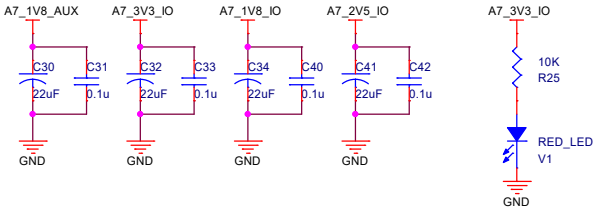




0.6	OPEN
1.0	90.9K
1.2	60.4k
1.5	40.2k
1.8	30.1k
2.5	19.1k
3.3	13.3k
5	8.25k





Title	<Title>		
Size A3	Document Number <Doc>		Rev <RevCode>
Date: Wednesday, September 25, 2024	Sheet 1 of 13		

SOM_CONNECTOR_A/B

L7/FEL	BOOT DEVICE
1	Micro SD-> SPI NOR -> eMMC -> NAND 已内部上拉
0	USB0

CON1A

V1/TVOUT0 V2/TVOUT1 V3/TVOUT2 V4/TVOUT3 W2/TVIN0 Y1/TVIN1 Y2/TVIN2 W3/TVIN3 AGND_TVIN V6/PHONEOUTP V5/PHONEOUTN AGND_AUDIO AA6/TPX1 AB4/TPY2 AB5/TPY1 AB6/TPX2

AD10/PC2/NCLE/SPI0_CLK/1V8 AC10/PC1/NALE/SPI0_MISO/1V8 AB11/PC0/NWEn/SPI0_MOSI/1V8 AB17/PC23/SPI0_CS0/1V8

A2	V1/TVOUT0	A1	AA1/HPOUTR
A4	V2/TVOUT1	A3	AA2/HPOUTL
A6	V3/TVOUT2	A5	W4/HPCOMFB
A8	V4/TVOUT3	A7	Y3/HPCOM
A10	W2/TVIN0	A9	AA3/LINEINL
A12	Y1/TVIN1	A11	AB2/LINEINR
A14	Y2/TVIN2	A13	AB3/MICIN1
A16	W3/TVIN3	A15	AD2/MICIN2
A18	AGND_TVIN	A17	AC3/VMIC
A20	V6/PHONEOUTP	A19	AGND_AUDIO
A22	V5/PHONEOUTN	A21	AA4/KEYADC1
A24	AGND_AUDIO	A23	AD3/KEYADC0
A26	AA6/TPX1	A25	GND
A28	AB4/TPY2	A27	AA10/USB2_DM
A30	AB5/TPY1	A29	AB10/USB2_DP
A32	AB6/TPX2	A31	GND
A34	AB6/TPX2	A33	AC8/USB0_DM
A36	GND	A35	AD8/USB0_DP
A38	AD10/PC2/NCLE/SPI0_CLK/1V8	A37	GND
A40	AC10/PC1/NALE/SPI0_MISO/1V8	A39	AC9/USB1_DM
A42	AB11/PC0/NWEn/SPI0_MOSI/1V8	A41	AD9/USB1_DP
A44	AB17/PC23/SPI0_CS0/1V8	A43	GND
A46	GND	A45	Y11/PF1/SDC0_D0/JTAG_DI1/3V3
A48	L7/FEL/3V3	A47	AA11/PF0/SDC0_D1/JTAG_MS1/3V3
A50	C20/AP-NMIn/PU/3V3	A49	W11/PF2/SDC0_CLK/UART0_TX/3V3
A52	R24/AP-RESETn/3V	A51	W13/PF5/SDC0_D2/JTAG_CK1/3V3
A54	PMIC_PWRON	A53	Y13/PF4/SDC0_D3/UART0_RX/3V3
A56	GND	A55	AA13/PF3/SDC0_CMD/JTAG_DO1/3V3
A58	GND	A57	GND
A60	GND	A59	GND
A62	NC1	A61	NC2
A64	VDD_5V_SOM	A63	VDD_5V_SOM
A66	VDD_5V_SOM	A65	VDD_5V_SOM
A68	VDD_5V_SOM	A67	VDD_5V_SOM
A70	VDD_5V_SOM	A69	VDD_5V_SOM

SOM-TLT3_A40i

H1

AA1/HPOUTR AA2/HPOUTL W4/HPCOMFB Y3/HPCOM AA3/LINEINL AB2/LINEINR AB3/MICIN1 AD2/MICIN2 AC3/VMIC AGND_AUDIO AA4/KEYADC1 AD3/KEYADC0

AA10/USB2_DM AB10/USB2_DP AC8/USB0_DM AD8/USB0_DP AC9/USB1_DM AD9/USB1_DP

USB2.0
Max Date Rate:480Mbps
Layout:90Ω Differential impendance

Y11/PF1/SDC0_D0/JTAG_DI1/3V3 <7>
AA11/PF0/SDC0_D1/JTAG_MS1/3V3 <7>
W11/PF2/SDC0_CLK/UART0_TX/3V3 <7>
W13/PF5/SDC0_D2/JTAG_CK1/3V3 <7>
Y13/PF4/SDC0_D3/UART0_RX/3V3 <7>
AA13/PF3/SDC0_CMD/JTAG_DO1/3V3 <7>

TF Card

R26 0R/NC — L7/FEL/PU/3V3
C20/AP-NMIn/PU/3V3
R24/AP-RESETn/3V
PMIC_PWRON
BTN SW1

VDD_5V_SOM
C44 0.1u C45 0.1u C46 0.1u CP1 100uF

VDD_3V3_MAIN R27 10K
<8,9> SYS_RESETn/3V3 — R24/AP-RESETn/3V
SW2 BTN

D1 TPS3808G33DBVR
RESETn VDD GND SENSE MRn CT
C47 0.1u C48 10nF

<13> MCU_U1_TX — R28 NC — R23/PI21/PS2_SDA0/UART7_RX/HSDA/PWM3/3V3 <2>
<13> MCU_U1_RX — R29 NC — T21/PI20/PS2_SCK0/UART7_TX/HSCL/PWM2/3V3 <2>

CON1B

J4/MIPI_DSI_D2N J3/MIPI_DSI_D2P K4/MIPI_DSI_D3N K3/MIPI_DSI_D3P J2/MIPI_DSI_D0N J1/MIPI_DSI_D0P K2/MIPI_DSI_D1N K1/MIPI_DSI_D1P L2/MIPI_DSI_CKN L1/MIPI_DSI_CKP

MIPI DSI
Max Date Rate:1Gbps
Layout:100Ω Differential impendance

M1/PD1/LCD0_D1/LVDS0_VN0/3V3 M2/PD0/LCD0_D0/LVDS0_VP0/3V3 M3/PD3/LCD0_D3/LVDS0_VN1/3V3 N2/PD2/LCD0_D2/LVDS0_VP1/3V3 P2/PD5/LCD0_D5/LVDS0_VN2/3V3 P1/PD4/LCD0_D4/LVDS0_VP2/3V3 P3/PD7/LCD0_D7/LVDS0_VNC/3V3 R1/PD6/LCD0_D6/LVDS0_VPC/3V3 R3/PD9/LCD0_D9/LVDS0_VN3/3V3 R2/PD8/LCD0_D8/LVDS0_VP3/3V3

LVDS0
Max Clock Rate:75MHz
Layout:100Ω Differential impendance

T2/PD20/LCD0_D20/CSI1_MCLK/3V3
<9> T3/PD23/LCD0_D23/SMC_DET/3V3
U1/PD21/LCD0_D21/SMC_VPPEN/3V3
U2/PD22/LCD0_D22/SMC_VPPPP/3V3
T4/PD24/LCD0_CLK/SMC_VCCEN/3V3

B2	J4/MIPI_DSI_D2N	B1	V21/PI13/SPI0_MISO/UART6_RX/CLK_OUT_B/EINT25/3V3
B4	J3/MIPI_DSI_D2P	B3	U18/PI12/SPI0_MOSI/UART6_TX/CLK_OUT_A/EINT24/3V3
B6	GND	B5	V23/PI10/SPI0_CS0/UART5_TX/EINT22/3V3
B8	K4/MIPI_DSI_D3N	B7	V24/PI11/SPI0_CLK/UART5_RX/EINT23/3V3
B10	K3/MIPI_DSI_D3P	B9	U22/PI15/SPI1_CS1/PS2_SDA1/TCLKIN1/EINT27/3V3
B12	GND	B11	U23/PI14/SPI0_CS1/PS2_SCK1/TCLKIN0/EINT26/3V3
B14	J2/MIPI_DSI_D0N	B13	T19/PI16/SPI1_CS0/UART2_RTS/EINT28/3V3
B16	J1/MIPI_DSI_D0P	B15	T22/PI19/SPI1_MISO/UART2_RX/EINT31/3V3
B18	GND	B17	T24/PI18/SPI1_MOSI/UART2_TX/EINT30/3V3
B20	K2/MIPI_DSI_D1N	B19	T23/PI17/SPI1_CLK/UART2_CTS/EINT29/3V3
B22	K1/MIPI_DSI_D1P	B21	T21/PI20/PS2_SCK0/UART7_TX/HSCL/PWM2/3V3
B24	GND	B23	R23/PI21/PS2_SDA0/UART7_RX/HSDA/PWM3/3V3
B26	L2/MIPI_DSI_CKN	B25	R21/PA16/ECOL/CAN_TX/UART1_DCD/GCLKIN/ECOL/I2S1_DO/3V3
B28	L1/MIPI_DSI_CKP	B27	R20/PA17/ETH1_RESETn/3V3 <8>
B30	GND	B29	N19/PA12/EMDIO/UART6_TX/UART1_RTS/GMDIO/3V3 <8>
B32	M1/PD1/LCD0_D1/LVDS0_VN0/3V3	B31	GND
B34	M2/PD0/LCD0_D0/LVDS0_VP0/3V3	B33	GND
B36	GND	B35	L4/PD11/LCD0_D11/LVDS1_VN0/3V3
B38	M3/PD3/LCD0_D3/LVDS0_VN1/3V3	B37	L5/PD10/LCD0_D10/LVDS1_VP0/3V3
B40	N2/PD2/LCD0_D2/LVDS0_VP1/3V3	B39	GND
B42	GND	B41	M4/PD13/LCD0_D13/LVDS1_VN1/3V3
B44	P2/PD5/LCD0_D5/LVDS0_VN2/3V3	B43	L3/PD12/LCD0_D12/LVDS1_VP1/3V3
B46	P1/PD4/LCD0_D4/LVDS0_VP2/3V3	B45	GND
B48	GND	B47	N4/PD15/LCD0_D15/LVDS1_VN2/3V3
B50	P3/PD7/LCD0_D7/LVDS0_VNC/3V3	B49	N3/PD14/LCD0_D14/LVDS1_VP2/3V3
B52	R1/PD6/LCD0_D6/LVDS0_VPC/3V3	B51	GND
B54	GND	B53	P4/PD17/LCD0_D17/LVDS1_VNC/3V3
B56	R3/PD9/LCD0_D9/LVDS0_VN3/3V3	B55	P5/PD16/LCD0_D16/LVDS1_VPC/3V3
B58	R2/PD8/LCD0_D8/LVDS0_VP3/3V3	B57	GND
B60	GND	B59	R4/PD19/LCD0_D19/LVDS1_VN3/3V3
B62	T2/PD20/LCD0_D20/CSI1_MCLK/3V3	B61	R5/PD18/LCD0_D18/LVDS1_VP3/3V3
B64	T3/PD23/LCD0_D23/SMC_DET/3V3	B63	GND
B66	U1/PD21/LCD0_D21/SMC_VPPEN/3V3	B65	T5/PD25/LCD0_DE/SMC_RST/3V3
B68	U2/PD22/LCD0_D22/SMC_VPPPP/3V3	B67	U5/PD26/LCD0_HSYNC/SMC_SLK/3V3
B70	T4/PD24/LCD0_CLK/SMC_VCCEN/3V3	B69	U6/PD27/LCD0_VSYNC/SMC_SDA/3V3

SOM-TLT3_A40i

H2

V21/PI13/SPI0_MISO/UART6_RX/CLK_OUT_B/EINT25/3V3 <5>
U18/PI12/SPI0_MOSI/UART6_TX/CLK_OUT_A/EINT24/3V3 <5>
V23/PI10/SPI0_CS0/UART5_TX/EINT22/3V3 <5>
V24/PI11/SPI0_CLK/UART5_RX/EINT23/3V3 <5>
U22/PI15/SPI1_CS1/PS2_SDA1/TCLKIN1/EINT27/3V3 <5>
U23/PI14/SPI0_CS1/PS2_SCK1/TCLKIN0/EINT26/3V3 <5>
T19/PI16/SPI1_CS0/UART2_RTS/EINT28/3V3
T22/PI19/SPI1_MISO/UART2_RX/EINT31/3V3
T24/PI18/SPI1_MOSI/UART2_TX/EINT30/3V3
T23/PI17/SPI1_CLK/UART2_CTS/EINT29/3V3
T21/PI20/PS2_SCK0/UART7_TX/HSCL/PWM2/3V3 <2>
R23/PI21/PS2_SDA0/UART7_RX/HSDA/PWM3/3V3 <2>
R21/PA16/ECOL/CAN_TX/UART1_DCD/GCLKIN/ECOL/I2S1_DO/3V3
R20/PA17/ETH1_RESETn/3V3 <8>
N19/PA12/EMDIO/UART6_TX/UART1_RTS/GMDIO/3V3 <8>

ETH1 1000M

L4/PD11/LCD0_D11/LVDS1_VN0/3V3 L5/PD10/LCD0_D10/LVDS1_VP0/3V3 M4/PD13/LCD0_D13/LVDS1_VN1/3V3 L3/PD12/LCD0_D12/LVDS1_VP1/3V3 N4/PD15/LCD0_D15/LVDS1_VN2/3V3 N3/PD14/LCD0_D14/LVDS1_VP2/3V3 P4/PD17/LCD0_D17/LVDS1_VNC/3V3 P5/PD16/LCD0_D16/LVDS1_VPC/3V3 R4/PD19/LCD0_D19/LVDS1_VN3/3V3 R5/PD18/LCD0_D18/LVDS1_VP3/3V3

LVDS0
Max Clock Rate:75MHz
Layout:100Ω Differential impendance

T5/PD25/LCD0_DE/SMC_RST/3V3 U5/PD26/LCD0_HSYNC/SMC_SLK/3V3 U6/PD27/LCD0_VSYNC/SMC_SDA/3V3

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Size A3	Document Number <Doc>		Rev <RevCode>
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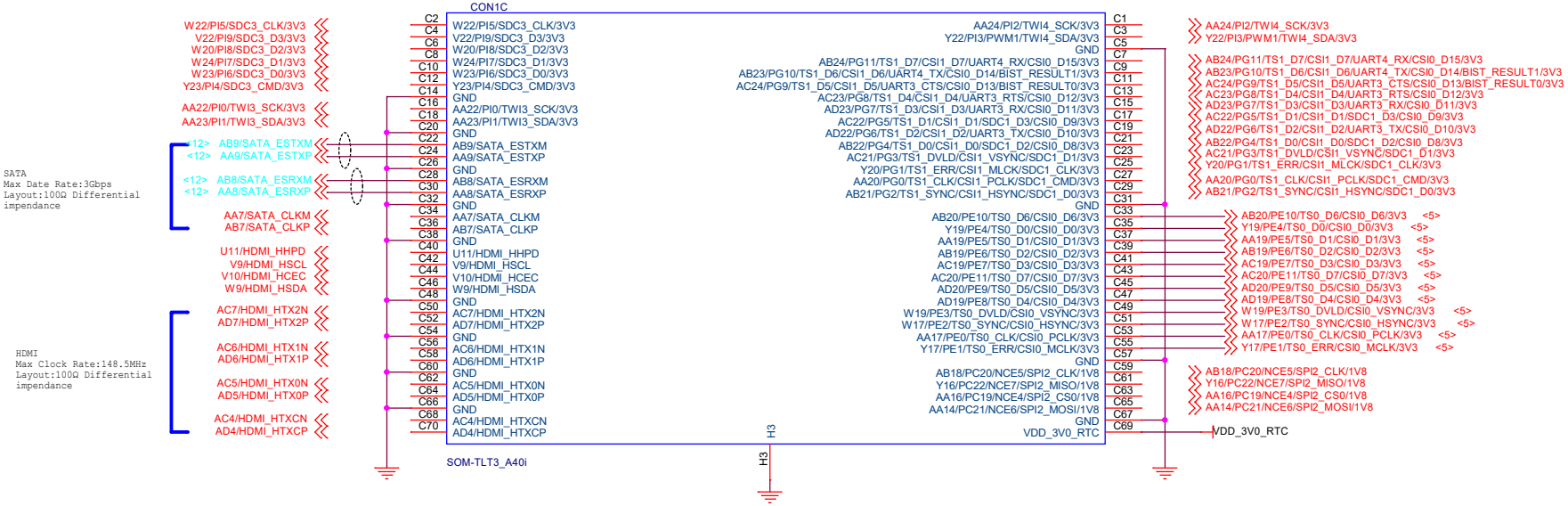
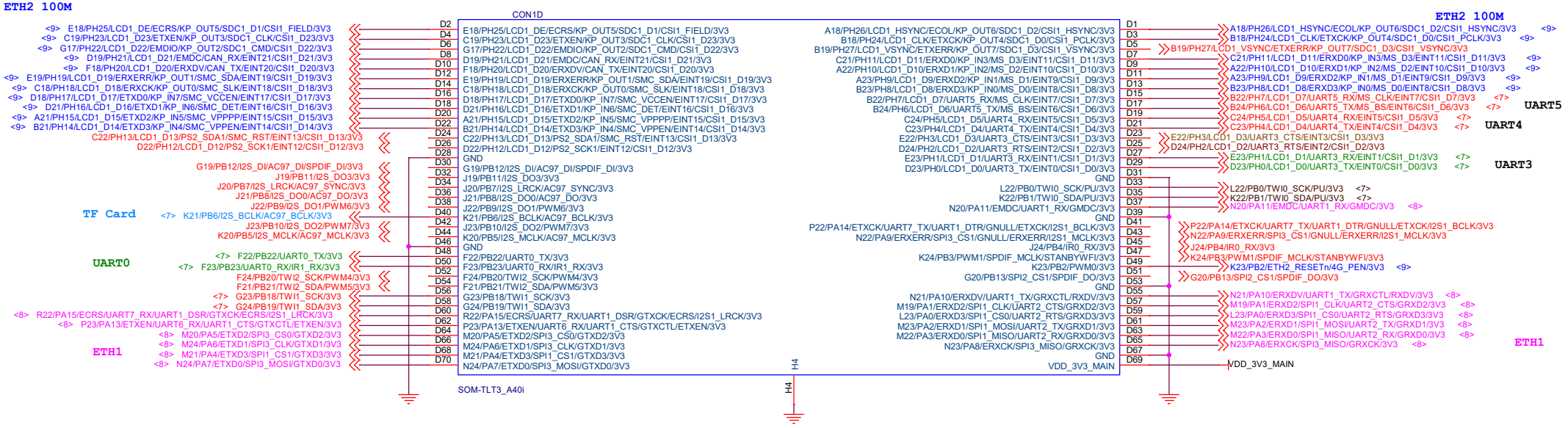
SOM_CONNECTOR_C/D



ETH2 100M



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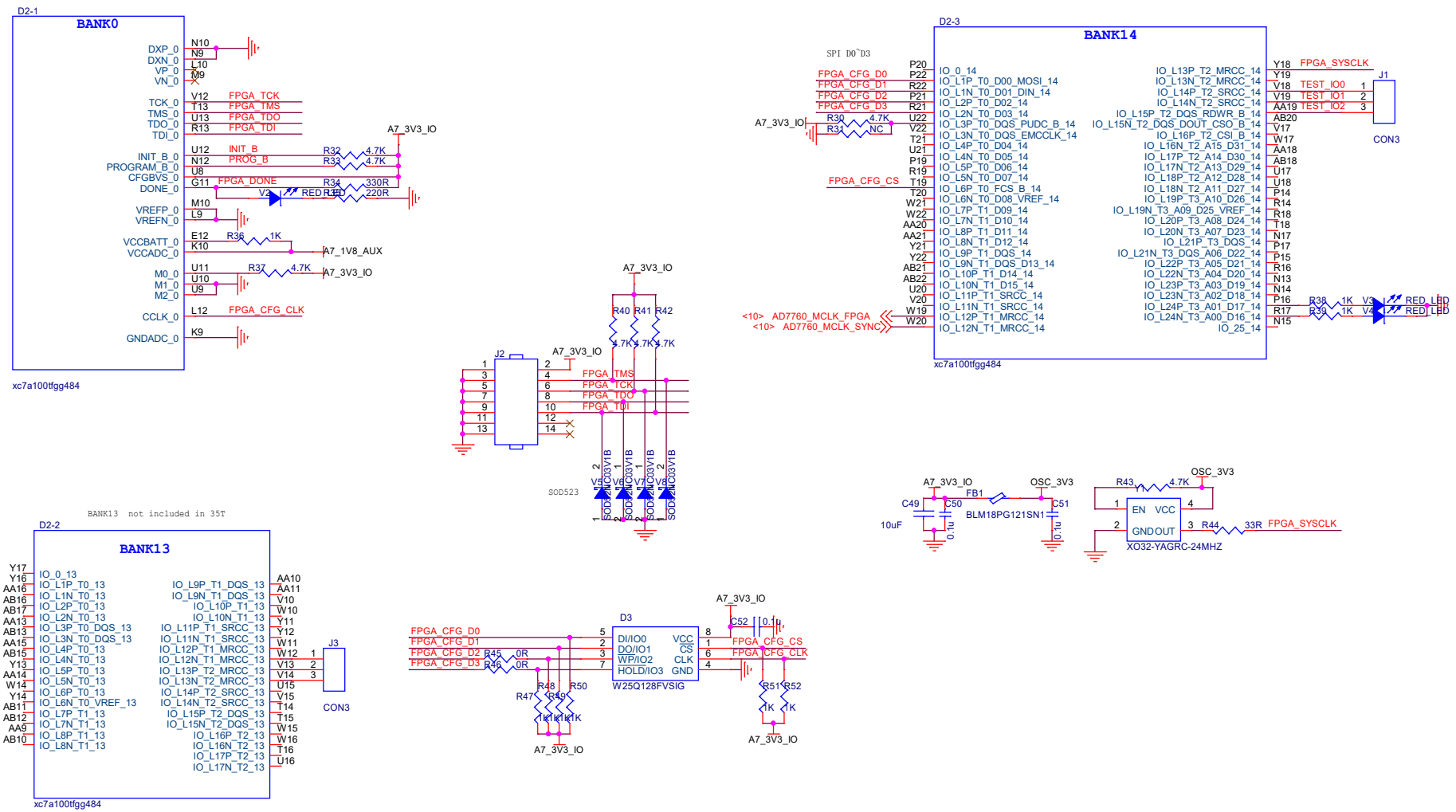
Size A3	Document Number <Doc>		Rev <RevCode>
Date: Friday, September 20, 2024	Sheet 3	of 13	



Designed by 715

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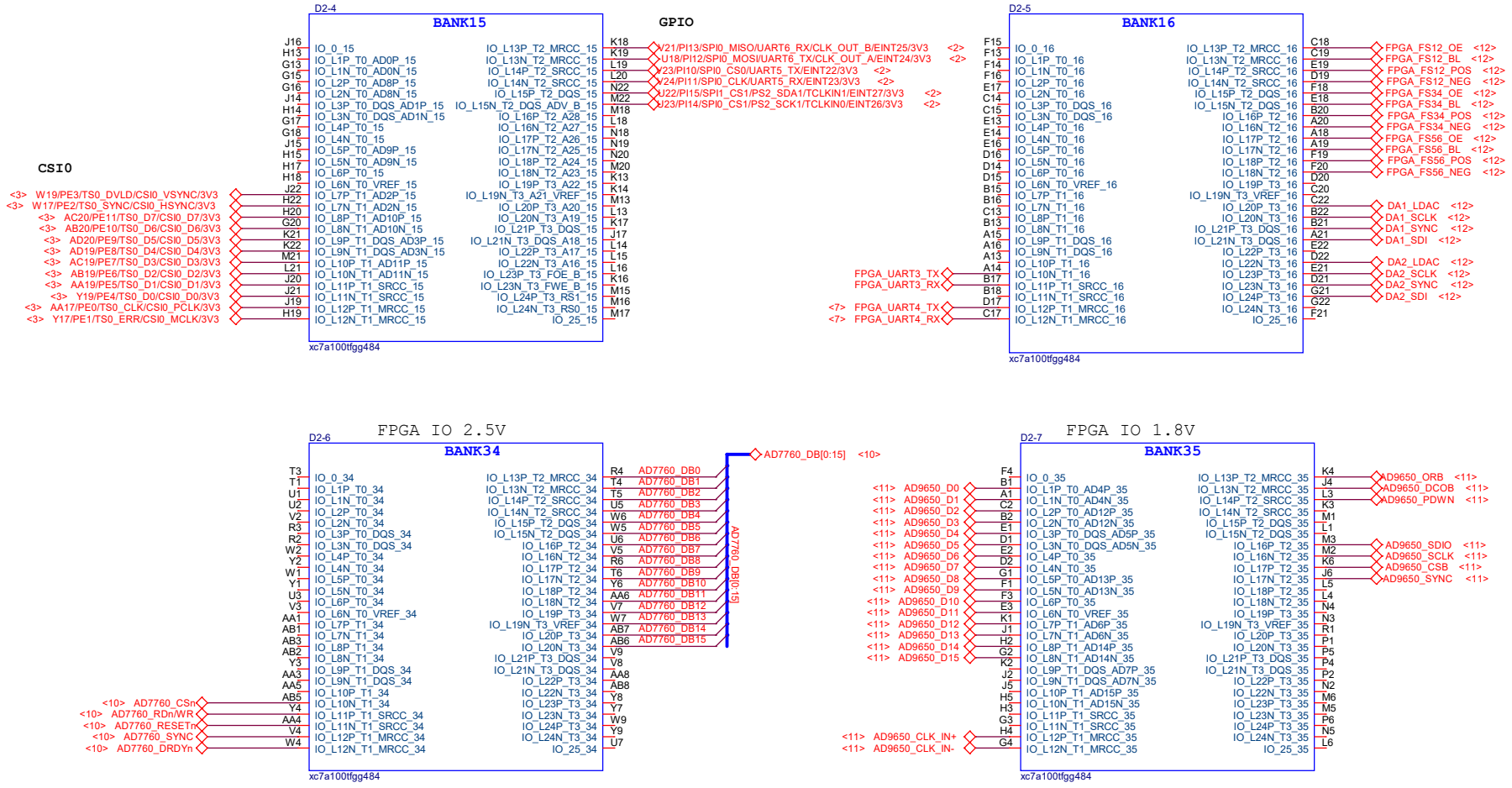
Date: Monday, September 23, 2024	Sheet 4 of 13		



Designed by 715

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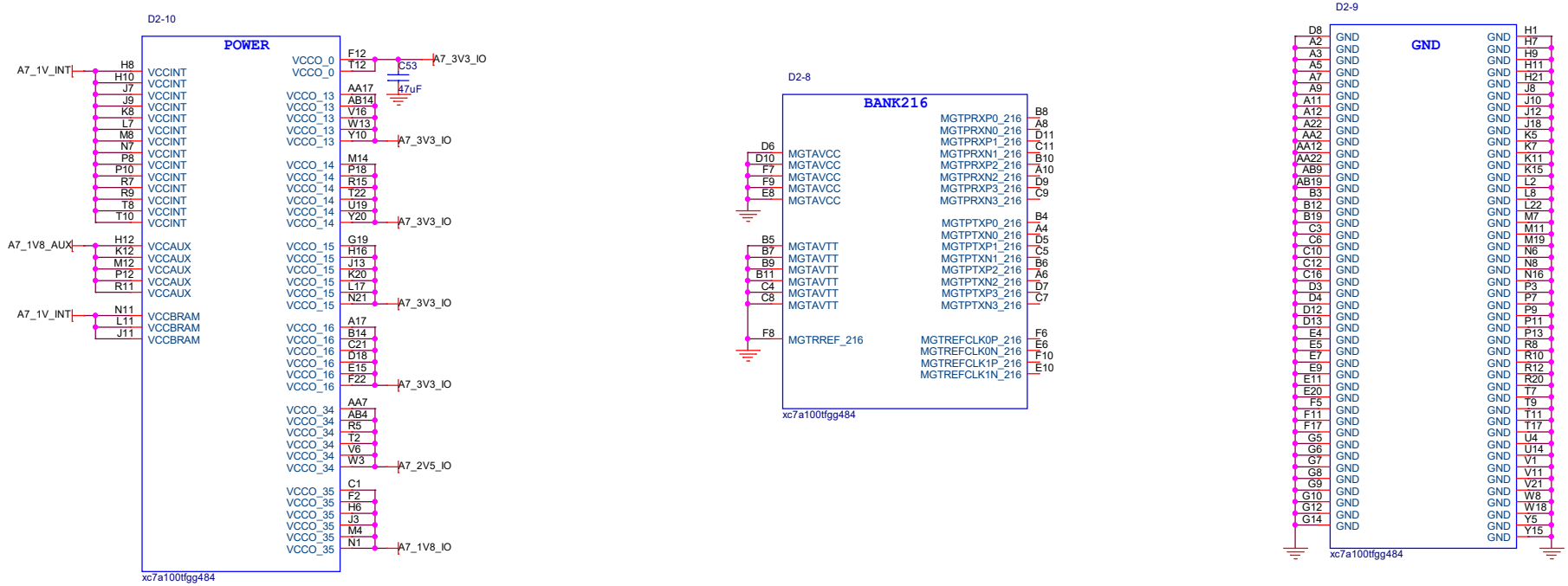
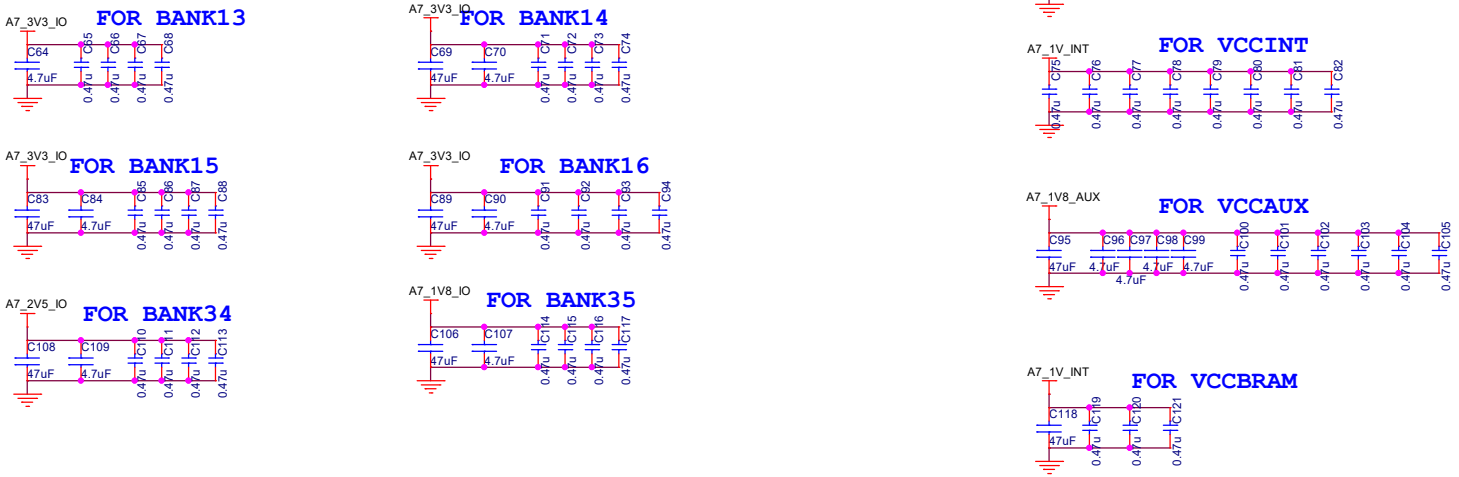
Date: Friday, September 20, 2024	Sheet 5 of 13		





Designed by 715			
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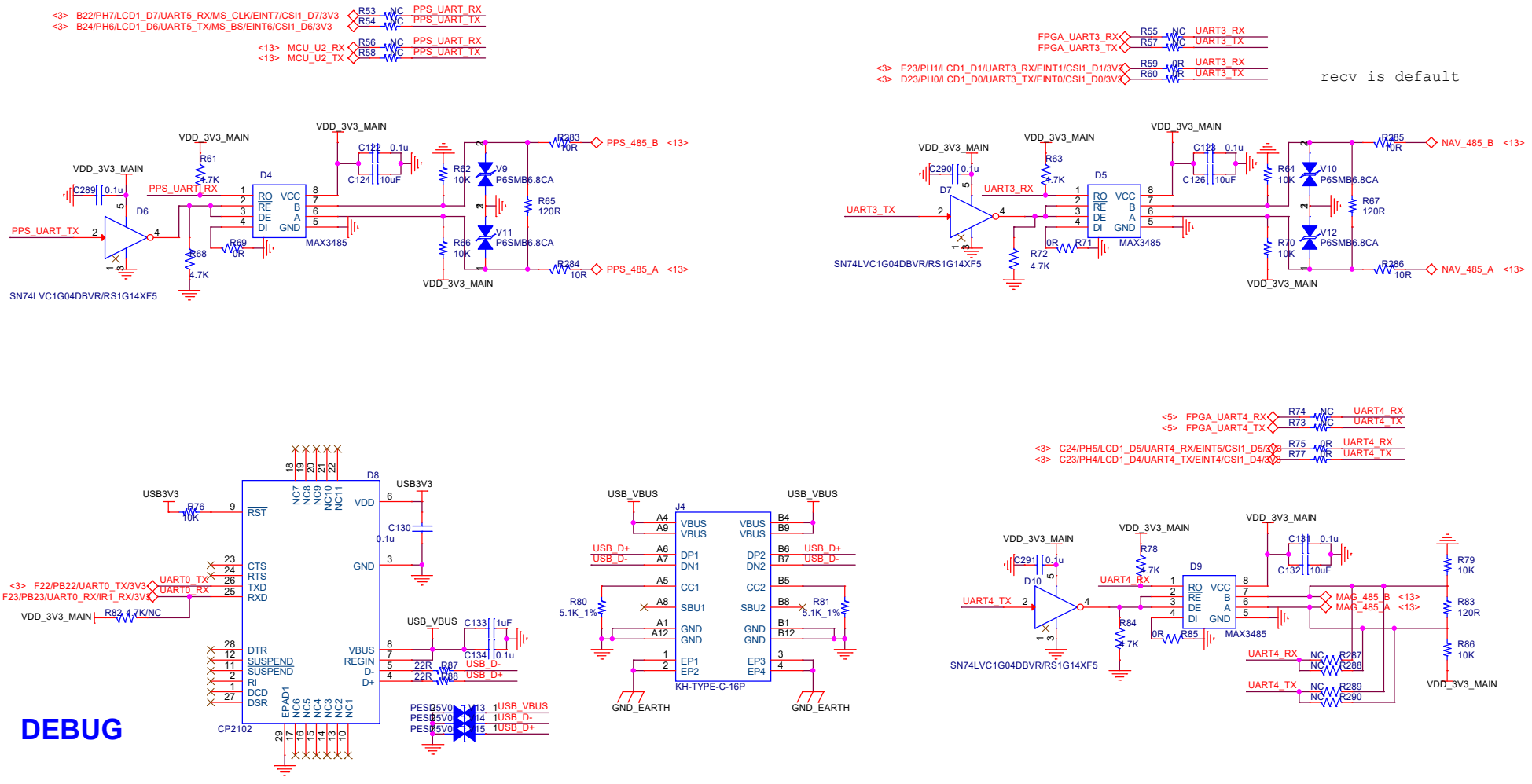
Date: Wednesday, September 25, 2024	Sheet 6 of 13		


recv is default
DEBUG
TF
RTC
SN74LVC1G04DBVR/RS1G14XF5
MAX3485
CP2102
KH-TYPE-C-16P
DS3232
TWI0 bus have been pulled up in the SOM
Title
<Title>
Size A3
Document Number
<Doc>
Rev
<RevCode>
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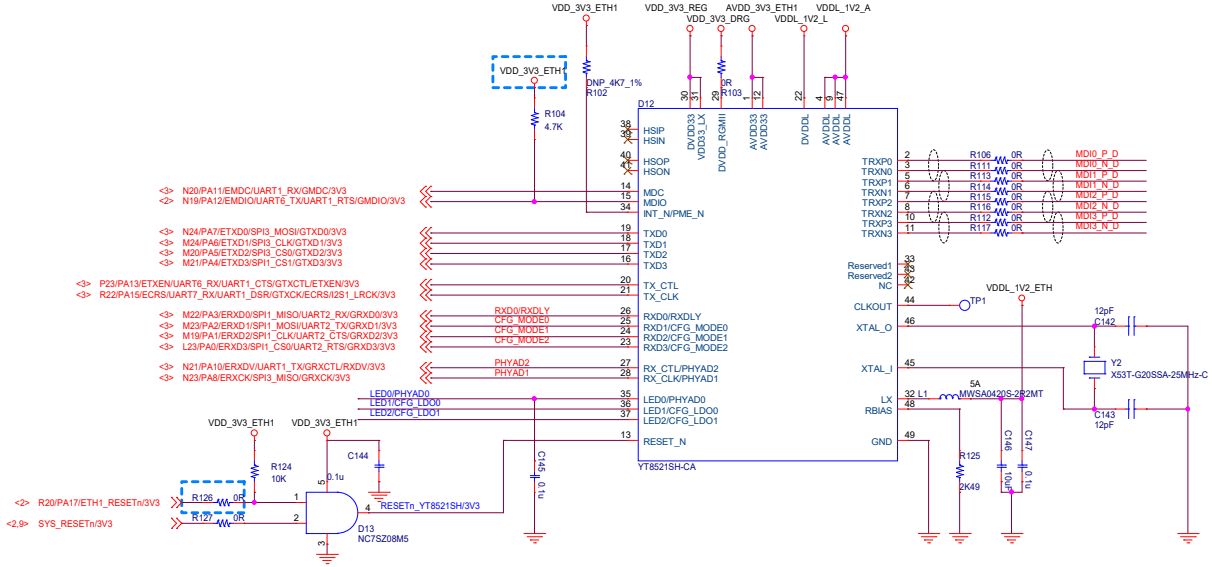
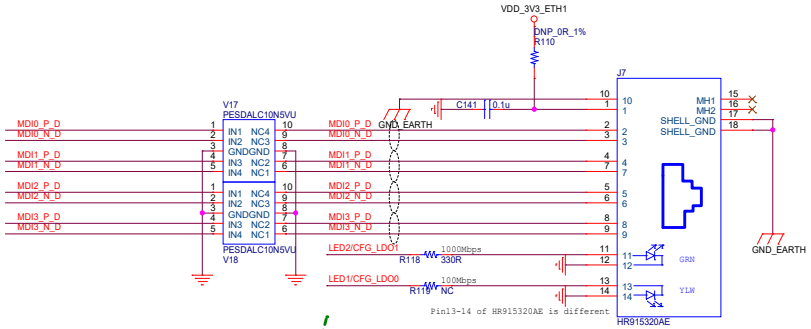
ETH1 (RGMII,10/100/1000Mbps)



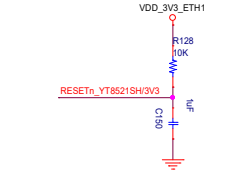


NOTE：

1. DVDD_RGMII（1.8V/2.5V/3.3V) Voltage Level: RGMII I/O（TXD3、TXD2、TXD1、TXD0、TX_CTL、TX_CLK、RXD3/CFG_MODE2、RXD2/CFG_MODE1、 RXD1/CFG_MODE0、RXD0/RXDLY、RX_CTL/PHYAD2、RX_CLK/PHYAD1）,MDC、MDIO
2. 3.3V Voltage Level: LED0/PHYAD0、LED1/CFG_LDO0、LED2/CFG_LDO1、RESET_N

LED Configuration

LED0~LED2 External Pull-up OR Pull-down	LEDx IO Output	LEDx Design
pull-up	active low	LEDx IO connected to the cathode of the LED
pull-down	active high	LEDx IO connected to the anode of the LED

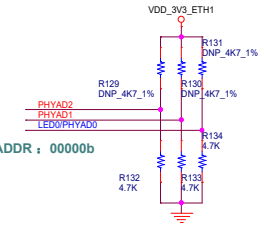


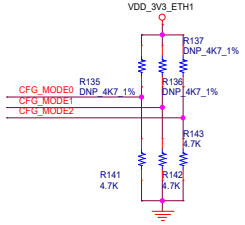
CFG_MODE[2:0]	Operation Mode
3'b000	UTP <=> RGMII
3'b001	FIBER <=> RGMII
3'b010	UTP/FIBER <=> RGMII
3'b011	UTP <=> SGMII
3'b100	SGMII (PHY) <=> RGMII
3'b101	SGMII (MAC) <=> RGMII
3'b110	UTP <=> FIBER (AUTO)
3'b111	UTP <=> FIBER (FORCE)

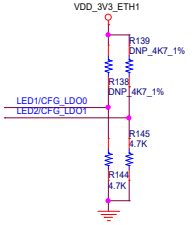
CFG_LDO[1:0]	RGMII Voltage Selection
2'b00	External 3.3V
2'b01	Internal 2.5V
2'b10	Internal 1.8V
2'b11	Not Available

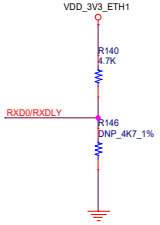
35	LED0	O/LI/PU	Light = Link up at 10Mbps Blinking = Transiting or Receiving
36	LED1	O/LI/PU	Light = Link up at 100Mbps Blinking = Transiting or Receiving
37	LED2	O/LI/PD	Light = Link up at 1000Mbps Blinking = Transiting or Receiving

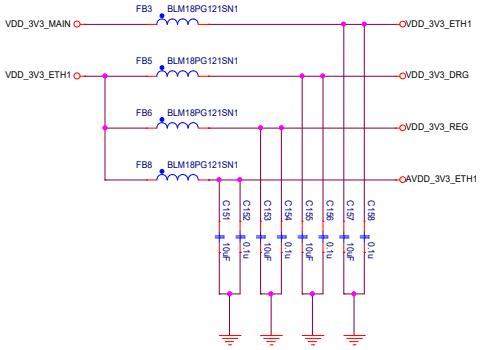
PHY ADDR ： 00000b

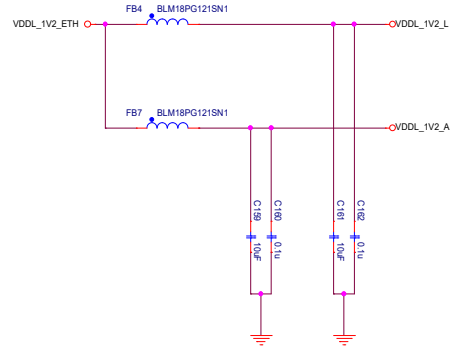












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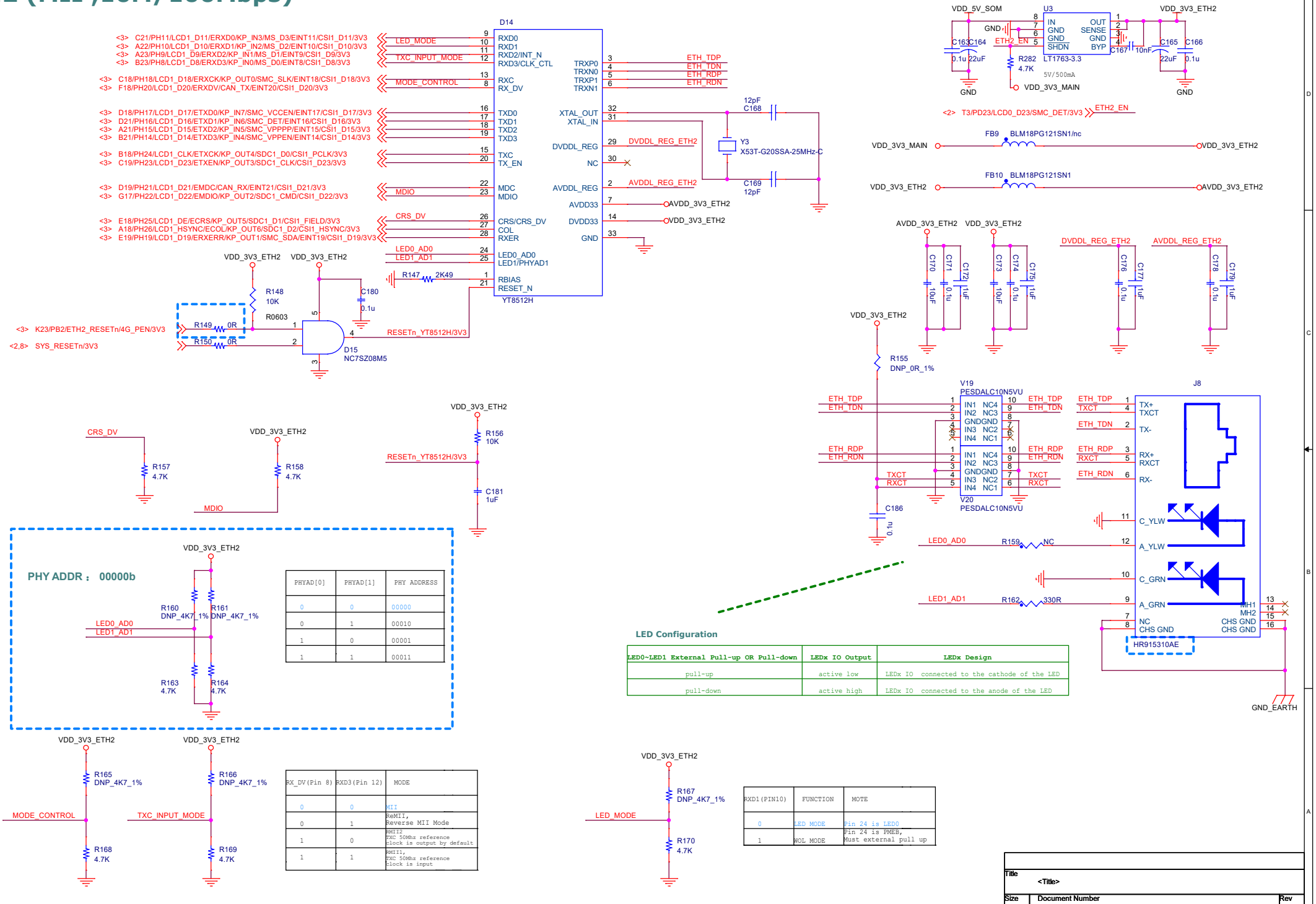
ETH2 (MII ,10M/100Mbps)



LED Configuration

LED0~LED1 External Pull-up OR Pull-down	LEDx IO Output	LEDx Design
pull-up	active low	LEDx IO connected to the cathode of the LED
pull-down	active high	LEDx IO connected to the anode of the LED

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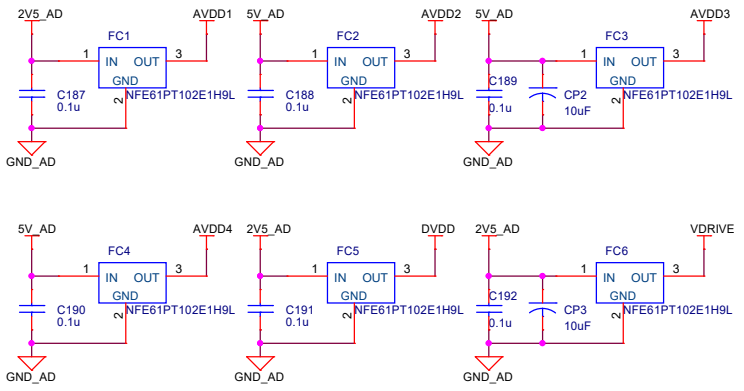

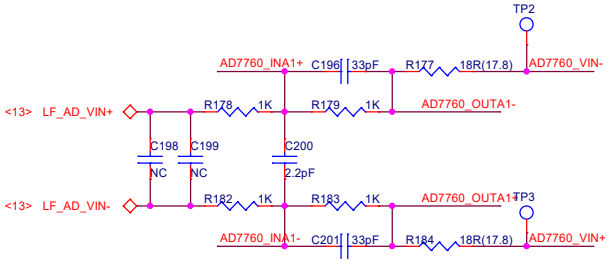

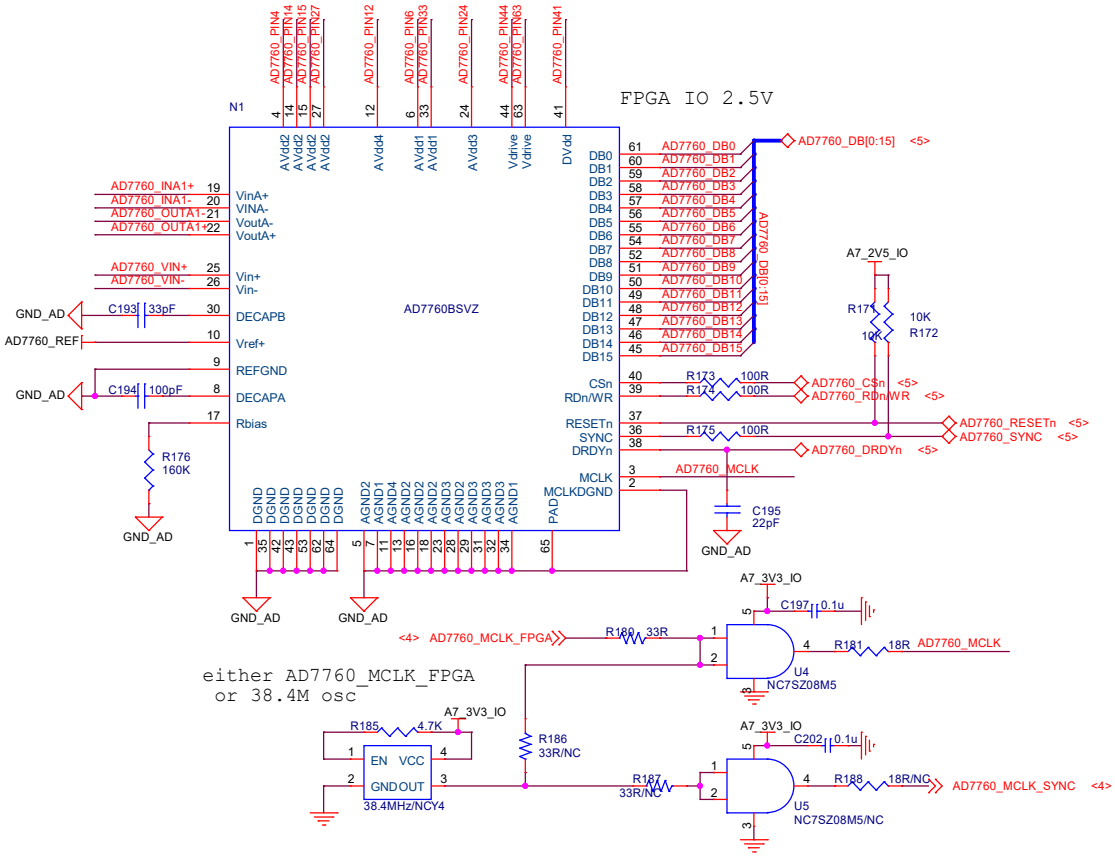

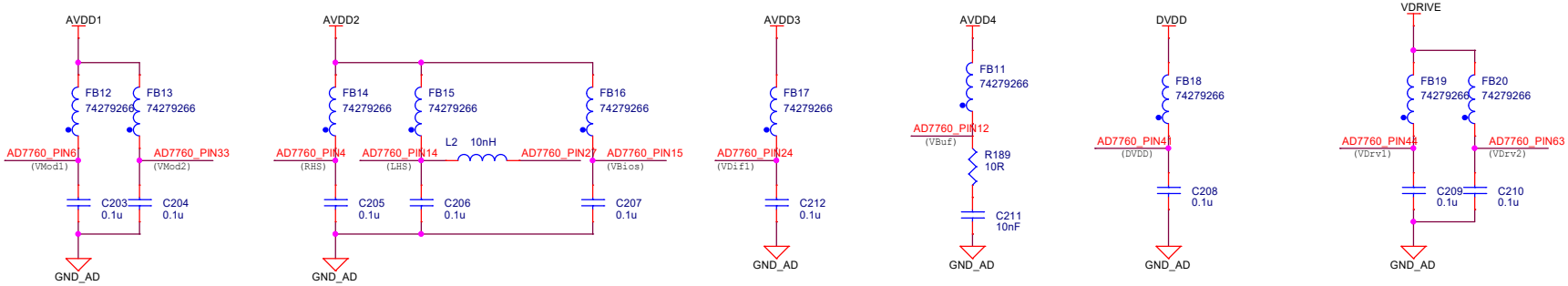

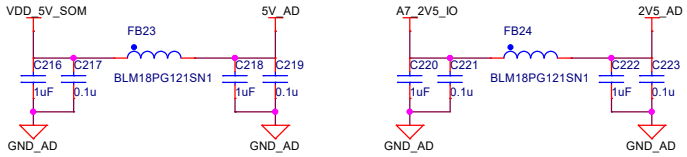

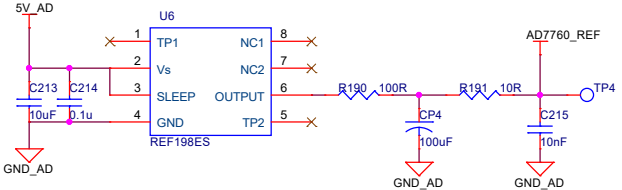

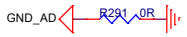

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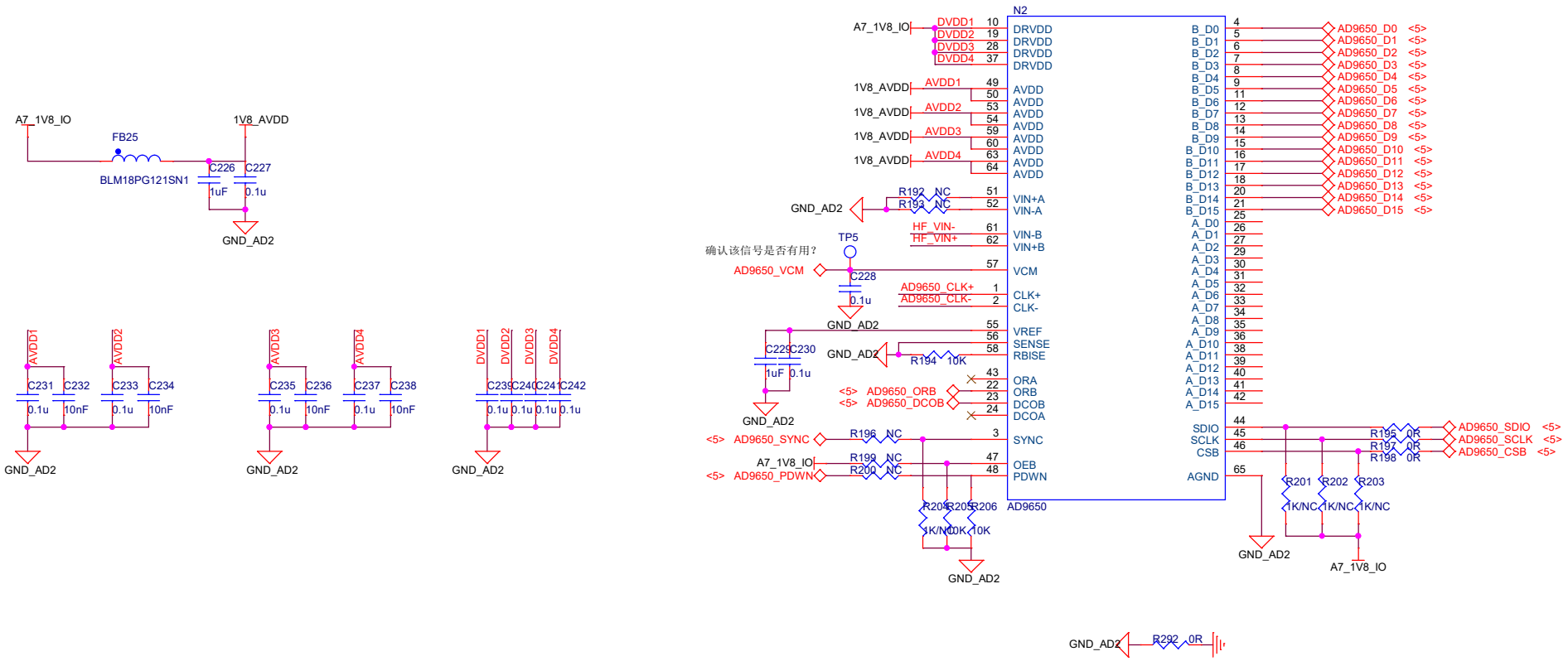

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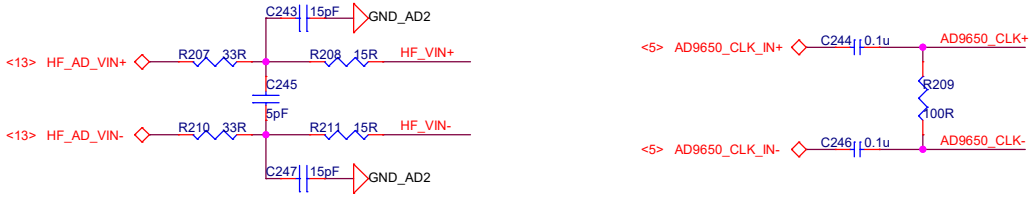

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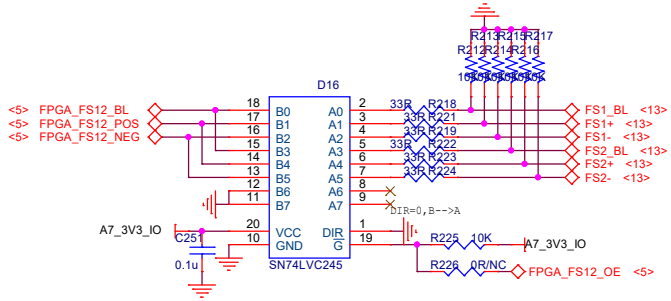

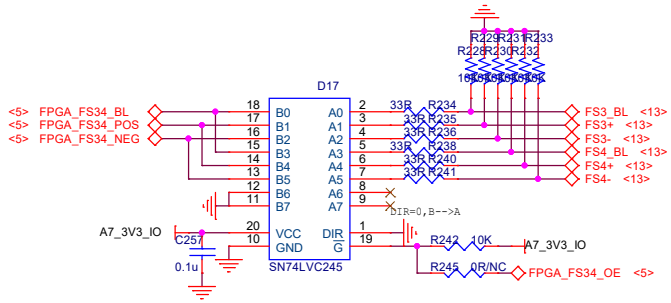

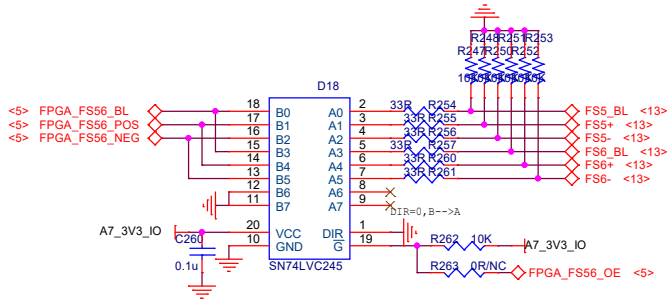

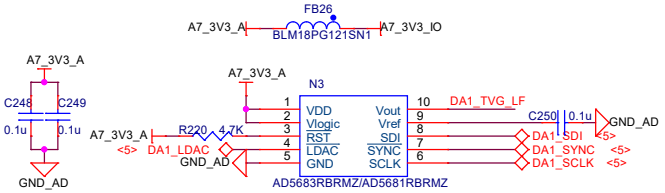

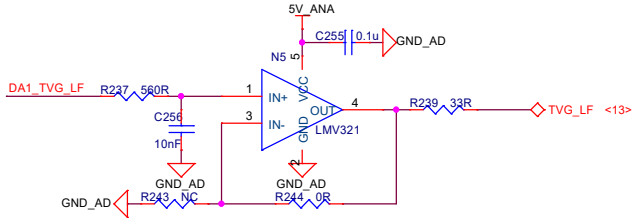

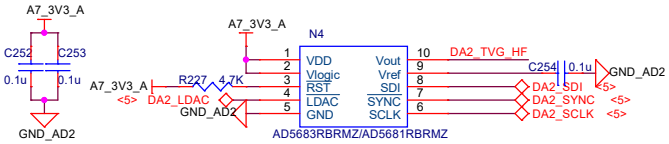

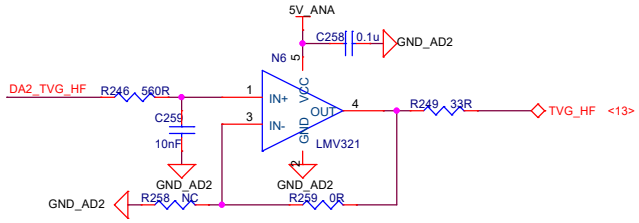

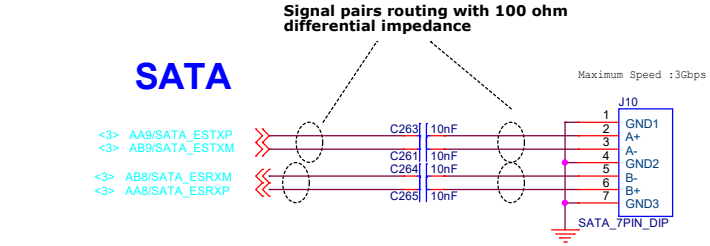

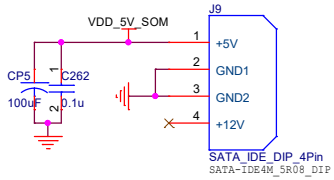

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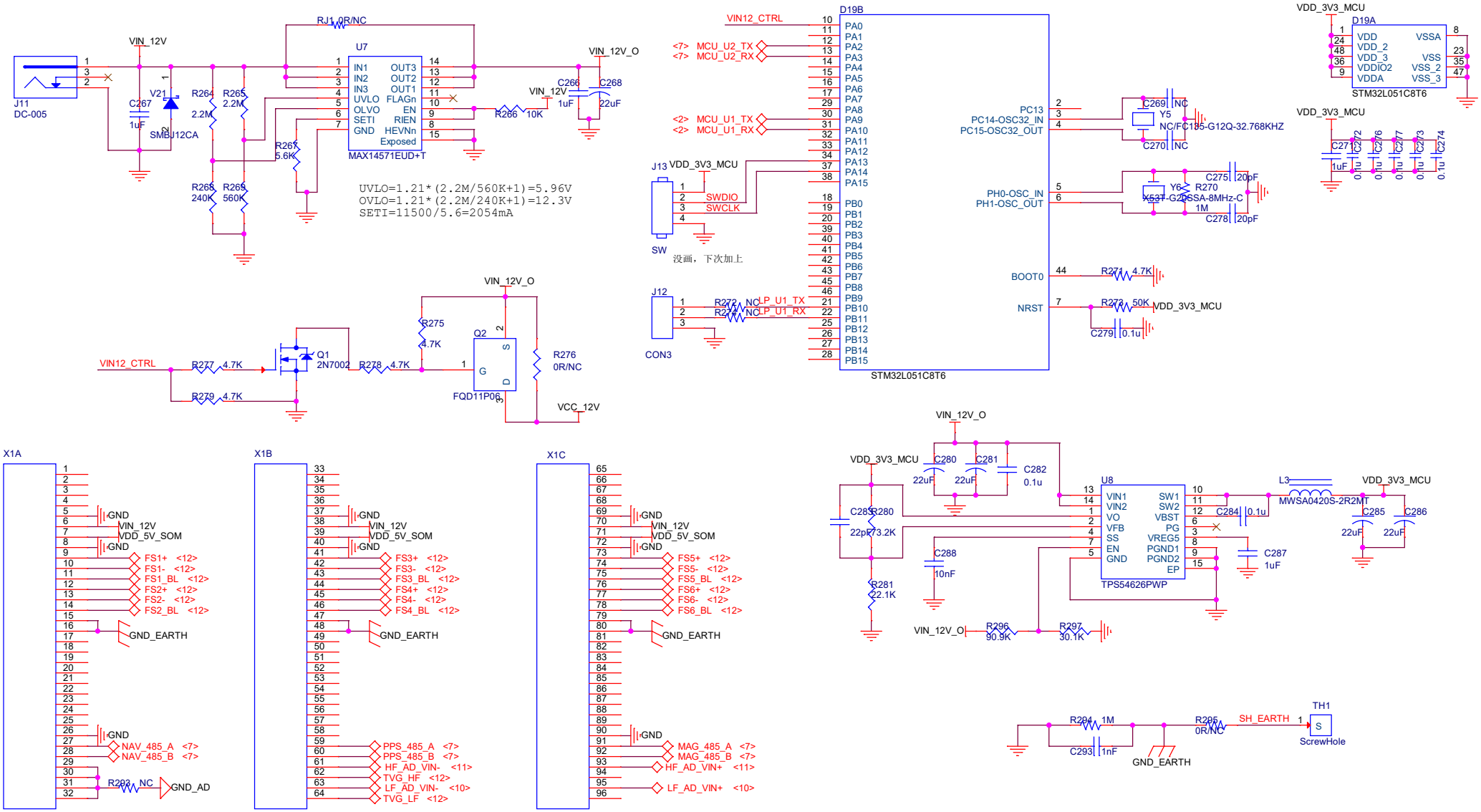

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