Yanze Wu

Cyber Security Engineering Department | **George Mason University**
(+1) 571-604-4865 | ywu42@gmu.edu | https://github.com/Yanze66

Education

- **George Mason University** — Virginia, U.S.
  Ph.D. in Information Technology. GPA 3.95 — *Jan. 2024 – Present.*
- **Hohai University** — Changzhou, China
  Master of Communication and Information Systems. — *Sep. 2020 – Jun. 2023*
- **Hohai University** — Changzhou, China
  Bachelor of Electronic Science and Technology. — *Aug. 2016 – Jun. 2010*

Awards

- **Graduate Student Travel Fund** — Virginia, U.S.
  Awarded to students giving presentation and provides financial support for conference-related travel. — *Sept. 2025.*
- **Daniel R. Bannister PhD fellowship** — Virginia, U.S.
  Supported by the Bannister family. Awarded to the top 4 graduate students at GMU. — *Dec. 2024.*
- **National Scholarship** — Changzhou, China
  National Level. Awarded to top 2% students in the college. — *Oct. 2022.*
- **First-class Scholarship** — Changzhou, China
  Bachlor's and Master's Level. Awarded to top 10% students in the college. — *2017/2018/2019/2020/2021.*

Skills and Interests

- **Programming skills**: Verilog, C, Python (have experience building hardware accelerators for cryptographic algorithms, modular multiplications, and neural networks.) **Board**: ZYNQ, VCK190, Artix-7
- **Research interests**: Hardware accelerating, spatial computing architecture, post-quantum cryptography, side-channel attack, neural network, ising model.

Publications

- Andrew Fan, **Y. Wu**, Tanvir Arafin. "GPU Acceleration of the Sum-Check Protocol Over Binary Tower Fields for Verifiable Computing ", DATE'25, Verona, Italy.
- **Y. Wu**, Qian Wang, Tanvir Arafin. "SHAFI: Securing Hash-Based Post-Quantum Cryptography from Hardware Fault Injection Attacks", AsianHOST'25, Nanjing, China.
- **Y. Wu**, Tanvir Arafin. "Energy-Efficient Acceleration of Hash-Based Post-Quantum Cryptographic Schemes on Embedded Spatial Architectures", PACT'25, Irvine, California, USA. **(27.8% acceptance rate, 34 of 122)**

- **Y. Wu**, Tanvir Arafin. "Accelerating Torus Fully Homomorphic Encryption on Energy-Efficient Heterogeneous Architecture" , ICCD'25, Dallas, USA. **(25.5% acceptance rate)**
- **Y. Wu** and M. T. Arafin, "ArKANe: Accelerating Kolmogorov-Arnold Networks on Reconfigurable Spatial Architectures," IEEE Embedded Systems Letters, 2025 **(Impact Factor 1.7)**.
- **Y. Wu** and M. T. Arafin, "Ising Model Processors on a Spatial Computing Architecture," 2024 IEEE 67th International Midwest Symposium on Circuits and Systems (MWSCAS), Springfield, MA, USA, 2024, pp. 1383-1387, doi: 10.1109/MWSCAS60917.2024.10658926.
- Y. Cao, **Y. Wu**, L. Qin, S. Chen, and CH. Chang, "Areas, Time and Energy Efficient Multicore Hardware Accelerator for Extended Merkle Signature Scheme" in IEEE TCAS-1: Regular Paper, Early Access, 2022, doi: 10.1109/TCSI.2022.3200987. **(Impact Factor 1.18)**
- Y. Cao, **Y. Wu**, X. Lu, S. Chen, J. Ye and CH. Chang, "An Efficient Full Hardware Implementation of Extended Merkle Signature Scheme" in IEEE TCAS-1: Regular Papers, vol.69, no.2, pp. 682-693, Feb. 2021. **(Impact Factor 1.18)**
- W. Zheng, **Y. Wu**, et al. "Accelerating hybrid and compact neural networks targeting perception and control domains with coarse-grained dataflow reconfiguration" 2020, J. Semiconductor., vol. 41, no. 2. **(Impact Factor 0.23)**

Talks and Presentations

- **Adaptive Acceleration Arrays for Cryptography**: Achieve high-performance cryptographic algorithm on spatial computing architecture. *George Mason University, Apr. 2024*
- **Security on Heterogeneous Architecture**: Discussing the transition of hybrid computing architecture and security issues exposed on modern multiple-processor systems. *George Mason University, Feb. 2024*

Experience

- **Fisilink Microelectronics Technology Co., Ltd.** Suzhou, China

  Internship of Digital Integrated Circuit Design *Jun. 2020 - Sep. 2020*
  - **XMSS Hardware Accelerators**: Learn and implement XMSS in hardware.
  - **Electronic Control Unit**: Construct fast verify modules for vehicles at the standard of 2200 times per second.
  - **Fast Modular Application Accelerators**: Construct fast modular accelerators for high-performance NTT implementation.
- **University of Chinese Academy of Sciences** Shenzhen, China

  Research Assistant *Oct. 2019 - Jan. 2020*
  - **Implementation of LSTM Hardware Accelerators**: Learn Long Short-Term Memory (LSTM) neural networks and construct hardware accelerators.
  - **Accelerators for Float-point Numbers**: Build lightweight accelerators for float-point numbers utilized in neural networks.

Reference

- **Tanvir Arafin, Ph.D.** marafin@gmu.edu

  Assistant Professor, Cyber Security Engineering Department, George Mason University