SPLL Design to flux oriented of a VSC interface for Wind Power Applications

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***Abstract* - Accurate phase information is crucial for most of modern power electronic systems such as VSC connected to the grid. In this paper, it is proposed an algorithm software phase-locked loop (SPLL) to obtain phase and frequency information of the grid voltage. This is based in an algorithm of on-line separation of the grid voltage sequences (DSC), and a discrete traditional PLL. A criterion to tune the SPLL constants from a PLL discrete linearized model is discussed. The SPLL response is evaluated for different grid disturbances and different SPLL parameters. Besides, a VSC connected to the grid through and L filter with the SPLL obtained in this paper has been tested for different configurations of SPLL and different grid perturbations. Conclusions about where to apply the SPLL different configurations are obtained from these last tests.**

I. INTRODUCTION

Fig. 1 shows the control diagram of a VSC connected to the grid through an L-filter with its controllers [1]. The current controller is working in positive *dq*-frame, and then it has to implement the transformations represented in Fig. 2 [2]. These are synchronized with the θ angle, which is the output of the SPLL block of Fig. 2.

θ is the grid voltage phase, and with this angle is achieved the transformation of the grid voltage vector: $\vec{e}_{g\_abc}$ to $\vec{e}_{dq}$. To make easy the VSC control, this transformation is calculated so that to arrange the *dq*-frame to the integral of grid voltage vector ($e_d = 0$ and $e_q = |\vec{e}_g|$). This VSC control is called "flux oriented VSC control".

The PLL functions depend on the VSC application and the VSC controllers. In general, for a VSC connected to the grid and that works as regenerative circuit, the functions are:

- Exact synchronization of the VSC current control with the phase of the positive sequence of the fundamental harmonic voltage.
- Flux oriented VSC control.
- Separation of the positive and negative sequences of grid voltages.
- Fast response in presence of grid disturbances [3].
- Synchronization with the fundamental harmonic when the grid voltages have harmonics.

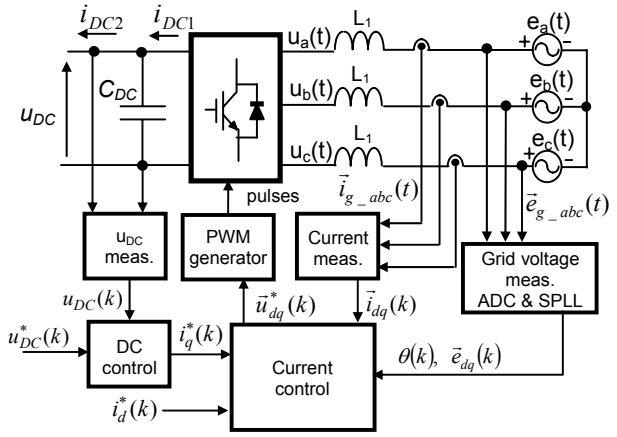


Fig. 1. Block diagram of VSC controllers.

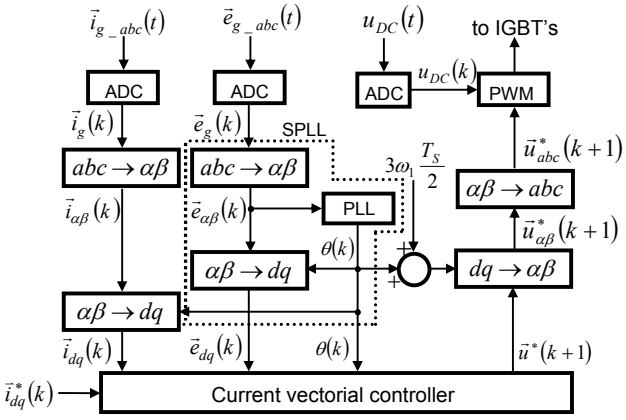


Fig. 2. Block scheme of the vector current controller with the necessary transform axis.

Some works about PLL for VSC's connected to the grid are [3], [4], [5], etc. In this paper, the SPLL (software PLL) algorithm by a VSC that works as a regenerative system is presented. The main contributions respect to the previous works are:

- The SPLL filter constants are obtained by direct design techniques based on root locus in the *z* plane.
- Also, in this work, the SPLL response is evaluated for different grid disturbances and different filter constants.
- The dynamic of SPLL with and without DSC (Delay Signal Cancellation) is analysed in function of different grid disturbances.
- Finally, the VSC control response will be evaluated in function of SPLL constants.

The proposed algorithms are validated through simulations of a 100KVA VSC with L-filter, whose parameters and component values are shown at Table I.

TABLE I.
VALUES USED IN SIMULATIONS.

Grid L filter	DC-bus variables
$L_1 = 0.75mH$ $R_1 = 7.5m\Omega$	$C = 1000\mu F$ $R_{LOAD} = 10\Omega$ $u_{DC} = 750V$
Grid variables	System periods
$f_1 = 50Hz$ $E_n = 400V$	$T_S = 200\mu s$ $T_{Sw} = 400\mu s$

II. SPLL STRUCTURE

A block diagram of the proposed SPLL is depicted in Fig. 3. The operational principle of the SPLL was explained by the authors in [6]. Fig. 4 shows the DSC method [7] for separating on-line the positive and the negative sequences.

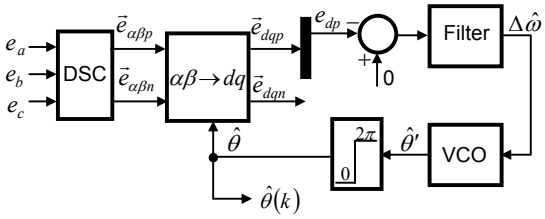


Fig. 3. SPLL.

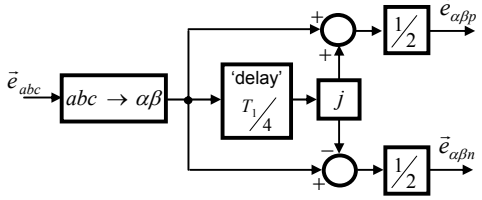


Fig. 4. DSC (Delay Signal Cancellation) [7].

Fig. 5 represents the SPLL continuous linearized model. The closed loop transfer function can be expressed as:

$$H_c(s) = \frac{\hat{\theta}(s)}{\theta(s)} = \frac{k_f(s) k e_m}{s + k_f(s) k e_m} \quad (1)$$

where $\hat{\theta}(s)$ and $\theta(s)$ are the Laplace transform of $\hat{\theta}$ and θ, respectively; e_m is the phase voltage peak value; $k = \sqrt{3/2}$ (power invariant transformation); and $k_f(s)$ is the filter transfer function. There are several methods to design the loop filter. A sub-damped second-order loop is commonly used as good trade-off of the filter performance and system stability. The proportional-integral filter (PI) for the second-order loop can be given as:

$$k_f(s) = K_{pPLL}\left(\frac{1 + s\tau}{s\tau}\right) \quad (2)$$

where K_{pPLL} and $K_{iPLL} = K_{pPLL}/\tau$ are the proportional and integral gains of the PI, respectively. The closed loop transfer function is rewritten in the general form of the second-order loop as:

$$H_c(s) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad (3)$$

where $\omega_n = \sqrt{\frac{k_p k E_m}{\tau}}$ $\zeta = \frac{k_p k E_m}{2\omega_n} = \frac{\sqrt{k_p k E_m \tau}}{2}$.

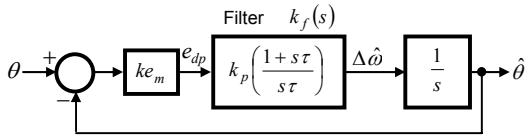


Fig. 5. SPLL continuous linearized model.

III. SPLL CONSTANTS TUNING

A. Specifications of the closed loop behaviour

ω_n sets the system band-width, and therefore, the response speed, whereas ζ sets the damping of the closed loop temporal response. It is checked in Fig. 6. For $\zeta = 1/\sqrt{2}$ the overshoot is 20%, but the final response is reached in half of the fundamental period for any ω_n, between $2\pi 100\, rad/s$ and $2\pi 1000\, rad/s$. It is a good relation between having a fast response and having good characteristics of filtering for the grid voltage variations. The chosen value of ζ coincides with the chosen value in [4] using the Wiener optimization method.

B. Configuration of the SPLL linearized discrete model constant.

Fig. 7 represents SPLL discrete linearized model. The plant (VCO), $\frac{\hat{\theta}(z)}{\Delta\hat{\omega}(z)} = \frac{T_S}{(z-1)}$, is the z transformation by ZOH method of the Fig. 5 continuous VCO. The transfer function of the discrete controller is $k_d(z) = K_{pPLL}\frac{z - \alpha_{PLL}}{z-1}$ and it is developed by direct design techniques based on root locus in the z plane. The expression to calculate K_{pPLL} and α_{PLL} are:

$$K_{pPLL} = \frac{2}{T_S k e_m}\left[1 - e^{-\zeta\omega_n T_S}\cos\left(\omega_n T_S\sqrt{1-\zeta^2}\right)\right]$$

$$\alpha_{PLL} = \frac{1 - e^{-2\zeta\omega_n T_S}}{2\left[1 - e^{-\zeta\omega_n T_S}\cos\left(\omega_n T_S\sqrt{1-\zeta^2}\right)\right]} \quad (4)$$

The design specifications are based on the conclusions obtained in the previous section, and they are: $\zeta = 1/\sqrt{2}$, $\omega_{n1} = 2\pi 100\, rad/s$ and $\omega_{n2} = 2\pi 1000\, rad/s$. The two values

of ω_n are used to perform tests of the SPLL behaviour under grid disturbances with different SPLL response speech. Table II shows the poleplacement in closed loop and the values of K_{pPLL} and α_{PLL} according to ω_n.

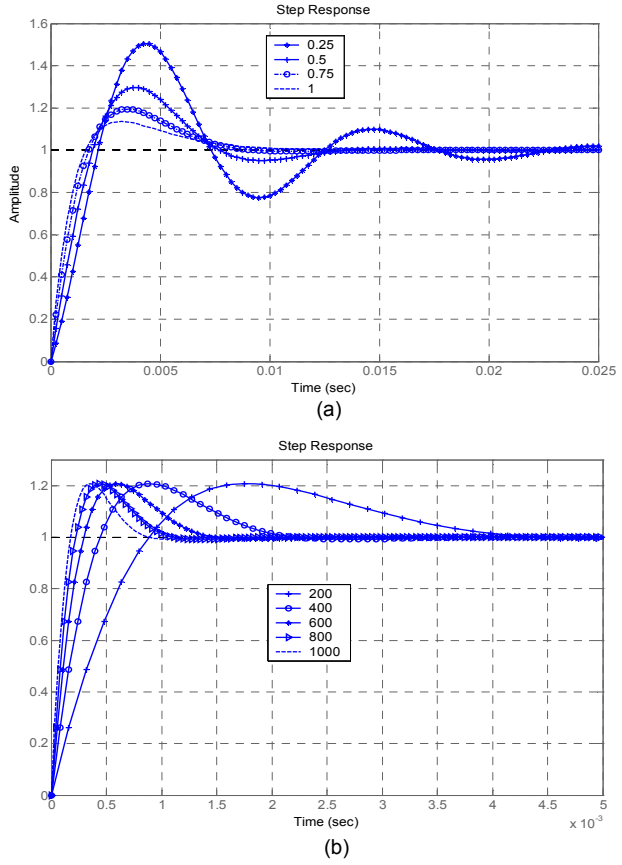


Fig. 6. Temporal response of Fig. 5 according to: a) ζ for $\omega_n = 2\pi 100\, rad/s$, and b) ω_n for $\zeta = 1/\sqrt{2}$.

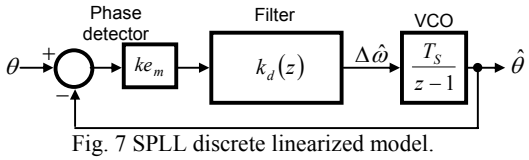


Fig. 7 SPLL discrete linearized model.

Table II.
CONSTANT VALUES OF $k_d(z)$ ACCORDING TO THE ω_n VALUE.

ω_n	Closed loop poleplacement	K_{pPLL}	α_{PLL}
$2\pi 100\, rad/s$	$0.91 \pm 0.08j$	2.21	0.92
$2\pi 1000\, rad/s$	$0.26 \pm j0.32$	18.52	0.561

IV. SPLL PRACTICAL RESULTS

The aim of this section is to analyze the SPLL behaviour in the presence of grid perturbations for: SPLL without and with DSC, and, also, in function of bandwidth (ω_n). The initial grid voltages are:

$$e_a(t) = 400\sqrt{\frac{2}{3}}\cos(2\pi 50t)$$
$$e_b(t) = 400\sqrt{\frac{2}{3}}\cos(2\pi 50t - 2\pi/3) \quad (5)$$
$$e_c(t) = 400\sqrt{\frac{2}{3}}\cos(2\pi 50t + 2\pi/3)$$

and, the SPLL is tested for the following perturbations:

1. Dip type A. Between 0.2s and 0.3s $\hat{e}_a = \hat{e}_b = \hat{e}_c = 200\sqrt{\frac{2}{3}}$ (Fig. 8.1).
2. Dip type B. Between 0.2s and 0.3s $\hat{e}_b = 350\sqrt{\frac{2}{3}}$ (Fig. 8.2).
3. Phase change in the three voltages (balanced system). An increase in the phase of 30º is produced between 0.2s and 0.3s (Fig. 8.3).
4. Harmonics in the grid during the simulation time (0 to 0.5s). The values are $\hat{e}_{a1} = \hat{e}_{b1} = \hat{e}_{c1} = 400\sqrt{\frac{2}{3}}$, $\hat{e}_{a5} = \hat{e}_{b5} = \hat{e}_{c5} = \frac{400}{15}\sqrt{\frac{2}{3}}$, $\hat{e}_{a7} = \hat{e}_{b7} = \hat{e}_{c7} = \frac{400}{17}\sqrt{\frac{2}{3}}$. The result of this is a balanced three phase system in the three harmonic components (Fig. 8.4).
5. Frequency jumping in the three phases. Between 0.2s and 0.3s $f_a = f_b = f_c = 49Hz$. The results for this perturbation are very similar for the different SPLL configurations and for this reason they are not presented.

The resultant *dqp* (positive) components for each perturbation are represented are in Fig. 8. In all the cases $\zeta = 0.707$ and ω_n is $2\pi 100\, rad/s$ or $2\pi 1000\, rad/s$, such as it is indicated in the figure. The general first conclusion is that the SPLL without DSC is more dependent of the bandwidth (ω_n) and, therefore, the SPLL control loop rate.

For the case 1 (Fig. 8.1), the temporal response is very similar in the four configurations. In the case 2 (Fig. 8.2), unbalanced voltages are applied to the SPLL input. The SPLL with DSC *dqp* components do not have ripple; whereas the SPLL without DSC behaviour depends of the bandwidth, and the ripple of the *dqp* components is bigger for $\omega_n = 2\pi 1000\, rad/s$.

The worse perturbation for the SPLL is a phase change (case 3) (Fig. 8.3). The SPLL behaviour with and without DSC is very similar. In the two configurations, a slow response is better because the transient *dqp* components are

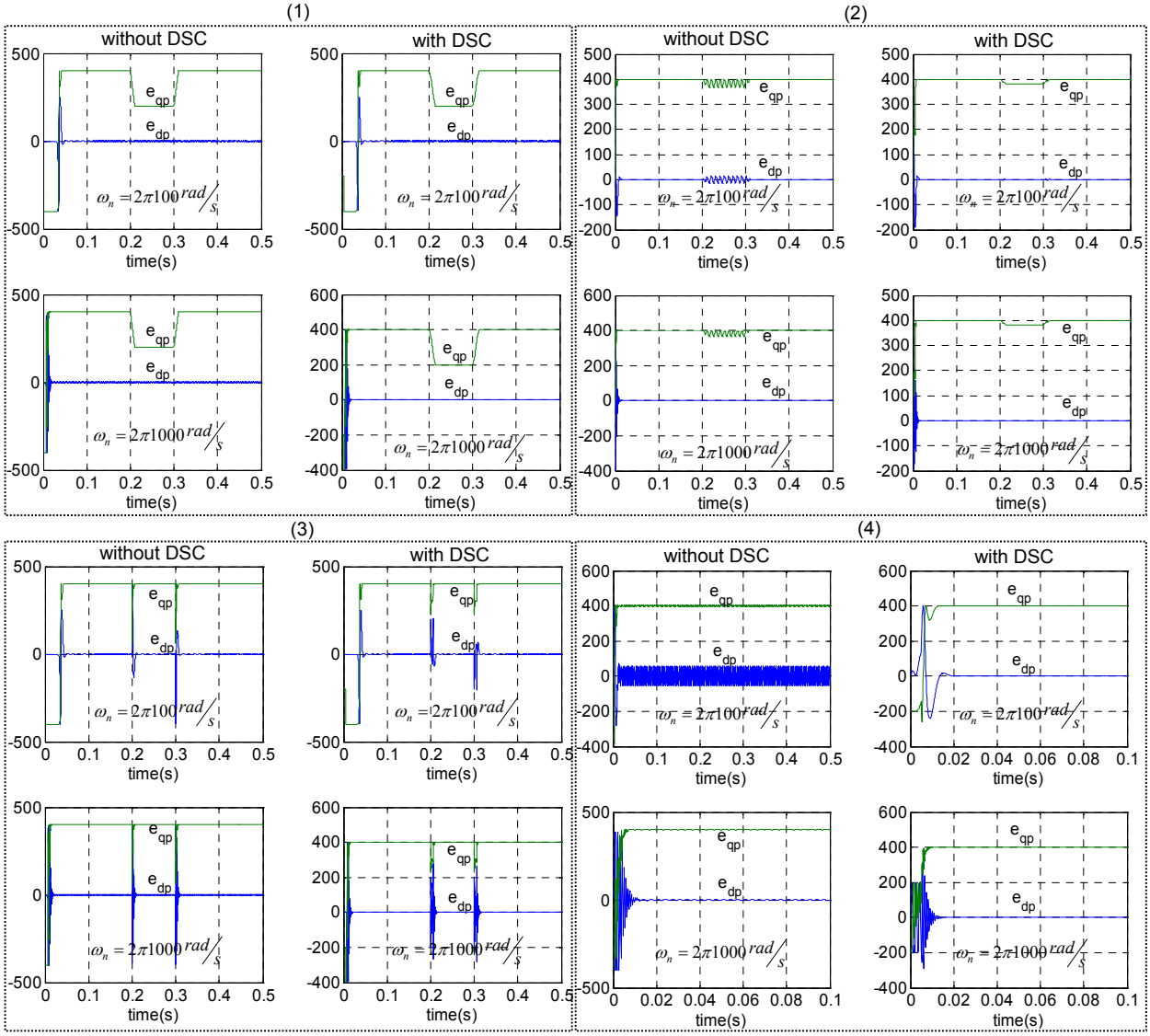


Fig. 8. Temporal response of the *dqp* components in presence of grid perturbations.

smaller.

When the grid has harmonics (case 4) (Fig. 8.4), the SPLL with DSC tracks the fundamental frequency phase. On the other hand, the *dqp* components of the SPLL without DSC present a ripple which is smaller for $\omega_n = 2\pi 1000\, rad/s$.

Fig. 8 conclusions are that SPLL with DSC response is practically independent of the ω_n. The reason of this is that the 'on-line' detection of sequences eliminates the ripple in the *αβp* and *αβn* components due to the grid harmonics and the unbalanced voltages. So, the input to the PLL of the SPLL is an ideal signal in each channel (positive and negative). On other hand, the Table 3 shows the SPLL without DSC rate for obtaining the better behaviour in presence of grid perturbations.

These conclusions are obtained analyzing the SPLL behaviour in open loop, and, besides, establishing as criterion of optimal behaviour that the *dqp* components do not contain ripple. In this case, the SPLL with DSC response looks ideal for any configuration, but in next section, these conclusions are re-analyzed when the SPLL is introduced in the VSC controller.

TABLE III.
SPLL WITHOUT DSC RATE FOR OBTAINING THE BETTER BEHAVIOUR.

Grid Perturbation Type	SPLL without DSC
Dip A	Same
Unbalanced voltage	Fast
Phase Change	Slow
Harmonics	Fast
Frequency Change	Same

IV. BEHAVIOUR OF A VSC CONNECTED TO THE GRID IN FUNCTION OF THE SPLL

In a system as Fig.1, if the SPLL has a response very slow, the VSC general response will be very slow in presence of some grid perturbations. On the other hand, if the SPLL is very fast, it can generate perturbations to the system rest and it can submit to an excessive stress to the current controller.

Fig. 9 represents the temporal response of the *dq* grid current component for the Fig. 1 system. The VSC is working as PWM rectifier, $u_{DC}^{*} = 750V$ and an L-filter is used. The current controller chosen for this test is a single dead-beat controller that uses the positive synchronous reference frame [1]. The SPLL constants are $\zeta = 0.707$ and $\omega_n = 2\pi 100\, {}^{rad}/_{s}$. In this Fig., the responses of the SLL without DSC (left column) and SPLL with DSC (right column) are compared for the same perturbations of the Fig. 8. So, the Fig. 9 numbers correspond to the section 4 perturbations.

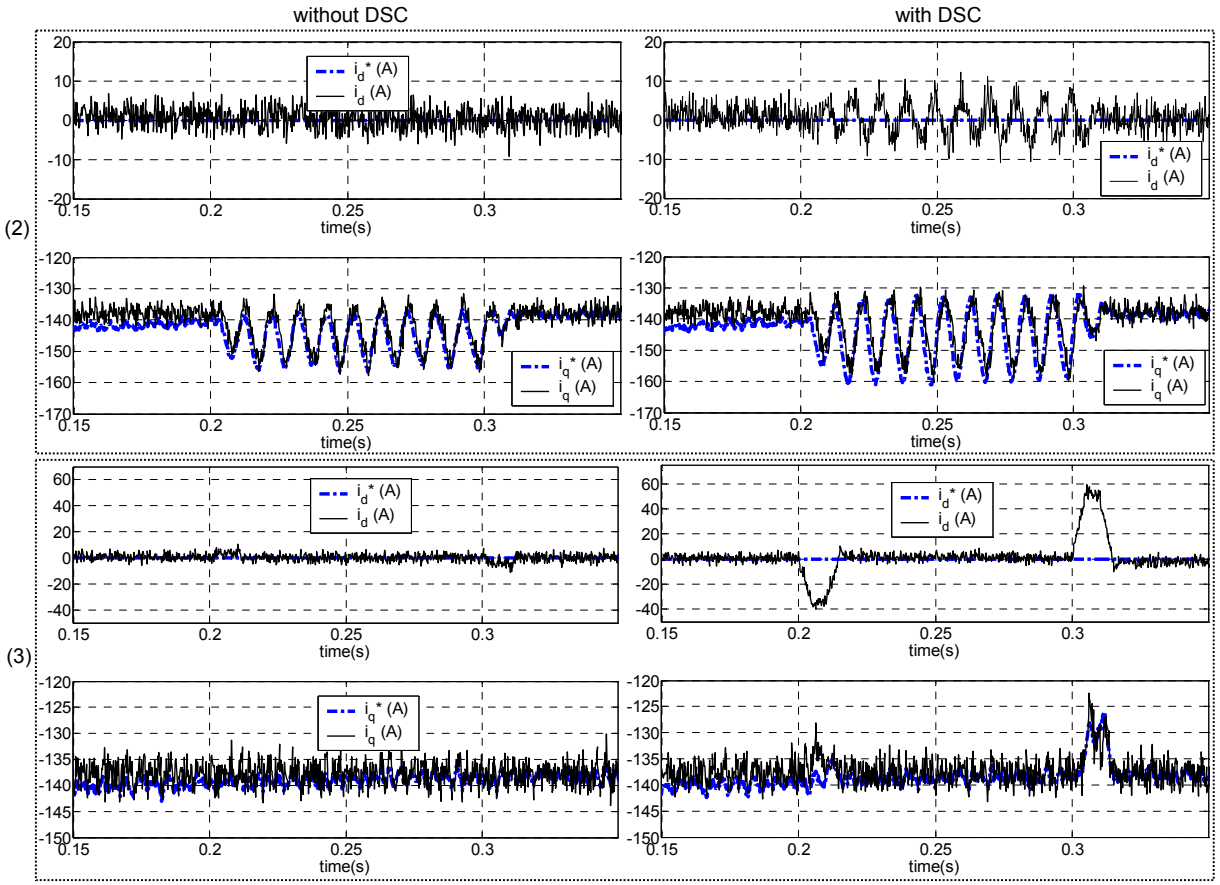
From the results shown in Fig. 9, it can be deduced that, in general, the SPLL without DSC response is better. The justification of this is that the SPLL with DSC eliminates almost any perturbation of the output *dqp* grid components. In the controller used in Fig. 1, these components also are used as feedforward variables, so that if the perturbations are eliminated, the feedforward action is useless. On the other hand, the grid perturbations appear in the SPLL without DSC output, and they compensate a part of the grid perturbations by the feedforward action.

The use of the SPLL with DSC depends on the converter application and the used current controller. The SPLL with DSC is optimal in system with a dual current controller [7], or in controllers where the feedforward is not the SPLL output but the exact information of the grid signals. Under other circumstances, a SPLL without DSC is the better option.

In previous section, it was proved that the open loop responses of SPLL with DSC and SPLL without DSC are very similar, when this last has fast configuration. So, the SPLL without DSC behaviour with $\omega_n = 2\pi 1000\, {}^{rad}/_{s}$ inside of Fig.1 VSC is similar to the SPLL with DSC, and, also, the conclusions are similar.

V. CONCLUSIONS

In this paper, a SPLL (software PLL) has been presented for VSCs connected to the grid working as regenerative circuit. The open loop SPLL behaviour has been analyzed for the following SPLL configurations: without DSC, with DSC, fast and slow. From this first study, it can be deduced that the SPLL with DSC and fast SPLL without DSC are better, because the *dqp* components do not have ripple in presence of grid perturbations. Then, the behaviour of a VSC



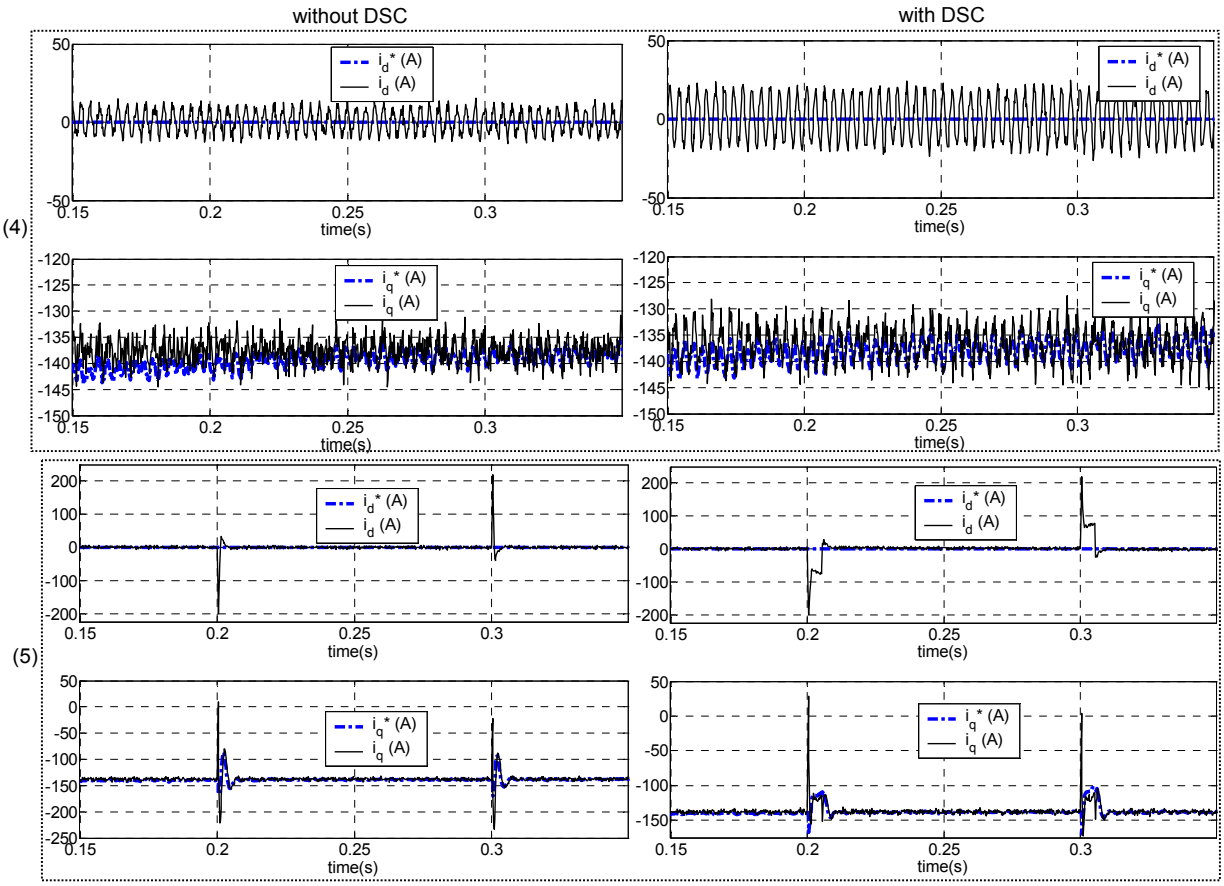


Fig. 9. Temporal responses of the *dq* current components for the Fig. 1 VSC. The left column represents the SPLL without DSC responses, and the right column represents the SPLL with DSC responses. In both cases $\omega_n = 2\pi 100\, {}^{rad}/_{s}$.

connected to the grid with SPLL has been tested for the same SPLL configurations. From this second study, it can be checked that the better SPLL configuration depends on the VSC current controller. For example, if it is a single dead-beat controller that uses the positive synchronous reference frame is better a slow SPLL without DSC, because the feedforward action is more useful.

VI. ACKNOWLEDGMENT

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