A Phase Tracking System for Three Phase Utility Interface Inverters

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***Abstract*—The analysis and design of the phase-locked loop (PLL) system is presented for the phase tracking system of the three phase utility interface inverters. The dynamic behavior of the closed loop PLL system is investigated in both continuous and discrete-time domains, and the optimization method is considered for the second order PLL system. In particular, the performance of the three phase PLL system is analyzed in the distorted utility conditions such as the phase unbalancing, harmonics, and offset caused by the nonlinear load conditions and measurement errors. The tracking errors under these distorted utility conditions are also derived. The phase tracking system is implemented in a digital manner using a digital signal processor (DSP) to verify the analytic results. The design considerations for the phase tracking system are deduced from the analytic and experimental results.**

***Index Terms*—Phase-locked loop, utility interface.**

I. Introduction

As increasing demands for the high quality, reliability, and usability of electric power source, the utility interface operation of power converters is often used in advanced power conversion and conditioning systems such as the static VAR compensators, active power filters, uninterruptible power supplies (UPS's), and grid-connected photovoltaic or wind power generation systems [3]. Since the control of the power factor is common goal of these systems and requires the accurate phase information of the utility voltages, the phase tracking system is one of the most important parts of these systems.

The phase-locked loop (PLL) technique has been used as a common way of recovering and synthesizing the phase and frequency information in electrical systems [1], [2]. In the area of power electronics, the PLL technique has been adopted in the speed control of electric motors [5], [6]. This is also available for synchronizing the utility voltages and the controlled currents or voltages in utility interface operation of power electronic systems. A simple method of obtaining the phase information is to detect the zero crossing point of the utility voltages [1]. However, since the zero crossing point can be detected only at every half cycle of the utility frequency, the phase tracking action is impossible between the detecting points and thus the fast dynamic performance can not be obtained. An improved method is the technique using the quadrature of the input waveform shifted by 90° [1]. This technique has been often employed in the various applications for the phase or position detecting [7]. In the three phase systems, the dq transform of the three phase variables has the same behaviors with this technique and the PLL system can be implemented by using the dq transform and appropriate loop filter.

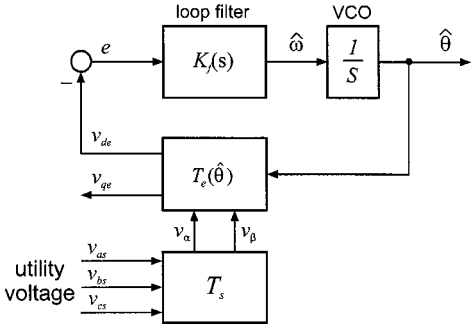

Fig. 1. Block diagram of three phase PLL system.

This paper describes the characteristics of the three phase PLL systems and discusses the proper design method. Especially, the performance of the PLL system is analyzed and the tracking errors are derived for the distorted utility conditions such as the phase unbalancing, harmonics, and offset. Besides the analytic studies, the experimental verifications are carried out using the digital signal processor (DSP) system under various utility conditions. Through these analytic and experimental works, the important considerations are provided for the design of the phase tracking system in the three phase utility interface inverters.

II. Three Phase PLL System

The block diagram of the three phase PLL system can be described as shown in Fig. 1. In this system, the three phase utility voltages can be represented as

$$v_{abcs} = V_m \cdot \begin{pmatrix} \cos\theta \\ \cos\left(\theta - \frac{2\pi}{3}\right) \\ \cos\left(\theta + \frac{2\pi}{3}\right) \end{pmatrix}. \tag{1}$$

where $v_{abcs} = [v_{as} \;\; v_{bs} \;\; v_{cs}]^T$. Under the assumption of the balanced utility voltage, (1) can be expressed in the stationary reference frame as

$$v_{\alpha\beta} = T_s \cdot v_{abcs} \tag{2}$$

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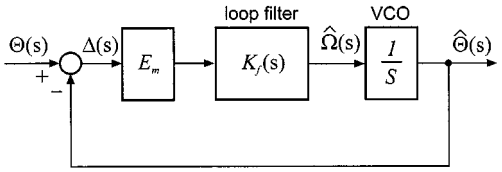

Fig. 2. Linearized model of three phase PLL system.

where $v_{\alpha\beta} = [v_\alpha \;\; v_\beta]^T$ and T_s denotes the transform matrix given by

$$T_s = \frac{2}{3} \cdot \begin{pmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & -\frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \end{pmatrix}. \tag{3}$$

These can be rewritten in the synchronous reference frame using the PLL output $\hat{\theta}$ as

$$v_{qde} = T_e(\hat{\theta}) \cdot v_{\alpha\beta} \tag{4}$$

where $v_{qde} = [v_{qe} \;\; v_{de}]^T$ and $T_e(\hat{\theta})$ denotes the rotating matrix given by

$$T_e(\hat{\theta}) = \begin{pmatrix} \cos\hat{\theta} & -\sin\hat{\theta} \\ \sin\hat{\theta} & \cos\hat{\theta} \end{pmatrix}. \tag{5}$$

The voltage of interest is the d-axis component and derived as

$$\begin{aligned} v_{de} &= E_m \sin\delta \\ &= e \end{aligned} \tag{6}$$

where $E_m = -V_m$ and $\delta = \theta - \hat{\theta}$. The angular frequency of the PLL system can be represented as

$$\hat{\omega} = \frac{d\hat{\theta}}{dt} = K_f \cdot e \tag{7}$$

where K_f denotes the gain of the loop filter. If it is assumed that the phase difference δ is very small, (6) can be linearized as

$$e \cong E_m \delta. \tag{8}$$

Hence, the PLL frequency $\hat{\omega}$ and phase $\hat{\theta}$ can track the utility frequency ω and phase angle θ, respectively, by the proper design of the loop filter.

III. Closed Loop System

A. Second Order Loop in Continuous-Time Domain

The linearized model of the three phase PLL system can be described as shown in Fig. 2. The transfer function of the closed loop system can be represented as

$$H_c(s) = \frac{\hat{\Theta}(s)}{\Theta(s)} = \frac{K_f(s)E_m}{s + K_f(s)E_m} \tag{9}$$

$$H_\delta(s) = \frac{\Delta(s)}{\Theta(s)} = \frac{s}{s + K_f(s)E_m} \tag{10}$$

where $\Theta(s), \hat{\Theta}(s)$, and $\Delta(s)$ denote the Laplace transform of $\theta, \hat{\theta}$, and δ, respectively. There are various methods in designing the loop filter. The second order loop is commonly used as a good trade-off of the filter performance and system stability [1]. The proportional-integral (PI) type filter for the second order loop can be given as

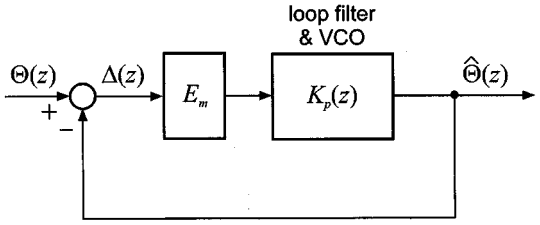

Fig. 3. Discrete-time domain model of three phase PLL system.

$$K_f(s) = K_p \cdot \left(\frac{1 + s\tau}{s\tau}\right) \tag{11}$$

where K_p and τ denote the gains of the PI type filter. The transfer functions of the closed loop system are rewritten in the general form of the second order loop as

$$H_c(s) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{12}$$

$$H_\delta(s) = \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{13}$$

where

$$\omega_n = \sqrt{\frac{K_p E_m}{\tau}}, \quad \zeta = \frac{K_p E_m}{2\omega_n} = \frac{\sqrt{\tau \cdot K_p E_m}}{2}.$$

B. Second Order PLL in Discrete-Time Domain

Since the PLL system is implemented in a digital manner using a digital signal processor (DSP), the discrete-time model is more useful than the continuous-time one. The block diagram of the PLL system in the discrete-time domain is shown in Fig. 3. The block $K_d z$ is the z-transform of the loop filter and voltage-controlled oscillator (VCO). The closed loop transfer function can be represented as

$$H_c(z) = \frac{\hat{\Theta}(z)}{\Theta(z)} = \frac{E_m K_d(z)}{1 + E_m K_d(z)}. \tag{14}$$

For the second order loop using the PI type filter, $K_d(z)$ can be obtained as

$$K_d(z) = K_p \frac{z(z - \alpha)}{(z - 1)^2} \tag{15}$$

where $\alpha = 1 - T/\tau$ and T denotes the sampling period of the digital system. The transfer function of the closed loop system in the discrete-time domain can be derived by substituting (15) into (14) as

$$H_c(z) = H_{cm} \cdot \frac{z(z - \alpha)}{z^2 - az + b} \tag{16}$$

where

$$H_{cm} = \frac{E_m K_p}{1 + E_m K_p}, \quad a = \frac{2 + E_m K_p \alpha}{1 + E_m K_p}, \quad b = \frac{1}{1 + E_m K_p}.$$

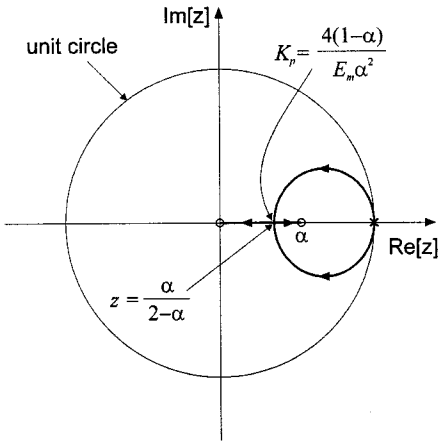

Fig. 4. Root loci of discrete-time PLL system with second order.

Fig. 4 shows the root loci of the closed loop system. When $T > 2\tau$, the closed loop system is unstable in which the open loop zero α is located at the outside of unit circle.

C. Optimization of Closed Loop Performance

It should be considered in the design of the closed loop system that the dynamic performance satisfies the fast tracking and good filtering characteristics. However, both requirements can not be satisfied simultaneously because these two conditions are inconsistency. Therefore, a trade-off is required in designing of the dynamic behavior of the PLL system.

One of the most widely used techniques is the Wiener method [1], which is known as the best optimization method. For the second order loop, the transfer function is given as

$$H_c(s) = \frac{\sqrt{2}\omega_n s + \omega_n^2}{s^2 + \sqrt{2}\omega_n + \omega_n^2}. \tag{17}$$

From (12), the damping ratio can be derived as $\zeta = 0.707$ in this optimization method. The closed loop bandwidth of the PLL can be determined by using the stochastic information of the signal and noise, and can be given in the Wiener method as

$$\omega_n^2 = \Delta\omega\lambda\sqrt{\frac{2P_s}{W_o}} \tag{18}$$

where $\Delta\omega$ is the deviation of the frequency, P_s is the input signal power, W_o is the input noise spectral density, and λ is the Lagrangian multiplier that determines the relative proportions of the noise and transient error. However, because it is very difficult to estimate the stochastic information of the noise and this relation does not provide the optimum results under the distorted voltage waveform, the empirical trade-off is used as mentioned below.

The steady state performance of the PLL system is related to the shape of the input and the order of the loop filter. The errors can be derived from (10) and (13). In the second order PLL, the errors for three types of input are summarized in Table I, where $\Delta\dot{\omega}$ denotes the deviations of the acceleration. It is shown in this table that the PI type second order PLL has the steady state error, known as the tracking error, for the step change of the acceleration which the frequency varies in time.

TABLE I
STEADY STATE ERRORS FOR THREE TYPES OF INPUT

Type of Input	Steady state error for 2nd order PLL	Steady state error for PI-type 2nd order PLL
Position Step	0	0
Velocity Step	$\frac{\Delta\omega}{K_f(0)E_m}$	0
Acceleration Step	$\frac{\Delta\dot{\omega}t}{K_f(0)E_m} + \frac{\Delta\dot{\omega}}{\omega_n^2}$	$\frac{\Delta\dot{\omega}}{\omega_n^2}$

Fig. 5 shows the simulated results of the proposed PLL system with the Wiener optimization when the natural frequency $\omega_n = 628$ [rad/sec]. The gains of loop filter are calculated from (12) and (17) as $K_p = -2.85$ and $\tau = 0.002\,247$ for $V_m = 311$ [V]. In this case, the input is the step change of the frequency from zero to 60 [Hz] and the error converges to zero in the steady state. When the frequency varies in time, the second order PLL shows the tracking error. This error can be reduced by choosing the higher natural frequency that gives the higher bandwidth as shown in Table I. However, the use of higher bandwidth does not provide better results in all conditions. In some practical cases such as the distorted utility, the tracking error increases as the bandwidth increases. Therefore, the selection of the bandwidth is a compromise between various factors, which will be discussed in next chapters.

IV. Error Analysys for Distorted Utility

In practice, the utility voltage is not pure sinusoid but distorted by the various external factors such as the nonlinearities of the load and measurement devices and the signal conversion errors, which results in the phase unbalancing, harmonics, and offset. The distorted utility waveform causes various types of the error in the PLL system, which degrade the control performance of the utility interface inverter system. The errors caused by the distortion of the utility voltage are derived in this chapter.

A. Phase Unbalancing

The utility voltage considering the unbalanced phase can be given as follows:

$$v_{as} = V_m \cos\theta \tag{19}$$

$$v_{bs} = V_m(1+\beta)\cos\left(\theta - \frac{2\pi}{3}\right) \tag{20}$$

$$v_{cs} = V_m(1+\gamma)\cos\left(\theta + \frac{2\pi}{3}\right) \tag{21}$$

where β and γ are constants. These can be rewritten in the stationary reference frame using (3) as

$$v_\alpha = V_m\cos\theta + V_m\left[\frac{\beta+\gamma}{6}\cos\theta - \frac{\beta-\gamma}{2\sqrt{3}}\sin\theta\right] \tag{22}$$

$$v_\beta = -V_m\sin\theta + V_m\left[\frac{\beta-\gamma}{2\sqrt{3}}\cos\theta - \frac{\beta+\gamma}{2}\sin\theta\right]. \tag{23}$$

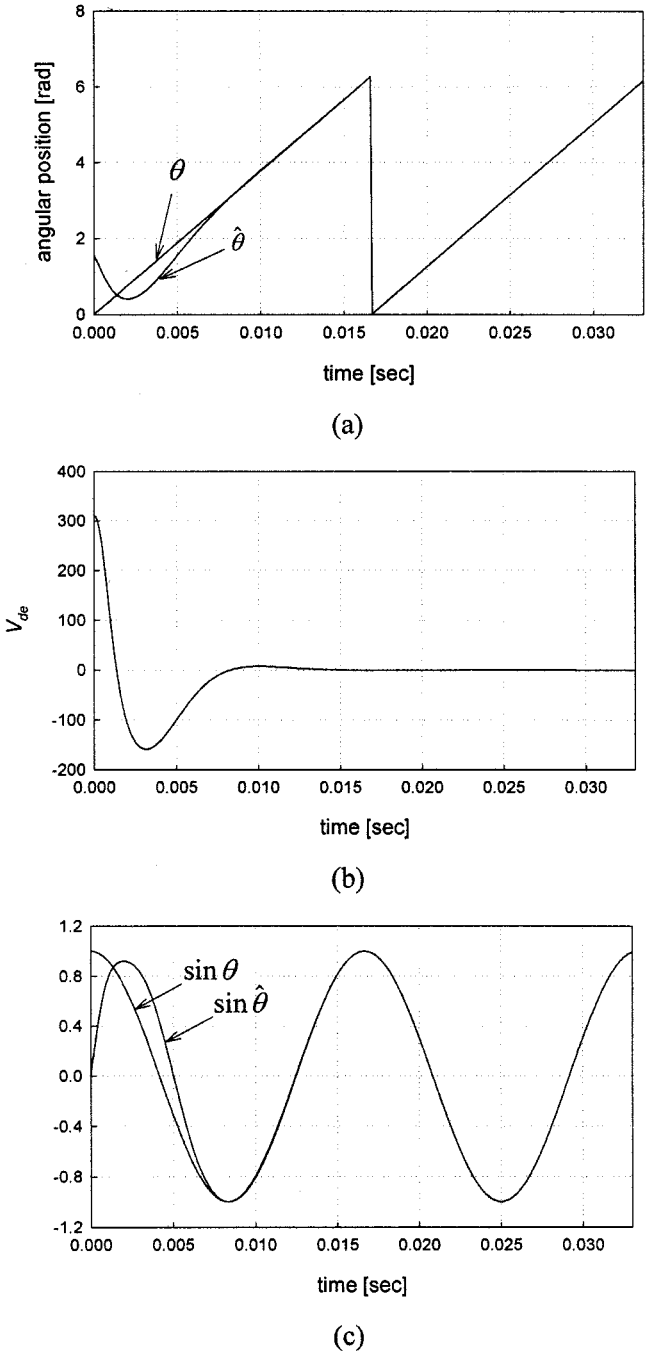

Fig. 5. Simulated results of three phase PLL system ($\zeta = 0.707, \omega_n = 628$ rad/sec). (a) Angular position. (b) d-axis voltage. (c) Sine functions using θ and $\hat{\theta}$.

The second terms of the right hand side of (22) and (23) are produced by the phase unbalancing. The d-axis voltage after the dq transform using (5) can be derived as

$$v_{de} = E_m \sin\delta - E_m \left[\frac{\beta-\gamma}{2\sqrt{3}}(\cos\theta\cos\hat{\theta} - \sin\theta\sin\hat{\theta}) + \frac{\beta+\gamma}{6}(\sin\theta\cos\hat{\theta} + \cos\theta\sin\hat{\theta})\right] \quad (24)$$

Under the assumption that the error $\delta = \theta - \hat{\theta}$ is very small and $\theta + \hat{\theta} \cong 2\theta$, (24) can be simply represented as

$$v_{de} \cong E_m\delta - E_m\left[\frac{\beta-\gamma}{2\sqrt{3}}\cos 2\theta + \frac{\beta+\gamma}{6}\sin 2\theta\right] \quad (25)$$

or

$$v_{de} \cong E_m\delta - E_m E_{\rm pu}\cos(2\theta + \phi_{\rm pu}) \quad (26)$$

where

$$E_{\rm pu} = \sqrt{\left(\frac{\beta-\gamma}{2\sqrt{3}}\right)^2 + \left(\frac{\beta+\gamma}{6}\right)^2},$$
$$\phi_{\rm pu} = -\tan^{-1}\left(\frac{1}{\sqrt{3}}\frac{\beta+\gamma}{\beta-\gamma}\right).$$

Since the d-axis voltage is controlled to zero by the PI type loop filter, the resultant error caused by the phase unbalancing is given as

$$\delta \cong E_{\rm pu}\cos(2\theta + \phi_{\rm pu}). \quad (27)$$

It is noted that the phase unbalancing produces the error with 2ω frequency component, where ω is the frequency of the utility voltage as $\omega = d\theta/dt$.

B. Voltage Harmonics

The source of the voltage harmonics can be considered as the nonlinearities of the measurement devices and nonlinear load such as the rectifier load. The utility voltage with harmonics can be represented as follows:

$$v_{as} = V_1\cos\theta + V_5\cos 5\theta + V_7\cos 7\theta + \cdots \quad (28)$$
$$v_{bs} = V_1\cos\left(\theta - \frac{2\pi}{3}\right) + V_5\cos 5\left(\theta - \frac{2\pi}{3}\right) + V_7\cos 7\left(\theta - \frac{2\pi}{3}\right) + \cdots \quad (29)$$
$$v_{cs} = V_1\cos\left(\theta + \frac{2\pi}{3}\right) + V_5\cos 5\left(\theta + \frac{2\pi}{3}\right) + V_7\cos 7\left(\theta + \frac{2\pi}{3}\right) + \cdots \quad (30)$$

where $V_1, V_5, V_7, \ldots$ denote the magnitude of the harmonic components. The stationary frame representations of (28) through (30) are given as

$$v_\alpha = V_1\cos\theta + V_5\cos 5\theta + V_7\cos 7\theta + \cdots \quad (31)$$
$$v_\beta = -V_1\sin\theta + V_5\cos 5\theta - V_7\cos 7\theta + \cdots \quad (32)$$

The d axis voltage can be derived by using (5) and the assumption of the small δ as

$$v_{de} = -V_1\sin\delta + V_5\sin(\hat{\theta} + 5\theta) + V_7\sin(\hat{\theta} - 7\theta) + \cdots \cong -V_1\delta + (V_5 - V_7)\sin 6\theta + (V_{11} - V_{13})\sin 12\theta + \cdots \quad (33)$$

Therefore, the error caused by the utility harmonics can be represented as

$$\delta = E_{h6}\sin 6\theta + E_{h12}\sin 12\theta + \cdots \quad (34)$$

where

$$E_{h6} = \frac{V_5 - V_7}{V_1}, \quad E_{h12} = \frac{V_{11} - V_{13}}{V_1}, \cdots.$$

It is noted in (34) that the utility harmonics causes the error with the frequency components of $6\omega, 12\omega, \ldots$, which is the multiples of six of the utility frequency.

C. Voltage Offset

The voltage offset is often produced by the offset of the signal measurement and conversion circuits. The utility voltage with the offset can be expressed as

$$v_{as} = V_m \cos\theta + V_{ao} \tag{35}$$

$$v_{bs} = V_m \cos\left(\theta - \frac{2\pi}{3}\right) + V_{bo} \tag{36}$$

$$v_{cs} = V_m \cos\left(\theta - \frac{2\pi}{3}\right) + V_{co}. \tag{37}$$

These voltages can be transformed using (3) as follows:

$$v_\alpha = V_m \cos\theta + V_{\alpha o} \tag{38}$$

$$v_\beta = V_m \cos\theta + V_{\beta o} \tag{39}$$

where

$$V_{\alpha o} = \frac{2}{3}(V_{ao} + V_{bo} + V_{co}), \quad V_{\beta o} = \frac{1}{\sqrt{3}}(V_{co} - V_{bo}).$$

The d-axis voltage in the synchronous frame can be represented using (5) and the assumption of small δ as

$$\begin{aligned} v_{de} &= -V_m \sin\delta + V_{\alpha o}\sin\hat{\theta} + V_{\beta o}\cos\hat{\theta} \\ &\cong E_m\delta + E_o\cos(\theta + \phi_o) \end{aligned} \tag{40}$$

where

$$E_o = \sqrt{V_{\alpha o}^2 + V_{\beta o}^2}, \quad \phi_o = -\tan^{-1}\left(\frac{V_{\alpha o}}{V_{\beta o}}\right).$$

Therefore, the error caused by the voltage offset can be shown as

$$\delta \cong E_{do}\cos(\theta + \phi_o) \tag{41}$$

where

$$E_{do} = -\frac{E_o}{E_m}.$$

It is shown in this result that the error caused by the offset has the same frequency component with that of the utility voltage.

V. Experiments

A. Implementation

Fig. 6 shows the experimental setup for the proposed three phase PLL system, which consists of the DSP TMS320C31 system with a clock frequency of 40 [MHz] and the arbitrary three phase voltage generator [8], [9]. The proposed PLL scheme is implemented in the software of the DSP and the sampling frequency is set as 15 [kHz]. The three phase voltages are measured by the isolation transformer and the measured signals are converted to digital ones using the analog-to-digital (A/D) converters with the resolution of 12 bits. The arbitrary voltage generator can produce various conditions of the utility voltage such as the phase unbalancing, harmonics, and offset, which can be used to test the performance of the PLL system.

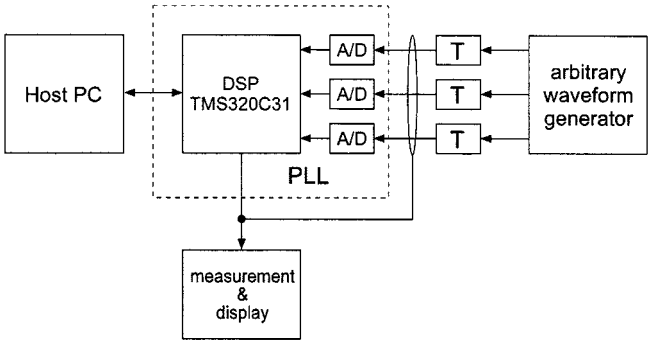

Fig. 6. Experimental steup for theree phase PLL system.

B. Experimental Results and Discussions

Fig. 7 shows the responses of the proposed PLL system when the closed loop bandwidth are chosen as 50 [Hz], 100 [Hz], and 1 [kHz], i.e. $\omega_n = 314, 628$, and 6280 [rad/sec], respectively, where the damping ratio is chosen as $\zeta = 0.707$ and the peak of the utility voltage V_m is 311 [V]. Under these conditions, the gains of the loop filter are given as $K_p = 1.43, 2.85$, and 28.5, and $\tau = 0.004\,506, 0.002\,247$, and $0.000\,225\,1$, respectively. It is shown in Fig. 7 that the higher bandwidth gives the faster dynamic response.

Fig. 8 shows the PLL errors under the phase unbalancing of the utility voltage. The voltages of the phases b and c are given as 90% and 110% of the phase a. As derived in (27), it is shown that the errors caused the phase unbalancing have 2ω frequency component. It can be also noted in this figure that the magnitude of the error is reduced as the bandwidth decreases. The error in 50 [Hz] bandwidth is about 50% of that in 1 [kHz] bandwidth. This is the low pass filtering effect of the loop filter and it is known that the lower bandwidth is more effective to reduce the error caused by the phase unbalancing.

The responses of the PLL system under the voltage harmonics are shown in Figs. 9 and 10, where the fifth and seventh harmonics are given as 5% and 3% of the fundamental voltage, respectively. Figs. 9 and 10 show the time responses and frequency spectrums, respectively. It is shown in Fig. 9 that error has the frequency component of 6ω as shown in (34). The low pass filtering effect is also shown and thus the magnitude of the error decreases as the bandwidth decreases. Fig. 10 shows the frequency spectrums of the utility voltage and $\cos\hat{\theta}$ using the PLL output. It is noted that the fifth and seventh harmonics are reduced as the bandwidth decreases.

Fig. 11 shows the responses of the PLL under the voltage offset. The dc voltage, which is 10% of the peak utility voltage, is added to the phase a. It is shown in this figure that the error has the same frequency component with that of the utility voltage as shown in (41). Since the frequency of the error is relatively low, the low pass filtering effect of the loop filter can not be expected. The extremely low bandwidth can provide the filtering effect. However, this degrades the dynamic performance.

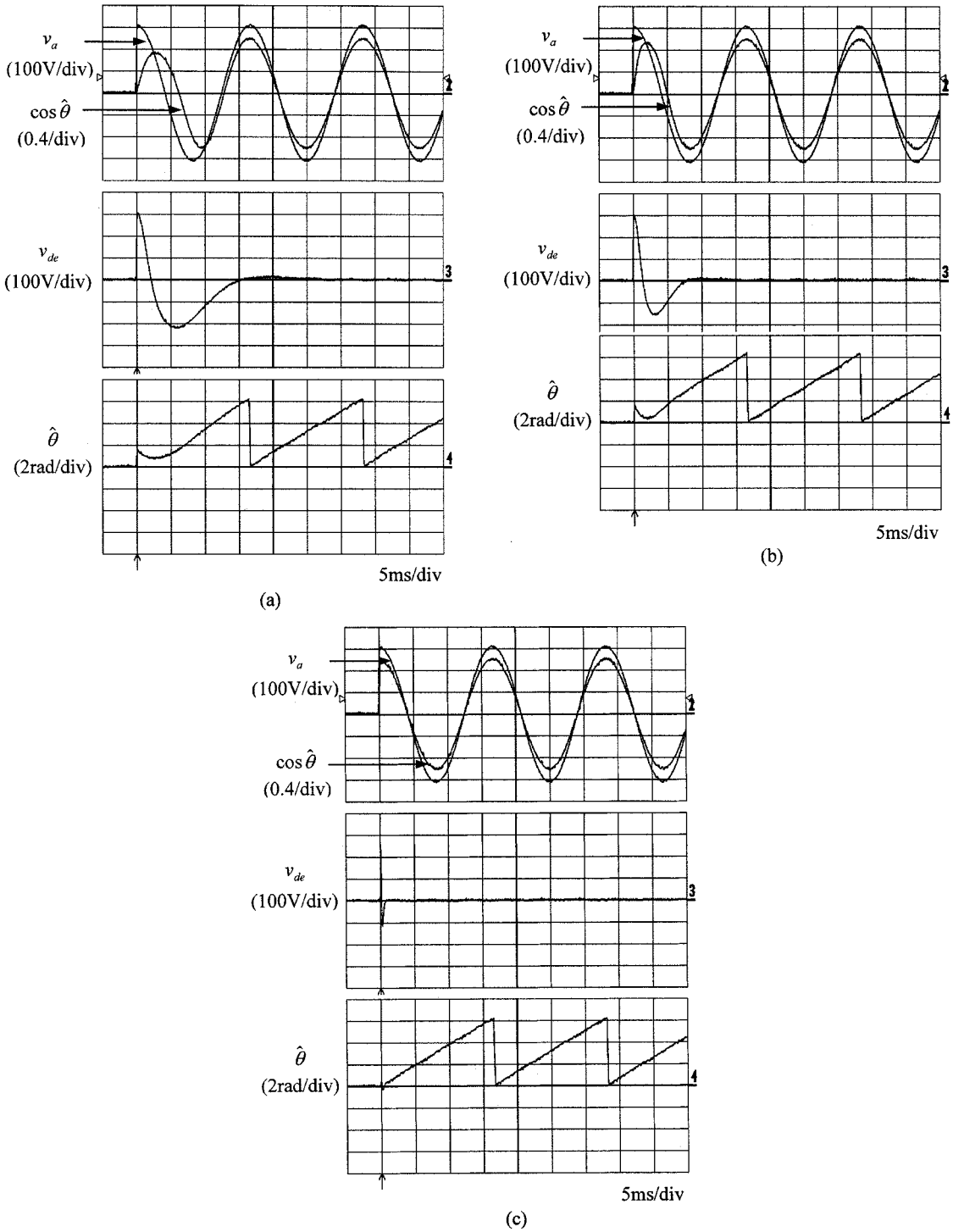

Fig. 7. Resposens of three phase PLL system ($v_a = V_m \cos\theta, V_m = 311$ V). (a) $\omega_n = 314$ rad/sec, $\zeta = 0.707$. (b) $\omega = 628$ rad/sec, $\zeta = 0.707$. (c) $\omega_n = 6280$ rad/sec, $\zeta = 0.707$.

VI. Conclusion

The analysis and design of the three phase PLL system for the utility interface inverter have been presented in this paper. The dynamic modeling, characteristics, and optimization of the three phase PLL system have been discussed. Particularly, the errors caused by the distorted utility voltage have been analyzed. From the analytic and experimental studies, the design considerations of the three phase PLL system can be deduced.

The PLL system consists of two major parts, the phase detecting devices and loop filter. The phase detecting can be readily implemented by using the dq transform in the three phase system without additional phase detecting devices. The design parameters of the loop filter are the damping ratio ζ and the natural frequency ω_n, which determines the dynamic characteristics. The damping ratio can be chosen by the Wiener method that has been generally accepted as the best optimiza-

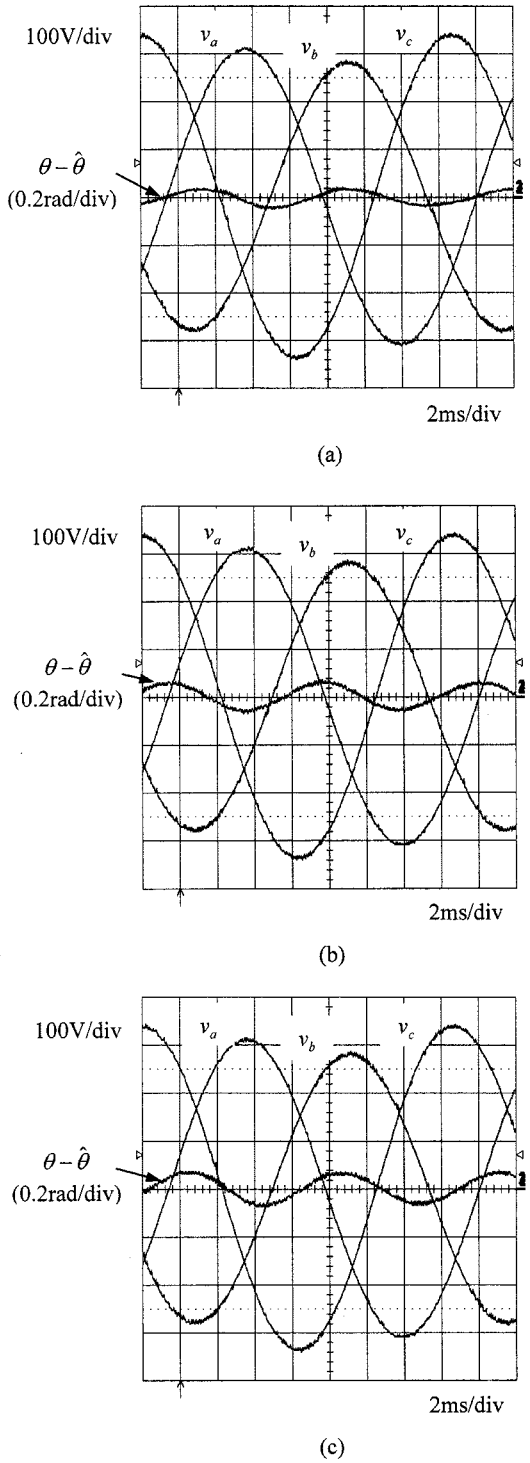

Fig. 8. Errors of three phase PLL system under phase unbalancing ($v_a = V_m \cos\theta, V_m = 311$ V). (a) $\omega_n = 314$ rad/sec, $\zeta = 0.707$. (b) $\omega_n = 628$ rad/sec, $\zeta = 0.707$. (c) $\omega_n = 6280$ rad/sec, $\zeta = 0.707$.

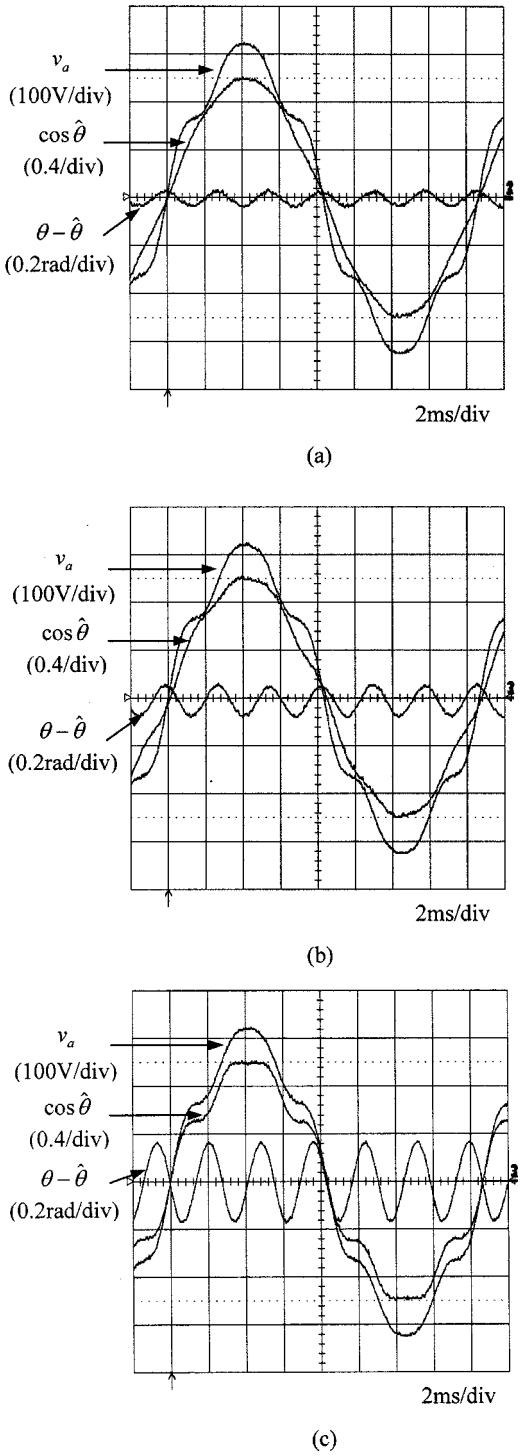

Fig. 9. Errors of three phase PLL system under voltage harmonics ($v_a = V_m \cos\theta, V_m = 311$ V). (a) $\omega_n = 314$ rad/sec, $\zeta = 0.707$. (b) $\omega_n = 628$ rad/sec, $\zeta = 0.707$. (c) $\omega_n = 6280$ rad/sec, $\zeta = 0.707$.

tion. The bandwidth of the loop filter is a trade-off between the filtering characteristics and fast responses. While the higher bandwidth ensures the faster dynamic responses, the tracking error is increased under the distorted utility conditions. The errors caused by the phase unbalancing and harmonics have the frequency components of 2ω and multiples of 6ω, respectively, and can be considerably reduced by using the loop filter with the low bandwidth. The errors caused by the voltage offset are the same frequency with that of the utility voltage. In order to reduce this error by the loop filter, the extremely low bandwidth is required. However, this degrades the dynamic performance and is not acceptable.

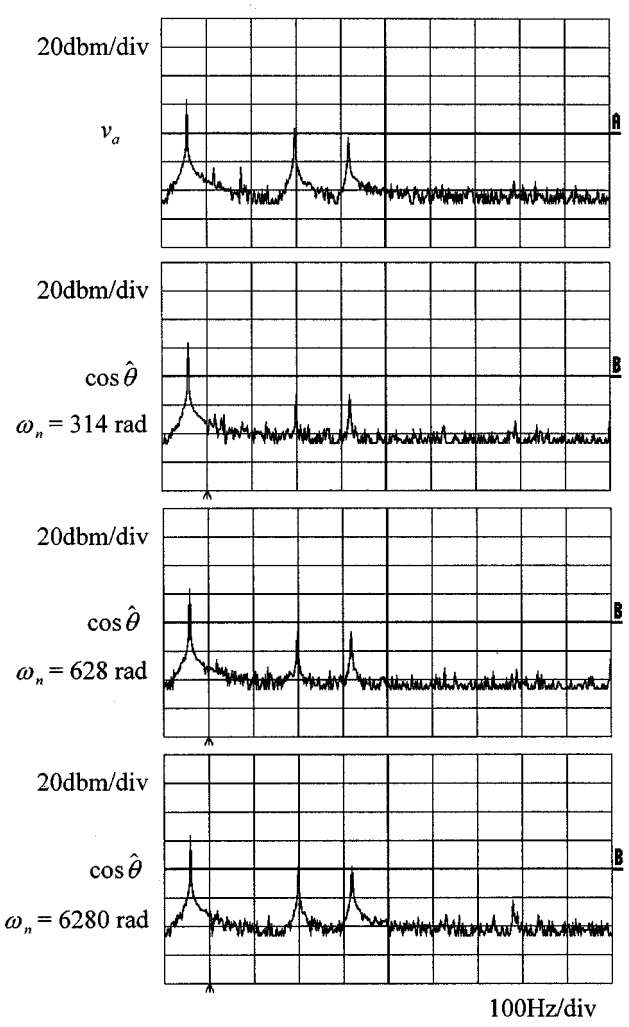

Fig. 10. Frequency spectrums of utility voltage and $\cos\hat{\theta}$ under utility harmonics for various bandwidths.

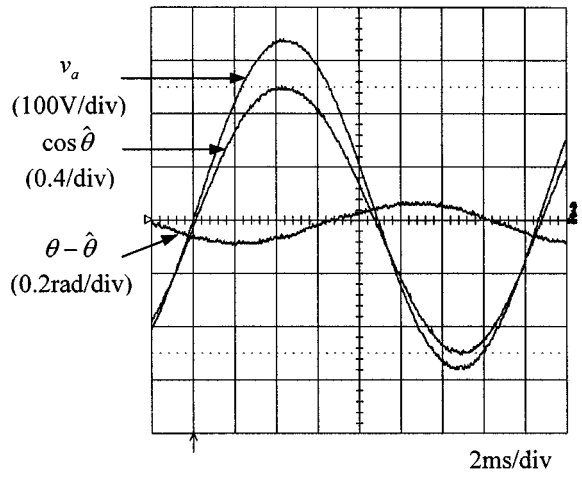

Fig. 11. Errors of three phase PLL system under voltage offset ($v_a = V_m \cos\theta, V_m = 311$ V, $\omega_n = 314$ rad/sec, $\zeta = 0.707$).

Consequently, the errors caused by the phase unbalancing and harmonics can be reduced by the appropriate design of the loop filter and the bandwidth is a compromise between the filtering performance and fast response. For more efficient filtering characteristics, the high order PLL system can be considered. Since the error caused by offset can not be handled in the loop filter, it should be eliminated in the stage of the voltage measurement and phase detection.

In order to more improve the PLL performance under the distorted utility conditions, several techniques will be considered such as the high order PLL and adaptive cancellation techniques. These are being considered as further works.

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