Performance Analysis of Reduced Common-Mode Voltage PWM Methods and Comparison With Standard PWM Methods for Three-Phase Voltage-Source Inverters

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Abstract—This paper surveys the reduced common-mode voltage pulsewidth modulation (RCMV-PWM) methods for three-phase voltage-source inverters, investigates their performance characteristics, and provides a comparison with the standard PWM methods. PWM methods are reviewed, and their pulse patterns and common-mode voltage (CMV) patterns are illustrated. The inverter input and output current ripple characteristics and output voltage linearity characteristics of each PWM method are thoroughly investigated by analytical methods, simulations, and experiments. The research results illustrate the advantages and disadvantages of the considered methods, and suggest the utilization of the near-state PWM and active zero state PWM1 methods as overall superior methods. The paper aids in the selection and application of appropriate PWM methods in inverter drives with low CMV requirements.

Index Terms—Common-mode voltage (CMV), harmonics, inverter, pulsewidth modulation (PWM), three phases.

I. INTRODUCTION

THREE-PHASE voltage-source inverters (VSIs) are widely utilized to drive ac motors with high-motion-control quality and energy efficiency. Pulsewidth modulation (PWM) is the standard approach to operate the inverter switches in order to generate the required high-quality output voltages. Conventional continuous PWM (CPWM) methods, such as space vector PWM (SVPWM) [1], and discontinuous PWM (DPWM) methods, such as DPWM1 [2], perform satisfactorily in terms of voltage linearity, output current ripple, dc-bus current ripple, and average switching frequency requirements [3], [4]. However, they have poor common-mode voltage (CMV) characteristics leading to prohibitive amount of common-mode current (CMC, leakage current) in ac motors.

In the standard three-phase two-level VSI with diode rectifier front-end, which is shown in Fig. 1, the CMV is defined as the potential of the star point of the load with respect to the power line ground (v_{ng}) . With $v_{ng} = v_{no} + v_{og}$ and v_{og} being much smaller and slowly varying signal compared to v_{no} , the

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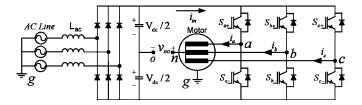


Fig. 1. Three-phase inverter drive with diode rectifier front-end.

 v_{og} term can be neglected. Therefore, the CMV of the inverter is defined as the load star point to the center of the dc-bus of the VSI $(v_{no}$ in Fig. 1) potential and can be expressed as follows:

$$v_{no} = \frac{v_{ao} + v_{bo} + v_{co}}{3}. (1)$$

Since the VSI cannot provide purely sinusoidal voltages and has discrete output voltages synthesized from the fixed dc-bus voltage $V_{
m dc}$, the CMV is always different from zero and may take the values of $\pm V_{\rm dc}/6$ or $\pm V_{\rm dc}/2$, depending on the inverter switch states selected. During switch state changes, the CMV changes by $\pm V_{\rm dc}/3$, regardless of the changing states. All conventional CPWM and DPWM methods exhibit high CMV and CMC characteristics that pose problems in the application field. At switching frequencies above several kilohertz, switching times of several hundred nanoseconds or less, and $V_{\rm dc}$ levels above several hundred volts, excessive CMV with sharp edges can result in high CMC. In motor drive applications, this may lead to motor bearing failures, electromagnetic interference noise that causes nuisance trip of the inverter drive, or interference with other electronic equipment in the vicinity. In the application field, such problems have increased recently due to increasing PWM frequencies and faster switching times (aimed for higher efficiency, control bandwidth, smaller ripple, filter size, etc.) [5]-[7], and CMV reduction techniques have gained importance.

Passive [8]–[11] or active [12] filters can be utilized to suppress the effect of the CMV of the two-level inverter. Also, a three-level inverter [13], [14] could be employed to decrease the CMV from the source. However, all these methods involve external/additional hardware, and thus, they significantly increase the drive cost and complexity. An alternative approach is to modify the PWM pulse pattern of the classical two-level

inverter such that the CMV is substantially reduced from its source and its effects are mitigated at no cost.

In the literature, various PWM pulse-pattern-modificationbased CMV reduction methods have been reported. To be classified as reduced CMV PWM (RCMV-PWM) methods, these include the recently reported AZSPWM1 [15]-[17], RSPWM [18], AZSPWM2 [19]-[21], AZSPWM3 [15], and NSPWM [22], [23] methods as the most successful representatives (these acronyms are given by the authors and will be expanded in the next section). The theoretical CMV and PWM ripple performance investigation of all these methods shows that the maximum CMV is successfully reduced in all these methods from $\pm V_{\rm dc}/2$ of the conventional PWM methods to $\pm V_{\rm dc}/6$. In some of these methods, the theoretically low CMV values cannot be realized practically due to some constraints, which will be later discussed in the paper. Furthermore, the performance of a PWM method is not based only on the CMV characteristic. The main modulator characteristics, such as the PWM output current ripple, the dc-link current ripple, the fundamental component voltage linearity, the switching loss, the pulse reversal behavior, etc., must also be taken into account when considering a PWM method for an application. With such considerations, the feasibility of these new methods should be evaluated further. While the main modulator characteristics of the conventional CPWM and DPWM methods [such as sinusoidal PWM (SPWM), SVPWM, and DPWM1 (center $2 \times 60^{\circ}$ bus-clamped modulation waves)] are well known [3], [4], the characteristics of RCMV-PWM method are neither well explored nor there is a comparative study among the RCMV-PWM methods (also between the conventional and RCMV-PWM methods). Since each PWM method has unique performance characteristics, these characteristics are not easy to obtain. Thus, the modulator choice currently appears as a difficult task, and the advantages and the disadvantages of these methods have not been clearly illustrated as a whole. Therefore, it is necessary to quantify the performance characteristics (ripple current, linearity, etc.) of the recently developed RCMV-PWM methods. Furthermore, a comparison with the standard PWM techniques is required for evaluation of feasibility.

This paper first reviews the important RCMV-PWM methods. The switch logic signal, CMV, and output voltage pulse patterns over a PWM cycle are illustrated and discussed. Then, performance characteristics of the RCMV-PWM method are thoroughly investigated via analytical and numerical methods. The output current ripple, the dc-link current ripple, and voltage linearity characteristics are obtained and compared to those of the conventional methods. The analytical results are confirmed by computer simulations and laboratory experiments. Considering practical conditions involving inverter deadtimes, unidentical switch dynamic characteristics, propagation delays, parasitic circuit components, and implementation constraints, the feasibility of the RCMV-PWM methods is evaluated. Therefore, a guideline is established regarding the choice of a PWM method for an application when taking the CMV characteristics into account.

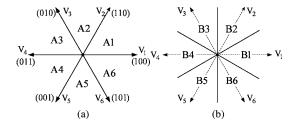


Fig. 2. Voltage space vectors and the definitions of A- and B-type regions.

II. SWITCH LOGIC SIGNAL, OUTPUT VOLTAGE, AND CMV PATTERNS FOR VARIOUS PWM METHODS

This section involves the review of PWM methods and their voltage patterns. The performance characteristics of a PWM method are primarily dependent on the modulation index M_i (voltage utilization level) that is defined as follows [3]:

$$M_i = \frac{V_{1\text{m}}}{V_{1\text{m 6-step}}} \tag{2}$$

where $V_{\rm 1m~6-step}=2V_{\rm dc}/\pi$ and $V_{\rm 1m}$ is the magnitude of the phase-voltage fundamental component.

Based on the implementation technique, PWM methods are defined as scalar or space vector techniques. In the scalar approach, a modulation wave is compared with a triangular carrier wave, and the intersections define the switching instants. The injection of a zero-sequence signal makes each PWM method unique in terms of performance attributes [3], [4]. In the space vector approach, the reference and inverter voltages are transformed to vectors by the following complex variable transformation:

$$V = \frac{2}{3}(V_a + aV_b + a^2V_c)$$
 (3)

where $a=e^{j2\pi/3}$ is the phase-shift operator. The vector transformation yields six active and two zero vectors for the inverter, and as shown in Fig. 2(a), the vectors divide the space into six segments. These regions are utilized in programming the PWM pulses. In some cases, 30° phase-shifted regions, as defined in Fig. 2(b), are utilized. In the space vector approach, the duty cycles of the voltage vectors are calculated according to the vector volt-seconds balance rule. The voltage vectors and their sequences are selected based on a specified performance criterion such as the minimum output voltage ripple and switching count, and the vectors are programmed accordingly.

Many high-performance scalar PWM methods have an equivalent space vector implementation. Scalar methods are more favorable for implementation (both digital and analog) while vector methods are more attractive for pulse pattern study and performance analysis. Based on the modulation signal or switch duty cycle function shapes, conventional PWM methods are classified as the CPWM (SVPWM, SPWM, etc.) method and the DPWM (DPWM1, 2, etc.) method. The pulse pattern of the CPWM and DPWM methods involves utilization of at least one of the two zero-voltage vectors V_0 and V_7 during each PWM cycle. The switch pulse pattern of the classical SVPWM method $(t_0 = t_7)$ in A1 [Fig. 2(a)] is shown in Fig. 3. In DPWM, one

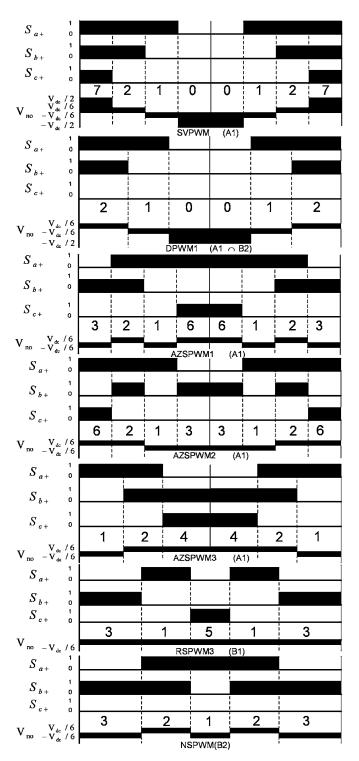


Fig. 3. Inverter switch state and CMV pulse patterns of various PWM methods.

of the zero states is eliminated and one switch is retained in a fixed state for a full PWM cycle. For example, in DPWM1, over every 60° segment in space every PWM cycle, one phase is locked to the positive or negative dc rail, yielding a total of 120° lockout of the switching signals for each leg. As shown in Fig. 3, for all CPWM and DPWM methods, regardless of the scalar or vector implementation techniques, such pulse patterns yield high CMV $(\pm V_{\rm dc}/2)$.

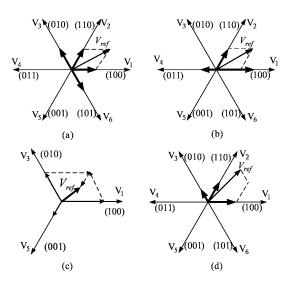


Fig. 4. Voltage space vectors. (a) AZSPWM1–2. (b) AZSPWM3. (c) RSPWM. (d) NSPWM.

Recently, several PWM methods that yield reduced CMV have been reported [15]–[23]. Of these methods, active zero state PWM1 (AZSPWM1) [15]–[17], AZSPWM2 [19]–[21], AZSPWM3 [15], remote-state PWM (RSPWM) [18], and near-state PWM (NSPWM) [22], [23] deserve dedicated attention and will be investigated in detail in this paper. The pulse patterns and the resulting CMVs for specific regions of the vector space (according to Fig. 2) for these methods are shown in Fig. 3. As shown in the figure, in these RCMV-PWM methods, the inverter zero states are avoided and low CMVs result ($\pm V_{\rm dc}/6$). Since the space vector illustration is intuitive, all these methods will be described using this approach.

The conventional CPWM and DPWM methods utilize the inverter voltage vectors that are adjacent to the reference voltage vector and at least one of the two inverter zero states (V_0 and V_7) to generate output volt-seconds that match the reference volt-seconds. The RCMV-PWM methods utilize only the active voltage vectors (avoid the zero states/vectors). Depending on the choice of the voltage vectors, various RCMV-PWM methods exist. In the AZSPWM methods, the classical active (adjacent) voltage vectors are complemented with either two near opposing active vectors (AZSPWM1, AZSPWM2) or one of the adjacent states and its opposite vector (AZSPWM3) with equal time to effectively create a zero-voltage vector. The RSPWM methods synthesize the output voltage from three inverter voltage vectors that are 120° apart from each other (most remote vectors). The NSPWM method utilizes a group of three neighbor voltage vectors to match the output and reference volt-seconds. These three voltage vectors are selected such that the voltage vector closest to reference voltage vector and its two neighbors (to the right and left) are utilized. The formation of each method discussed is illustrated in Fig. 4.

In each PWM method, with a specific performance optimization criterion, the voltage vectors are selected, and their sequences depend on the region of the reference voltage vectors defined in Fig. 2(a) and (b). The utilized voltage vectors and

		A 1		A	2	A	13	_ 4	1 4		A5		A6	
CPWM	72	210127	7	7230	327	743)347	745	0547	76	50567	76	10167	
AZSPWM1	1	321612	23	4321	234	543	2345	654	13456	16	5456	1 21	65612	
AZSPWM2	6213126		26	1324231		2435342		3546453		4651564		4 51	62615	
AZSPWM3	12421			23532		34643		45154		56265		6	1316	
RSPWM1	31513		;	31513		31513		31513		31513		3	31513	
RSPWM2A	31513		3	13531		13531		15351		15351		3	31513	
RSPWM2B	42624		1	42624		24642		24642		26462		2	26462	
		B1		В	2	F	33]	34	B5			B6	
RSPWM3	31513		3	42624		13531		24642		15351		26462		
NSPWM	21612		2	32123		43234		54345		65456		1	16561	
	B1	A1	B2	A2	В3	A3	B4	A4	B5	A5	В6	A6	B1	
DPWM1	72127		2:	23032 74		1347	347 450		54 765		67 61			
		210)12	72	327	43	034	745	47	650)56	761	67	

TABLE I
REGION-DEPENDENT PULSE (VECTOR) PATTERNS OF VARIOUS PWM METHODS

their sequences for the conventional and RCMV-PWM methods are given in Table I. As shown in the table, in the conventional CPWM and DPWM methods, two adjacent states with two or one zero-voltage vectors, respectively, are utilized to program the output voltage. Every 60° , the active voltage vectors change, but the zero states and their locations are retained. For example, in region A1, the pattern of CPWM is 7210127 and that of DPWM is 72127 in A1 \cap B1 (A1 and B1 intersection) and 21012 in A1 \cap B2.

In the AZSPWM methods, the choice of active voltage vectors is the same as in CPWM. However, instead of the real zerovoltage vectors $(V_0 \text{ and } V_7)$, two active opposite voltage vectors with equal duration are utilized. Here, various choices exist. For AZSPWM, any of the pairs V_1V_4 , V_2V_5 , or V_3V_6 can be utilized. In AZSPWM1 and AZSPWM2, for each region (A1–A6), of the three pairs, the adjacent pair is utilized. For example, in A1, the V_3V_6 pair is utilized since these vectors are adjacent to the active vectors V_1V_2 . The sequence of the active zero vectors (in this example, V_3 and V_6) defines the two types of the AZSPWM methods. AZSPWM1 involves only 60° jumping vectors. For example, as shown in Table I, in A1, the sequence 3216123 is utilized and results in 60° output-voltage-vector rotation during every commutation. AZSPWM2 utilizes the sequence 6213126, and it results in 120° jumps in the output voltage vectors during commutation from the active vectors $(V_1 \text{ and } V_2)$ to the active zero vectors (V_3 and V_6). In AZSPWM3, the active zero vectors are formed by utilizing one of the adjacent voltage vectors and its opposite vector. In A1, the V_1V_2 active states are complemented with the V_1V_4 (alternatively with V_2V_5) active zero set. Thus, only three voltage vectors $V_1V_2V_4$ are utilized to program the output voltage. The pulse pattern of this method is given in Table I.

RSPWM methods utilize the vector group $V_1V_3V_5$ and/or $V_2V_4V_6$ in various sequences. Various pulse patterns can be generated. RSPWM1 utilizes only one vector group and applies the vectors in a fixed sequence throughout the voltage vector space. Thus, there exist three pulse patterns per group, yielding a total of six pulse patterns. In Table I, one of the six patterns is displayed. In RSPWM2, only one group is utilized throughout the vector space. However, in this case, a variable sequence is selected. With the output-voltage-distortion mini-

mization being the performance criterion, the sequence is varied in a specific manner. Two patterns yielding relatively good voltage quality performance are displayed in Table I (RSPWM2A, RSPWM2B). RSPWM3 utilizes both vector groups (alternates each group every 60°) and also applies the variable sequence, as shown in Table I, according to the region definitions of Fig. 2(b) [19].

NSPWM employs only three neighbor voltage vectors and sequences them in the order that the minimum switching count is obtained. Thus, one of the phases is not switched within each PWM cycle. The resulting vector sequence is shown in Table I. For example, for the region between 30° and 90° [B2 in Fig. 2(b)], the applied voltage vectors are V_1 , V_2 , and V_3 [Fig. 4(d)] with the sequence $V_3V_2V_1V_2V_3$. As a result, the PWM pulse pattern of the method in B2 becomes as shown in Fig. 3. Notice that phase "c" is not switched within this cycle (thus, over B2).

Investigating the voltage vectors of NSPWM and RSPWM, the relationship between these two methods can be seen clearly. In B2 (which is included in the union of A1 and A2), RSPWM2A utilizes V_1 , V_3 , and V_5 while NSPWM utilizes V_1 , V_2 , and V_3 . At low M_i , NSPWM yields negative vector duty cycle for V_2 that cannot be realized. However, utilizing the V_5 vector instead of V_2 results in a positive vector duty cycle, which defines RSPWM2A. Therefore, NSPWM and RSPWM2 complement each other such that an overall mathematically feasible solution is obtained in the whole vector space.

With the pulse patterns shown in Table I applied, the RCMV-PWM methods yield a low CMV magnitude of $V_{\rm dc}/6$, as illustrated in Fig. 3. The frequency and polarity of CMV of each RCMV-PWM method is unique. In methods such as RSPWM1 and RSPWM2, not only the CMV magnitude is low, but its frequency is also zero, implying no CMV variation, which is the most favorable feature. In RSPWM3, the CMV is constant every 60° in space. In AZSPWM2 and AZSPWM3, the CMV varies at the PWM frequency. In all other discussed methods, the CMV frequency and number of steps are higher, thus less attractive. However, the theoretical investigation is alluring.

Careful observation of Fig. 3 reveals that SVPWM, DPWM1, AZSPWM1, and NSPWM have one switching at a time, while all other methods involve simultaneous switching of two inverter legs. In practice, it is almost impossible to switch two inverter legs simultaneously (due to unidentical electronic and power hardware in each phase and also the existence of inverter deadtime). Even if this becomes possible, the simultaneous switching is prohibited for the reason that an instantaneous line-to-line voltage reversal results in significant overvoltages at the motor terminals (in particular, in long cable applications, where cable capacitance is large). Thus, in the mentioned methods, if the switching is simultaneous, significant motor overvoltages are created, and if the switching is not simultaneous, additional inverter zero states, which yield high-CMV pulses with short duration (most harmful in terms of noise), may be created. As a result, it becomes obvious that except for AZSPWM1 and NSPWM, the RCMV-PWM methods are prohibitive. Even AZSPWM1, at some operating conditions, exhibits instantaneous line-toline voltage polarity reversal [22], [23], but this problem is

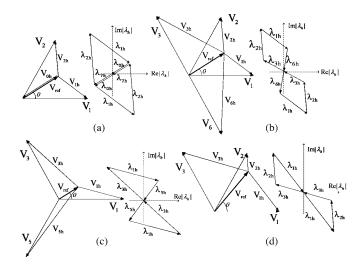


Fig. 5. (Left) harmonic voltage and (right) flux vectors of various PWM methods. (a) SVPWM. (b) AZSPWM1. (c) RSPWM. (d) NSPWM.

solved with a small patch to the PWM algorithm [19], [24]. The problems of the other methods are difficult to cure, and the reader is cautioned on their overvoltages and CMV exacerbation. Therefore, discussion on these methods will be continued for the sake of completeness.

In a PWM method, the choice of the voltage vectors, along with their sequence and duty cycles, defines the waveform quality of the inverter's output phase voltages and phase currents. The inverter dc-link current and the output voltage linearity are also affected. The detailed performance characteristics study of the output voltage, dc-link current, and voltage linearity follows.

III. HARMONIC DISTORTION FACTOR (HDF)

The inverter output voltage waveform quality can be best studied with the aid of space vectors. A three-phase inverter can generate eight different voltage vectors [Fig. 2(a)]. Since the reference voltage vector is fixed over a PWM cycle, the difference between the reference and the inverter output voltage vector is the harmonic voltage vector (Fig. 5) that creates the inverter output current ripple. The current ripple has undesirable effects such as torque ripple and harmonic losses. With the typical ac motor switching frequency model being an inductance, the harmonic voltage integral (harmonic flux [3]) is proportional to the harmonic current. Defined in the following, the harmonic flux over an arbitrary cycle (Nth cycle) is a measure of the ripple current for each PWM method:

$$\lambda_h(M_i, \theta, V_{dc}) = \int_{NT}^{(N+1)T} (V_k - V^*) dt.$$
 (4)

Normalizing λ_h in (5), the harmonic performance can be comparatively evaluated for various modulation methods [3]

$$\lambda_{hn} = \frac{\pi}{V_{\text{dc}}T}\lambda_h. \tag{5}$$

Since each PWM method differs in the utilization of the voltage vectors and their sequence, the harmonic flux vector of each PWM method is unique. For example, the SVPWM voltage

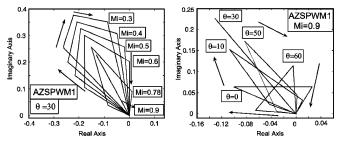


Fig. 6. Parametric harmonic flux trajectories of AZSPWM1.

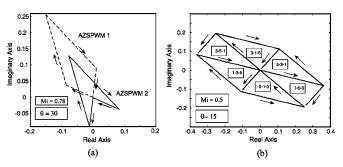


Fig. 7. Voltage vector sequence dependency of harmonic flux trajectories for (a) AZSPWM and (b) RSPWM.

vector sequence in sector A1 is $V_7V_2V_1V_0V_1V_2V_7$ and results in the two-symmetric-triangles harmonic flux trajectory shown in Fig. 5(a). In the same sector, the trajectories of AZSPWM1 are of double-diamond shape [Fig. 5(b)]. All the RSPWM trajectories resemble the butterfly shape [Fig. 5(c)]. NSPWM trajectories also have butterfly wings shape but with different wing dimensions [Fig. 5(d)]. Not shown here, the AZSPWM2 trajectories are of a double-arrowhead shape [19].

The harmonic flux trajectories of each PWM method vary depending on the angle and magnitude of the reference voltage vector. The trajectories of the standard PWM methods such as SVPWM and DPWM were reported in [3]. Here, the RCMV-PWM trajectories will be evaluated. It is shown in Fig. 6 that the AZSPWM1 trajectories are strongly dependent on θ and M_i . For constant θ , the harmonic flux vector magnitude (thus, the current ripple) increases with decreasing M_i . For constant M_i , the harmonic flux becomes maximum at $\theta = 30^{\circ}$. Not shown in the graphic, in AZSPWM2, the M_i dependency is similar to AZSPWM1, while the θ dependency is variant and complex. A comparison between AZSPWM1 and AZSPWM2 (at $M_i = 0.78$ and $\theta = 30^{\circ}$) reveals the superiority of the latter. As shown in Fig. 7(a), while the AZSPWM2 harmonic flux vector is centered around the origin, the AZSPWM1 vector is quite distant from it. In RSPWM, various sequences (Table I) with unique harmonic flux trajectories are possible. For RSPWM1 and the $V_1V_3V_5$ set, of the available three sequences, as shown in Fig. 7(b), the 315–513 sequence is closer to the origin, yielding less harmonic flux than the other sequences. The M_i and θ dependency of its harmonic flux is shown in Fig. 8. The harmonic flux magnitude decreases with increasing M_i and decreasing θ . In NSPWM, for constant θ , as M_i increases, the harmonic flux trajectories get noticeably narrower (Fig. 9). However, the θ dependency is not strong. Although the shapes of harmonic flux

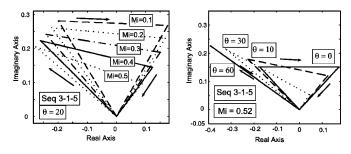


Fig. 8. Harmonic flux trajectories for the 315-513 sequence of RSPWM1.

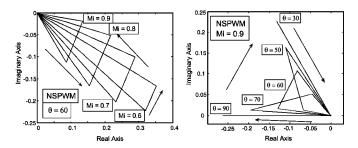


Fig. 9. Parametric harmonic flux trajectories of NSPWM.

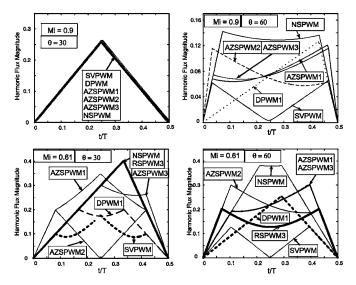


Fig. 10. Normalized harmonic flux magnitudes of PWM methods.

trajectories are different for different θ -values, all have similar sizes.

In order to clearly show the harmonic content, the magnitude of the harmonic flux vector is illustrated over a half PWM cycle with the time axis normalized to T_s in Fig. 10 for various PWM methods and operating points at $M_i=0.61$ and $M_i=0.9$ for two different θ -values, $\theta=30^\circ$ and $\theta=60^\circ$. The curves are obtained for the same carrier frequency. The area under the harmonic flux magnitude curve is proportional to the harmonic content [19]. For $M_i=0.9$ and $\theta=30^\circ$, all methods utilize only V_1 and V_2 with the same duty cycles, resulting in the same harmonic flux vector magnitudes. When migrating from this operating point, the characteristics begin to differ. In general, SVPWM has the least harmonic flux while NSPWM has the largest. However, in this evaluation, the switching count

 $\begin{tabular}{ll} TABLE II \\ Number of Commutations Per Cycle and K_f \\ \end{tabular}$

	# Commutations	$K_{\rm f}$
CPWM & AZSPWM1 -3	6	1
DPWM	4	2/3
NSPWM	4	2/3
RSPWM	8	4/3
AZSPWM2	10	5/3

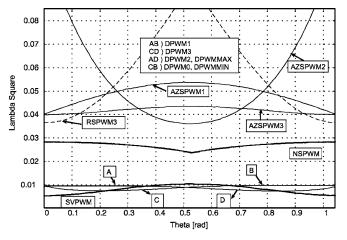


Fig. 11. $\lambda^2 = f(\theta)$ spatial variation for $M_i = 0.61$.

is not considered. For fair comparison, in order to obtain the same number of commutations (per fundamental cycle) in each method, the switching (carrier) frequency of each method must be divided by K_f , which is shown in Table II. Thus, the harmonic voltage/flux quantities are scaled with the K_f factor.

Considering K_f , the harmonic flux curves of Fig. 10 should be scaled with K_f . Evaluation based on this criteria favors NSPWM as its performance becomes better than AZSPWM and RSPWM methods, especially at high M_i .

The normalized harmonic flux vector rms value over a PWM cycle (duty cycle δ of 0–1) is calculated as follows [3]:

$$\lambda_{hn-\text{rms}}(M_i,\theta) = \sqrt{\int_0^1 \lambda_{hn}^2 \, d\delta}.$$
 (6)

The rms harmonic flux can be analytically or numerically calculated over a PWM cycle via computational software. Due to the complexity of the switch pulse patterns, the calculations of the RCMV-PWM methods have been carried numerically via MATLAB [26], and for the integration, the Euler method has been used. Over a PWM cycle, 1000 data points are utilized in order to obtain accurate results. The rms value of the harmonic flux is calculated for various PWM methods for $M_i = 0.61$ (low M_i) and $M_i = 0.9$ (high M_i). The square-rms harmonic flux is scaled with K_f^2 for fair comparison. Figs. 11 and 12 illustrate that the square of the rms value of the harmonic flux is strongly dependent on θ . At low M_i ($M_i = 0.61$), CPWM methods provide the lowest harmonic flux square-rms. DPWM methods have larger value. The RCMV-PWM methods have significantly higher distortion than these methods. NSPWM is the closest to the standard methods. AZSPWM1 and AZSPWM3

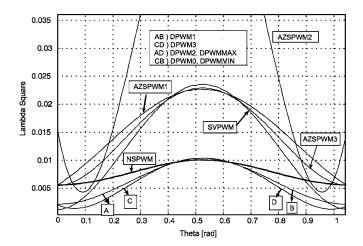


Fig. 12. $\lambda^2 = f(\theta)$ spatial variation for $M_i = 0.9$.

are very similar to each other and have significantly less distortion than the remaining RCMV-PWM methods. At high M_i ($M_i=0.9$), as Fig. 12 illustrates, NSPWM and DPWM methods exhibit the best performance. SVPWM, AZSPWM1, and AZSPWM3 have similar distortion, which is much higher. AZSPWM2 has the worst distortion.

Taking the average value of the local square-rms harmonic flux function over the full fundamental cycle (spanning the whole vector space) and scaling it with $288/\pi^2$, the harmonic distortion factor (HDF), which is a true measure of ac current ripple rms value, can be calculated by [3]

$$HDF = f(M_i) = \frac{288}{\pi^2} \frac{1}{2\pi} \int_0^{2\pi} \lambda_{hn-\text{rms}}^2 d\theta.$$
 (7)

HDF is only M_i -dependent, and each PWM method has a unique HDF characteristic. It can be calculated analytically or numerically. Due to the complexity of the switch pulse patterns, the calculations of the RCMV-PWM methods are performed numerically via MATLAB. The integral is calculated with the Euler method, and the vector space is spanned with 628 data points for accurate results. In the HDF calculation, K_f is taken into account (as in Table II).

As shown in Fig. 13, HDF of each method is unique. Over the full linear modulation range, the CPWM and DPWM methods provide lower HDF than the RCMV-PWM methods. Near zero M_i , the difference is in orders of magnitude. However, as M_i increases, the differences rapidly decrease. Throughout its linearity range, NSPWM has the least harmonic distortion among all RCMV-PWM methods, and at high M_i , it approaches those of DPWM methods. At low M_i , among the RCMV-PWM methods, AZSPWM1, AZSPWM3, and RSPWM3 are similar to each other and provide less HDF than the remaining RCMV-PWM methods.

IV. DC-LINK CURRENT HARMONICS

The dc-link current of the inverter $i_{\rm in}$ (Fig. 1) is important for dc-bus capacitor sizing as the capacitor suppresses all the PWM ripple current. The dc-link current ripple of each PWM method is unique, and for each method, it is a function of M_i

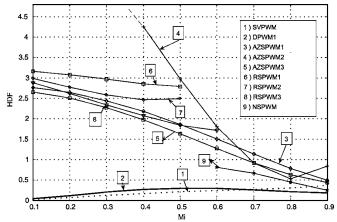


Fig. 13. HDF = $f(M_i)$ for various PWM methods.

and the power factor (PF) angle φ . In order to compare the dc-link current ripple performance of the PWM methods, the ratio of the harmonic rms value of the dc-link current $I_{\rm in\ h\ rms}$ to the inverter ac output fundamental component current rms value $I_{\rm 1\ rms}$ is evaluated, and its square is termed as the dc-link current coefficient $K_{\rm dc}$

$$K_{\rm dc} = \frac{I_{\rm in \, h \, rms}^2}{I_{1 \, \rm rms}^2}.$$
 (8)

For given M_i and φ , the rms dc-link current is calculated over a PWM cycle as a function of θ , and this result is calculated over 360° to obtain $I_{\rm in\ h\ rms}$. Then, (8) is calculated. For all the methods discussed, (8) is calculated analytically. $K_{\rm dc}$ for the standard PWM methods is given in [3]. $K_{\rm dc}$ of RSPWM3 is given in (9). $K_{\rm dc}$ of other RSPWM methods are similar to that of RSPWM3, and are not discussed further. $K_{\rm dc}$'s of AZSPWM1 and AZSPWM2 are the same and given in (10). For AZSPWM3 and NSPWM, $K_{\rm dc}$ is given in (11) and (12), respectively

$$K_{\rm dc}^{\rm RSPWM3} = 1 + M_i \frac{6}{\pi^2} \cos 2\varphi - M_i^2 \frac{18}{\pi^2} \cos^2 \varphi$$
 (9)

$$K_{\rm dc}^{\rm AZSPWM1-2} = 1 - \frac{3\sqrt{3}}{2\pi} \cos 2\varphi + M_i \frac{9\sqrt{3}}{\pi^2} \cos 2\varphi$$
 (10)

$$- M_i^2 \frac{18}{\pi^2} \cos^2 \varphi$$
 (10)

$$K_{\rm dc}^{\rm AZSPWM3} = 1 + \frac{3\sqrt{3}}{2\pi} \left[\left(\frac{1}{2} + \frac{M_i}{\pi} \right) \cos 2\varphi + \left(\frac{\sqrt{3}}{2} - \frac{5M_i}{\sqrt{3}\pi} \right) \sin 2\varphi \right]$$
 (11)

$$K_{\rm dc}^{\rm NSPWM} = 1 + \left(M_i \frac{24}{\pi^2} - \frac{3\sqrt{3}}{\pi} \right) \cos 2\varphi$$
$$- M_i^2 \frac{18}{\pi^2} \cos^2 \varphi. \tag{12}$$

Evaluating $K_{\rm dc}$ reveals some important attributes of the modulators. As Fig. 14 indicates, all methods are φ -dependent. The RCMV-PWM methods have several times higher dc-link

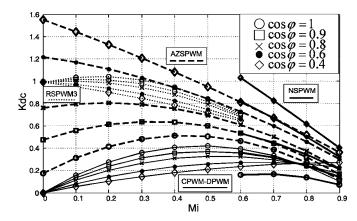


Fig. 14. $K_{\rm dc} = f(M_i, \cos \varphi)$ for various PWM methods.

current stress than the CPWM and DPWM methods. At low M_i , the AZSPWM (especially at low $\cos\varphi$) and RSPWM methods exhibit large stresses. At higher $\cos\varphi$, the AZSPWM1 and AZSPWM2 stresses become less. At higher M_i , the dc-link current stresses of the AZSPWM1–2 methods become comparable to the conventional methods due to the expiration of the active zero-state duration. AZSPWM3 has $K_{\rm dc}$ magnitude similar to that of AZSPWM1-2, but its φ -dependency is less. The dc-link current harmonic content of NSPWM is strongly dependent on PF = $\cos\varphi$ and M_i . $K_{\rm dc}$ of NSPWM decreases with increasing M_i and PF. For PF = 1, NSPWM has lower dc-link ripple content than all other PWM methods. For PF of 0.8–0.9, $K_{\rm dc}$ of all PWM methods are similar. However, for PF lower than 0.6, $K_{\rm dc}$ of NSPWM is less than that of other methods.

V. VOLTAGE LINEARITY

Each PWM method has a specific PWM-cycle-based linearity region and a fundamental cycle-based voltage linearity region. Outside the voltage linearity region (nonlinear modulation region), the output voltage magnitude is always different from the reference value. Outside the fundamental cycle linearity region, the fundamental cycle behavior involves generation of low-frequency output voltage harmonics, resulting in significant distortion of the motor current waveform. Outside the PWM-cycle-based linearity region, the dynamic performance of a modulator also becomes poor and affects the drive dynamic capability of following a current command during transients. Therefore, a wide linear modulation range is desirable. In Fig. 15, the per-fundamental-cycle linearity regions (dark gray circular zones) and the per-PWM-cycle linearity regions (dark + light gray zones) of the discussed PWM methods are illustrated. The standard SVPWM and DPWM methods provide per-fundamental-cycle voltage linearity for $0 \le M_i \le 0.907$. The per-carrier-cycle linearity range of these modulators covers the inverter voltage hexagon shown in Fig. 15(a) [3]. The AZSPWM methods have the same voltage linearity characteristics as SVPWM. However, RSPWM methods exhibit different characteristics. Both RSPWM1 and RSPWM2 [Fig. 15(b)] are linear inside either triangle T1 or T2, depending on which vector groups are selected. For the vectors $V_1V_3V_5$, T1 and

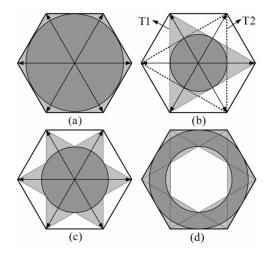


Fig. 15. Voltage linearity regions. (a) SVPWM, DPWM1, AZSPWM1–2–3. (b) RSPWM1–2. (c) RSPWM3. (d) NSPWM.

for the vectors $V_2V_4V_6$, T2 define the per-carrier-cycle linearity region. The per-fundamental-cycle linearity range of either method is $0 \le M_i \le 0.52$. RSPWM3 is linear inside the union of T1 and T2, which corresponds to a six-edged star [Fig. 15(c)]. The per-fundamental-cycle linearity of RSPWM3 is valid for $0 \le M_i \le 0.604$ (corresponding to the largest circle inside the star). In contrast to RSPWM methods, NSPWM is linear at high M_i [0.61 $\leq M_i \leq$ 0.907, Fig. 15(d)]. In fact, these methods for some regions complement each other. This is evident from the fact that in some regions, NSPWM and RSPWM utilize two identical and one exactly opposite vector. For example, in B2, NSPWM utilizes $V_1V_2V_3$, and in A1, RSPWM1–2 utilize $V_1V_3V_5$, and in this case, the two different vectors V_2 and V_5 are opposite. It is apparent from this discussion that in terms of voltage linearity, AZSPWM methods are advantageous, and RSPWM and NSPWM methods have limitation regarding voltage utilization.

VI. COMPUTER SIMULATION RESULTS

To verify the analytical results, a 4-kW, 380-V $_{\rm rms}$ lineto-line, four-pole, $1440 - min^{-1}$ induction motor that is driven from a PWM-VSI with fixed 500-V dc-bus voltage is simulated via Ansoft Simplorer [27] and plotted with MATLAB graphics [26]. The drive is tested at no-load where the ripple current can be observed clearly. The open-loop constant V/f algorithm is employed. The inverter average switching frequency f_{s-ave} is 6.6 kHz, and the corresponding carrier frequencies of each considered method is adjusted accordingly $(f_{s-DPWM1} = f_{s-NSPWM} = 10 \text{ kHz},$ $f_{\text{s-SVPWM}} = f_{\text{s-AZSPWM1-3}} = 6.6 \text{ kHz},$ 5 kHz, $f_{\text{s-AZSPWM2}} = 4 \text{ kHz}$). Results for two M_i values are illustrated. $M_i = 0.4$ with V/f value of 90 $V_{\rm rms}/25$ Hz (where RSPWM has a solution) and $M_i = 0.8$ corresponding to $180.3 \ V_{\rm rms}/51 \ Hz$ (where NSPWM has a solution) are considered.

In Fig. 16, the motor phase current waveforms for various PWM methods at $M_i=0.4$ corresponding to low-speed operation are shown. As the figure illustrates, SVPWM and DPWM1

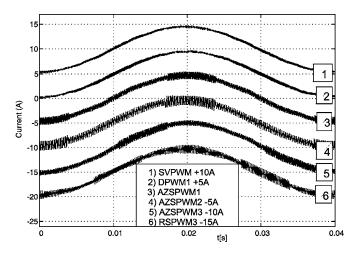


Fig. 16. Phase current waveforms of various PWM methods for $M_i = 0.4$.

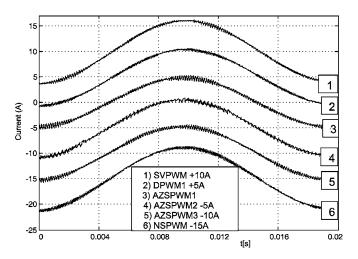


Fig. 17. Phase current waveforms of various PWM methods for $M_i = 0.8$.

have the lowest ripple. AZSPWM1 and AZSPWM3 have ripples approximately two to three times that of SVPWM, and the ripple is not significantly θ -dependent. The remaining methods have significantly larger ripple and are also θ -dependent. These results are in correlation with those of Section III. In Fig. 17, the motor phase current waveforms for various PWM methods at $M_i=0.8$ corresponding to near-rated speed operation are shown. As the figure illustrates, the waveform quality difference among various methods vanishes at high M_i . However, it is visible from the waveforms that SVPWM, DPWM1, and NSPWM have the lowest ripple, as predicted in Section III.

The analytical results of the dc-link ripple current performance index $K_{\rm dc}$ have been verified by means of the full model inverter drive simulations for all the methods considered for two M_i values (0.6 and 0.9) at no-load and rated-load. It has been found that the error between the simulation and analytical results is less than 5% in the worst case [19]. Thus, the accuracy of the parametric $K_{\rm dc}$ curves of Fig. 14 has been verified. The HDF calculation involves the virtual quantity of harmonic flux. Therefore, it is difficult to precisely extract the HDF value directly from simulations. Instead, the current ripple has been correlated with HDF, and it has been observed that methods

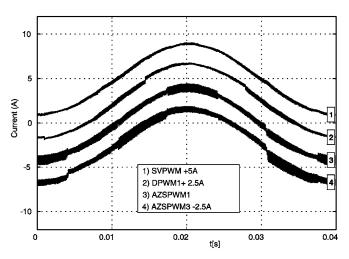


Fig. 18. Experimental phase current waveforms of various PWM methods for $M_i = 0.4$.

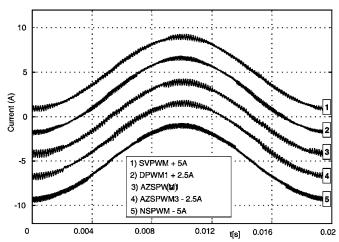


Fig. 19. Experimental phase current waveforms of various PWM methods for $M_i = 0.8$.

with larger HDF value have larger peak ripple and rms ripple current [19]. This characteristic can also be observed from current waveforms shown in Figs. 16 and 17. The data involving the simulation-based $K_{\rm dc}$ values and the current ripple correlated with HDF is omitted for the sake of brevity. Also, in the experiments, as measuring the dc-link current poses problems (inserting the available current probe in the dc-link current path results in large inductance that puts significant voltage stress on the switches) and measuring HDF involves difficulties, the direct experimental verification approach for $K_{\rm dc}$ and HDF will not be pursued.

VII. EXPERIMENTAL RESULTS

The simulation results have been verified with experiments conducted on a drive with the same ratings, parameters, and operating conditions as those of the simulations. In the experiments, of AZSPWM2, AZSPWM3, and RSPWM3, only AZSPWM3 has been implemented. As discussed in Section II, these methods have simultaneous inverter-leg switchings that prohibit their practical application. Therefore,

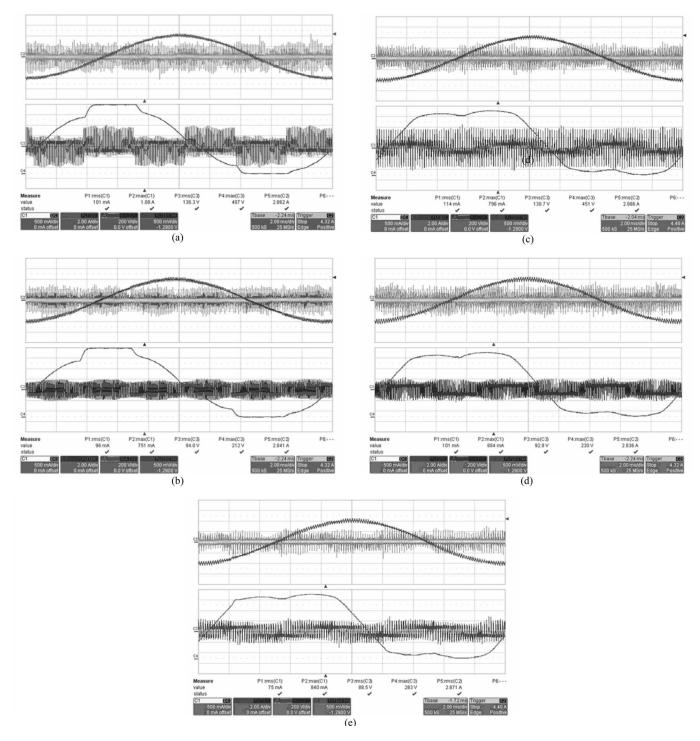


Fig. 20. Experimental phase current (top, 2 A/division), CMC (top, 0.5 A/division), CMV (bottom, 200 V/division), and modulation signal (bottom, 0.2 unit/division) waveforms ($M_i=0.8,\,f_{s-ave}=6.6~\mathrm{kHz}$). (a) DPWM1. (b) NSPWM. (c) SVPWM. (d) AZSPWM1. (e) AZSPWM3.

AZSPWM3, which is easy to implement, is experimentally evaluated as a representative of this group. Figs. 18 and 19 are the experimental results corresponding to the simulation waveforms of Figs. 16 and 17, respectively. There is strong correlation between the waveforms of experiments and simulations. The PWM ripple characteristics are the same as predicted by simulation. In the experimental waveforms, slightly larger ripple than the simulation waveforms is observed.

In Fig. 20, the detailed waveforms are shown for $M_i=0.8$. The phase currents are sinusoidal, and the PWM current ripple is small and comparable in all the methods. The CMV comparison indicates that both DPWM1 and SVPWM have high CMV compared to others. With RCMV-PWM methods, for example, with NSPWM, the peak and rms CMV are, respectively, reduced to approximately 50% and 70% of the conventional methods. Comparing the CMC characteristics, the difference is

	SVPWM	DPWM	AZSPWM1	AZSPWM2	AZSPWM3	RSPWM	NSPWM	
CMV magnitude (vno)	High	High	Low	Low	Low	Low	Low	
CMV frequency	f_s	\mathbf{f}_{s}	3 f _s	$\mathbf{f_s}$	f_s	DC-3 f _e	$2f_s$	
Voltage linearity	0-0.91	0-0.91	0-0.91	0-0.91	0-0.91	0- 0.52 or 0 0.60	0.61-0.91	
HDF (M _i <0.61)	Low	Low	Very high	Extremely high	Very high	Very high	NA	
HDF (M _i >0.61)	Low	Low	High	High	High	NA	Moderate	
Switching # per T _s	6	4	6	10	6	8	4	
K _{dc}	Low	Low		te near PF=1 th near PF=0	High	High	Very low near PF=1 High near PF=0	
V _{LL} pulse pattern	Unipolar	Unipolar	2- phase bipolar	2- phase bipolar	2- phase bipolar	3- phase bipolar	1- phase bipolar	
Zero voltage time	NA	NA	Sufficient with MAZSPWM	Problematic	Problematic	Problematic	Sufficient	
Simultaneous switchings	No	No	No	Yes	Yes Yes		No	

TABLE III
PERFORMANCE COMPARISON OF VARIOUS PWM METHODS

NA: not applicable; fe: fundamental frequency.

not as emphasized as the CMV characteristic, because the *dldt* of CMV is the same in all methods. However, the differences are still notable in terms of rms and peak CMC values, and the CMC values of SVPWM and DPWM1 are higher than those of NSPWM, AZSPWM1, and AZSPWM3 by approximately 10%–20% [25].

Inserting a 70-m cable between the motor and the inverter and conducting the same experiments, large overvoltages have been measured with AZSPWM3, while all other methods performed satisfactorily. In this test, the modified version of AZSPWM1 (MAZSPWM) has been employed instead of AZSPWM1 in order to avoid overvoltage stresses [24]. In MAZSPWM, when they occur, the pulse reversals with small zero-voltage time intervals are avoided by increasing the zero-voltage time intervals by modifying the vector duty cycles [24]. With $V_{\rm dc} = 500 \, \rm V$, all the tested methods had a peak motor line-to-line terminal voltage of 1000 V ($2V_{\rm dc}$) except for AZSPWM3, which frequently exceeded 1260 V ($2.5V_{\rm dc}$) due to simultaneous inverterleg switchings [24], [25]. Thus, AZSPWM3 is not favorable for practical applications involving long cables. From the experiments, it has been concluded that, in particular, NSPWM is favorable for high- M_i operation as all its performance characteristics have been found superior to other methods. Similarly, for low M_i and low CMV/CMC, MAZSPWM has been found superior. Thus, the combination of MAZSPWM and NSPWM to cover all the voltage linearity range is the favorable approach. Detailed performance results of this hybrid algorithm have been reported in [24]. Also, further detailed experimental results are reported in [25].

VIII. PERFORMANCE COMPARISONS

The performance study results of the paper are summarized in Table III. In general, RCMV-PWM methods increase the stress on both the ac and dc sides of the inverter compared to standard CPWM/DPWM methods. In addition, except for NSPWM, all RCMV-PWM methods exhibit pulse reversal and/or simultaneous switching problems, which prohibit their practical utilization. In applications with low CMV requirement, NSPWM is a

viable solution due to its acceptable PWM ripple. However, it is not operable for $M_i < 0.61$. The pulse pattern of AZSPWM1 can be slightly modified, and its pulse reversal problems can be overcome [19], [24] such that it can be utilized in $M_i < 0.61$ where NSPWM is not feasible. Although in this range, HDF and $K_{\rm dc}$ of AZSPWM1 are relatively high compared to the conventional methods, if the application tolerates these values, the method can be utilized successfully. Thus, NSPWM and AZSPWM1 can complement each other in the vector space such that the inverter is utilized with low CMV and acceptable PWM ripple.

IX. CONCLUSION

This paper reviewed the RCMV-PWM methods, investigated their performance characteristics, and provided a comparison with the standard PWM methods. The RCMV-PWM methods were classified, and their pulse patterns defined and illustrated. Analytical and computer-simulation-based methods were utilized to obtain the dc-link current ripple and ac output voltage and current ripple characteristics. The voltage linearity characteristics were also investigated and illustrated via voltage space vector diagrams. The theory and simulation results were supported with experimental results.

The study results illustrate that the standard methods have less dc-link and ac output current ripple than the RCMV-PWM methods. Most of the RCMV-PWM methods have bipolar line-to-line voltage pulse pattern and require simultaneous switching. Since these characteristics are not favored in the application, the methods do not appear feasible. This argument is further supported with the PWM ripple characteristics of these methods that are worse than the conventional methods. Of the RCMV-PWM methods, only NSPWM and AZSPWM1 methods are free from the simultaneous switching and pulse-reversal problems. Further, NSPWM has PWM ripple performance comparable to the conventional methods in the high- M_i operating range where it is feasible. AZSPWM1 is favorable only for low-CMV applications and strictly at low- M_i operation. Thus, a low-CMV drive favors utilization of NSPWM at high M_i and AZSPWM1

at low M_i in a combined algorithm. The paper aids in selection of appropriate PWM methods in drives that have low CMV requirements.

REFERENCES

- H. V. D. Broeck, H. Skudelny, and G. Stanke, "Analysis and realization of a pulse width modulator based on voltage space vectors," in *Conf. Rec. IEEE IAS Annu. Meeting*, 1986, pp. 244–251.
- [2] M. Depenbrock, "Pulse width control of a 3-phase inverter with nonsinusoidal phase voltages," in *Proc. IEEE ISPC*, 1977, pp. 399–403.
- [3] A. M. Hava, R. J. Kerkman, and T. A. Lipo, "Simple analytical and graphical methods for carrier-based PWM-VSI drives," *IEEE Trans. Power Electron.*, vol. 14, no. 1, pp. 49–61, Jan. 1999.
- [4] J. Holtz, "Pulsewidth modulation for electronic power conversion," *Proc. IEEE*, vol. 82, no. 8, pp. 1194–1214, Aug. 1994.
- [5] J. M. Erdman, R. J. Kerkman, D. W. Schlegel, and G. L. Skibinski, "Effect of PWM inverters on AC motor bearing currents and shaft voltages," *IEEE Trans. Ind. Appl.*, vol. 32, no. 2, pp. 250–259, Mar./Apr. 1996.
- [6] A. Muetze and A. Binder, "Don't lose your bearings—Mitigation techniques for bearing currents in inverter-supplied drive systems," *IEEE Ind. Appl. Mag.*, vol. 12, no. 4, pp. 22–31, Jul./Aug. 2006.
- [7] G. L. Skibinski, R. J. Kerkman, and D. Schlegel, "EMI emissions of modern PWM AC drives," *IEEE Ind. Appl. Soc. Mag.*, vol. 5, no. 6, pp. 47–81, Nov./Dec. 1999.
- [8] Y. Murai, T. Kubota, and Y. Kawase, "Leakage current reduction for a high-frequency carrier inverter feeding an induction motor," *IEEE Trans. Ind. Appl.*, vol. 28, no. 4, pp. 858–863, Jul./Aug. 1992.
- [9] S. Ogasawara and H. Akagi, "Modeling and damping of high-frequency leakage currents in PWM inverter-fed AC motor drive systems," *IEEE Trans. Ind. Appl.*, vol. 32, no. 5, pp. 1105–1114, Sep./Oct. 1996.
- [10] M. M. Swamy, K. Yamada, and T. Kume, "Common mode current attenuation techniques for use with PWM drives," *IEEE Trans. Power Electron.*, vol. 16, no. 2, pp. 248–255, Mar. 2001.
- [11] D. Rendusara and P. Enjeti, "New inverter output filter configuration reduces common mode and differential mode dv/dt at the motor terminals in PWM drive systems," in *Proc. IEEE PESC 1997*, pp. 1269–1275.
- [12] S. Ogasawara, H. Ayano, and H. Akagi, "An active circuit for cancellation of common-mode voltage generated by a PWM inverter," *IEEE Trans. Power Electron.*, vol. 13, no. 5, pp. 835–841, Sep. 1998.
- [13] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Trans. Ind. Appl.*, vol. IA-17, no. 5, pp. 518–523, Sep./Oct. 1981.
- [14] H. J. Kim, H. D. Lee, and S. K. Sul, "A new PWM strategy for common-mode voltage reduction in neutral-point-clamped inverter-fed AC motor drives," *IEEE Trans. Ind. Appl.*, vol. 37, no. 6, pp. 518–523, Nov./Dec. 2001
- [15] Y. S. Lai and F. S. Shyu, "Optimal common-mode voltage reduction PWM technique for inverter control with consideration of the dead-time effects—Part I: Basic development," *IEEE Trans. Ind. Appl.*, vol. 40, no. 6, pp. 1605–1612, Nov./Dec. 2004.
- [16] Y. S. Lai, P. S. Chen, H. K. Lee, and J. Chou, "Optimal common-mode voltage reduction PWM technique for inverter control with consideration of the dead-time effects—Part II: Applications to IM drives with diode front end," *IEEE Trans. Ind. Appl.*, vol. 40, no. 6, pp. 1613–1620, Nov./Dec. 2004.
- [17] G. Oriti, A. L. Julian, and T. A. Lipo, "A new space vector modulation strategy for common mode voltage reduction," in *Proc. IEEE PESC 1997*, pp. 1541–1546.
- [18] M. Cacciato, A. Consoli, G. Scarcella, and A. Testa, "Reduction of common-mode currents in PWM inverter motor drives," *IEEE Trans. Ind. Appl.*, vol. 35, no. 2, pp. 469–476, Mar./Apr. 1999.

- [19] E. Ün, "Common mode voltage and current reduction in voltage source inverter driven three phase AC motors" M.Sc. thesis, Middle East Tech. Univ., Ankara, Turkey, Nov. 2007.
- [20] J. Zitzelberger and W. Hofmann, "Reduction of bearing currents in inverter fed drive applications by using sequentially positioned pulse modulation," EPE J., vol. 14, no. 4, pp. 19–25, 2004.
- [21] W. Hofmann and J. Zitzelsberger, "PWM-control methods for common mode voltage minimization—A survey," in *Proc. SPEEDAM 2006*, pp. 8-30–8-35
- [22] E. Ün and A. M. Hava, "A near state PWM method with reduced switching frequency and reduced common mode voltage for three-phase voltage source inverters," in *Proc. IEEE-IEMDC* 2007, pp. 235–240.
- [23] E. Ün and A. M. Hava, "Performance characteristics of the reduced common mode voltage near state PWM method," in *Proc. EPE 2007*, pp. 1–10.
- [24] E. Ün and A. M. Hava, "A high performance PWM algorithm for common mode voltage reduction in three-phase voltage source inverters," in *Proc. IEEE PESC 2008*, pp. 1528–1534.
- [25] E. Ün and A.M. Hava, "On the contribution of PWM methods to the common mode (leakage) current in conventional three-phase two-level inverters as applied to AC motor drives," in *Conf. Rec. IEEE IAS Annu. Meeting*, 2008, pp. 1–8.
- [26] MATLAB 6.5, The MathWorks, Inc., Natick, MA, 2002.
- [27] Ansoft Simplorer, V7.0, Ansoft Corporation, Pittsburgh, PA, 2004.



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